■ **Preliminary Specifications**
□ **Final Specifications**

Module	55 Inch Color TFT-LCD
Model Name	G550ZVN01.0

Customer		**Approved by**	**Date**
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Record of Revision

Version	Date	Page	Old description	New Description
0.1	2023/03/08	All	First edition	

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1. General Description

This specification applies to the 55 inch Color TFT-LCD Module G550ZVN01.0. This LCD module has a TFT active matrix type liquid crystal panel 3840 x 2160 pixels, and diagonal size of 55 inch. This module supports 3840 x 2160 mode. Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 10-bit gray scale signal for each dot.

G550ZVN01.0 has been designed to apply the 8 lane V by one interface method. It is intended to support displays where high brightness, wide viewing angle, high color saturation, and high color depth are very important.

1.1 General Information:

Items	Unit	Specifications	Note
Screen Diagonal	[inch]	55	
Active Area	[mm]	1209.6(H) x 680.4(V)	
Outline Dimension	[mm]	1231.4(H) x 701.3(V) x 26.4(D)	
Driver Element		a-Si TFT active matrix	
Support Color	[color]	8 bit + FRC (1.07 billion)	
Resolution	[Pixel]	3840 x 2160	
Pixel Pitch	[mm]	0.315 x 0.315	
Display Operation Mode		Normally Black, VA	
Nominal Input Voltage VDD	[V]	12V	
Power Consumption	[W]	Total = 151.7W	
Surface Treatment		Anti-Glare, 3H	
Frame Rate	Hz	60	See Chapter 5.1 for details
LED Life-Time	hours	50K	See Chapter 6.1 for details

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2. Absolute Maximum Ratings

The followings are maximum values which, if exceeded, may cause faulty operation or damage to the unit.

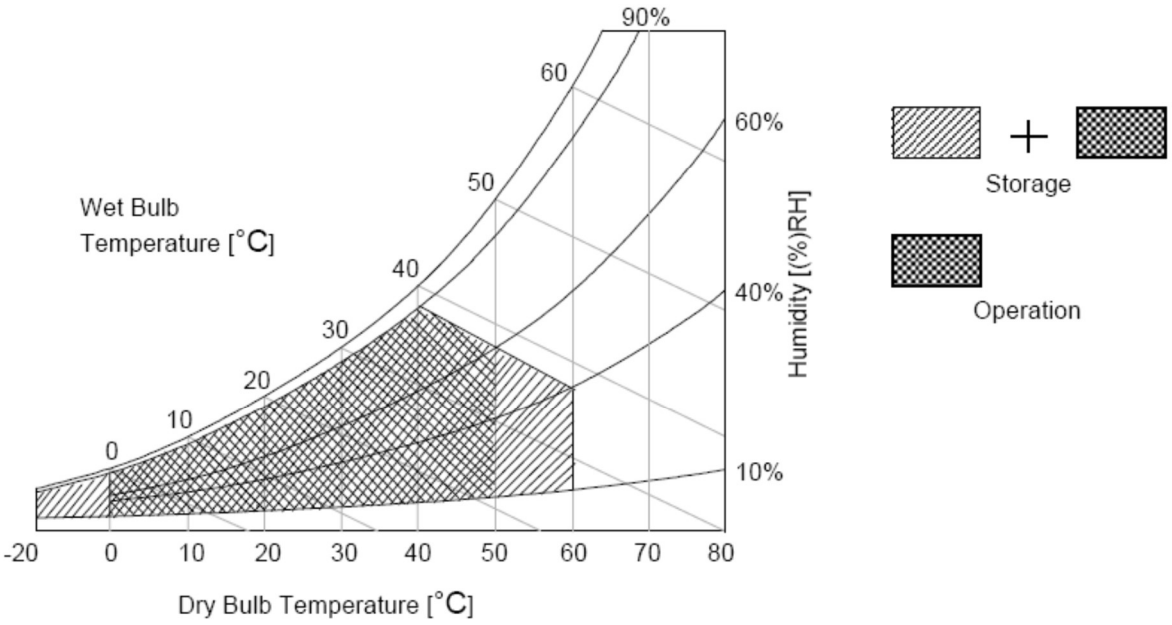
Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive Voltage	V_{DD}	-0.3	14	[Volt]	Note 1
Input Voltage of Signal	Vin	-0.3	4	[Volt]	Note 1
Operating Temperature	TOP	0	+50	[°C]	Note 2
Operating Humidity	HOP	10	90	[%RH]	Note 2
Storage Temperature	TST	-20	+60	[oC]	Note 2
Storage Humidity	HST	10	90	[%RH]	Note 2
Panel SurfaceTemperature	PST		(50)	[°C]	Note 3

Note 1: Duration:50 msec.

Note 2 : Maximum Wet-Bulb should be 39℃and No condensation.

The relative humidity must not exceed 90% non-condensing at temperatures of 40 ℃or less. At temperatures greater than 40℃, the wet bulb temperature must not exceed 39℃.

Note 3: The surface temperature of any single point in active area when operating in 50°C Dry condition.



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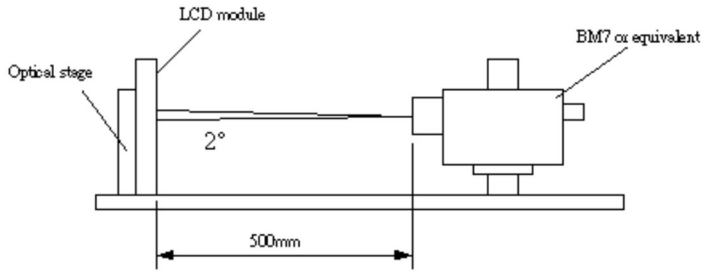
3. Optical Characteristics

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 45 minutes in a dark environment at 25°C. The values specified are at an approximate distance 500 mm from the LCD surface at a viewing angle of φ and θ equal to 0°.

Fig.1 presents additional information concerning the measurement equipment and method.



Parameter	Symbol	Values			Unit	Notes
		Min.	Typ.	Max.		
Contrast Ratio	CR	(1800)	3000	--		1
Surface Luminance (White)	LWH	560	700	--	cd/m2	2
Luminance Variation	δWHITE(9P)	--	--	1.33		3
Response Time (G to G)	TY	--	8.5	16	Ms	4
Color Gamut	NTSC		72		%	
Color Corrdinates						
Red	Rx	Typ. -0.03	TBD	Typ. +0.03		
	Ry		TBD			
Green	Gx		TBD			
	Gy		TBD			
Blue	Bx		TBD			
	By		TBD			
White	Wx		0.280			
	Wy		0.290			
Viewing Angle (CR>20:1)						
x axis, right(φ=0°)	θr	--	(88)	--	degree	
x axis, left(φ=0°)	θr	--	(88)	--	degree	
y axis, up(φ=90°)	θr	--	(88)	--	degree	
y axis, down (φ=270°)	θr	--	(88)	--	degree	

Note:

1. Contrast Ratio (CR) is defined mathematically as:

$$\text{Contrast ratio (CR)} = \frac{\text{Brightness on the "White" state}}{\text{Brightness on the "Black" state}}$$

2. Surface luminance is luminance value at point 5 across the LCD surface 50cm from the surface with all pixels displaying white. From more information see FIG 2. LED current I_F = typical value (without driver board), LED input VDDB =24V, $I_{DDB.}$ = Typical value (with driver board), LWH=Lon5 where Lon5 is the luminance with all pixels displaying white at center 5 location.

3. The variation in surface luminance, δWHITE is defined (center of Screen) as:
   δWHITE(9P)= Maximum(L_{on1}, L_{on2},…,L_{on9})/ Minimum(L_{on1}, L_{on2},…L_{on9})

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4. Response time Tγ is the average time required for display transition by switching the input signal for five luminance ratio (0%,25%,50%,75%,100% brightness matrix) and is based on Frame rate = 60Hz to optimize.

Measured Response Time		Target				
		0%	25%	50%	75%	100%
Start	0%					
	25%	25% to 0%				
	50%	50% to 0%	50% to 25%		50% to 75%	50% to 100%
	75%	75% to 0%	75% to 25%	75% to 50%		75% to 100%
	100%	100% to 0%	100% to 25%	100% to 50%	100% to 75%	

Tγ is determined by 10% to 90% brightness difference of rising or falling period. (As illustrated)
The response time is defined as the following figure and shall be measured by switching the input signal for “any level of gray(bright) “ and “any level of gray(dark)”.

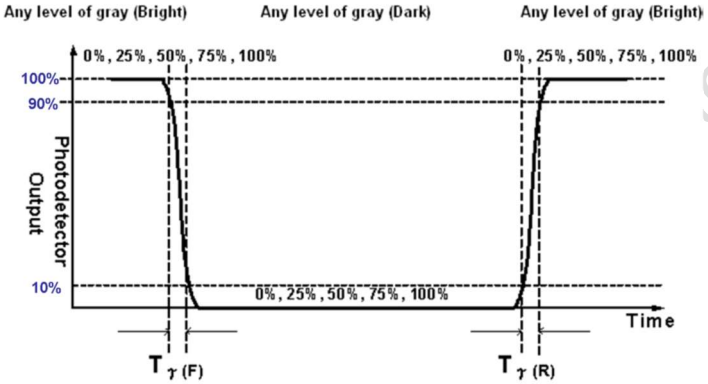
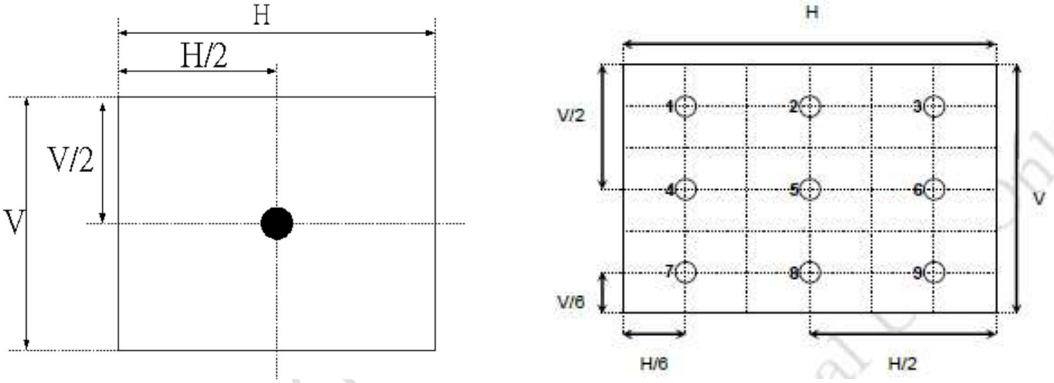
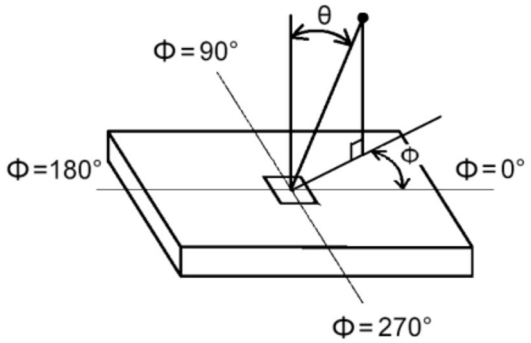


FIG. 2 Luminance



5. Viewing angle is the angle at which the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to the LCD surface. For more information see FIG3.

FIG.3 Viewing Angle



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4. Interface Specification

4.1 Input power

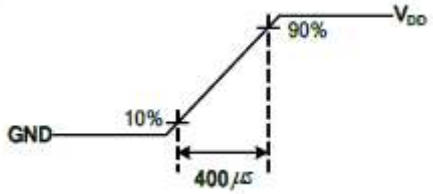
The G550ZVN01.0 module requires 1 power inputs(14-pin) which are employed to power the LCD electronics and to drive the TFT array and liquid crystal.

Item		Symbol	Min.	Typ.	Max	Unit	Note
Power Supply Input Voltage		V_{DD}	10.8	12	13.2	V	1
Power Supply Input Current	White pattern	I_{DD}	-	TBD	TBD	A	2
Power Consumption	White pattern	P_C	-	TBD	TBD	Watt	
Inrush Current		I_{RUSH}	--	--	5	A	3

Note1. The ripple voltage should be fewer than 5% of VDD.

Note2. Test Condition: (1) V_{DD} = 12.0V, (2) Fv = 60Hz, (3) Fclk= 74.25MHz, (4) Temperature = 25 ℃

Note3. Measurement condition : Rising time = 400us



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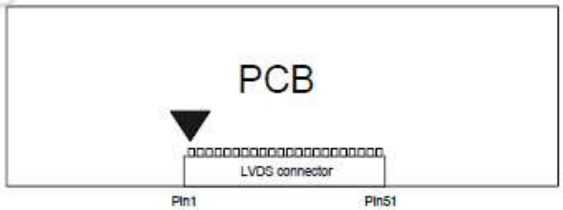
4.2 Input Connection

LCD connector: (JAE) SJ11346-FI-RTE51SZ-HF

PIN	Symbol	Description	Note	PIN	Symbol	Description	Note
1	VDD	12Vin		26	LOCKN	Vx1 LOCK	
2	VDD	12Vin		27	GND	Ground	
3	VDD	12Vin		28	RX0N	Vx1 lane 0	
4	VDD	12Vin		29	RX0P	Vx1 lane 0	
5	VDD	12Vin		30	GND	Ground	
6	VDD	12Vin		31	RX1N	Vx1 lane 1	
7	VDD	12Vin		32	RX1P	Vx1 lane 1	
8	VDD	12Vin		33	GND	Ground	
9	N.C.	No connection	2	34	RX2N	Vx1 lane 2	
10	GND	Ground		35	RX2P	Vx1 lane 2	
11	GND	Ground		36	GND	Ground	
12	GND	Ground		37	RX3N	Vx1 lane 3	
13	GND	Ground		38	RX3P	Vx1 lane 3	
14	GND	Ground		39	GND	Ground	
15	N.C.	No connection		40	RX4N	Vx1 lane 4	
16	N.C.	No connection		41	RX4P	Vx1 lane 4	
17	N.C.	No connection	2	42	GND	Ground	
18	N.C.	No connection	2	43	RX5N	Vx1 lane 5	
19	N.C.	No connection	2	44	RX5P	Vx1 lane 5	
20	N.C.	No connection	2	45	GND	Ground	
21	N.C.	No connection	2	46	RX6N	Vx1 lane 6	
22	N.C.	No connection	2	47	RX6P	Vx1 lane 6	
23	N.C.	No connection	2	48	GND	Ground	
24	GND	Ground		49	RX7N	Vx1 lane 7	
25	HTPDN	Vx1 HTPDN		50	RX7P	Vx1 lane 7	
				51	GND	Ground	

Note1. Pin number start from the left side as the following figure.



Note2. Please leave this pin unoccupied. It cannot be connected with any signal (Low/GND/High).

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4.3 Input Data Format

4.3.1 V by one Data mapping

Mode	Packer input & Unpacker output		30bpp RGB / YcbCr444 (10bit)
4 byte mode	Byte0	D[0]	R/Cr[2]
		D[1]	R/Cr[3]
		D[2]	R/Cr[4]
		D[3]	R/Cr[5]
		D[4]	R/Cr[6]
		D[5]	R/Cr[7]
		D[6]	R/Cr[8]
		D[7]	R/Cr[9]
	Byte1	D[8]	G/Y[2]
		D[9]	G/Y[3]
		D[10]	G/Y[4]
		D[11]	G/Y[5]
		D[12]	G/Y[6]
		D[13]	G/Y[7]
		D[14]	G/Y[8]
		D[15]	G/Y[9]
	Byte2	D[16]	B/Cb[2]
		D[]17	B/Cb[3]
		D[18]	B/Cb[4]
		D[19]	B/Cb[5]
		D[20]	B/Cb[6]
		D[21]	B/Cb[7]
		D[22]	B/Cb[8]
		D[23]	B/Cb[9]
	Byte3	D[24]	--
		D[25]	--
		D[26]	B/Cb[0]
		D[27]	B/Cb[1]
		D[28]	G/Y[0]
		D[29]	G/Y[1]
		D[30]	R/Cr[0]
		D[31]	R/Cr[1]

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4.3.2 Color Input Data Reference

The brightness of each primary color (red, green and blue) is based on the 10 bit gray scale data input for the color; the higher the binary input, the brighter the color. The table below provides a reference for color versus data input.

COLOR DATA REFERENCE

Color		Input Color Data																													
		RED										GREEN										BLUE									
		MSB									LSB	MSB									LSB	MSB									LSB
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue(1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R	RED(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(001)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	RED(1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
G	GREEN(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0

	GREEN(1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	GREEN(1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
B	BLUE(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

	BLUE(1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	BLUE(1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

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5. Signal Timing Specification

This is the signal timing required at the input of the user connector. All of the interface signal timing should be satisfied with the following specifications for its proper operation.

5.1 Input Timing

5.1.1 Timing table

Timing Table (DE only Mode)

Signal	Item	Symbol	Min	Typ	Max	Unit
Vertical Section	Period	Tv	2200	2250	2715	Th
	Active	Tdisp(v)		2160		Th
	Blanking	Tblk (v)	40	90	555	Th
Horizontal Section	Period	Th	530	550	600	Tclk
	Active	Tdisp(h)		480		Tclk
	Blanking	Tblk (h)	50	70	120	Tclk
Clock	Frequency	Fclk=1/Tclk	66	74.25	77	MHz
Vertical Frequency	Frequency	Fv	47	60	63	Hz
Horizontal Frequency	Frequency	Fh	120	135	139.2	KHz

Note:

(1) Display position is specific by the rise of DE signal only.
Horizontal display position is specified by the rising edge of 1st DCLK after the rise of 1st DE, is displayed on the left edge of the screen.
(2) Vertical display position is specified by the rise of DE after a “Low” level period equivalent to eight times of horizontal period. The 1st data corresponding to one horizontal line after the rise of 1st DE is displayed at the top line of screen.
(3) If a period of DE “High” is less than 1920 DCLK or less than 1080 lines, the rest of the screen displays black.
(4) The display position does not fit to the screen if a period of DE “High” and the effective data period do not synchronize with each other.

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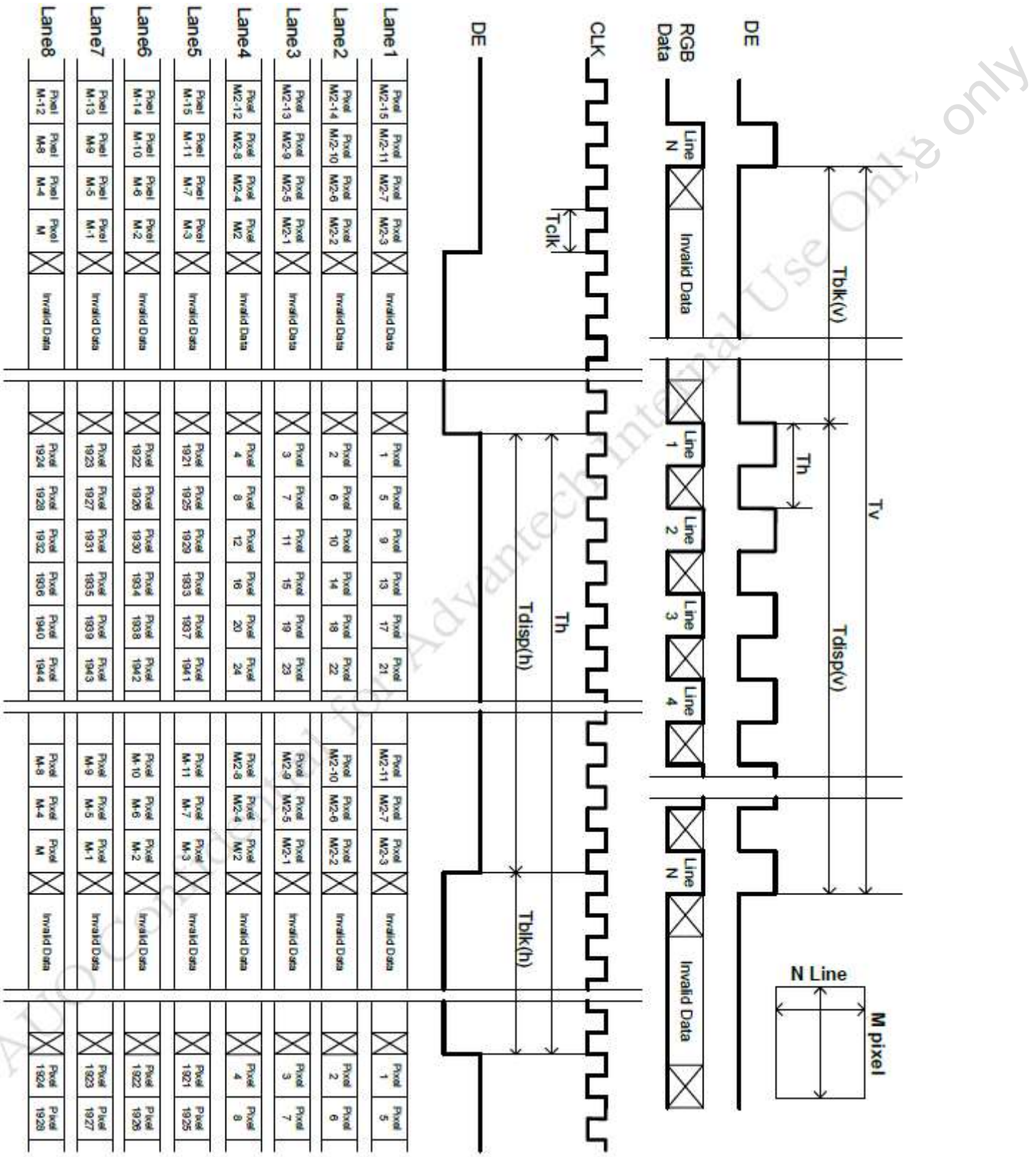
5.1.2 Signal Timing Waveform



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5.2 Input interface characteristics

5.2.1 V by one

Item		Symbol	Min.	Typ.	Max	Unit	Note
V-by-one interface	VRXINP/N input each bit Period	TRRIP (UI)	310	-	379	Ps	10bit 1
	Receiver Clock : Spread Spectrum Modulation range	Fclk_ss	Fclk -0.5%	-	Fclk +0.5%	MHz	2
	Receiver Clock : Spread Spectrum Modulation frequency	Fss		30		KHz	2
	CDRtraining pattern time	TLOCK	-	500	-	us	1
	Latency from LOCKN 'HIGH' to clock training pattern	L1	0	-		us	1
	Latency from LOCKN 'LOW' to normal 8b 10b data	L2	-	-	70	us	1
	CML Differential Input High Threshold	VRTH	+50	-	-	mVDC	
	CML Differential Input Low Threshold	VRTL	-	-	-50	mVDC	
	CML Common mode Bias Voltage	VRCT	0.8	0.9	1.0	Vdc	
	Intra-pair skew	TINTRA	-	-	0.3	UI	3
	Inter-pair skew	TINTER	-	-	5	UI	4
	Eye diagram at receiver	A_X	-	0.25	-	UI	5
		A_Y	-	0	-	mV	
		B_X	-	0.3	-	UI	
		B_Y	-	50	-	mV	
		C_X	-	0.7	-	UI	
		C_Y	-	50	-	mV	
		D_X	-	0.75	-	UI	
		D_Y	-	0	-	mV	
		E_X	-	0.7	-	UI	
		E_Y	-	-50	-	mV	
		F_X	-	0.3	-	UI	
		F_Y	-	-50	-	mV	

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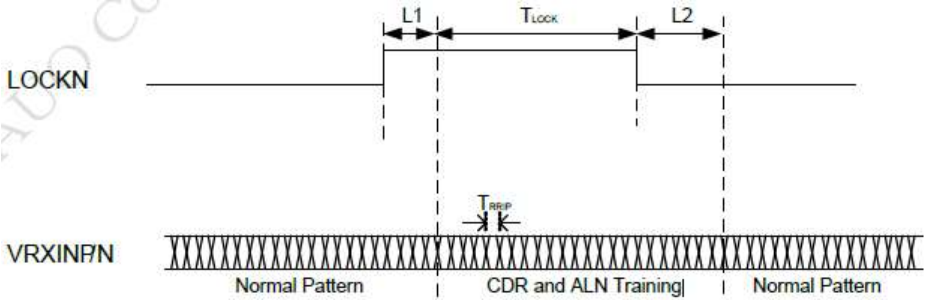
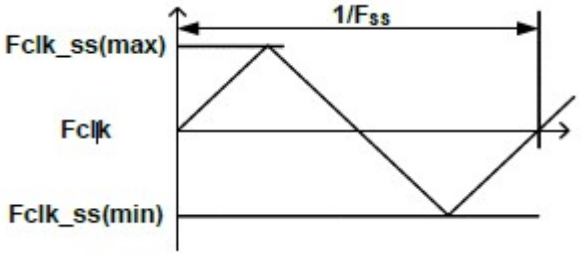
Note :

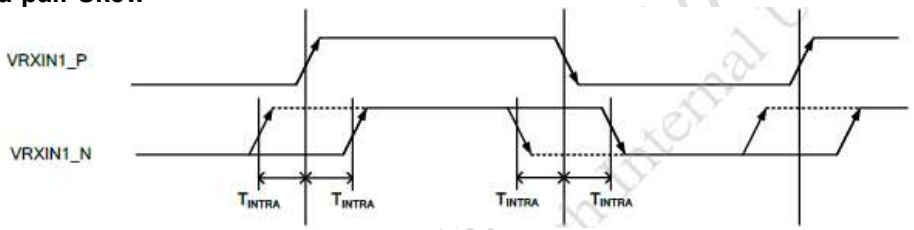
1. V-by-one Signal diagram



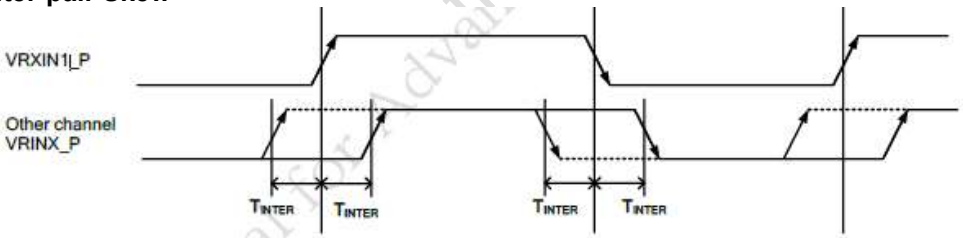
2. Receiver Clock SSCG (Spread spectrum clock generator) is defined as below figures.



3. V-by-one Intra-pair Skew



4. V-by-one Inter-pair Skew



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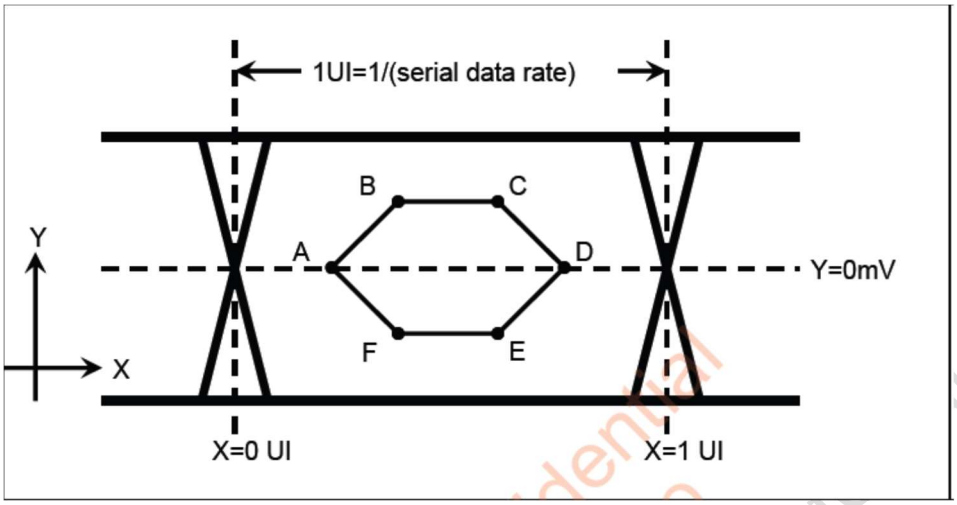
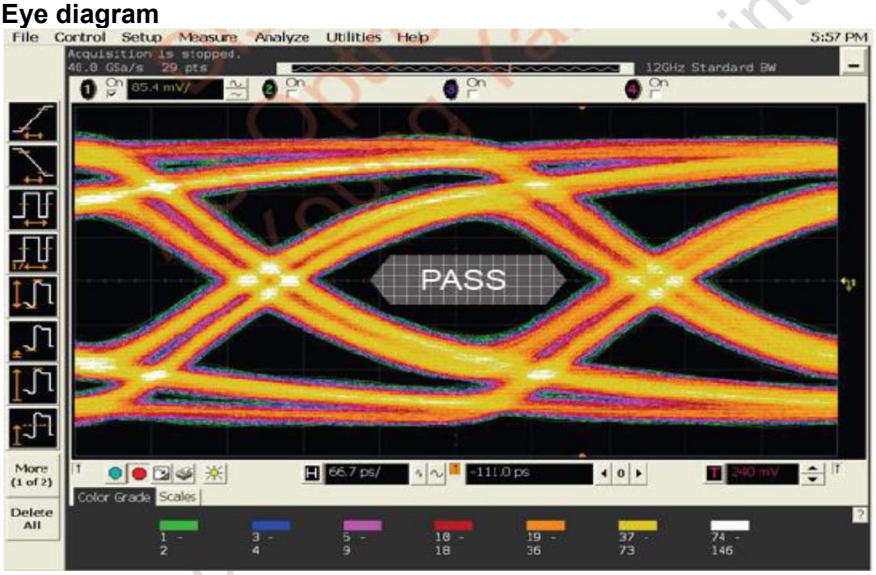
5. Eye diagram at receiver

Eye Mask



Example of Eye diagram



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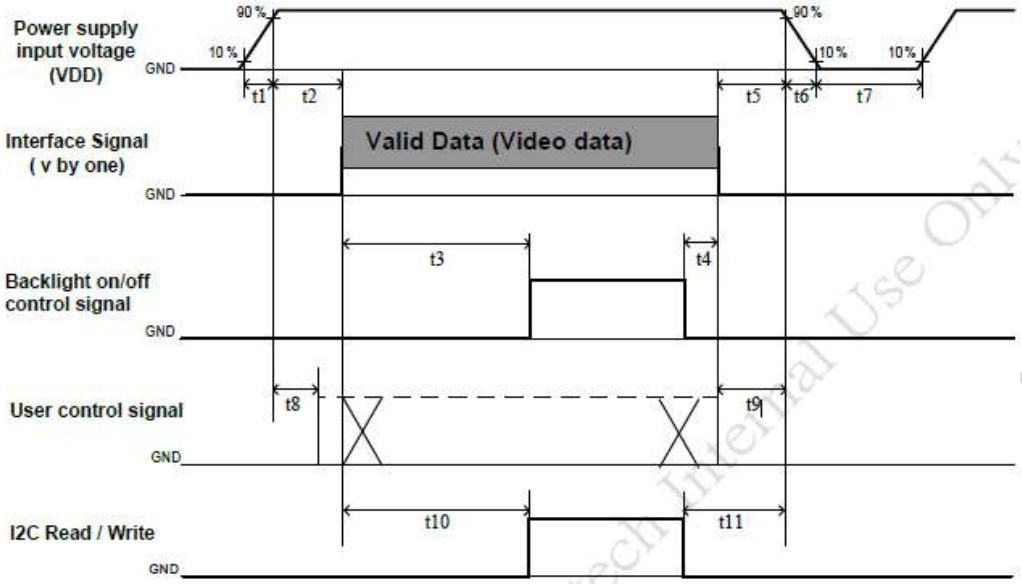
5.3 Power Sequence for LCD



Parameter	Values			Unit
	Min.	Type.	Max	
t1	0.4	---	30	ms
t2	40	---	---	ms
t3	640	---	---	ms
t4	0*1	---	---	ms
t5	0	---	---	ms
t6	--	---	---*2	ms
t7	1000*3	---	---	ms
t8	20*4	---	50	ms
t9	0	---	---	ms
t10	640	---	---	ms
t11	150	---	---	ms

Note:
(1) t4=0 : concern for residual pattern before BLU turn off.
(2) t6 : voltage of VDD must decay smoothly after power-off. (customer system decide this value)
(3) t7 : When the power supply input voltage(VDD) is off, be sure to pull down the valid and invalid data to 0V.
(4) When user control signal is N.C. (no connection), opened in Transmitted end, t8 timing spec can be negligible.

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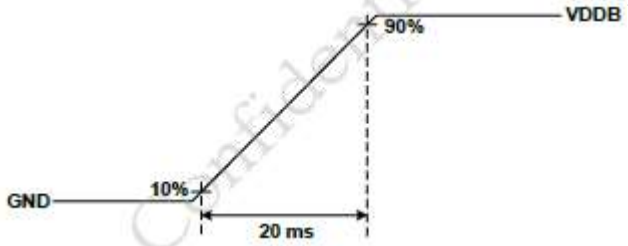
6. Backlight Specification

6.1 Electrical specification

	Item	Symbol		Condition	Min	Typ	Max	Unit	Note
1	Power Supply Input Voltage	V_{DDB}		-	22.8	24	25.2	V	-
2	Power Supply Input Current	I_{DDB}		V_{DDB}=24V		TBD	TBD	A	1
3	Power Consumption	P_{DDB}		V_{DDB}=24V		TBD	TBD	Watt	1
4	Inrush Current	I_{RUSH}		V_{DDB}=24V			10	A	2
5	Control signal votlage	Vsignal	Hi	V_{DDB}=24V	2	-	3.3	V	-
			Low	V_{DDB}=24V	0	-	0.8		3
6	Control signal current	Isignal		V_{DDB}=24V	-	-	1.5	mA	-
7	External PWM Duty ratio (input duty ratio)	D_EPWM		V_{DDB}=24V	10	-	100	%	
8	External PWM Frequency	F_EPWM		V_{DDB}=24V	18K	-	20K	Hz	
9	DET status signal	DET	Hi	V_{DDB}=24V	Open Collector			V	4
			Lo	V_{DDB}=24V	0	-	0.8	V	4
10	Input Impedance	Rin		V_{DDB}=24V	300	-	-	Kohm	
11	LED lifetime	LTLED			50,000	-	-	Hr	5

Note 1: Dimming ratio= 100%,（Ta=25±5℃, Turn on for 45minutes）

Note 2: MAX input current while DB turn on, measurement condition VDDB rising time=20ms(VDDB: 10%~90%)



Note 3: When BLU off (VDDB = 24V , VBLON = 0V) , IDDB (max) = 0.1A
Note 4: Normal: 0~0.8V ; Abnormal : Open collector
Note 5: The LED lifetime is defined as the time which luminance of LED is 50% compared to its original value.
[Operating condition: Continuous operating at Ta = 25±2℃, for single LED only]

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6.2 Input Pin Assignment

LED DB connector: CI0114M1HRL-NH(CviLux)

Pin	Symbol	Description	Note
1	VDDB	Operating Voltage Supply, +24V DC regulated	
2	VDDB	Operating Voltage Supply, +24V DC regulated	
3	VDDB	Operating Voltage Supply, +24V DC regulated	
4	VDDB	Operating Voltage Supply, +24V DC regulated	
5	VDDB	Operating Voltage Supply, +24V DC regulated	
6	BLGND	Ground and Current Return	
7	BLGND	Ground and Current Return	
8	BLGND	Ground and Current Return	
9	BLGND	Ground and Current Return	
10	BLGND	Ground and Current Return	
11	DET	BLU status detection	1
12	VBLON	BL On-Off Control	2,3
13	NC	No Connect	4
14	PDIM	Ecternal PWM	2,5

Note1. DET status

DET	BLU status
0~0.8V	Normal
Open collector	Abnormal

Recommend pull high R > 10K ohm, pull high voltage VDD = 3.3V

Note2. input control signal threshold voltage definition

Item	Symbol	Min.	Typ.	Max.	Unit
Input High Threshold Voltage	VIH	2	-	5.5	V
Input Low Threshold Voltage	VIL	0	-	0.8	V

Note3. VBLON

Mode selection

VBLON	Note
H or OPEN	BL On
L	BL On

Note4. Please leave this pin unoccupied. It cannot be connected by any signal (Low/GND/High).

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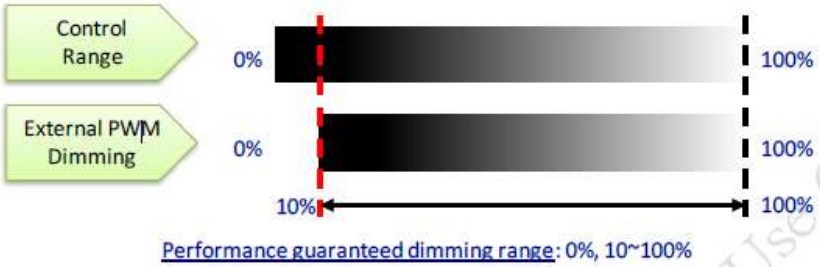
Note5. PDIM

PWM Dimming range:

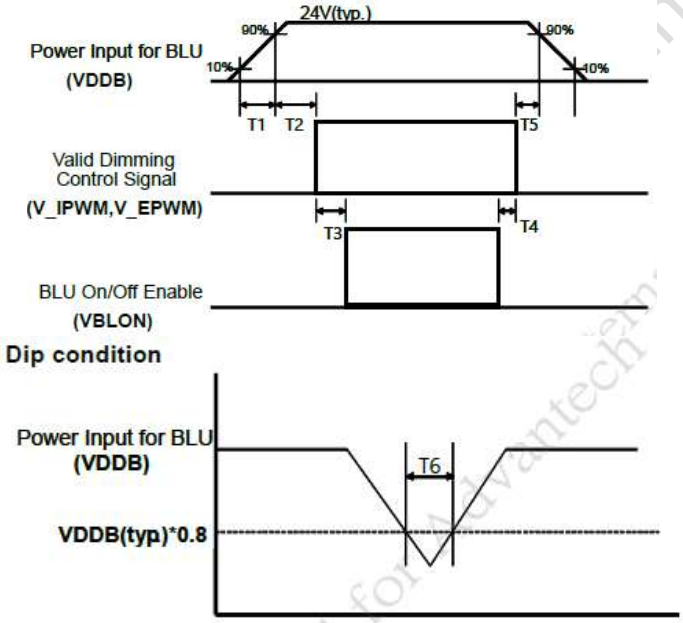


Performance guaranteed dimming range: 0%, 10~100%

External PWM function dimming ratio 0%~100%, Judge condition as below:
(1)Backlight module must be lighted ON normally.
(2)All protection function must work normally.

(3)Uniformity and flicker could be guaranteed at External PWM function dimming ratio 10%~100%

6.3 Power Sequence for Backlight



Parameter	Min	Typ	Max	Units
T1	20			ms*1
T2	250			ms
T3	2200			ms
T4	0			ms
T5	0		1000	ms*2

Note:1. T6 describes VDDB dip condition and VDDB couldn't lower than 10% VDDB.

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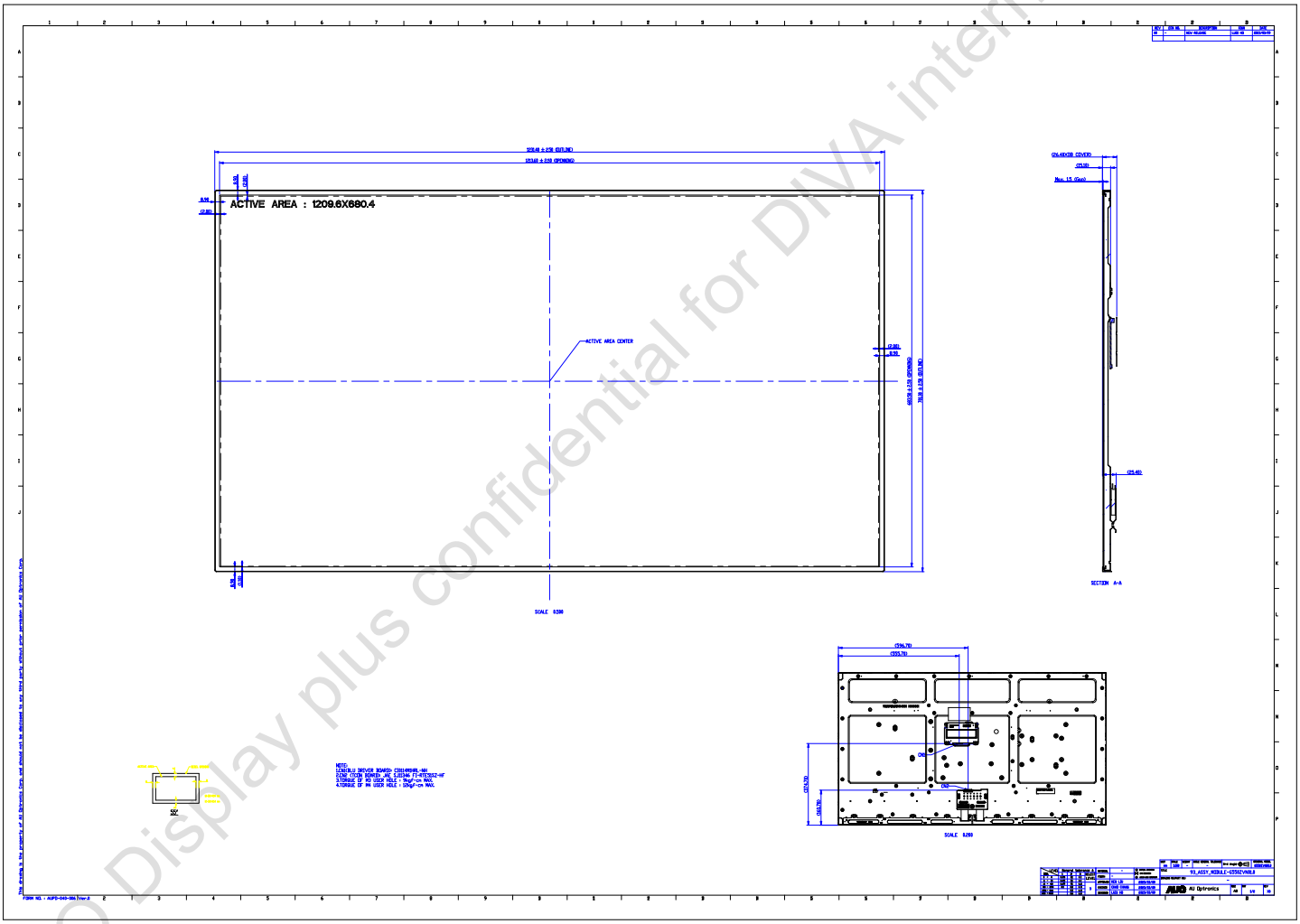
7. Mechanical Characteristics

The contents provide general mechanical characteristics and detailed mechanical drawing of the LCD.

Item		Dimension	Unit	Note
Outline Dimension	Horizontal	1231.4	mm	
	Vertical	701.3	mm	
	Depth (Dmax)	26.4	mm	
	Bezel Width	8.9/8.9/8.9/8.9		U/D/L/R
Weight	14.3		kg	

Front View



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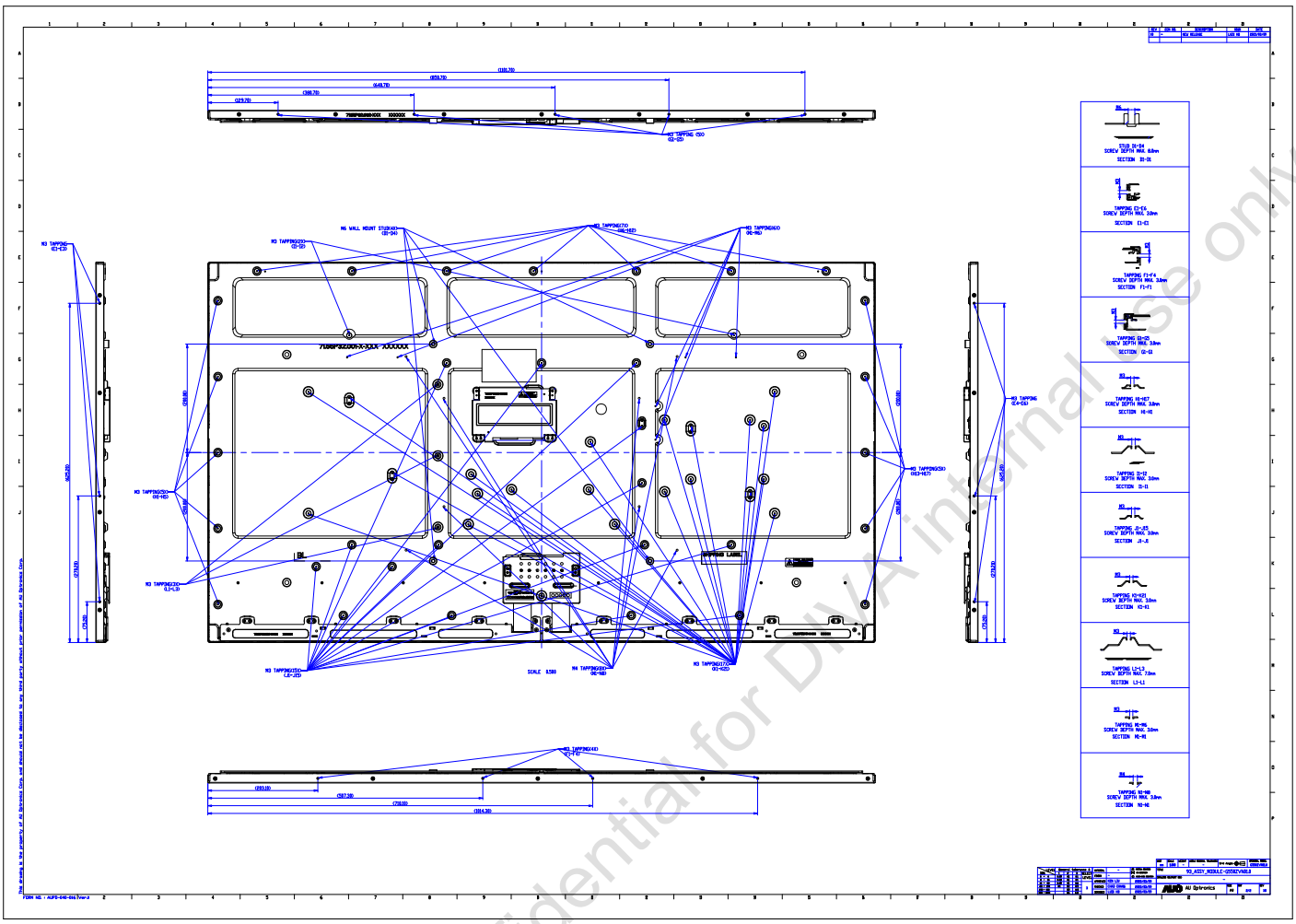
Back View



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8. Reliability Test Items

	Test Item	Condition
1	High temperature storage test	**60℃, 500hrs**
2	Low temperature storage test	**-20℃, 500hrs**
3	High temperature operation test	**50℃, 500hrs**
4	Low temperature operation test	**0℃, 500hrs**
5	Vibration test (with carton)	**Random wave (1.04Grms 2~200Hz)** **Duration : X,Y,Z 20min per axes**
6	Drop test (with carton)	**Height: 25.4 cm** **Direction: Only bottom flat twice** **(ASTMD4169-I)**

9. Safety

9.1 Sharp Edge Requirements

There will be no sharp edges or comers on the display assembly that could cause injury.

9.2 Materials

(1) Toxicity

There will be no carcinogenic materials used anywhere in the display module. If toxic materials are used, they will be reviewed and approved by the responsible AUO toxicologist.

(2) Flammability

The printed circuit board will be made from material rated 94-V1 or better. The actual UL flammability rating will be printed on the printed circuit board..

9.3 Capacitors

If any polarized capacitors are used in the display assembly, provisions will be made to keep them from being inserted backwards.

9.4 International Safety Standard Compliance

The TFT-LCD Module will satisfy all requirements for compliance to IEC/UL 62368-1.

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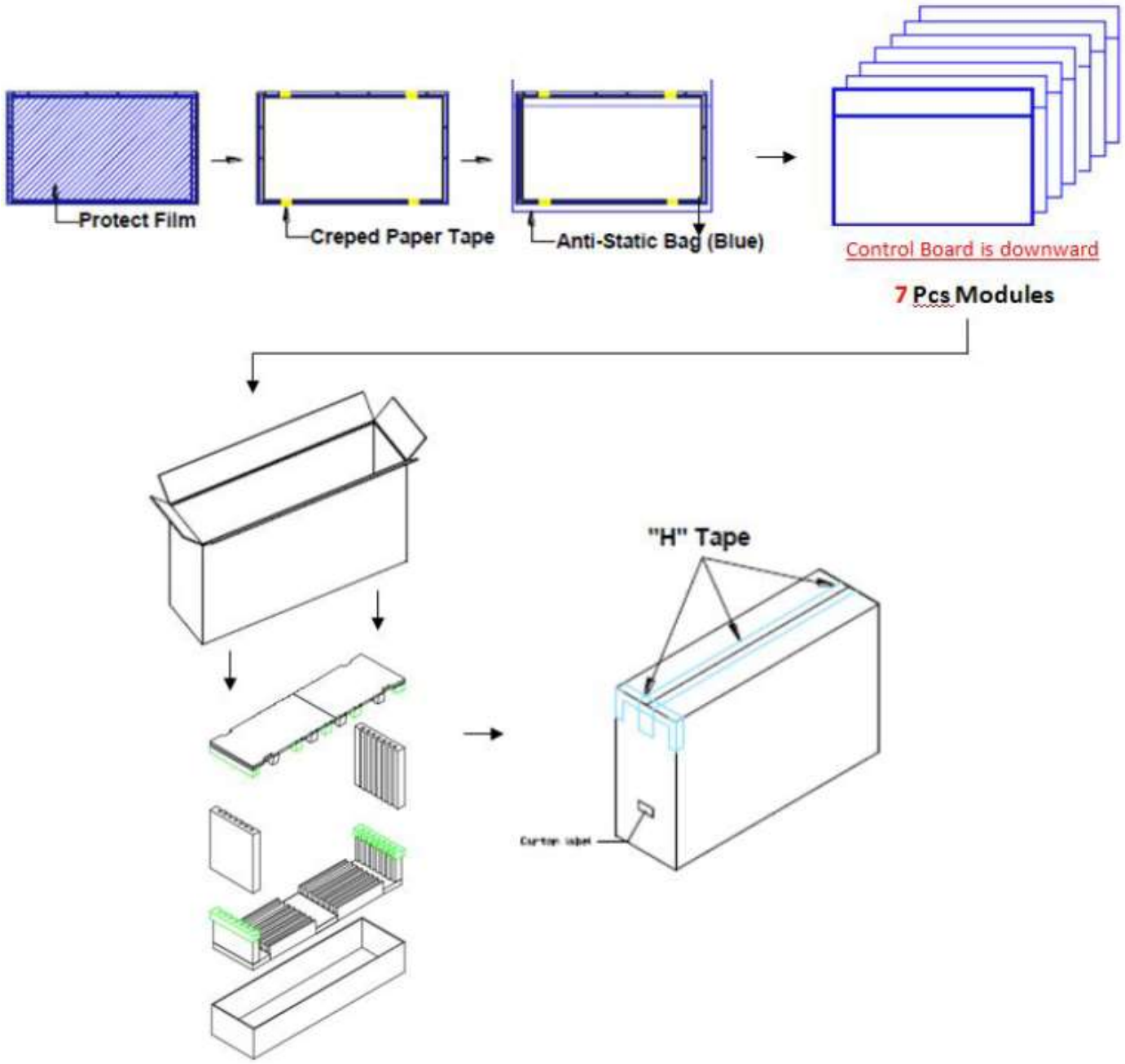
10. Packing

10.1 Definition of Label

A. Panel Label: TBD

10.2 Packing Methods



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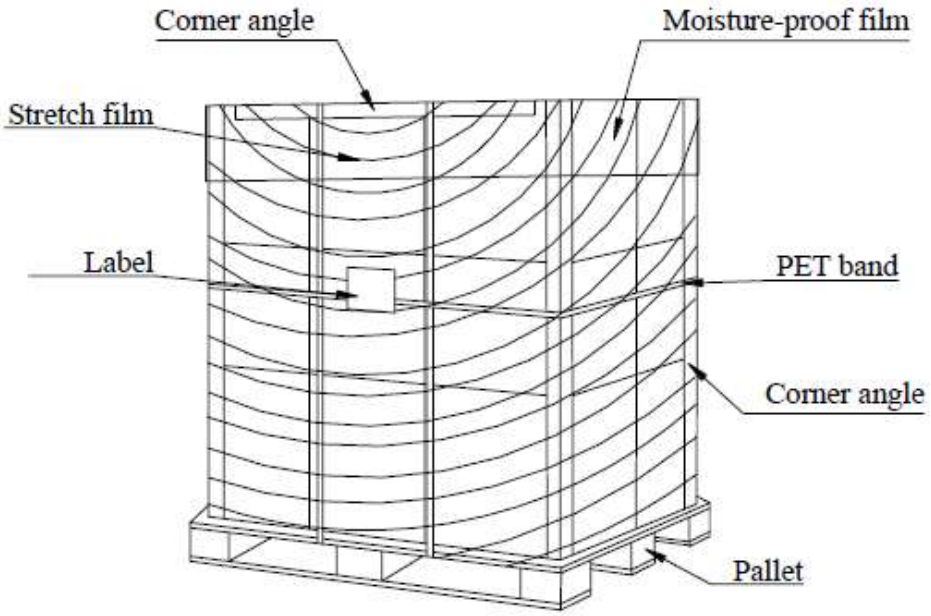
10.3 Pallet and Shipment Information

	Item	Specification			Packing Remark
		Qty.	Dimension	Weight (kg)	
1	Packing BOX	7pcs/box	1305mm*383mm*800mm	106.6	Box = 4.2kg Cushion = 2.3kg
2	Pallet	1	1315mm*1150mm*138mm	17.1	
3	Boxes per Pallet	3 boxes/pallet			
4	Panels per Pallet	21 pcs/pallet			
	Pallet after packing	21	1315mm*1150mm*938mm	336.9	



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11. Precautions

Please pay attention to the followings when you use this TFT LCD module.

11.1. Mounting Precautions

(1) You must mount a module using holes arranged in four corners or four sides.

(2) You should consider the mounting structure so that uneven force (ex. twisted stress) is not applied to module. And the case on which a module is mounted should have sufficient strength so that external force is not transmitted directly to the module.

(3) Please attach the surface transparent protective plate to the surface in order to protect the polarizer. Transparent protective plate should have sufficient strength in order to the resist external force.

(4) You should adopt radiation structure to satisfy the temperature specification.

(5) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the polarizer at high temperature and the latter cause circuit broken by electro-chemical reaction.

(6) Do not touch, push or rub the exposed polarizer with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of polarizer for bare hand or greasy cloth. (Some cosmetics are detrimental to the polarizer.)

(7) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach front/ rear polarizer. Do not use acetone, toluene and alcohol because they cause chemical damage to the polarizer.

(8) Wipe off saliva or water drops as soon as possible. Their long time contact with polarizer causes deformations and color fading.

(9) Do not open the case because inside circuits do not have sufficient strength.

11.2. Operating Precautions

(1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage: V=±200mV(Over and under shoot voltage)

(2) Response time depends on the temperature. (In lower temperature, it becomes longer.)

(3) Brightness depends on the temperature. (In lower temperature, it may become lower.) And in lower temperature, response time (required time that brightness is stable after turned on) becomes longer.

(4) Be careful for condensation at sudden temperature change. Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.

(5) When fixed patterns are displayed for a long time, remnant image is likely to occur.

(6) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimize the interface.
(7) The conductive material and signal cables are kept away from LED driver inductor to prevent abnormal display, sound noise and temperature rising.

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11.3. Operating Condition for Public Information Display

To optimize module's lifetime and function, below operating usages are required.

(1) Normal operating condition

A. Operating temperature: 0~50℃

B. Operating humidity: 10~90%

C. Display pattern: dynamic pattern (Real display).

Note) Long-term static display would cause image sticking.

(2) Operation usage to protect against image sticking due to long-term static display.

A. Suitable operating time: under 24 hours a day

(* The moving picture can be allowed for 24 hours a day)

B. Liquid Crystal refresh time is required. Cycling display between 5 minutes' information (static) display and 10 seconds' moving image.

C. Periodically change background and character (image) color.

D. Avoid combination of background and character with large different luminance.

(3) Periodically adopt one of the following actions after long time display.

A. Running the screen saver (motion picture or black pattern)

B. Power off the system for a while

(4) LCD system is required to place in well-ventilated environment. Adapting active cooling system is highly recommended.

(5) Product reliability and functions are only guaranteed when the product is used under right operation usages. If product will be used in extreme conditions, such as high temperature/ humidity, display stationary patterns, or long operation time etc…, it is strongly recommended to contact ADP for filed application engineering advice. Otherwise, its reliability and function may not be guaranteed. Extreme conditions are commonly found at airports, transit stations, banks, stock market and controlling systems.

11.4. Electrostatic Discharge Control

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wristband etc. And don't touch interface pin directly.

11.5. Precautions for Strong Light Exposure

(1) Strong light exposure causes degradation of polarizer and color filter.

(2) To keep display function well as a digital signage application, especially the component of TFT is very sensitive to sunlight, it is necessary to set up blocking device protecting panel from radiation of ambient environment.

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11.6. Storage

When storing modules as spares for a long time, the following precautions are necessary.

(1) Store them in a dark place. Do not expose the module to sunlight or fluorescent light. Keep the temperature between 5℃ and 35℃ at normal humidity.

(2) The polarizer surface should not come in contact with any other object. It is recommended that they be stored in the container in which they were shipped.

(3) Storage condition is guaranteed under packing conditions.

(4) The phase transition of Liquid Crystal in the condition of the low or high storage temperature will be recovered when the LCD module returns to the normal condition.

11.7. Handling Precautions for Protection Film

(1) The protection film is attached to the bezel with a small masking tape. When the protection film is peeled off, static electricity is generated between the film and polarizer. This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.

(2) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the bezel after the protection film is peeled off.

(3) You can remove the glue easily. When the glue remains on the bezel or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

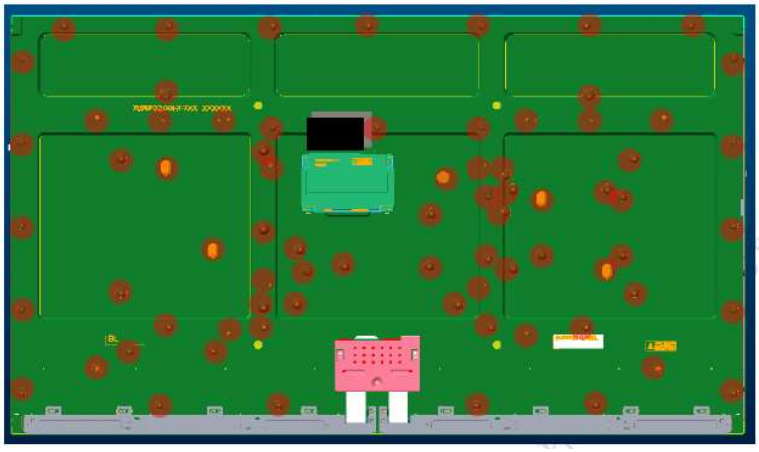
11.8. Dust Resistance

(1) ADP module dust tests are conducted with marked areas (e.g., holes and slits around the front bezel and back cover) sealed, to comply with JIS D0207 (see Figure 1).

(2) To prevent particles from entering the module, please ensure the set has all the highlighted areas (holes and slits) adequately sealed or covered by set mechanism.

(3) ADP's testing procedure cannot replicate all real world operation scenarios. It is up to the module user to apply the most appropriate dust resistance solution for its particular application.

Figure 1



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