# 產品承認書

## *Specification for Approval*

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# FM-1288

## High Performance Voice Processor for Automotive Handsfree

Product Data Sheet
(Product Information) version 2.3

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# Status Information

The status of this Product Data Sheet is **Product Information**.

### Advance Information

Information for designers concerning Fortemedia product in development. All values specified in the document are the target values of the design. Minimum and maximum values, if specified, are only given as guidance to the final specification limits and must not be considered as the final values.

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### Product Information

Final Data Sheet including the guaranteed minimum and maximum limits for the electrical specifications.

Product Data Sheets supersede all previous document versions.

### Note

While every case has been taken to ensure the accuracy of the contents in this Data Sheet, Fortemedia cannot accept responsibility for any errors. Fortemedia reserves the right to make technical changes to its products as part of its development program.

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| 2.2 | Jan 06, 2015 | Clarified VDD_D and VDD_A , pp. 49 |
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# 1. Introduction

FM1288 is the new generation of Fortemedia's system-on-chip (SOC) solution that provides high performance voice processing for automotive hands-free applications. It delivers state of the art single-microphone and dual-microphone noise suppression with acoustic echo cancellation technologies for in-vehicle and personal navigation devices (PND) based hands-free voice communications.

## 1.1 Overview

Incorporating the latest Fortemedia technologies for removing ambient noise and acoustic echoes, the FM1288 preserves voice naturalness for greater speech intelligibility in a variety of noisy automotive enviroments. Designed to be compatible with a wide range of host processors and blue-tooth devices, the FM1288 voice processor is designed for easy system integration.

The FM1288 provides system designer the flexibilities to customize each processing module and fine-tune the algorithms to the unique needs and acoustic path characteristics of the manufacturer's automotive model cabin or handsfree communication device.

## 1.2 Key Features

- **Highly integrated SOC**
  - Digital Signal Processor(DSP) with Hardware Accelerators, RAM, and ROM
  - 3 ADC (Analog to Digital Converter)
  - 2 DAC (Digital to Analog Converter)
  - Differential I/O on all analogs to improve noise immunity
  - 2 On-chip analog microphone inputs
  - IIC-Compatible Serial (SHI) and UART control interface to host processor
  - IIS-Compatible and PCM data interface to host or Bluetooth processor
  - Built-in PLL supports highly flexible clocking input
  - Can operate as co-processor or as standalone processor
- **High performance**
  - Advanced algorithms for acoustic echo cancellation and noise reduction
  - Robust full-duplex for in-vehicle applications
  - Preserves voice naturalness and effective in automotive environment
  - Wideband (HD Voice) and narrowband voice processing
  - Bright Voice Enhancement (BVE) for downlink listening improvement
  - Dynamic Range Control (DRC) for range control
  - Equalization (EQL) on uplink and downlink voice paths
  - Line in and Line out signal path Automatic Gain Control (AGC)
  - Configurable processing modules performance
  - Non-invasive run-time performance tuning via UART and IIC-compatible port
  - Run time switching between processing mode and various by-pass modes
  - User-selectable between two microphone inputs (usage - one for front-seat passengers and another for back-seat passengers in vehicle cabins)
- **Available in 48-pin LQFP packages, Automotive Grade**

## 1.3 Pin Configuration (LQFP)

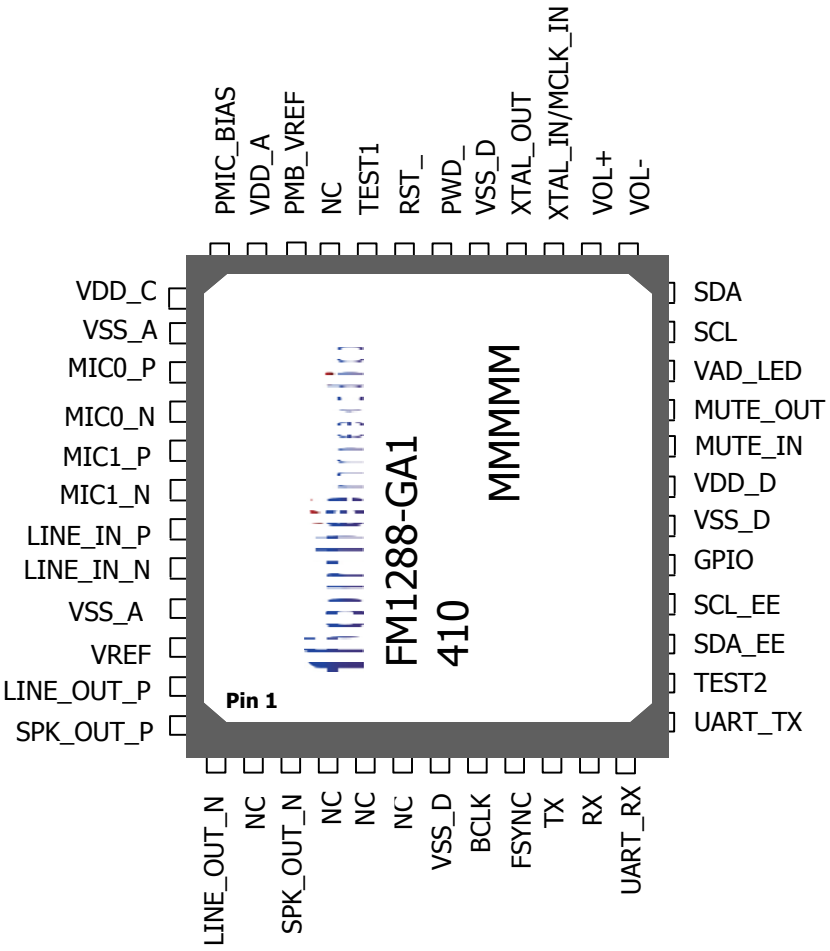



**Figure 1: LQFP 48-Pin Configuration -Top View**

## 1.4 Device Terminal Functions

| Analog Audio I/O | Lead | Pad Type | Supply Domain | Description |
|---|---|---|---|---|
| **LINE_OUT_N** | 1 | Analogue | VDD_A | Audio LINE OUTPUT (-) |
| **LINE_OUT_P** | 47 | Analogue | VDD_A | Audio LINE OUTPUT (+) |
| **SPK_OUT_N** | 3 | Analogue | VDD_A | Audio SPEAKER OUTPUT (-) |
| **SPK_OUT_P** | 48 | Analogue | VDD_A | Audio SPEAKER OUTPUT (+) |
| **LINE_IN_N** | 44 | Analogue | VDD_A | Audio LINE INPUT (-) |
| **LINE_IN_P** | 43 | Analogue | VDD_A | Audio LINE INPUT (+) |
| **MIC0_N** | 40 | Analogue | VDD_A | Audio MIC INPUT (-) |
| **MIC0_P** | 39 | Analogue | VDD_A | Audio MIC INPUT (+) |
| **MIC1_N** | 42 | Analogue | VDD_A | Audio MIC INPUT (-) |
| **MIC1_P** | 41 | Analogue | VDD_A | Audio MIC INPUT (+) |

| Oscillator and Clock | Lead | Pad Type | Supply Domain | Description |
|---|---|---|---|---|
| **XTAL_IN/MCLK_IN** | 27 | Digital | VDD_D | For crystal or external clock in |
| **XTAL_OUT/MCLK_OUT** | 28 | Digital | VDD_D | Drive for crystal |

| Serial EEPROM | Lead | Pad Type | Supply Domain | Description |
|---|---|---|---|---|
| **SDA_EE** | 15 | In/Out | VDD_D | IIC-compatible EEPROM Data |
| **SCL_EE** | 16 | In/Out | VDD_D | IIC-compatible EEPROM Clock |

| Serial Host Interface (SHI) | Lead | Pad Type | Supply Domain | Description |
|---|---|---|---|---|
| **SDA** | 24 | In/Out | VDD_D | IIC-compatible serial slave data |
| **SCL** | 23 | In/Out | VDD_D | IIC-compatible serial slave clock |

| UART Interface | Lead | Pad Type | Supply Domain | Description |
|---|---|---|---|---|
| **UART_RX** | 12 | In | VDD_D | UART receive |
| **UART_TX** | 13 | Out | VDD_D | UART transmit |

| Digital Audio I/O (PCM/IIS) | Lead | Pad Type | Supply Domain | Description |
|---|---|---|---|---|
| **BCLK** | 8 | In/Out | VDD_D | Synchronous data clock |
| **FSYNC** | 9 | In/Out | VDD_D | Synchronous data sync |
| **TX** | 10 | Out | VDD_D | Synchronous data output |
| **RX** | 11 | In | VDD_D | Synchronous data input |

| Controls | Lead | Pad Type | Supply Domain | Description |
|---|---|---|---|---|
| **TEST2** | 14 | Digital | VDD_D | Voice data by-pass control |
| **GPIO** | 17 | Digital | VDD_D | GPIO, usage currently undefined |
| **MUTE_IN** | 20 | Digital | VDD_D | Input control, mutes Line-Out |
| **MUTE_OUT** | 21 | Digital | VDD_D | Mute speaker indicator output |
| **VAD_LED** | 22 | Digital | VDD_D | Voice activity indicator output |
| **VOL-** | 25 | Digital | VDD_D | Volume decrease control |
| **VOL+** | 26 | Digital | VDD_D | Volume increase control |
| **PWD_** | 30 | Digital | VDD_D | Power down control |
| **RST_** | 31 | Digital | VDD_D | Reset control |

| Power Supplies | Lead | Description |
|---|---|---|
| **VDD_A** | 35 | Positive supply for analog circuitry, to 3.3V power supply |
| **VDD_D** | 19 | Positive supply for digital input/output, to 1.8V/3.3V power supply<br>(see **Table 15a/b/c** for details) |
| **VSS_D** | 7,18,29 | Ground Connection – Digital Ground |
| **VSS_A** | 38,45 | Ground Connection – Analog Ground |
| **VDD_C** | 37 | Connect via 1uF capacitor to ground, decoupling capacitor is for internal LDO that generates 1.2V for IC internal circuitry. |
| **PMB_VREF** | 34 | Connect via 0.47uF capacitor to ground, reference voltage for MIC Bias |
| **PMIC_BIAS** | 36 | Microphone Bias output, providing mic bias voltage = 0.9 * VDD_A |

## 1.5 Internal Hardware Block Diagram

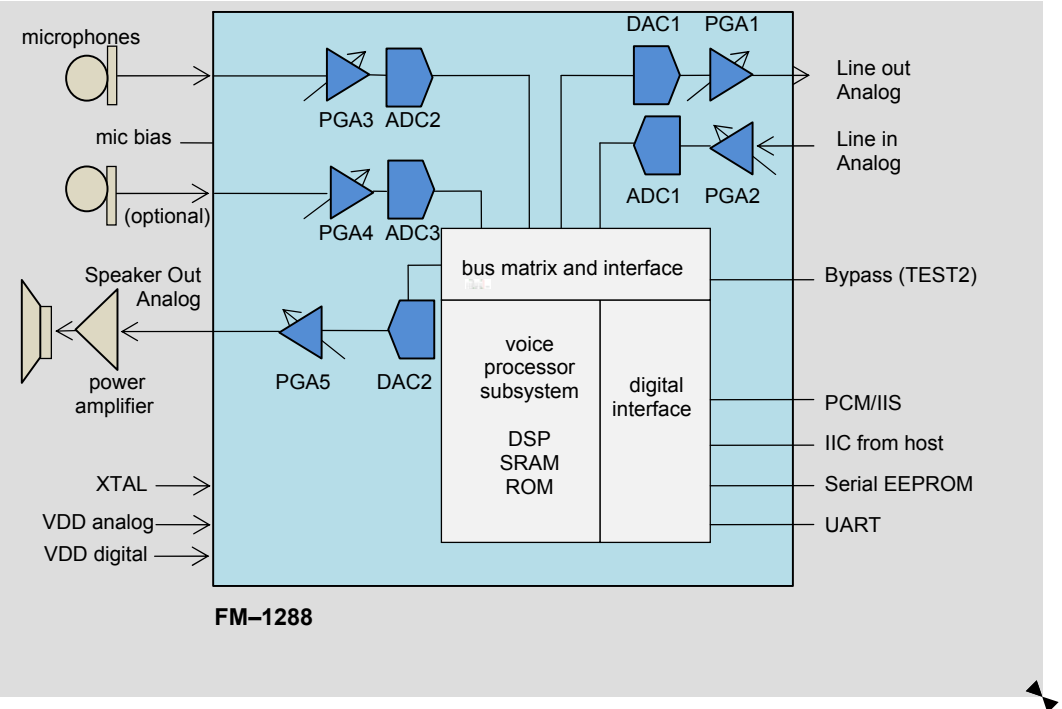
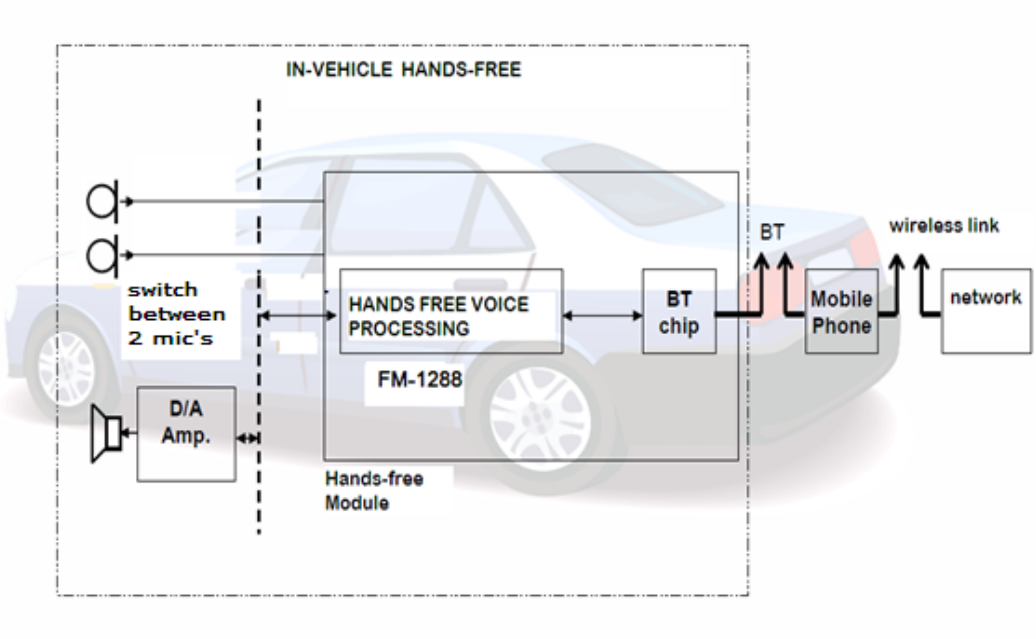



**Figure 2: IC Hardware Block Diagram**

## 1.6 System Application Block Diagram



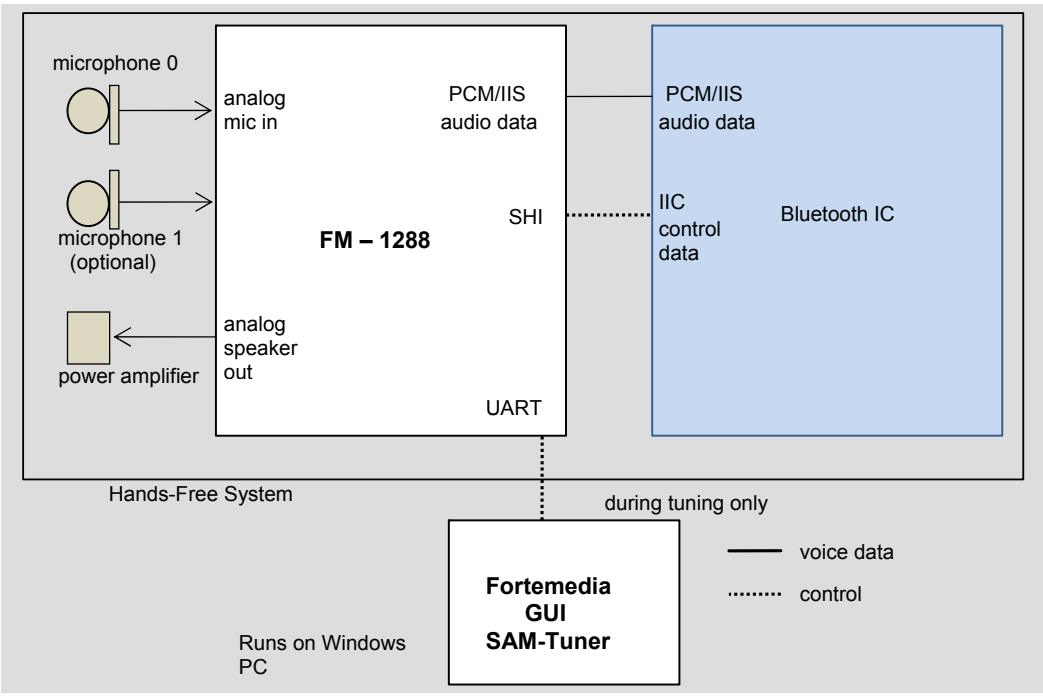




**Figure 3: Example Bluetooth Application Block Diagrams**

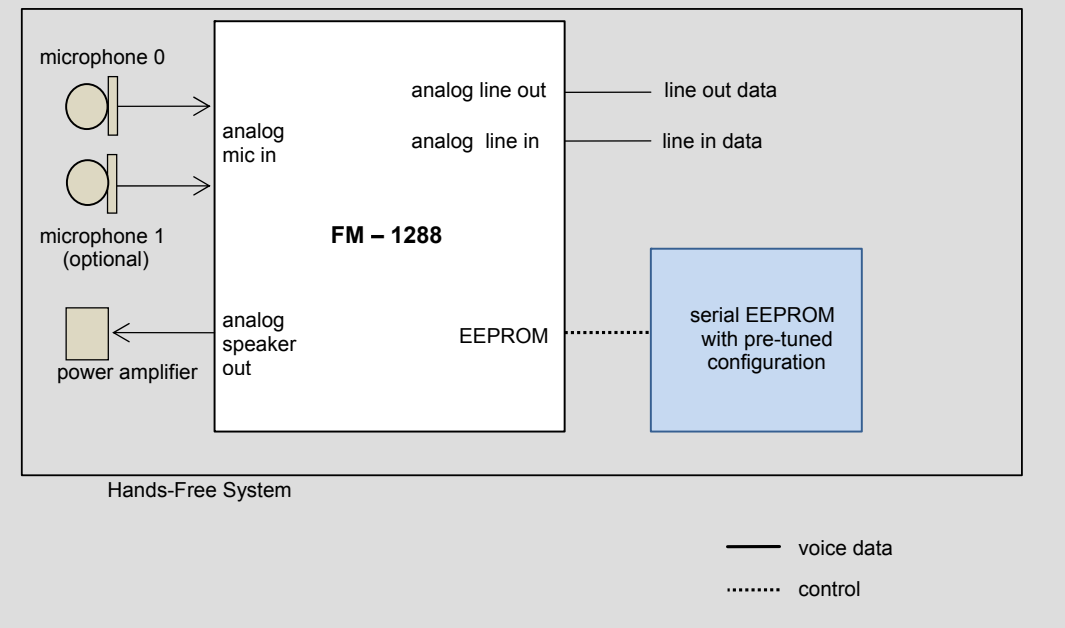



**Figure 4: FM-1288 as an example Stand-alone Minimal System**

# 2. Functional Description

## 2.1 Overview

The FM1288 voice processor digitizes the microphone input of near-end talker signal and performs acoustic echo cancellation and noise suppression on it, further enhancements such as gain adjustment and equalization can also be conducted. The processed signal is sent either through the PCM Serial Port digitally, or through the D/A converter and then via Line_Out pin as analog output. The far-end talker signal enters as the line input signal either digitally from Serial PCM Port, or from the Line_In analog signal pin. This far-end talker signal could be further enhanced by signal processing, such as Bright Voice Enhancement, Equalization, or Dynamic Range Control, before sending out to the analog SPK_Out pin via the D/A.

## 2.2 Serial EEPROM Interface (Pins 15, 16)

FM1288 supports an optional serial EEPROM boot-up, should the user elect to design the system with it. The serial EEPROM is used for

- Storing the configuration parameters required for system initialization during power-up and reset, should the system designer elect this option, and
- Storing "patch-program" provided by Fortemedia for either functional customizations or bug-fixes

It supports 16Kbit or larger IIC EEPROM devices such as 24c16, 24c32, 24c64, etc.

Upon power-up or reset, the FM-1288 processor will automatically attempt auto-detect via read operations from the serial EEPROM interface. If the system design includes an EEPROM and the EEPROM content conforms to the EEPROM format description below, the FM-1288 will be initialized to the pertinent state and becomes functional.

The EEPROM content are organized into contiguous bytes starting from address zero:

| Byte Address | Byte content | Comment |
|---|---|---|
| 0 | Any value | **First byte always a dummy byte** |
| 1 | Byte 1 command 1 | **Each EEPROM command sequence is 6 bytes** |
| 2 | Byte 2 command 1 | |
| 3 | Byte 3 command 1 | |
| 4 | Byte 4 command 1 | |
| 5 | Byte 5 command 1 | |
| 6 | Byte 6 command 1 | |
| 7 | Byte 1 command 2 | |
| 8 | Byte 2 command 2 | |
| . | . | |
| . | . | N is the last EEPROM command |
| 6N | Byte 5 command N | |
| 6N + 1 | Byte 6 command N | |
| 6N + 2 | **Must be 0xF0** | **Last byte ends read operation** |

When the FM-1288 processor reads from the EEPROM, it interprets the content according to the data organization depicted above, and executes the commands sequentially to perform initialization. Each command is constituted of a 6-byte sequence instructing the processor to perform an initialization to either the data memory (**DM**) space or program memory(**PM**).

The FM-1288 has an on-chip Harvard-architecture Digital Signal Processor (**DSP**) which works with separate on-chip data memory and instruction memory. The data memory is of 16-bit data width and program memory is of 24-bit data width, and each has 16-bit address. The initialization data and on-chip program are stored in on-chip Read-Only Memories (ROM). There is on-chip RAM (Random Access Memory) as well for data manipulation.

The instruction memory space is further divided into ordinary instruction memory on ROM and a small patch-RAM (Random Access Memory). This patch-RAM allows further enhancements or bug-fixes to the on-chip ROM code.

The data memory space are divided into ordinary data memory on the on-chip RAM and a set of memory-mapped control registers.

| **FM-1288** | | | | |
|---|---|---|---|---|
| **Memory Space** | **Content** | **Type** | **Data width** | **Can be written to by EEPROM command** |
| **DM** | data | RAM | 16 bit | yes |
| | control data | Memory-mapped Control Registers | 16 bit | yes |
| **PM** | program instruction | ROM | 24 bit | no |
| | Patch RAM | RAM | 24 bit | yes |

Therefore, each 6-byte instruction residing on the EEPROM belongs to one of the following.

| **EEPROM Program Memory Space Write Command** | | |
|---|---|---|
| **Byte** | **Byte content** | **Comment** |
| 1 | **0x5C** | Command byte |
| 2 | address high byte (bit 8 to 15) | Address to write Program Instruction |
| 3 | address low byte ( bit 0 to 7) | |
| 4 | instruction high byte (bit 16 to 23) | Program Instruction itself |
| 5 | instruction middle byte (bit 8 to 15) | |
| 6 | instruction low byte (bit 0 to 7) | |

| **EEPROM Data Memory Space Write Command** | | |
|---|---|---|
| **Byte** | **Byte content** | **Comment** |
| 1 | **0x3B** | Command byte |
| 2 | address high byte (bit 8 to 15) | Address to write Data |
| 3 | address low byte ( bit 0 to 7) | |
| 4 | data high byte (bit 8 to 15) | Data itself |
| 5 | data low middle byte (bit 0 to 7) | |
| 6 | 0x00 | Meaningless dummy byte |

Aside from the simple rules of starting with a dummy value at the first byte of the EEPROM and ending with the last byte with a value of 0xF0, the very last EEPROM command must be 6-byte command of writen the value 0x0000 into the DM address 0x22FB.

Lastly, for writing into the Program Memory Space Patch RAM there is a simple rule that the user must adhere to:

1. First must execute an EEPROM write command to the DM memory space address 0x3FCB, value = 0x0010 ;
2. Then do the EEPROM write command into Patch RAM sequentially ; and
3. After all writes into Patch RAM has finished, then do an EEPROM write command to DM memory space address 0x3FCB, value = 0x0000.

When the EEPROM is designed to be the source to initialize the parameters after reset, the FM1288 automatically detects the EEPROM via read attempts, and then retrieves data continuously in burst mode until

- Either the end of transfer byte "0xF0" is detected on the EEPROM,
- Or the DM address 0x22FB is being cleared to 0x0000.

The FM1288 will then enter into the normal operation mode.

Summarizing about EEPROM commands:

- The EEPROM commands can be used for boot-up system initialization.
- Data on EEPROM are contiguous bytes that must be organized into a starting dummy byte at address 0x0000 of the EEPROM, followed by 6-byte EEPROM commands defined above, and then concluded with an ending indicator of 0xF0 to signal termination of EEPROM command operations
- The 6-byte commands are each an initialization write either into DM space or into PM space
- The last EEPROM command should be a 6-byte command of writen the value 0x0000 into the DM address 0x22FB, this is to inform the FM-1288 processor that the last EEPROM command has been executed
- For writes into the Patch RAM area of the PM space, the rule of setting a specific DM memory space location at 0x3FCB first, and then clearing it upon done, was descrbed above and must be followed

System designers using the EEPROM please note the following:

1. Patch RAM initializations are intended for either bug fixes or further functional enhancements to the on-chip program residing already on ROM. Therefore Patch-RAM write comands, if any, will be provided by Fortemedia.
2. Data initialization are intended for either affecting the functional behaviors or for improving the performance via loading specifically tuned parameters over the default ones. Therefore Control Register and Data write commands, if any, are either provided by Fortemedia or supplied by the system designer after performing system tuning to obtain optimal parameters. Please also see "FM-1288 User Configuration Manual" for system tunings.
3. 24C16 is the smallest EEPROM size that the user can use.

The following detail normally does not concern system designer, but it affects the EEPROM size and is therefore included here for completeness. Fortemedia engineers working on the Patch RAM commands and Data Initialization commands on the EEPROM would need to understand these details:

| **EEPROM - maximum space utilization by commands** | | |
|---|---|---|
| | **Maximum Size** | **Effect on EEPROM** |
| PATCH RAM | 128 | A maximum of 128 x 6 = 768 bytes could be occupied by Patch RAM initializations on the EEPROM |
| Data space initialization associated with code to reside on PATCH RAM | 32 | A maximum of 32 x 6 = 192 bytes could be occupied by Data initializations associated with Patch RAM code on the EEPROM |

## 2.3 UART Interface (Pins 12, 13)

FM1288 has an UART interface which could be used to

- Transmit and receive control commands at run-time, and
- Also by the host processor to supply the necessary initialization configuration parameters during reset and power-up, should the system designer elect this option.

To use the UART interface immediately after power up, the clock/crystal frequency supplied to the FM-1288 must be an integer multiple of 18.432 MHz in order for the UART baud rate to communicate to the commonly used baud rate which would be an integer multiple of 9600.

| Clock/Crystal Input | UART baud rate after boot up |
|---|---|
| 4.608 MHz | 2400 baud |
| 9.216 MHz | 4800 baud |
| 18.432 MHz | 9600 baud |
| 36.864 MHz | 19200 baud |

Each UART transfer will have one command byte, one or two address bytes, and up to two data bytes. UART requires two bytes "**0xFC**" and "**0xF3**" to synchronize with each transfer.

The UART port is recommended as the run-time performance optimization interface to access the FM1288 for real-time non-invasive parameter tunings.

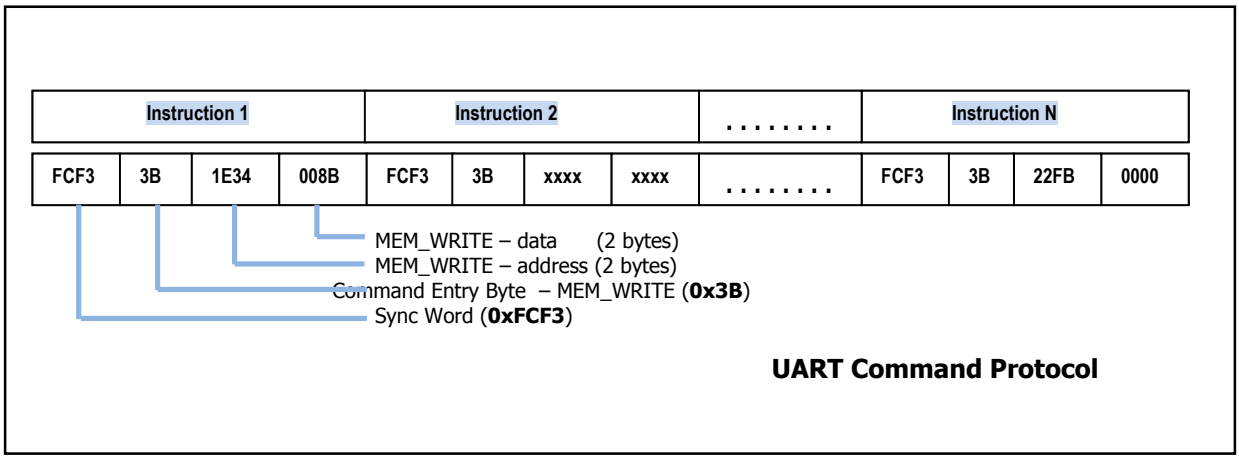
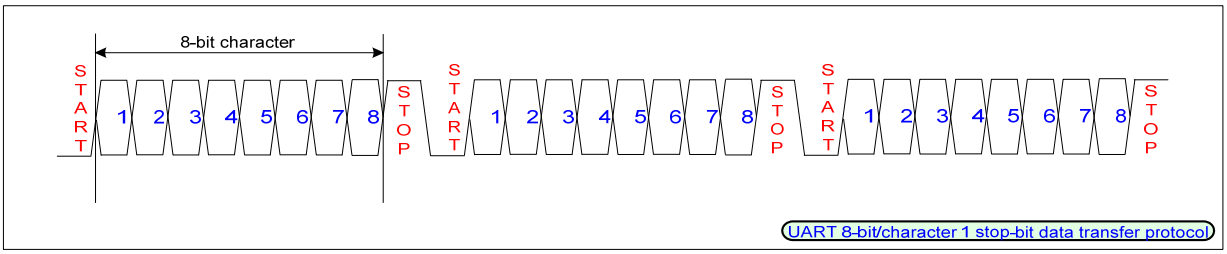



**Figure 5: Example UART Command Protocol**




UART_RX and UART_TX pins are normally held high between transfers

**Figure 6: UART Data Transfers (TX and RX)**

## 2.4 IIC compatible Serial Host Interface - SHI (Pins 23, 24)

The FM1288 implements a Serial Host Interface (SHI) which is an IIC-compatible serial interface between FM1288 and an external processor. It could be used to

- Transmit and receive control commands at run-time, and
- Also by the host processor to supply the necessary initialization configuration parameters during reset and power-up, should the system designer elect this option.

On this SHI, FM1288 communicates to the processor through a bi-directional serial data line (SDA) and a serial clock line (SCL). The FM-1288 SHI operates as a slave device and its serial clock is driven from the host. The master on the host processor controls SCL clocking, data transfer start bit and stop bit, and also addressing of slave devices. The FM1288 supports 8-bit address and its device address is "**0xC0**".

Depending on master's instruction, the SHI can operate as a transmitter (writing data) or a receiver (reading data). Note that the SHI interface supports the standard clock speed of 100 kHz or up to a maximum speed of 400 kHz (if MCLK is above 10MHz).

The standard byte format of SHI data line (Pin 24) must be 8–bit long in every byte. Each byte consists of 8 bits plus 1 acknowledge bit, and it is one data bit per clock pulse. If operating as a receiver, it will return an acknowledge bit upon each successful byte transfer, otherwise it will return a NOACK signal. There is no restriction on the maximum number of bytes per data transfer. Data transfer can be aborted if the master device generate a STOP condition to terminate a transfer. Each data transfer frame must start with a START or a RESTART symbol and ends by a STOP symbol.

**Table 1: SHI START and STOP data transition**

| | |
|---|---|
| S: START | SDA transition from 1 to 0 when SCL=1 |
| P: STOP | SDA transition from 0 to 1 when SCL=1 |

Within the data transfer frame, multiple command sequences are allowed and there is no restriction on the maximum numbers of bytes per frame. Each command sequence starts with a sync word "0xFCF3", follows by a command entry byte (e.g. 0x3B is MEM_WRITE) and number of bytes per specific command. The following figures and tables summarize the details for the SHI command sequence.

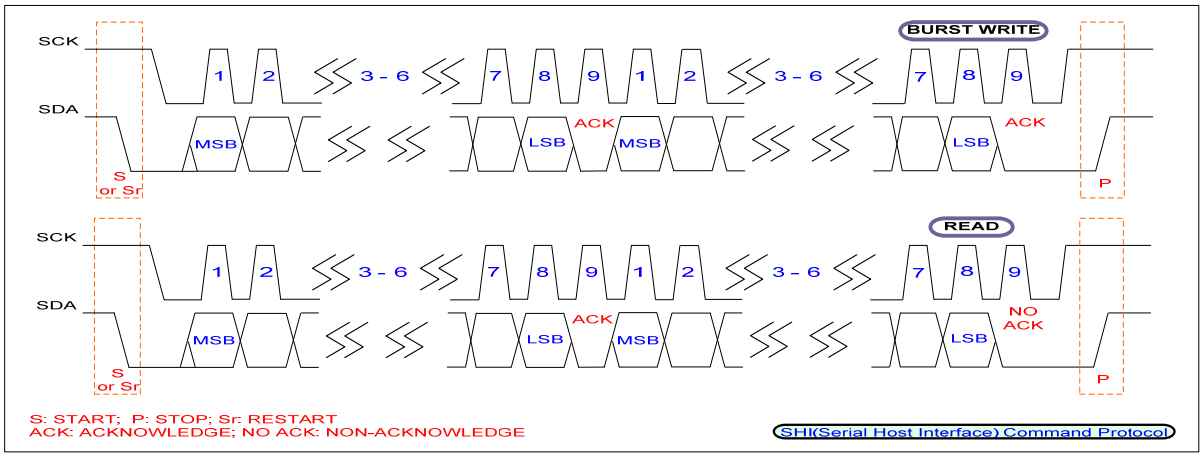



**Figure 7: SHI Data Transfer Command Protocol**

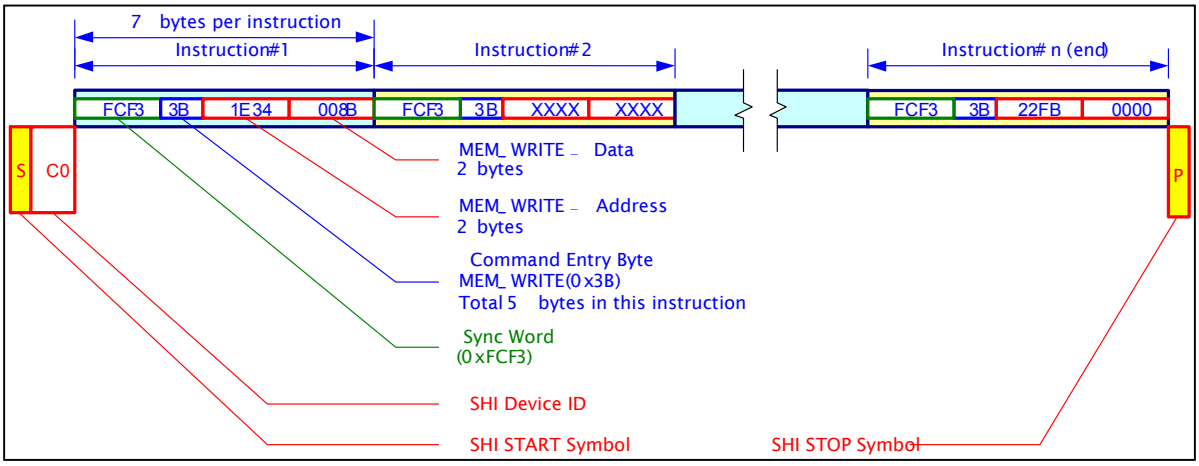



**Figure 8: SHI Command Sequence**

**Table 2: SHI Command Name**

| Command Entry Name Symbol | Command Entry Byte | Number of the bytes for each functional bytes | | |
|---|---|---|---|---|
| | | Address Byte | Data Byte | Total (cmd+address+data) |
| MEM_WRITE | 0x3B | 2 | 2 | 5 |
| MEM_READ | 0x37 | 2 | 0 | 3 |
| REG_READ | 0x60 | 1 | 0 | 2 |

**Table 3: SHI Command Byte - format**

| Serial Command Entry Byte | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Bit** | **D7** | **D6** | **D5** | **D4** | **D3** | **D2** | **D1** | **D0** |
| **Description** | Access object type | | | | Read /Write | Data byte number | | Address byte number |
| **Value Details** | Data Memory (0011b)<br>DataPort(0110b)(e.g. register) | | | | R: 0<br>W: 1 | 2bytes (01b)<br>1byte (00b)<br>0byte (11b) | | Two address bytes(1b)<br>Data memory access<br>One address byte(0b)<br>Data port access |

**Table 4: SHI Command Byte – bit definition**

| Data length | 1byte | |
|---|---|---|
| **Bit** | **Pattern** | **Descriptions** |
| D7 - D4 | 0011b | For accessing Data Memory |
| | 0110b | For reading the Data ports. |
| D3 | 0b | Read |
| | 1b | Write |
| D2-D1 | 00b | 1 byte data write, or in Data Port Read mode. |
| | 01b | 2 bytes data write |
| | 11b | 0 byte data (in Data Memory Read mode). |
| D0 | 1b | Two address bytes for accessing Data Memory |
| | 0b | One address byte for reading Data Port (Either 0x25 for lower byte or 0x26 for upper byte. |

## 2.5 Digital Voice Data Interfaces (Pins 8, 9, 10,11)

The FM1288 supports PCM/IIS serial interface to an external processor or device for digital voice data transfer of PCM/IIS encoded audio data. The digital voice data interface consists of four pins and these pins are multiplexed to be used as either PCM serial interface or IIS serial interface. The pin definition is described in the following table.

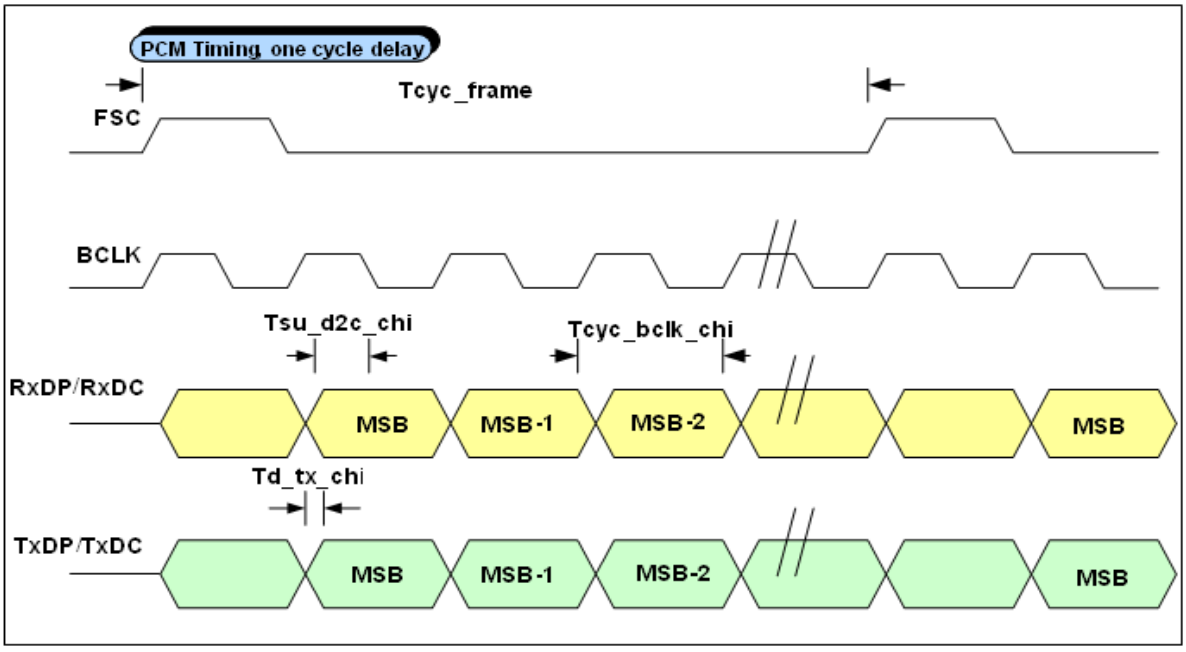
**Table 5: Digital Voice Data Interface ( Pins 8, 9, 10, 11)**

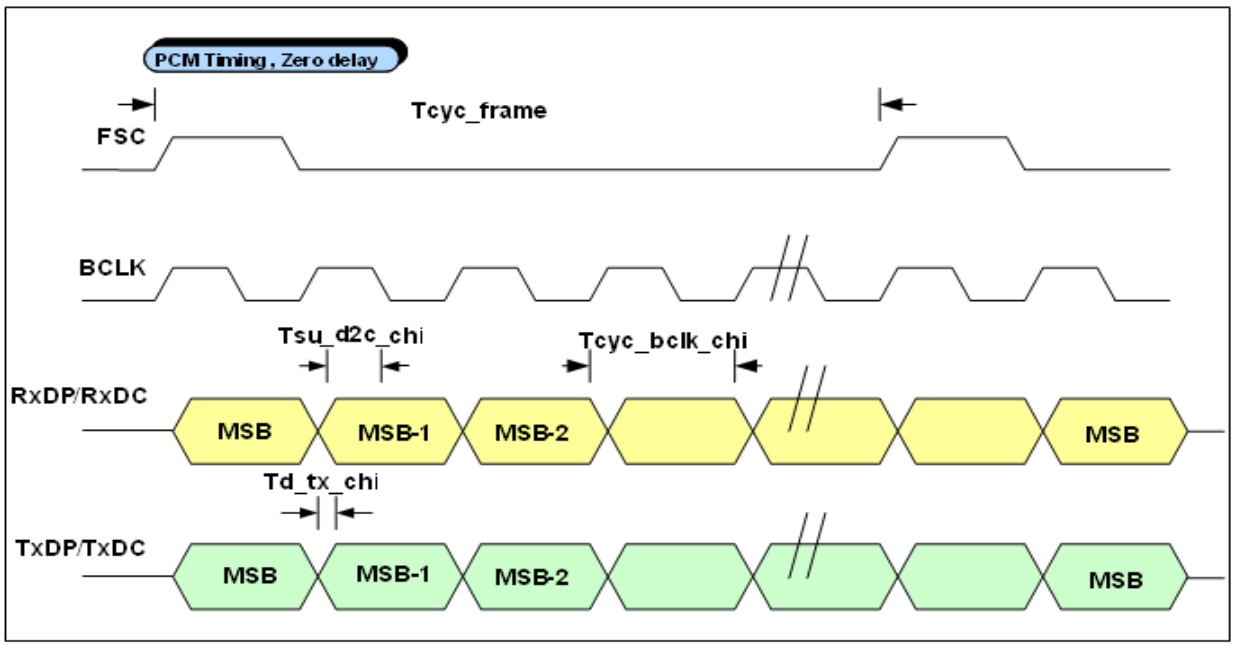
| | PIN Name | Usage: PCM mode | Usage: IIS mode |
|---|---|---|---|
| **Pin 8** | **BCLK** | PCM BCLK | IIS BCLK |
| **Pin 9** | **FSYNC** | PCM FSC | IIS LRCK |
| **Pin 10** | **TX** | PCM OUT | IIS TxDP |
| **Pin 11** | **RX** | PCM IN | IIS RxDP |

### 2.5.1 PCM Interface Master/Slave

The PCM serial port provides an interface to a host processor for digital voice data transfer. It could either operate in master or in slave mode, supporting, respectively, either an internal or an external clock source for the frame sync (FSYNC) and bit clock (BCLK) signals. The FSYNC runs at 8KHz and 16KHz rate, depending on the voice data sampling rate.

The figures below show the PCM timings with two different cycle delays.




PCM Timing , Zero delay
Tcyc_frame
FSC
BCLK
Tsu_d2c_chi
Tcyc_bclk_chi
RxDP/RxDC
MSB
MSB-1
MSB-2
MSB
Td_tx_chi
TxDP/TxDC
MSB
MSB-1
MSB-2
MSB

## 2.5.2 IIS Interface

When configured as IIS interface, the master/slave mode, delay and bit width, RxDP latch, and LRCK mapping to the left or right channel are all to be configured appropriately according to the system usage. If it is set to master mode, BCLK and LRCK frequencies are defined by system designer.

The following diagrams illustrate the different types of IIS timings in terms of cycle delay, edge latch and LRCK high for channels.

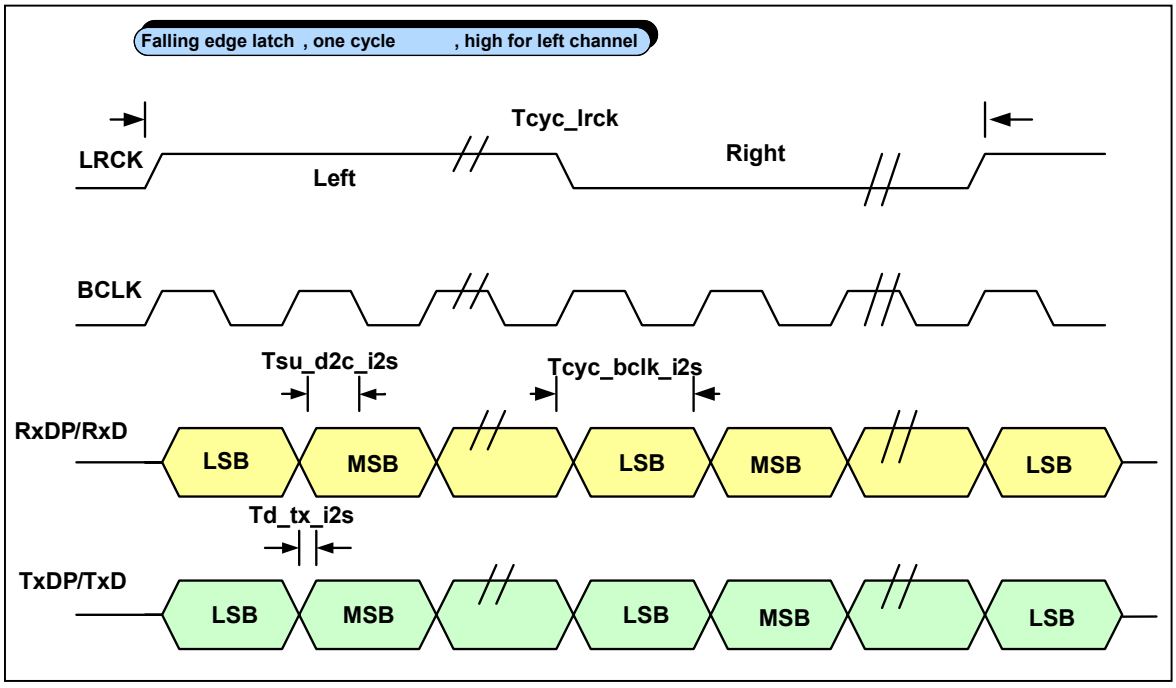



**Figure 9: IIS Falling Edge Latch, LRCK High for Left Channel, 1 Cycle Delay**

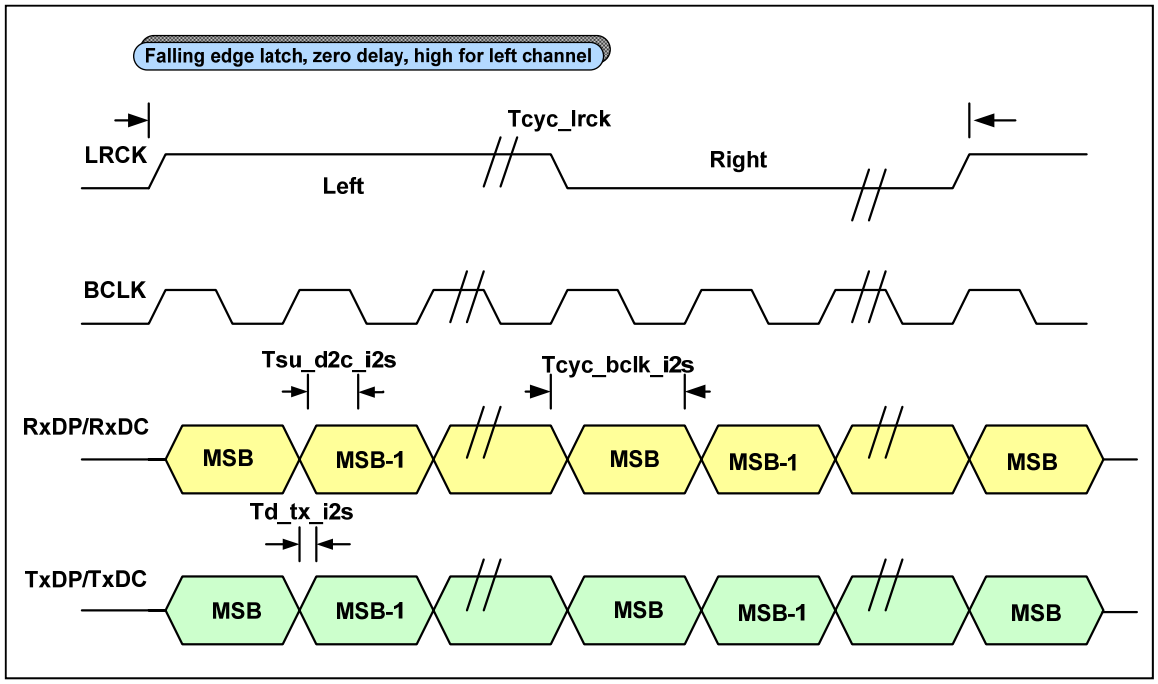



**Figure 10: IIS Falling Edge Latch, LRCK High for Left Channel, 0 Cycle Delay**

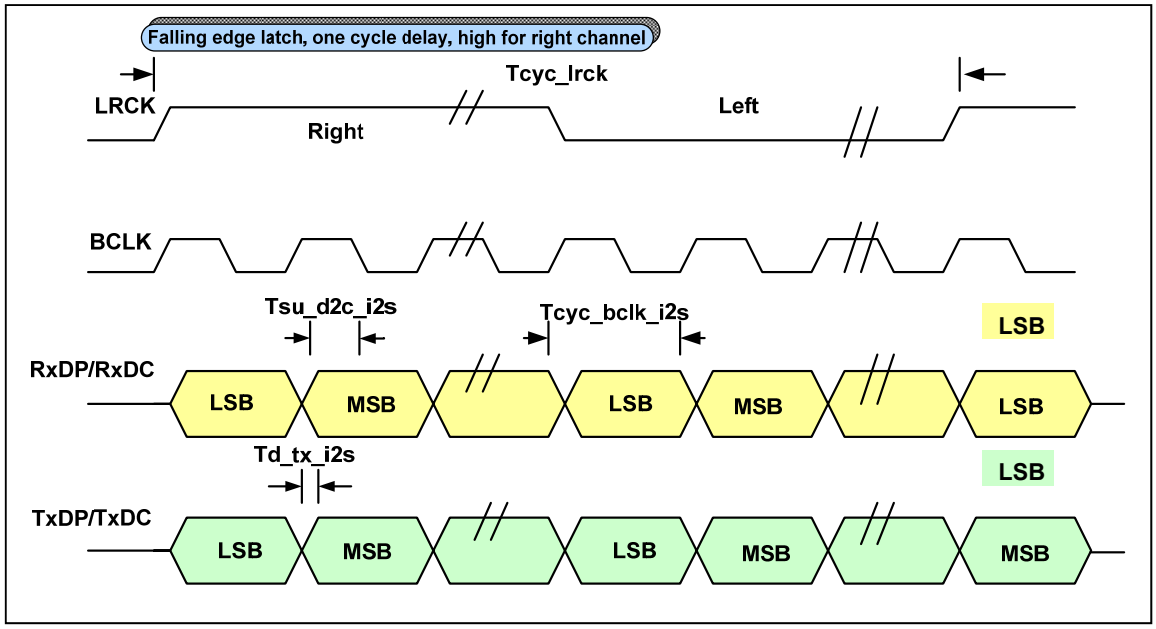



**Figure 11: IIS Falling Edge Latch, LRCK High for Right Channel, 1 Cycle Delay**

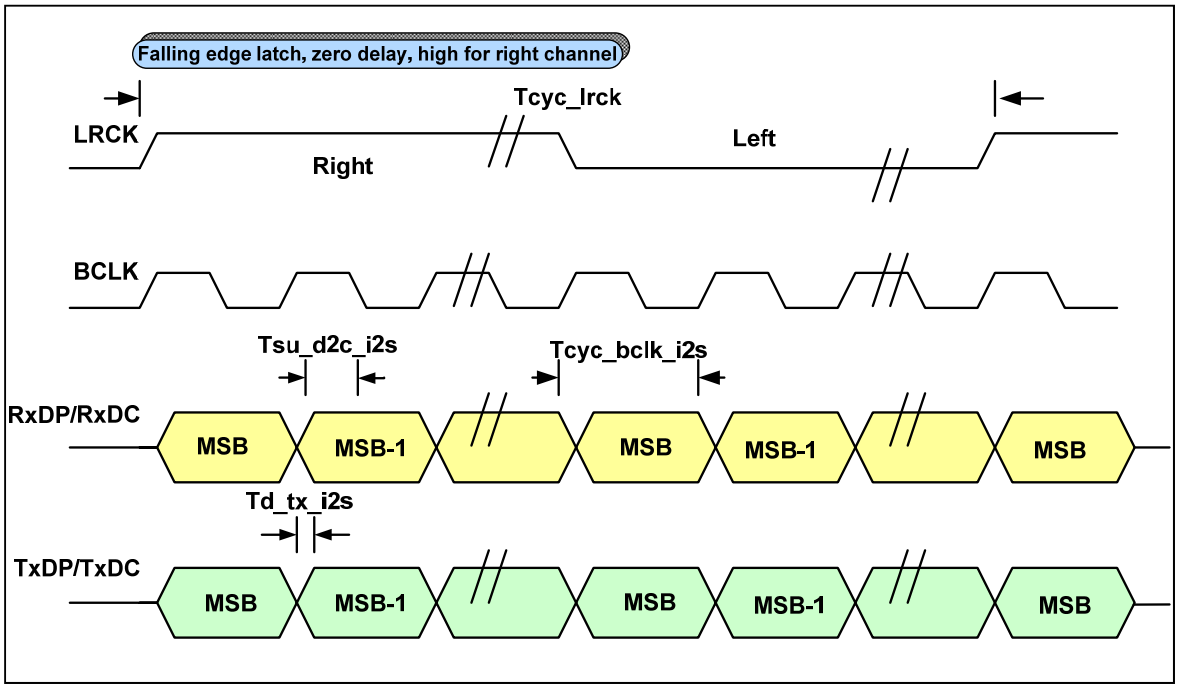



**Figure 12: IIS Falling Edge Latch, LRCK High for Right Channel, 0 Cycle Delay**

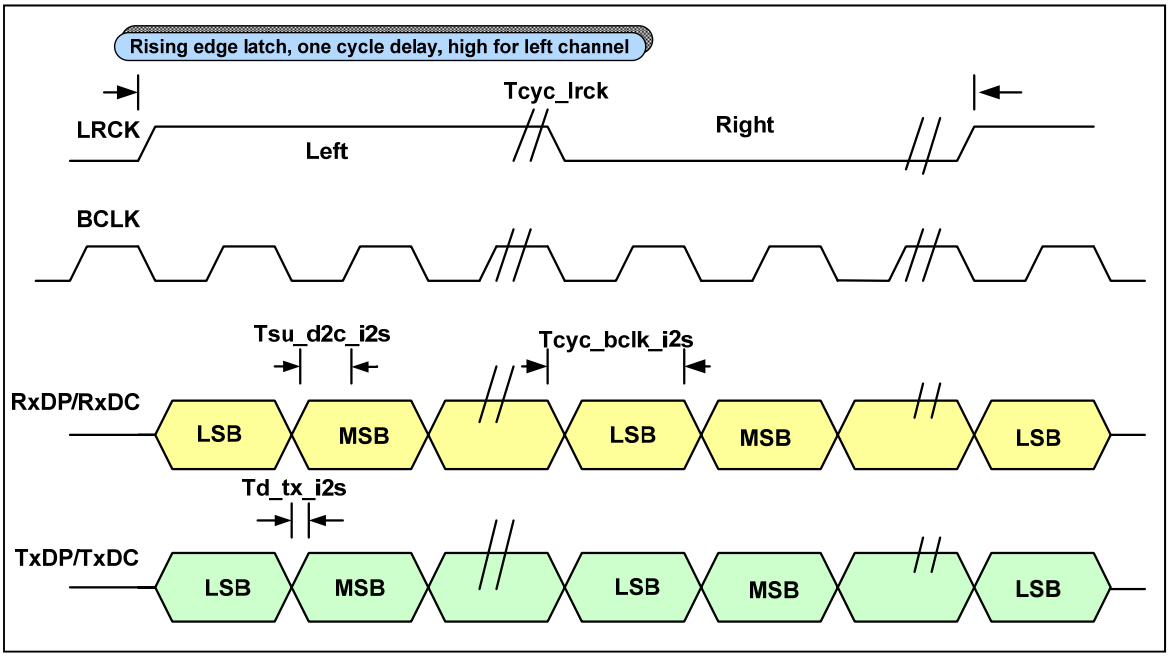



**Figure 13: IIS Rising Edge Latch, LRCK High for Left Channel, 1 Cycle Delay**

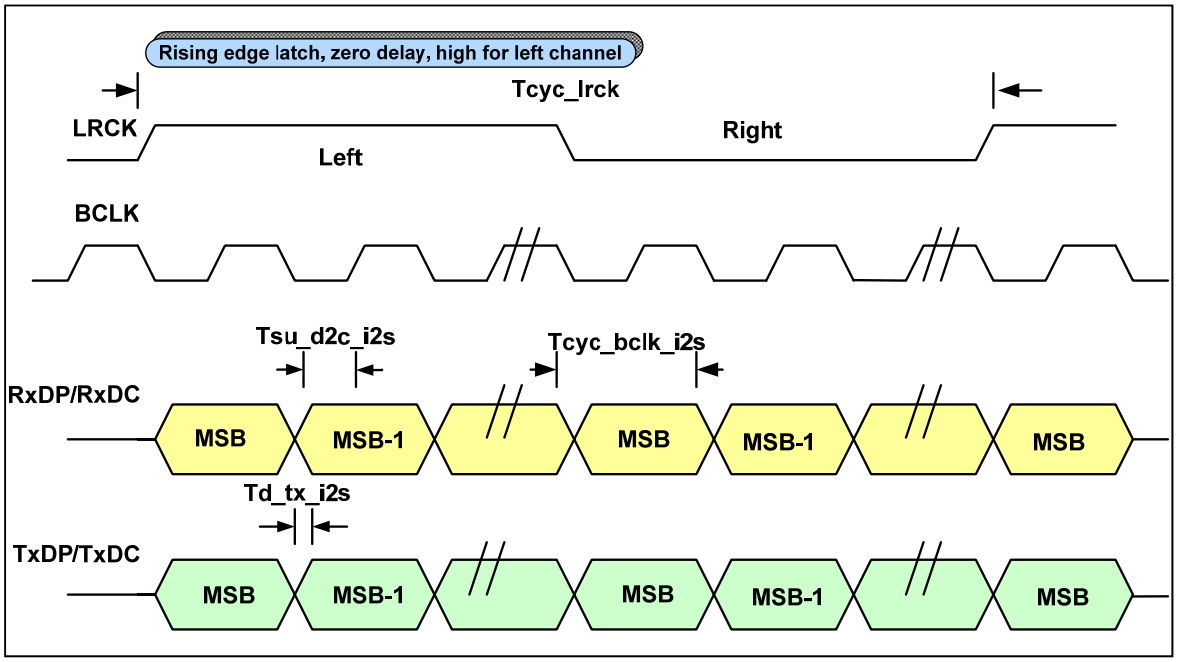



**Figure 14: IIS Rising Edge Latch, LRCK High for Left Channel, 0 Cycle Delay**

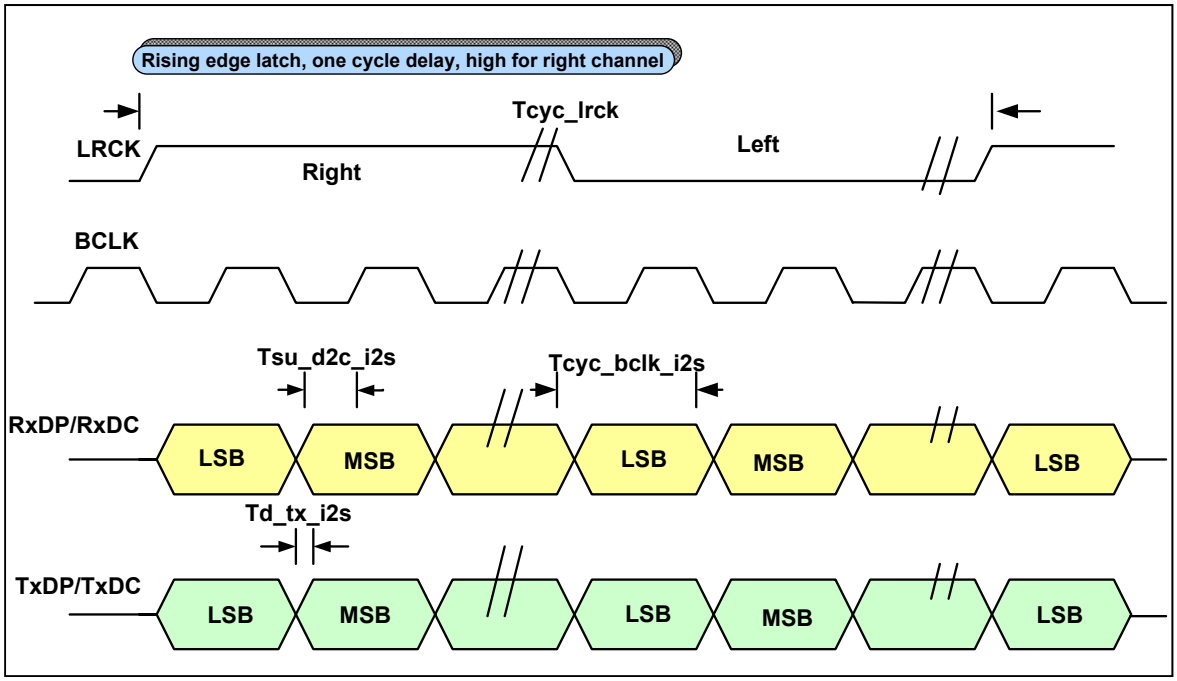



**Figure 15: IIS Rising Edge Latch, LRCK High for Right Channel, 1 Cycle Delay**

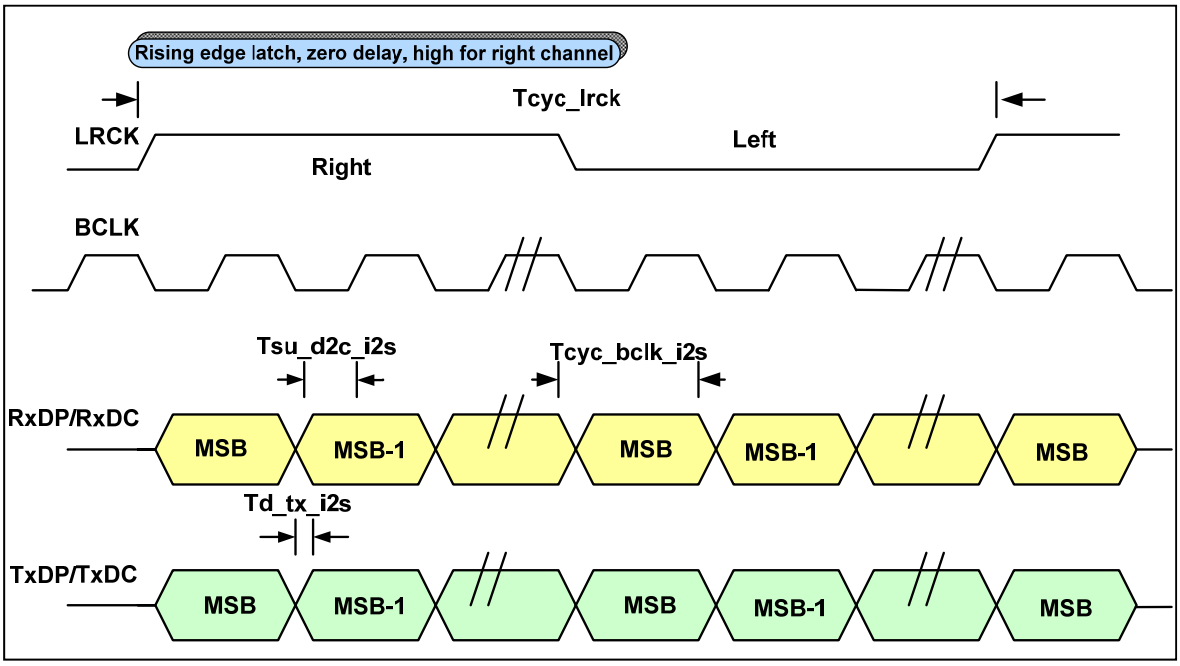



**Figure 16: IIS Rising Edge Latch, LRCK High for Right Channel, 0 Cycle Delay**

## 2.6 ADC (Pins 39, 40, 41, 42, 43, 44)

FM1288 includes three analog-to-digital converters (ADC). To the system designers these 16-bit precision Sigma Delta converters support data sampling rate at 16KHz, and all the analog inputs are differential. The MIC0_IN ADC and MIC1_IN ADC are for the primary microphone and secondary microphone inputs respectively, and the LINE_IN ADC is for line level input.

The maximum allowed differential input voltage to each of the microphone ADC's is 2.83 Vpp (at PGA gain selection value 0). The analogue gain stage has a Programmable Gain Adjustment (PGA) selection value of 0 to 15 with the associated ADC gain settings summarized in Table 6. For detailed information regarding how to set the PGA levels for each of the ADC blocks, please refer to the "*FM1288 User Configuration Manual*."

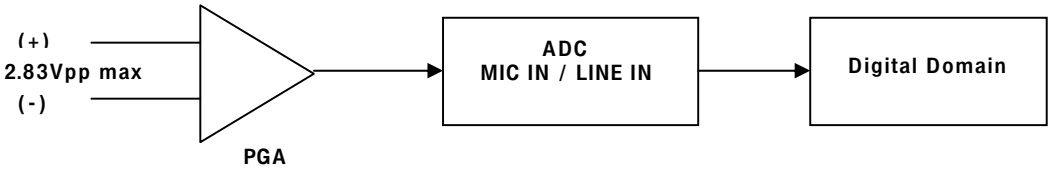



**Figure 17: Analog-to-Digital Converter Block Diagram**

**Table 6: ADC MIC_IN and LINE_IN PGA Controls**

| Gain Selection Value | PGA Gain Setting (dB) | Differential full scale Input Signal (Vpp) | Bypass Communication Gain (dB) |
|---|---|---|---|
| [ 0 0 0 0 ] | 0 | 2.83 | -2 |
| [ 0 0 0 1 ] | 1 | 2.52 | -1 |
| [ 0 0 1 0 ] | 2 | 2.25 | 0 |
| [ 0 0 1 1 ] | 4 | 1.78 | 2 |
| [ 0 1 0 0 ] | 6 | 1.42 | 4 |
| [ 0 1 0 1 ] | 8 | 1.13 | 6 |
| [ 0 1 1 0 ] | 10 | 0.89 | 8 |
| [ 0 1 1 1 ] | 12 | 0.71 | 10 |
| [ 1 0 0 0 ] | 14 | 0.56 | 12 |
| [ 1 0 0 1 ] | 16 | 0.45 | 14 |
| [ 1 0 1 0 ] | 18 | 0.36 | 16 |
| [ 1 0 1 1 ] | 20 | 0.28 | 18 |
| [ 1 1 0 0 ] | 22 | 0.22 | 20 |
| [ 1 1 0 1 ] | 24 | 0.18 | 22 |
| [ 1 1 1 0 ] | 26 | 0.14 | 24 |
| [ 1 1 1 1 ] | 28 | 0.11 | 26 |

## 2.7 DAC (Pins 1, 3, 47, 48)

FM1288 includes two digital-to-analog converters (DAC). To the system designer these 16-bit precison Sigma Delta converters support 16KHz data sampling rate, and all the analog outputs are differential. The LINE_OUT DAC is for the processed echo and noise free voice signal going towards the far end, and the SPK_OUT is for the arriving far-end voice signal going towards the near end loudspeaker.

The maximum differential output voltage from each of the DAC's is 3.0Vpp (at PGA gain selection value 0). The analogue gain stage has a Programmable Gain Adjustment (PGA) selection value of 0 to 15 with the associated DAC gain settings summarized in Table 7. For detailed information regarding how to set the analogue PGA levels for each of the DAC blocks, please refer to the "*FM1288 User Configuration Manual*."

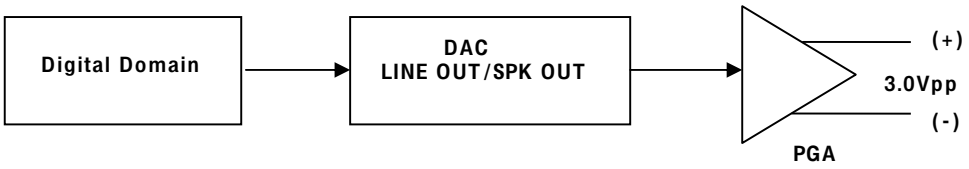



**Figure 18: Digital-to-Analog Converter Block Diagram**

**Table 7: DAC LINE_OUT and SPK_OUT PGA Controls**

| Gain Selection Value | PGA Gain Setting (dB) | Differential full scale Output Signal (Vpp) | Bypass Communication Gain (dB) |
|---|---|---|---|
| [ 0 0 0 0 ] | +2 | 3.00 | 0 |
| [ 0 0 0 1 ] | 0 | 2.40 | -2 |
| [ 0 0 1 0 ] | -2 | 1.91 | -4 |
| [ 0 0 1 1 ] | -4 | 1.51 | -6 |
| [ 0 1 0 0 ] | -6 | 1.20 | -8 |
| [ 0 1 0 1 ] | -8 | 0.95 | -10 |
| [ 0 1 1 0 ] | -10 | 0.76 | -12 |
| [ 0 1 1 1 ] | -12 | 0.60 | -14 |
| [ 1 0 0 0 ] | -14 | 0.48 | -16 |
| [ 1 0 0 1 ] | -16 | 0.38 | -18 |
| [ 1 0 1 0 ] | -18 | 0.30 | -20 |
| [ 1 0 1 1 ] | -20 | 0.24 | -22 |
| [ 1 1 0 0 ] | -22 | 0.19 | -24 |
| [ 1 1 0 1 ] | -24 | 0.15 | -26 |
| [ 1 1 1 0 ] | -26 | 0.12 | -28 |
| [ 1 1 1 1 ] | -28 | 0.09 | -30 |

## 2.8 Modes of Operation

Depending on the condition, the FM1288 operates in one of the following 4 modes.

**Hardware Reset Mode**

Whenever power is applied or RST_ is low, the processor enters into this mode and remains in it until 10ms (10 milliseconds) after the RST_ pin being pulled high. During that 10ms, the processor waits for the external clock and the internal PLL to stablize. 10ms after the RST_ pin is pulled high, the processor transitions into the Software Reset Mode.

Note that the RST_ pin should not be used as a power-down function, but instead as a power-down wake-up function.

**Software Reset Mode**

In this mode, the FM-1288 either takes command parameters from an external host through the IIC-compatible SHI, or it actively reads the configuration parameters from an external EEPROM. These commands and parameters are to establish the various operation configuration of the FM-1288. The processor has entered into the Operational Mode when the parameter value at location DM(0x22FB) has been set to 0, which is done by the FM-1288 on-chip DSP processor upon the completion of all parameter configuration.

**Operational Mode**

Entering this mode, the on-chip software sets up the hardware internal registers according to the parameter configuration and then performs a nominal 90 ms software initialization procedure. Afterwards, the FM1288 starts the data transfer from its input, performs processing, and delivers outputs through the analog/digital interfaces. While in the operational mode, whenever PWD_ pin is being asserted low, the processor transitions and enters into the Power Down Mode.

**Power Down Mode**

While in the Power Down mode, asserting the RST_ pin to high or the PWD_ pin to high will cause the FM-1288 to exit Power Down.

In the Power Down Mode, the on-chip power is switched off to reduce leakage. Also, after PWD_ pin is asserted high, external clock will be turned off after Tsu_pp2clkoff (section 4.5) to reduce leakage current.

In the Power Down Mode, if PWD_ is set to high, then the processor can either return into the Software Reset Mode or into the Operational Mode, depending on the setting of the pwrdwn_set parameter at internal location DM(0x22F1). If it enters into Operational Mode, no parameter setting is required since all the internal register values have been maintained. In order for the processor to exit the Power Down Mode correctly, the processor needs a 13ms internal state-management period before it can accept any new set of parameter download, or re-entering into the Operational Mode. Also please refer to the "FM-1288 Configuration Manual" for related details.

The following figure is a state transition diagram which shows the FM1288 chip transition between these 4 states.

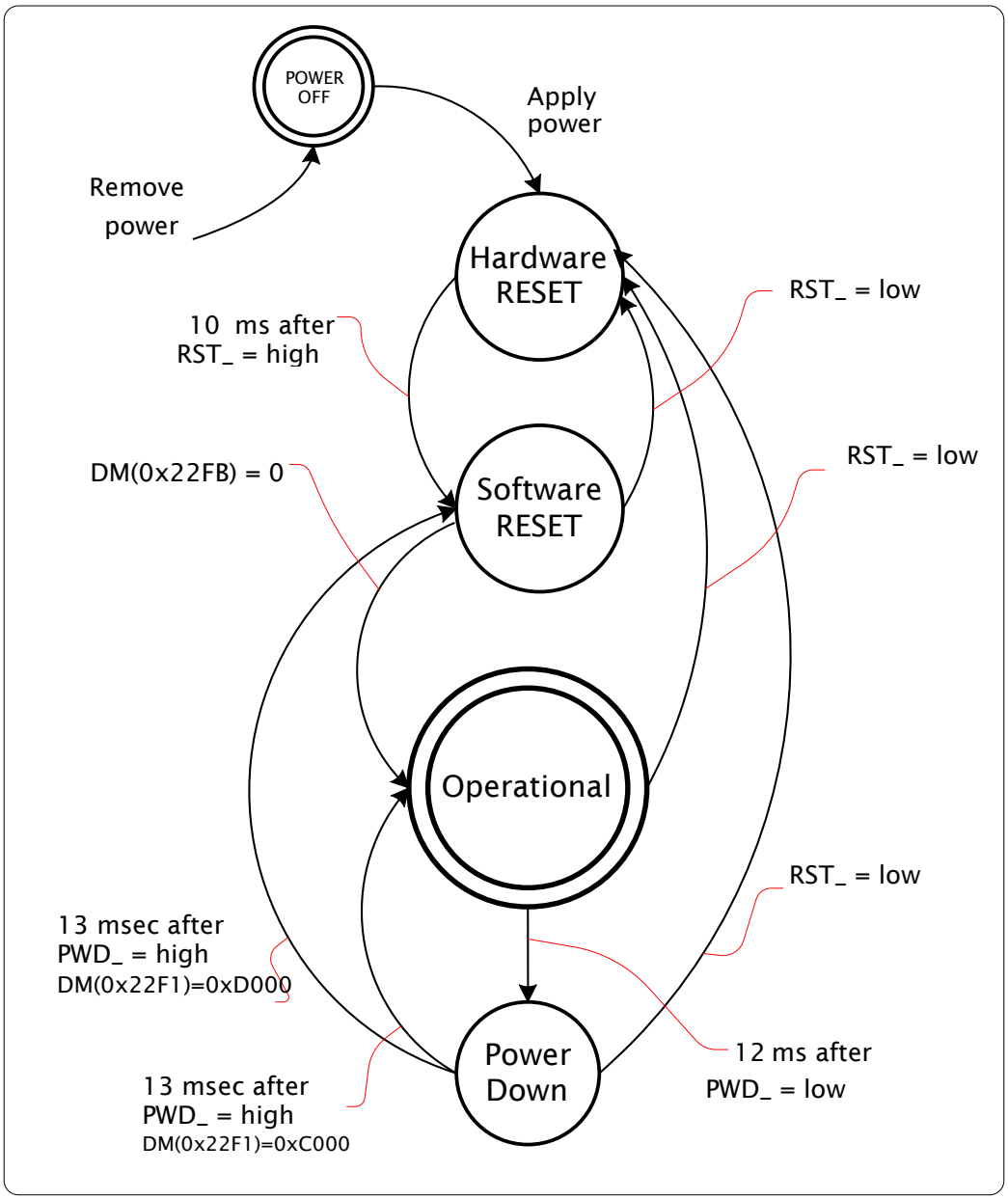



**Figure 19: State Transition Diagram**

## 2.9 Power-Up Stap Option (Pin 17)

Strap options are used to determine the desired operation of the chip. All the strap options mentioned below must be pulled high or low using a 100kΩ weak load. If pin left floating, the status will be unknown.

In the software reset mode, the chip samples different strap options, if any, to determine desired operation to decide on system configuration.

**Table 8: Strap Option Pins to Select Operation Mode**

| Mode | Pin 17 (GPIO) |
|---|---|
| reserved | currently usage is undefined, and no strap option available |

## 2.10 Mute Control and Indication (Pins 20, 21)

Mute control on the downlink voice signal to loudspeaker output can only be controlled via commands issued by UART or SHI. Pin 20 is an output indicator which would be asserted high when loudspeaker output has been switched into muted state. The user can, for example, tied this pin signal to provide an LED indicator.

Mute control on the uplink voice signal to send out can also be controlled via commands issued by UART or SHI. Alternatively, mute contrl on the uplink can be controlled directly by the Pin 21 input signal.

## 2.11 Speaker Volume Control (Pins 25, 26)

The speaker volume of FM1288 can be controlled by the Vol- (pin 25) and Vol+ (pin 26) pins. These input signals are level triggered and active high. The FM1288 will increase or decrease the volume by one step once it senses a level high signal on either pin (The minimum length of active high state is 150ms. The minimum length of de-active low state is 100ms). If the level stays high, every one second, it will continue to increase or decrease the volume until it hits the cap. The maximum volume is programmable (see "*FM1288 User Configuration Manual*").

If the pins are not used, they must be pulled low using a weak 100kΩ resistor.

## 2.11 System Clock Input and Generation (Pins 27, 28)

The FM1288 accepts a wide range of external clock sources, this external clock can be from 3MHz to 32 MHz in 1 MHz increments, or from 4.096MHz to 32.768MHz in 2.048MHz increments. Other popular system clock frequencies – 3.6864, 7.68, 14.4, 15.36, 16.8, 19.2, 19.68, 38.4, and 48 MHz are also supported.

However, if UART interface is to be used immediately after power up, then

- the clock/crystal frequency supplied to the FM-1288 must be an integer multiple of 18.432 MHz in order for the UART baud rate to communicate to the commonly used baud rate which would be an integer multiple of 9600.

| Clock/Crystal Input | UART baud rate after boot up |
|---|---|
| 4.608 MHz | 2400 baud |
| 9.216 MHz | 4800 baud |
| 18.432 MHz | 9600 baud |
| 36.864 MHz | 19200 baud |

A crystal applied to pins 27(XTAL_IN) and 28(XTAL_OUT) will also work. For more information on crystal specifications, please refer to Appendix I.

All FM-1288 internal digital clocks are generated using internal phase locked loops, which are locked to the frequency of the clock source.

## 2.12 Bypass Mode (Pin 14)

The FM1288 supports a Bypass Communication mode by asserting TEST2 pin to high.

In this Bypass Communication mode, the microphone input signal of MIC0_IN will be routed to LINE_OUT and input signal of LINE_IN to SPK_OUT directly. It bypasses the internal ADC, DSP, and DAC. The PGA gain setting and internal pre-amplifiers are still working with the input and output signal.

The mode can be toggled on and off during runtime by the hardware TEST2 pin.

# 3. Accessing FM1288 Through EEPROM, UART, SHI

| INTERFACE | Power Up/Reset<br>system parameter initialization | Runtime<br>Control and parameter modification |
|---|---|---|
| **EEPROM** | Yes | No |
| **UART** | Yes | Yes |
| **SHI** | Yes | Yes |

**Figure 20: Accessing FM1288**

Should the initialization of FM1288 need be done through UART/SHI, then the system needs to wait a nominal 12ms after initial power up before commencing the initialization.

During runtime, users can read or write to registers in FM1288 through one of the two interfaces: UART, or SHI. To access the registers in FM1288, designers must use a pre-defined command entry pattern. The UART or SHI interfaces are used if applications require control through an external host.

These interfaces can also be used to perform power up and reset system parameter initialization when they are connected to a host processor. As an option, the content in a supported IIC EEPROM can be automatically loaded into the registers after reset.

| Command Byte | Address Byte(s) | Data Byte(s) |
|---|---|---|

**Figure 21: Command Entry Data Pattern**

The table below shows the available command entries and the associated number of bytes required for each entry.

**Table 9: Command Entries**

| Command Entry | Available for Interface | Command Byte | No. of Address Bytes | No. of Data Bytes | Total No. of Bytes |
|---|---|---|---|---|---|
| Mem_write | UART, SHI, EEPROM | 0x3B | 2 | 2 | 5 |
| Mem_read | UART, SHI | 0x37 | 2 | 0 | 3 |
| Short_reg_write | UART, SHI | 68 | 1 | 1 | 3 |
| Long_reg_write | UART, SHI | 6A | 1 | 2 | 4 |
| reg_read | UART, SHI | 60 | 1 | 0 | 2 |

## 3.1 Accessing Through EEPROM

Please see Section 2.2(Serial EEPROM Interface) on the rules for EEPROM data organization.

Based on details provided in that section, an example of organizing the EEPROM would be:

| Operations | EEPROM content |
|---|---|
| **Starting dummy value for EEPROM** | Dummy value at byte 0 |
| **Initialize the Patch RAM** | EEPROM command, write into 0x3FCB, value = 0x0010, to start Patch RAM initialization<br><br>EEPROM commands to write into Patch RAM area<br><br>EEPROM command, write into 0x3FCB, value = 0x0000, to start Patch RAM initialization |
| **Initialize the Control Registers** | EEPROM commands to write into DM space and initialize memory mapped registers |
| **Initialize other Parameters** | EEPROM commands to write into DM space and initialize memory locations |
| **Terminate EEPROM transfer (Last EEPROM command)** | 3B 22 FB 00 00 00 |
| **Last byte for EEPROM** | 0xF0 |

## 3.2 Examples of Accessing Through EEPROM

The table below provides a few examples of updating parameters in FM1288 through the EEPROM interface. For more details, please refer to the *FM1288 User Configuration Manual*.

| operation | EEPROM command example |
|---|---|
| **Set up speaker volume** | 3B 1E 3E 02 00 00 |
| **Set up microphone PGA** | 3B 1E 34 00 33 00 |
| **Terminate EEPROM transfer** | 3B 22 FB 00 00 00 |

**Table 10: Examples of Accessing through EEPROM**

## 3.3 Accessing Through UART

UART serves as an interface between the FM1288 and a host PC or controller that it can send commands to program the chip's parameters. UART is an asynchronous bi-directional serial interface and the protocol is determined by a start bit, number of character bits, a parity bit and a stop bit.

There are 5 different types of command entries for the FM1288 UART interface. Two synchronize bytes "FC" and "F3" are required before each command entry. Since the speed of the UART interface is much slower than the internal clock of FM1288, it is safe to continue a "write" transfer without checking the status of the data transfer.

There are two access modes: mem_read and reg_read. Mem_read is used to read the memory contents and save the contents in registers 25 and 26 of FM1288. Reg_read then transfers the register contents to the UART interface output pin TXD. The micro-controller host will then receive the register contents by monitoring the TXD pin. No partial command entry is allowed. A partial command entry may cause system mal-function.

## 3.4 Examples of Accessing Through UART

The table below provides a few examples of updating parameters in FM1288 through the UART interface. For more details, please refer to the "*FM1288 User Configuration Manual*."

**Table 11: Examples of Accessing through UART**

| | |
|---|---|
| **mem_write transfer** | |
| FC F3 3B 1E 34 00 55 | -- write memory 1E34 with 0055 |
| **mem_read** | |
| FC F3 37 1E 34 | -- read memory contents of 1E34 |
| **long_reg_write** | |
| FC F3 6A 2A 00 30 | -- software reset of the voice processor |
| **reg_read** | |
| FC F3 60 25 | -- read register 25 |
| **read out contents of memory location 1E34** | |
| FC F3 37 1E 34<br>FC F3 60 26<br>FC F3 60 25 | <br>-- MSB of 1E34 will transmit through TXD<br>-- LSB of 1E34 will transmit through TXD |

## 3.5 Accessing Through SHI

## Examples of Accessing Through SHI

The table below provides a few examples of updating parameters in FM1288 through the SHI interface.

For more details, please refer to the "*FM1288 User Configuration Manual*".

**Table 12: SHI Command Symbols**

| Command Symbol | Definition | Command Symbol | Definition |
|---|---|---|---|
| W | SHI Write Control (Add as SHI ID Bit[0]) | *AH* | Address High Byte |
| R | SHI Read Control (Add as SHI ID Bit[0]) | *AL* | Address Low Byte |
| FC | Command Sync Byte-1 | *DH* | Data High Byte Write |
| F3 | Command Sync Byte-2 | *DL* | Data Low Byte Write |
| 3B | Memory Write Command Byte | *XX* | Dummy Byte used in Burst Write between W and FC |
| 37 | Memory Read Command Byte | RH | Read out Data High Byte |
| 60 | Byte Read Command | P | SHI Stop Condition |

Note: Command symbols in bold are reserved and must be followed in exact order.

**Table 13: Examples of Accessing through SHI**

**single memory write**

**S C0 W FC F3 3B** *AH AL DH DL* **P**
Example: S C0 W FC F3 3B 1E 41 00 01 P -- writes 0x0001 to memory address 0x1E41

**burst mode memory write**

**S C0 W** XX XX **FC F3 3B** *AH AL DH DL* …… **FC F3 3B** *AH AL DH DL* **P**
Example: S C0 W 00 1C FC F3 3B 1E 30 00 02 FC F3 3B 1E 41 00 01 FC F3 3B 1E 51 D0 00 P
-- writes 0x0002 to DM 0x1E30, 0x0001 to DM 0x1E41 and 0xD000 to DM 0x1E51 0x00 and 0x1C between **W** and **FC** are dummy bytes, and ignored.

**fast memory read**

**S C0 W FC F3 37** *AH AL* **P**
**S C0** R RH RL **P**
Examples: S C0 W FC F3 37 1E 41 P -- read memory address 0x1E41
S C0 R 00 01 P -- get value 0x0001.

# 4. Electrical and Timing Specification

Note that all data in this section are measured at room temperture and in normal operating condition.

## 4.1 Absolute Maximum Ratings

**Table 14: Absolute Maximum Ratings for FM1288-GA1-410**

| Parameter | Symbol | Condition | Max Rating | Unit |
|---|---|---|---|---|
| Power Supply Voltage | VDD_D | 3.3 | 3.465 | V |
| Power Supply Voltage | VDD_A | 3.3 | 3.465 | V |
| Storage Temperature | $T_{stg}$ | - | -40 to 150 | $^0$C |
| Junction Temperature | $T_J$ | | 125 | $^0$C |
| ESD(Human body model) | VESDHBM | | 2k | V |
| ESD(Machine model) | VESDMM | | 200 | V |

**Table 15: Absolute Maximum Ratings for FM1288-GE-410**

| Parameter | Symbol | Condition | Max Rating | Unit |
|---|---|---|---|---|
| Power Supply Voltage | VDD_D | 3.3 | 3.465 | V |
| Power Supply Voltage | VDD_A | 3.3 | 3.465 | V |
| Storage Temperature | $T_{stg}$ | - | -40 to 150 | $^0$C |
| Junction Temperature | $T_J$ | | 125 | $^0$C |
| ESD(Human body model) | VESDHBM | | 2k | V |
| ESD(Machine model) | VESDMM | | 200 | V |

**Table 16: Absolute Maximum Ratings for FM1288-GA1-400B and FM1288-GE-400B**

| Parameter | Symbol | Condition | Max Rating | Unit |
|---|---|---|---|---|
| Power Supply Voltage | VDD_D | 3.3 | 3.63 | V |
| Power Supply Voltage | VDD_A | 3.3 | 3.63 | V |
| Storage Temperature | $T_{stg}$ | - | -40 to 150 | $^0$C |
| Junction Temperature | $T_J$ | | 125 | $^0$C |
| ESD(Human body model) | VESDHBM | | 2k | V |
| ESD(Machine model) | VESDMM | | 200 | V |

## 4.2 Recommended Operating Conditions

**Table 17: Recommended Operating Conditions for FM1288-GA1-410**

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Analog Power Supply Voltage(1) | VDD_A | Supplied externally | 3.135 | 3.3 | 3.465 | V |
| Digital I/O Supply Voltage | VDD_D | Supplied externally | 3.135 | 3.3 | 3.465 | V |
| Operating Temperature | $T_{amb}$ | Automotive Grade | -40 | 25 | 85 | °C |

Notes: The power ripple (AC element) has to be limited within 100mV

**Table 18: Recommended Operating Conditions for FM1288-GE-410**

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Analog Power Supply Voltage(1) | VDD_A | Supplied externally | 3.135 | 3.3 | 3.465 | V |
| Digital I/O Supply Voltage | VDD_D | Supplied externally | 1.71 or 3.135, respectively | 1.8 or 3.3 | 1.89 or 3.465, respectively | V |
| Operating Temperature | $T_{amb}$ | Extended Grade | -20 | 25 | 70 | °C |

Notes: The power ripple (AC element) has to be limited within 100mV

**Table 19: Recommended Operating Conditions for FM1288-GA1-400B and FM1288-GE-400B**

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Analog Power Supply Voltage(1) | VDD_A | Supplied externally | 2.97 | 3.3 | 3.63 | V |
| Digital I/O Supply Voltage | VDD_D | Supplied externally | 1.62 | 1.8/3.3 | 3.63 | V |
| Operating Temperature | $T_{amb}$ | Automotive Grade FM1288-GA1-400B | -40 | 25 | 85 | °C |
| Operating Temperature | $T_{amb}$ | Extended Grade FM1288-GE-410 | -20 | 25 | 70 | °C |

Notes: The power ripple (AC element) has to be limited within 100mV

## 4.3 DC Characteristics

**Table 20: DC Characteristics**

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Active Power Supply Current | $I_{VDD_D}$ | Internal LDO enabled | | 15 | 25 | mA |
| | $I_{VDD_A}$ | Internal LDO enabled | | 5 | 15 | mA |
| Standby Current | $I_{VDD_D}$ | Internal LDO enabled | | 10 | 100 | µA |
| | $I_{VDD_A}$ | Internal LDO enabled | | 2 | 20 | µA |
| Input Leakage Current | $I_{IH}$ | VDD_D = 1.8V | -1 | - | 1 | µA |
| | $I_{IL}$ | VDD_D = 0V | -1 | - | 1 | µA |
| Digital Output Voltage High | $V_{OH}$ | $I_{OH}$ = 1mA | 0.9*VDD_D | - | - | V |
| Digital Output Voltage Low | $V_{OL}$ | $I_{OL}$ = = 1mA | - | - | 0.1*VDD_D | V |
| Digital Input Voltage High | $V_{IH}$ | VDD_D = 1.8V | 0.7*VDD_D | - | - | |
| Digital Input Voltage Low | $V_{IL}$ | | - | - | 0.45 | V |
| Digital Output Leakage Current | IO | | | | 10 | µA |
| Input Capacitance | CIN | | | 2 | | pF |
| Power Dissipation | $P_{PDN}$ | $T_{amb}$=25°C, LDO enabled | | 25 | 250 | µW |
| | $P_{SYS}$ | | | 43.5 | 95 | mW |

Notes:
VDDC=1.2V, VDD_D=1.8V, VDD_A=3.3V, 25°C, SR=16KHz FM-1288 in normal operating condition, unless otherwise noted

## 4.4 AC Characteristics

**Table 21: AC Characteristics**

| Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Mic0/Mic1 Input Range (differential) | Mic_In @ 0dB PGA gain | | 2.83 | | Vpp |
| Line_in Input Range (differential) | Line_In @ 0dB PGA gain | | 2.83 | | Vpp |
| Speaker Out Full Scale Output (differential) | SPK_Out @ 0dB PGA gain | | 2.4 | | Vpp |
| Line_out Full Scale Output (differential) | Line_Out @ 0dB PGA gain | | 2.4 | | Vpp |
| SNR for Speaker out (A-weghting) | SPK_OUT @ 0dB PGA Signal 2.4Vpp | | 90 | | dB |
| SNR for Line_out (A-weighting) | LINE_OUT@ 0dB PGA Signal 2.4Vpp | | 90 | | dB |
| THD+Noise at -1 dBFS for Mic0/Mic1 ADC | 1KHz sine wave test | | -65 | | dB |
| THD+Noise at -1 dBFS for Line_in ADC | 1KHz sine wave test | | -65 | | dB |
| THD+Noise at 0dBFS for Line_out and Spk_out DAC | 1KHz since wave test | | -65 | | dB |
| Noise Floor for Mic0/Mic1 ADC | Input = 0Vpp<br><br>Noise Bandwidth is 22-8KHz A-weighted | | -86 | | dBFS |
| Noise Floor for Line_in | | | -86 | | dBFS |
| Noise Floor for Line_out and Spk_out DAC | Input=0dBFS<br><br>Noise Bandwidth is 22-22KHz A-weighted | | -91.5 | | dBV |
| Power Supply Rejection (PSR) for Mic0/Mic1 | | | -70 | | dBFS |
| Power Supply Rejection (PSR) for Line_In | | | -70 | | dBFS |
| CODEC Sampling Frequency (to user) | | | 16 | | kHz |
| Input Impedance for Mic0/Mic1 In | PGA at largest setting=[0111] | | 44.17 | | kΩ |
| Input Impedence for Line in | PGA at lowest setting=[0000] | | 110 | | kΩ |
| DAC Output Driving Capabilityfor Line_out / Spk_out | | 1 | | | kΩ |
| Microphone Bias Voltage | | | 0.9* VDD_A | | V |
| Microphone Bias Load Current | | | 3 | | mA |
| Microphone Bias Output Noise | 22 – 22KHz A-weighted | | 20 | | uVrms |
| Microphone Bias PSRR | 217Hz, 100mVpp @VDD_A | | 50 | | dB |

Notes:
VDDC=1.2V, VDD_D=1.8V, VDD_A=3.3V, 25°C, SR=16KHz FM-1288 in normal operating condition, unless otherwise noted

**Table 22: ADC PGA (MIC0_IN, MIC1_IN, LINE_IN)**

| Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Gain Range | - | 0 | - | 28 | dB |
| Step Size | Range: 0dB to 2dB | - | 1 | - | dB |
| Step Size | Range: 2dB to 28dB | - | 2 | - | dB |
| Step Size Error | Range: 0dB to 2dB | -0.5 | - | 0.5 | dB |
| Step Size Error | Range: 2dB to 28dB | -1 | - | 1 | dB |

Notes:

1. All input pins become high impedance in the power down mode.
2. Refer to the FM1288 Tuning Guide for details on setting the ADC PGA gain.

**Table 23: DAC PGA (LINE_OUT, SPK_OUT)**

| Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Gain Range | - | -28 | - | 2 | dB |
| Step Size | Range: -28dB to +2dB | - | 2 | - | dB |
| Step Size Error | Range: -28dB to +2dB | -0.5 | - | 0.5 | dB |

## 4.5 Timing Characteristics

**Table 24: Timing Characteristics**

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Rise/fall time of input pins except for SCL/SDA | | - | - | 20 | ns |
| Setup time from Power to master clock | Tsu_vdd2clk | | 1 | | ms |
| VDD_D to VDD_A setup time | Tsu_vdd2vdda | 1 (4) | | | µs |
| Reset active low time | Trst | 120 | - | - | µs |
| Setup time from master clock to rising edge of RST_ | Tsu_clk2rst | 80 | - | - | µs |
| Reset to parameters programming start setup time | Tsu_rst2pp | 2(1) | 10 | - | ms |
| Parameters programming to Master clock off hold time | Tsu_pp2clkoff | 12 | - | - | ms |
| Master clock frequency | Tcyc | 30.5 | - | 333 | ns |
| Master clock high width | Thigh | 45% | - | 55% | Tcyc |
| Master clock low width | Tlow | 45% | - | 55% | Tcyc |
| PCM Frame Frequency | Tcyc_frame | 8 | 16 | - | kHz |
| PCM BCLK Frequency | Tcyc_bclk_chi | 32 * FSC/LRCK | | 4096 | kHz |
| PCM RX setup time | Tsu_d2c_chi | 20 | - | - | ns |
| PCM TX delay | Td_tx_chi | - | - | 20 | ns |
| IIS LRCK Frequency (2) | Tcyc_lrck | - | 16 | - | kHz |
| IIS BCLK Frequency(2) | Tcyc_bclk_IIS | 32 * FSC/LRCK | | 4096 | kHz |
| IIS RX setup time to clock edge(2) | Tsu_d2c_IIS | 20 | - | - | ns |
| IIS TX delay time(2) | Td_tx-IIS | - | - | 20 | ns |
| SCL Frequency | Tf_scl | - | 100 | 400(3) | kHz |
| Hold time Start condition | Th_sta | - | 4 | - | µs |
| SDA Setup time | Tsu_dat | 250 | - | - | ns |
| SDA Hold time | Th_dat | 0 | - | - | |
| Low period of SCL | Tlow_scl | 4.7 | - | - | µs |
| High period of SCL | Thigh_scl | 4.0 | - | - | µs |
| Setup time for START | Tsu_sta | 4.7 | - | - | µs |
| Rise time of both SDA and SCL | Tr | - | - | 1000(5) | ns |
| Fall time of both SDA and SCL | Tf | - | - | 300 | ns |
| Setup time for STOP | Tsu_sto | 4 | - | - | µs |
| Bµs free time between STOP and Start | Tbuf | 4.7 | - | - | µs |

Notes:

(1) Minimum timing is 2ms, including HW internal reset and SW reset, inside the DSP processor based on the MCLK being 24.576MHz. Need to raise the timing if MCLK is less than 24.576MHz. 10ms is nominal timing sufficient for all cases.

(2) Reference Figures 10 to 18 for PCM and IIS timing parameters

(3) Master mode supports up to 400kHz, Slave mode has no limitation and depends on the host system's capability.

(4) Please note that 3.3V can be used as the same power source for VDD_D and VDD_A, and the internal design of FM-1288 actually renders Tsu_vdd2vdda timing (even a nominal 1 µs is stated) not critical. User's design can simply power up VDD_D and VDD_A at the same time.

(5) Rise Time for both SDA and SCL is 1000 ns max in Standard Mode(100KHz), and 300 ns max in Fast Mode(400kHz)

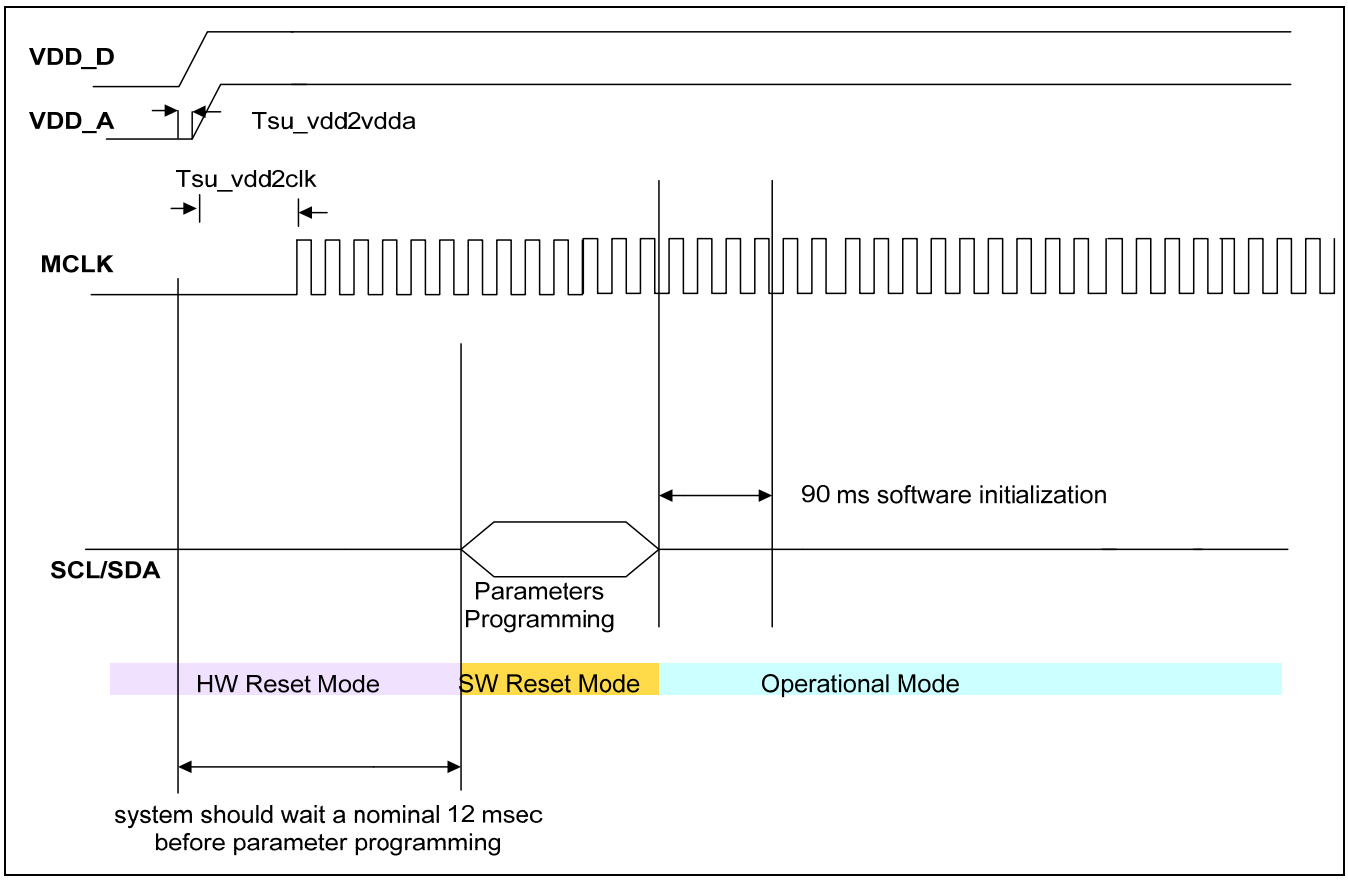



**Figure 22: Timing Chart: Normal Power-Up Sequence**

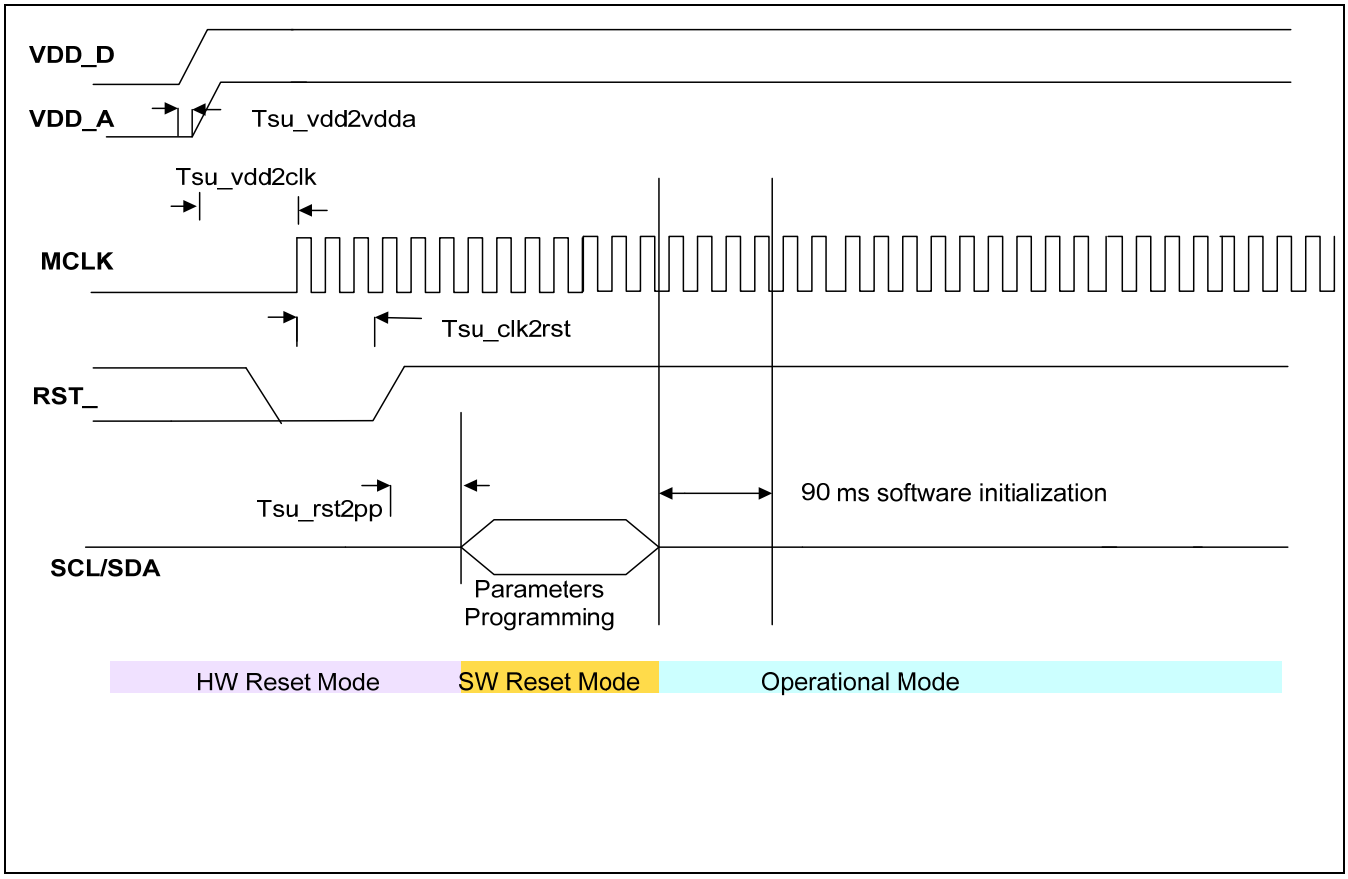



**Figure 23: Timing Chart: Reset while in Hardware Reset**

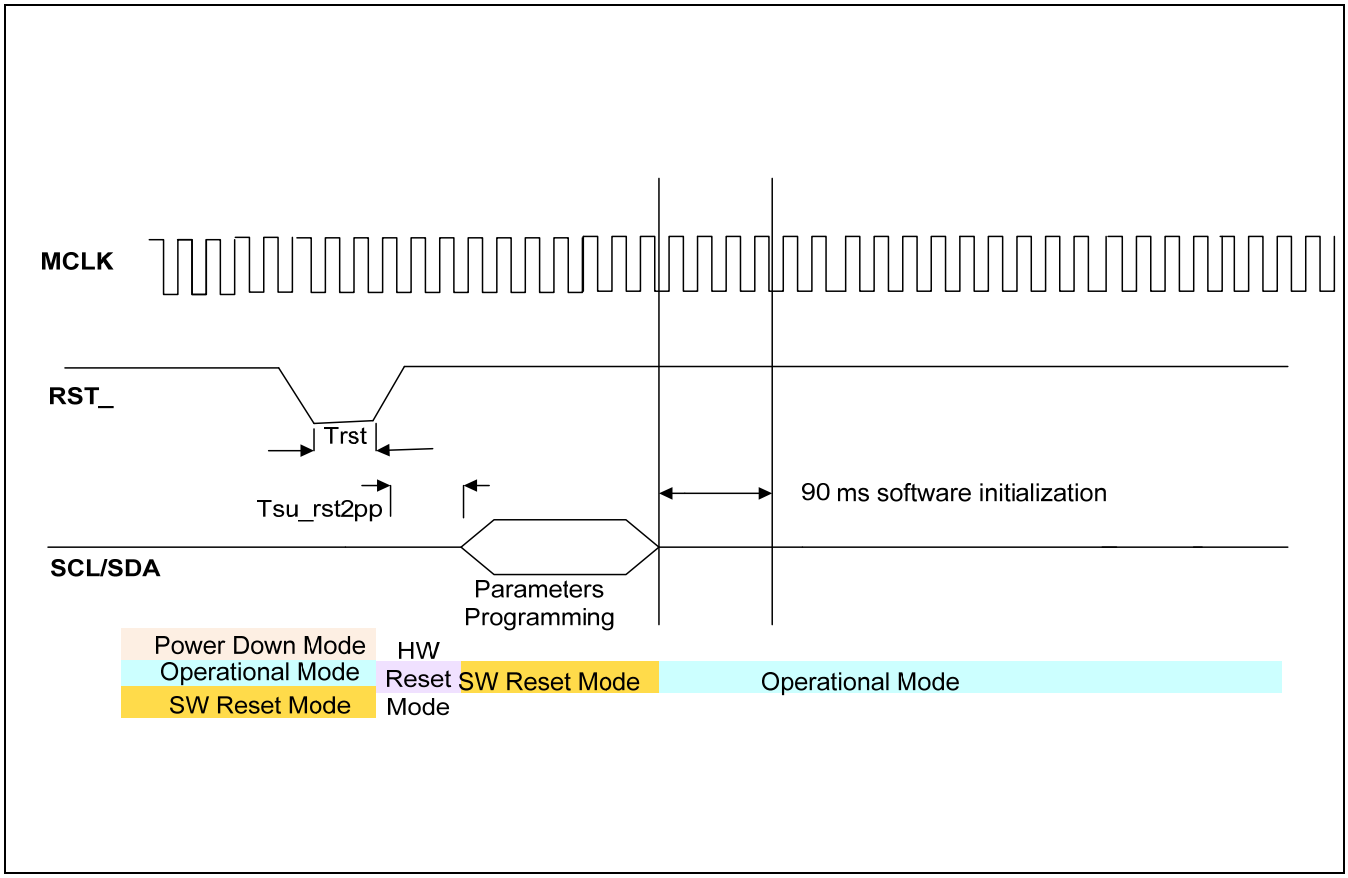



**Figure 24: Timing Chart: RESET while in Software Reset, Operational, and Power Down**

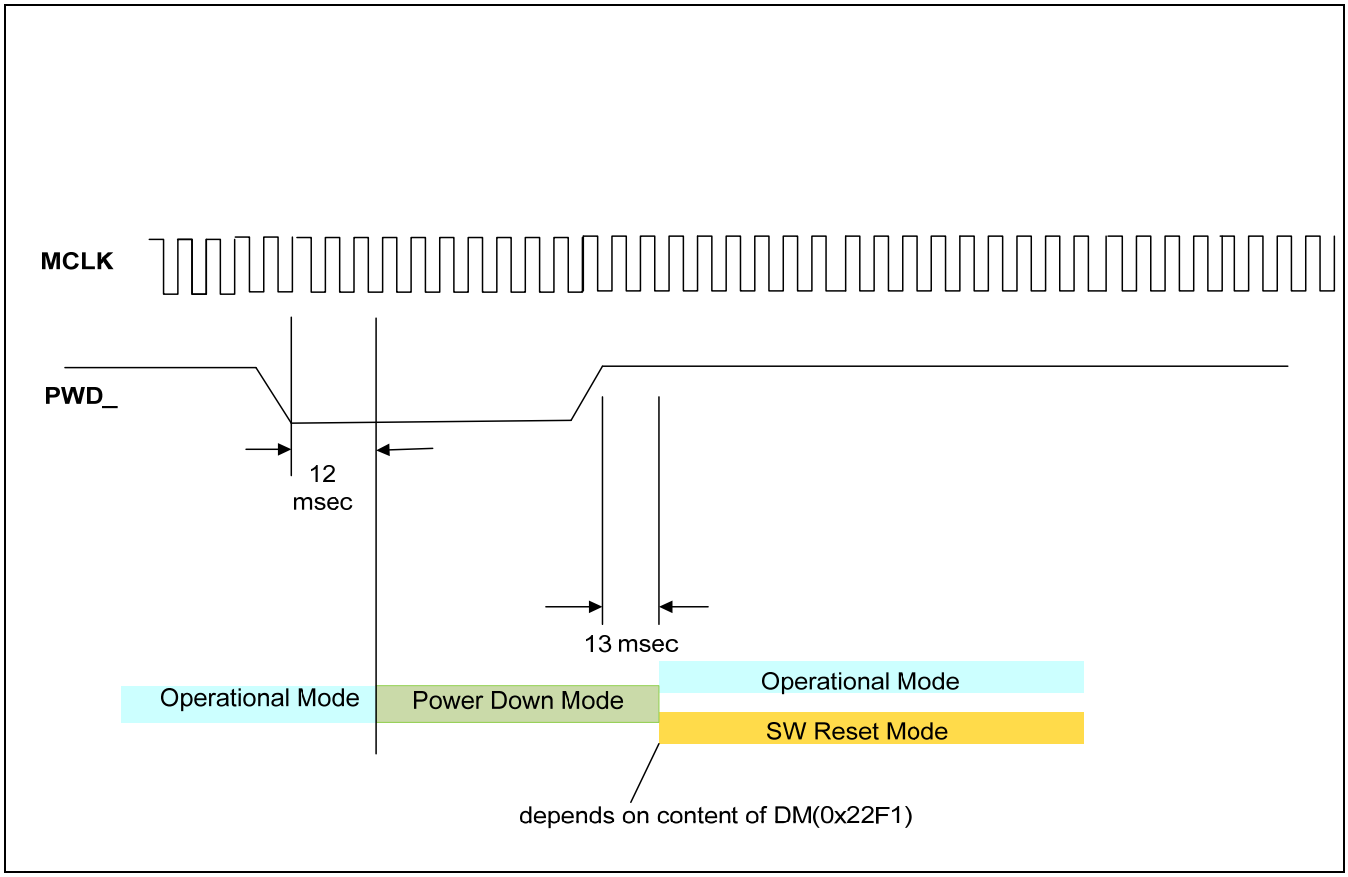



**Figure 25: Timing Chart: PWD_ and state transition**

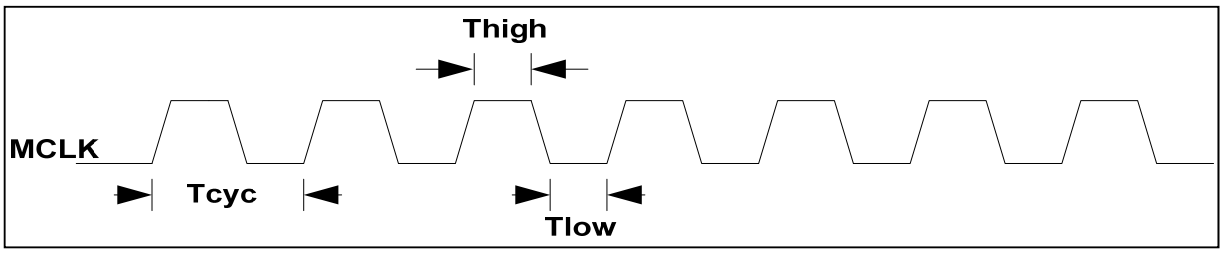



**Figure 26: Master Clock (MCLK) Timing**

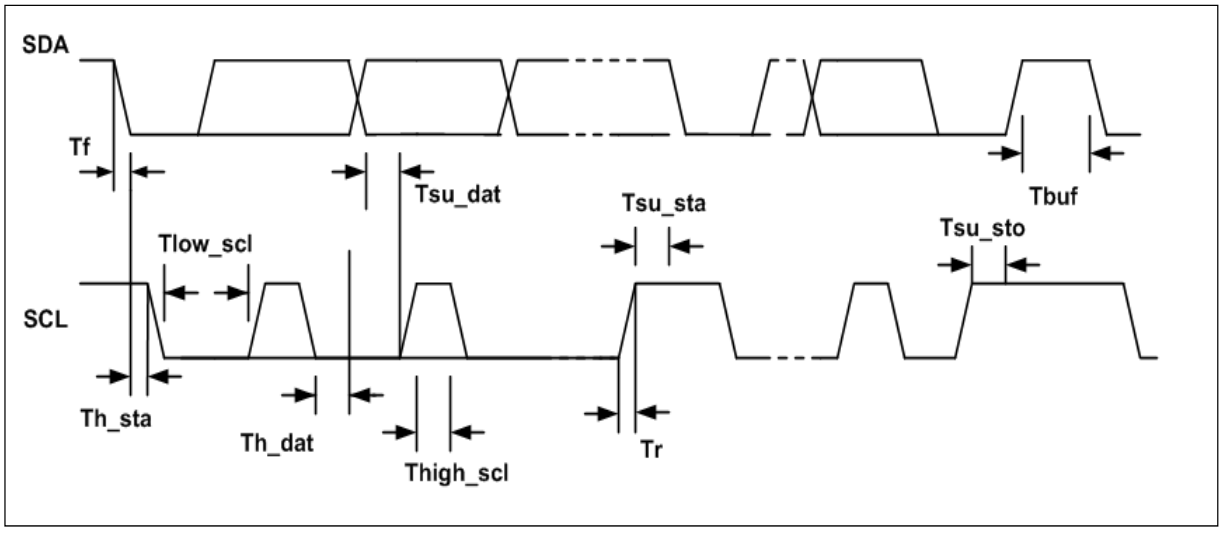



**Figure 27: SHI Timing**

# 5. Voice Processor Performance Details

**Table 25: Voice Processor Performance Details**

| Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Acoustic Echo Cancellation | Total ERLE | - | 60 | - | dB |
| Acoustic Echo Cancellation Double Talk Performance | Nominal, characterized by VDA Tests | | Type 2A | Type 1 | |
| Acoustic Echo Tail Length | | - | 50 | - | ms |
| Echo Cancellation Convergence | Nominal | - | < 60 | - | ms |
| Stationary Noise Suppression | Nominal | 6 | 12 | 30 | dB |
| Noise Suppresion Convergence | Nominal | 1.6 | 2.4 | 3.2 | s |
| Mic_in to Line_out Latency | Algorithm running | - | 47 | - | ms |
| Line_in to Speaker_out latency | Algorithm running | | 46 | | ms |

# 6. Pin Definition Details

**Table 26: Pin Description**

| Pin | Pin Name | Type | Electrical | Pin Description |
|---|---|---|---|---|
| 1 | LINE_OUT_N | Out | | Analog Line Out (-) |
| 2 | NC | NC | NC | No connect |
| 3 | SPK_OUT_N | Out | | Analog Speaker output (-) to external power amplifier |
| 4 | NC | NC | NC | No connect |
| 5 | NC | NC | NC | No connect |
| 6 | NC | NC | NC | No connect |
| 7 | VSS_D | GND | GND | Digital ground – to PCB Ground Plane |
| 8 | BCLK | In/Out | 1.8-3.3v I/O tolerance, 2mA | PCM/IIS: bit clock |
| 9 | FSYNC | In/Out | In | PCM/IIS: frame sync/word select |
| 10 | TX | In/Out | 1.8-3.3v I/O tolerance, 6mA | PCM/IIS : data out |
| 11 | RX | In | 1.8-3.3v I/O tolerance | PCM/IIS : data in |
| 12 | UART_RX | In | 1.8-3.3v I/O tolerance | UART data in (RX). |
| 13 | UART_TX | In/Out | 1.8-3.3v I/O tolerance, 2mA | UART data out (TX). |
| 14 | TEST2 | In | 1.8-3.3v I/O tolerance, 2mA | When asserted high, Voice Processor is in bypass mode, and by default analog line in is bypassed to analog speaker out, while analog mic0 in is bypassed to analog line out.(1)<br>Other bypass modes could be further configured during or after power-up initialization. |
| 15 | SDA_EE | In/Out | 1.8-3.3v I/O tolerance, 2mA | IIC / EEPROM data. |
| 16 | SCL _EE | In/Out | 1.8-3.3v I/O tolerance, 2mA | IIC / EEPROM clock. |
| 17 | GPIO | In/Out | 1.8-3.3v I/O tolerance, 2mA | Currently no defined usage. |
| 18 | VSS_D | GND | GND | Digital ground.<br>Connect to PCB Ground Plane. |
| 19 | VDD_D | POWER | 1.8V, 3.3V voltage supply | For FM1288-GE-400B, FM1288-GE-410, and FM1288-GA1-400B<br>From 1.8V/3.3V Power Supply Voltage(2) |
| | | | 3.3V voltage supply | For FM-1288-GA1-410<br>From 1.8V/3.3V Power Supply Voltage(2) |
| 20 | MUTE_IN | In/Out | 1.8-3.3v I/O tolerance, 2mA | Mute SEND_OUT control input pin. |
| 21 | MUTE_OUT | In/Out | 1.8-3.3v I/O tolerance, 2mA | Muted Loudspeaker Indicator output pin. |
| 22 | VAD_LED | In/Out | 1.8-3.3v I/O tolerance, 2mA | LED indicator output pin.<br>LED usage to be defined. |
| 23 | SCL | In/Out | 1.8-3.3v I/O tolerance, 2mA | SHI interface : Serial clock if IIC selected.<br>If not used, pull low using weak 100kΩ resistor. |
| 24 | SDA | In/Out | 1.8-3.3v I/O tolerance, 2mA | SHI interface : Serial data if IIC selected.<br>If not used, pull low using weak 100kΩ resistor. |

| | | | | |
|---|---|---|---|---|
| 25 | Vol- | In/Out | 1.8-3.3v I/O tolerance, 2mA | Volume Down control input pin.<br>Active high.<br>If not used, pull low using weak 100kΩ resistor. |
| 26 | Vol+ | In/Out | 1.8-3.3v I/O tolerance, 2mA | Volume Up control input pin.<br>Active high.<br>If not used, pull low using weak 100kΩ resistor. |
| 27 | XTAL_IN/ MCLK_IN | In | | Crystal Oscillator input, or clock from MCU if clock is used. |
| 28 | XTAL_OUT | Out | | Crystal Oscillator, or ground this pin if clock is used on XTAL_IN. |
| 29 | VSS_D | GND | 0V | Digital Ground - to PCB Ground Plane. |
| 30 | PWD_ | In | 1.8-3.3v I/O tolerance | Powerdown pin, active low.<br>To/from MCU or power down device. |
| 31 | RST_ | In | 1.8-3.3v I/O tolerance | Reset pin, active low.<br>To/from MCU or reset device. |
| 32 | TEST1 | In | 1.8-3.3v I/O tolerance | Test pin.<br>Connect a 100kΩ resistor to ground. |
| 33 | NC | NC | | No Connect |
| 34 | PMB_VREF | | | Reference Voltage for MICBIAS.<br>Connect via ~0.47uF capacitor to ground. |
| 35 | VDD_A | POWER | 3.3V | Analog power supply.<br>Connect to 3.3V power supply. |
| 36 | PMIC_BIAS | Out | 0.9 * VDD_A | Analog Output Mic Bias Voltage supply. |
| 37 | VDD_C | POWER | 1.2 V is generated by internal LDO | Connect this pin via 1µF capacitor to ground. |
| 38 | VSS_A | GND | 0V | Analog Ground for CODEC, to PCB ground plane. |
| 39 | MIC0_P | In | 2.83 Vpp | Analog Primary Mic (+) input. |
| 40 | MIC0_N | In | | Analog Primary Mic (-) input. |
| 41 | MIC1_P | In | 2.83 Vpp | Analog Secondary Mic (+) input. |
| 42 | MIC1_N | In | | Analog Secondary Mic (-) input. |
| 43 | LINE_IN_P | In | 2.83 Vpp | Analog Line_in (+) input. |
| 44 | LINE_IN_N | In | | Analog Line_in (-) input. |
| 45 | VSS_A | GND | | Analog Ground, connect to PCB ground plane. |
| 46 | VREF | | Reference Voltage for DAC | Connect a 1µF capacitor to ground. |
| 47 | LINE_OUT_P | Out | 2.4 Vpp | Analog Analog Line Out (+). |
| 48 | SPK_OUT_P | Out | 2.4 Vpp | Analog Speaker output (+) – to external power amplifier input. |

Notes:

(1) Active high: when Test 2 is "high", Voice Processor will bypass signals and Voice Processor will resume on high to low transition.

(2) This separate voltage source is designed to adapt to the level of the digital I/O interface voltage level; it can either be 1.8V, or 3.3V, depending on the interface logic level depending on the variant of the FM1288

# 7. Package Dimensions (LQFP)

**48 Pin LQFP Package Outline (Top View)**
**LQFP : 7x7x1.4mm (0.5 pitch pod)**

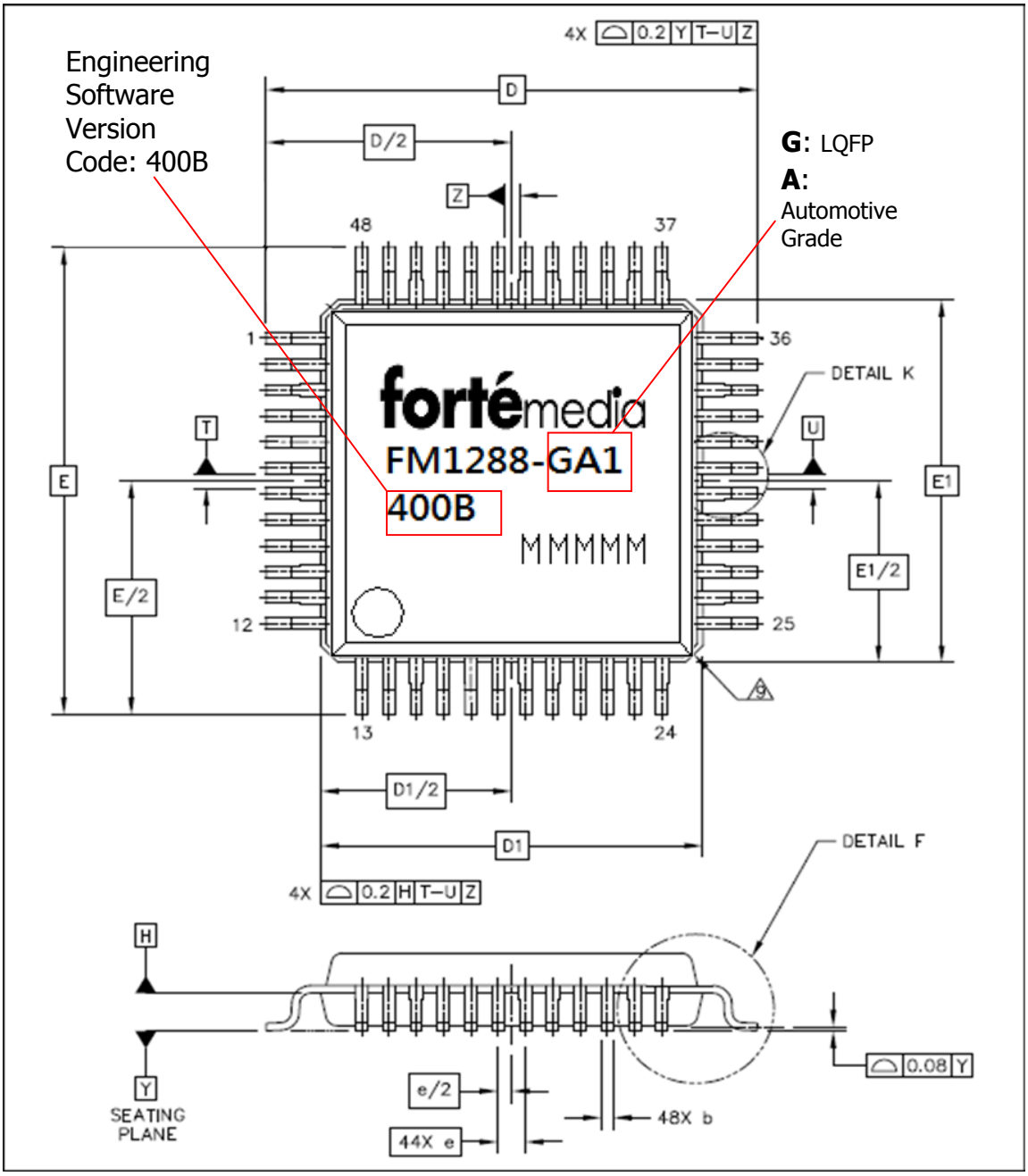



**Figure 28: 48-pin LQFP Package Drawing and Dimensions**

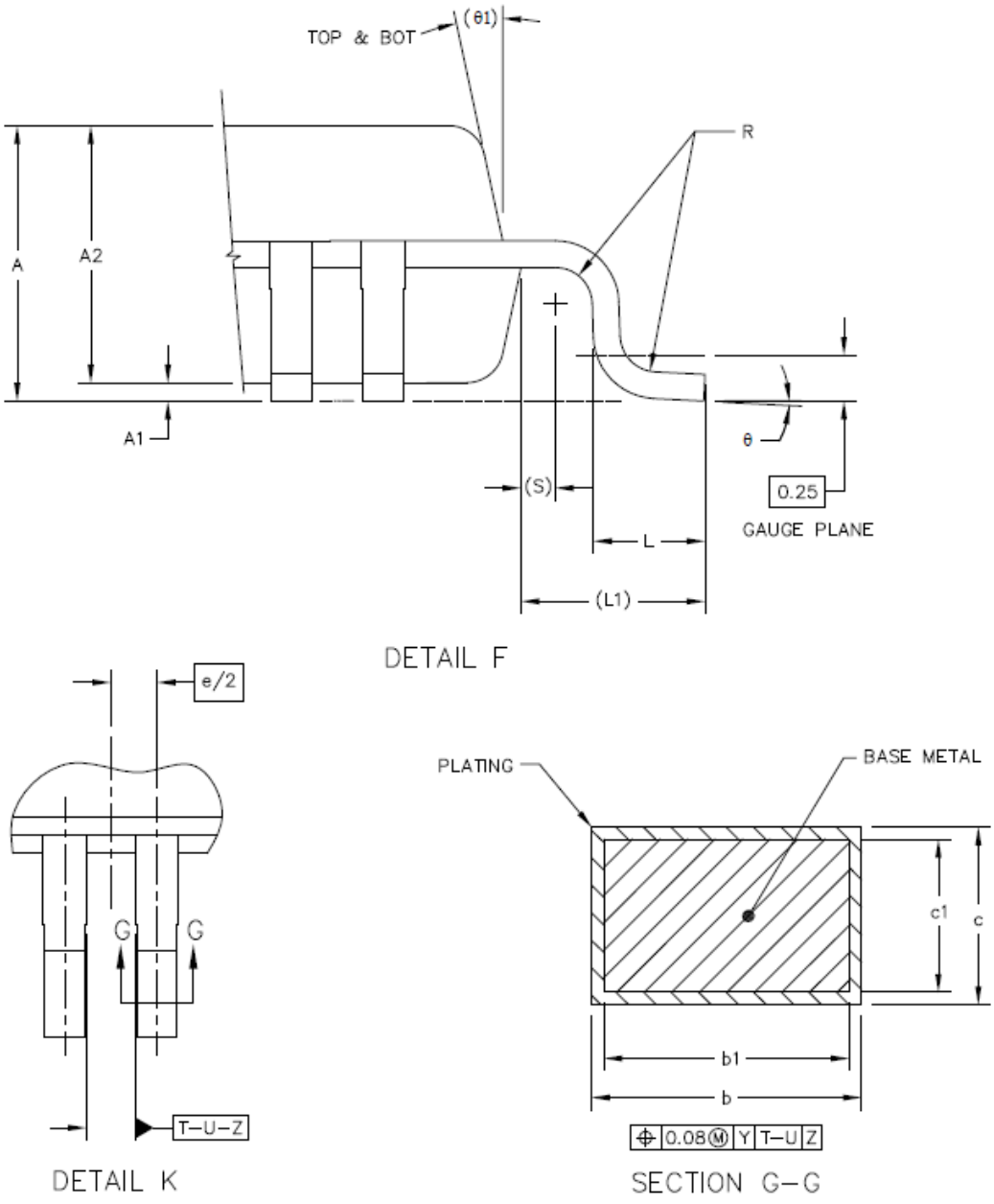



**Figure 29: 48-pin LQFP Package Side View**

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. DATUM PLANE H IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUM T, U AND Z TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE Y.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
7. DIMENSION b DOES NOT INCLUDE DAM BAR PROTRUSION. DAM BAR PROTRUSION SHALL NOT CAUSE THE b DIMENSION TO EXCEED 0.35.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.

9 EXACT SHAPE OF EACH CORNER IS OPTIONAL.

| DIM | MIN | MAX | DIM | MIN | MAX | DIM | MIN | MAX |
|---|---|---|---|---|---|---|---|---|
| A | 1.4 | 1.6 | L1 | 1 REF | | | | |
| A1 | 0.05 | 0.15 | R | 0.15 | 0.25 | | | |
| A2 | 1.35 | 1.45 | S | 0.2 REF | | | | |
| b | 0.17 | 0.27 | θ | 1° | 5° | | | |
| b1 | 0.17 | 0.23 | θ1 | 12° REF | | | | |
| c | 0.09 | 0.2 | | | | | | |
| c1 | 0.09 | 0.16 | | | | | | |
| D | 9 BSC | | | | | | | |
| D1 | 7 BSC | | | | | | | |
| e | 0.5 BSC | | | | | | | |
| E | 9 BSC | | | | | | | |
| E1 | 7 BSC | | | | | | | |
| L | 0.5 | 0.7 | | | | | | |




**Figure 30: 48-pin LQFP Package on FM-1288**

# 8. Ordering Information

**Table 27: Available Packages and Temperature Grade**

| Package | Green | Temperature Grade | Ordering Code |
|---|---|---|---|
| 48-pin LQFP | Yes | Extended | FM1288-GE-400B |
| 48-pin LQFP | Yes | Automotive | FM1288-GA1-400B |
| 48-pin LQFP | Yes | Extended | FM1288-GE-410 |
| 48-pin LQFP | Yes | Automotive | FM1288-GA1-410 |

**Note:**

Consumer = 0 to 70ºC
Extended = -20 to 70ºC
Automotive = -40 to 85ºC

Note that all new customer orders should be **FM1288-GE-410** or **FM1288-GA1-410** which are the respective updated versions of **FM1288-GE-400B** or **FM1288-GA1-400B**, unless there is a special reason to do otherwise.

# Appendix I: Required External Components for Operation

**Table 28: External Components Recommendations**

**Microphone Specification**

| Parameter | Value |
|---|---|
| Type | Electret Condenser Microphone |
| Sensitivity | -44 ~ -47 dB (1V/PA) |
| Operating Voltage | 2V (standard) |
| Impedance | 2.2kΩ maximum |

**External Loudspeaker Amplifier**

| Parameter | Value |
|---|---|
| Input Impedance | ~ 20kΩ (preferred) |

**Crystal/Oscillator Specification**

| Parameter | Value |
|---|---|
| Operating Frequency | 4.096 MHz to 24.576 MHz |
| Resonant Mode | Parallel |
| Frequency Tolerance | +/- 30ppm |
| Frequency Tolerence TC | +/- 50ppm |
| Operating Temperature Range | -40 to +85 C |
| Aging per Year | +/- 5ppm / yr |
| Operating Mode | Fundamental Mode |
| Crystal Co | 25 pF |
| Crystal Rs (ESR) | < 150 Ω |
| $R_S$ (external) | 1.8 KΩ |
| CL (external capacitance) | 47 pF |
| Drive Level | 27 µW (1.8V), 96 µW (3.3V) |

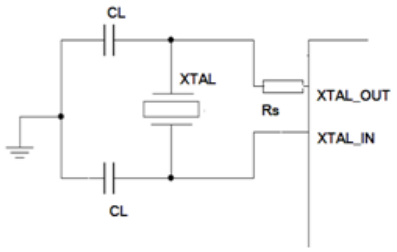



**Figure 31: External Crystal/Oscillator as Clock Source**

**Serial EEPROM (optional)**

For standalone application without a host processor, an IIC EEPROM of minimum size 16Kbit (24c16) or larger (24c32, 24c64, etc.) should be used to provide non-volatile storage of reset configuration parameters for the voice processor. The configuration parameters are read by the FM-1288 during power-up or reset boot up.

Please see earlier sections of this document regarding details.

# References

# I. Terminology

**Table 29: Terminology**

| Term | Definition |
|---|---|
| ADC | Analog to Digital |
| AEC | Acoustic Echo Cancellation |
| Codec | Coder-decoder |
| DAC | Digital to Analog |
| DM | Data Memory |
| DSP | Digital Signal Processor |
| EEPROM | Electrically Erasable Programmable Read-Only Memory |
| HFCK | Hands Free Car Kit |
| IC | Integrated Circuit |
| IIC | Inter-Integrated Circuit |
| IIS | Inter-Integrated Circuit Sound |
| I/O | Input/Output |
| LQFP | Low Profile Quad Flat Pad |
| MCU | Micro Controller Unit |
| MIC | Microphone |
| MIPS | Million instruction per second |
| NC | Not Connected |
| PCM | Pulse Code Modulation |
| PGA | Programmable Gain Amplification |
| PM | Program Memory |
| PND | Portable Navigation Device |
| RAM | Random Access Memory |
| ROM | Read Only Memory |
| SHI | Serial Host Interface |
| SRAM | Static Random Access Memory |
| UART | Universal Asynchronous Receiver/ Transmitter |
| Vpp | Voltage, Peak-to-Peak |
| XTAL | Crystal |

# II. Related Documents

**Table 30: Related Documents**

| Fortemedia Technology Documents | Document Location |
|---|---|
| "FM1288 User Configuration Manual" | Contact Fortemedia Sales |