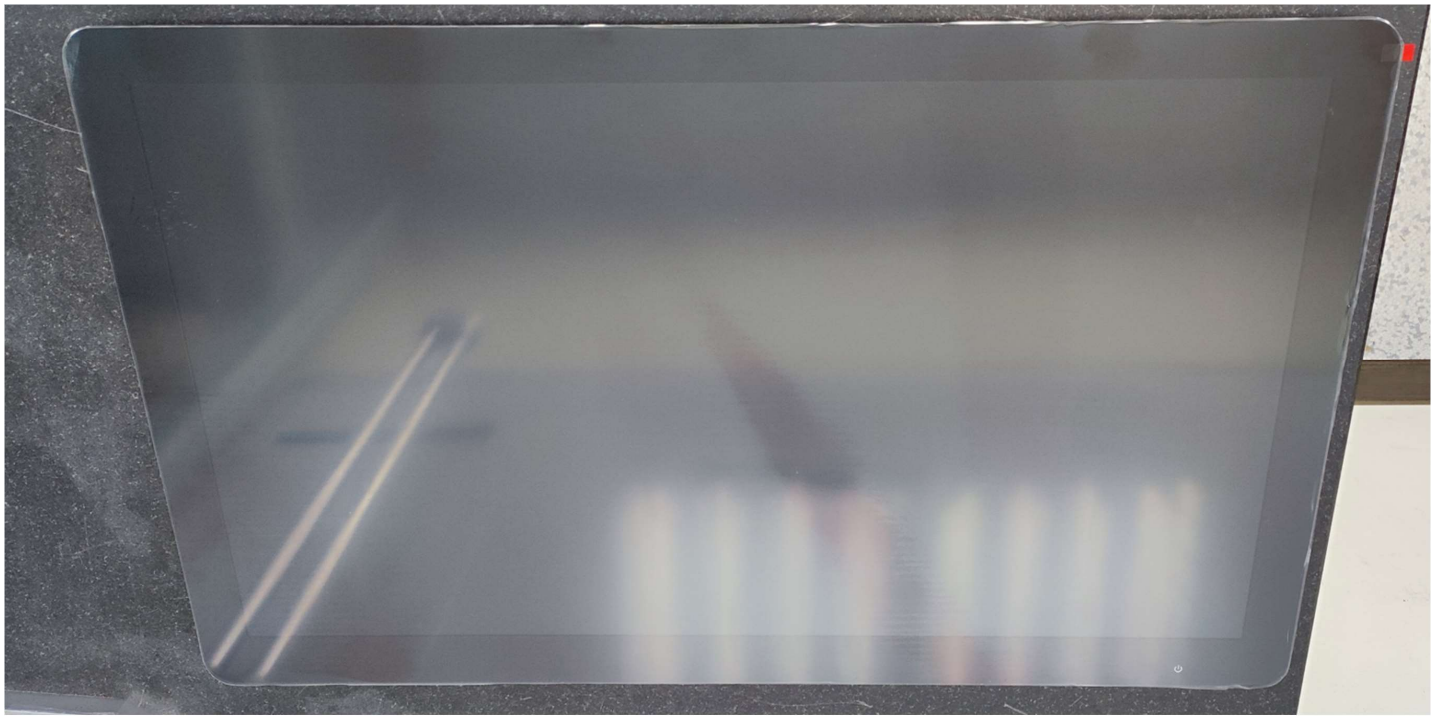




設計驗證
工程課
2023.08.15
發行
虹緯科技開發股份有限公司


QN7001322331-0001
FC270070DSSWNGC3
D15927G0100817R8D2N1211071600
70184WP6J8ZZ-Z50101
Manufactured 21/35
Model No:G270ZAN01.1
AU Optronics
MADE IN CHINA(S01)
E204356
RoHS


設計驗證
工程課
2023.08.15
發行
鈺緯科技開發股份有限公司


Source
EXIT
MENU
ENTER

DATA IMAGE CORPORATION
PRODUCT SPECIFICATION
MODEL NO.: FC270070DSSWNGC3

☐ Preliminary Specification

■ Approval Specification

2AAD642003T(T0201)

Customer :

APPROVED BY

設計驗證
工程課
2023.08.15
發行
虹緯科技開發股份有限公司

SIGNATURE **DATE**

R&D Approved By	Prepared By
Roger	WenChun
Issued Date	Revision
16/AUG/23’	A

2. RECORD OF REVISION

Rev	Date	Item	Page	Comment	Source
1	01/MAR/22'	All 6.1	All 17	Initial Preliminary Modify Outline Drawing from Rev.1 to 2 2)Modify Uniformity from 66.7% Min to 20% Max	ESR1102008
2	12/APR/22'	6.1	17	Modify Outline Drawing from Rev.2 to 3 3)Modify Ink Logo & Icon	NPDO-2475
3	03/MAY/22'	6.1	17	Modify Outline Drawing from Rev.3 to 4 4)Remove Peeling Tape	NPDO-2475
A	16/AUG/23'	6.1 8.2	17 21	Modify Outline Drawing from Rev 4 to A. A)Change the drawing from Rev 4 to A. Add CARTON PACKAGE Release Rev: A for production.	NPPR-230728001

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1. GENERAL DESCRIPTION

1.1 OVERVIEW

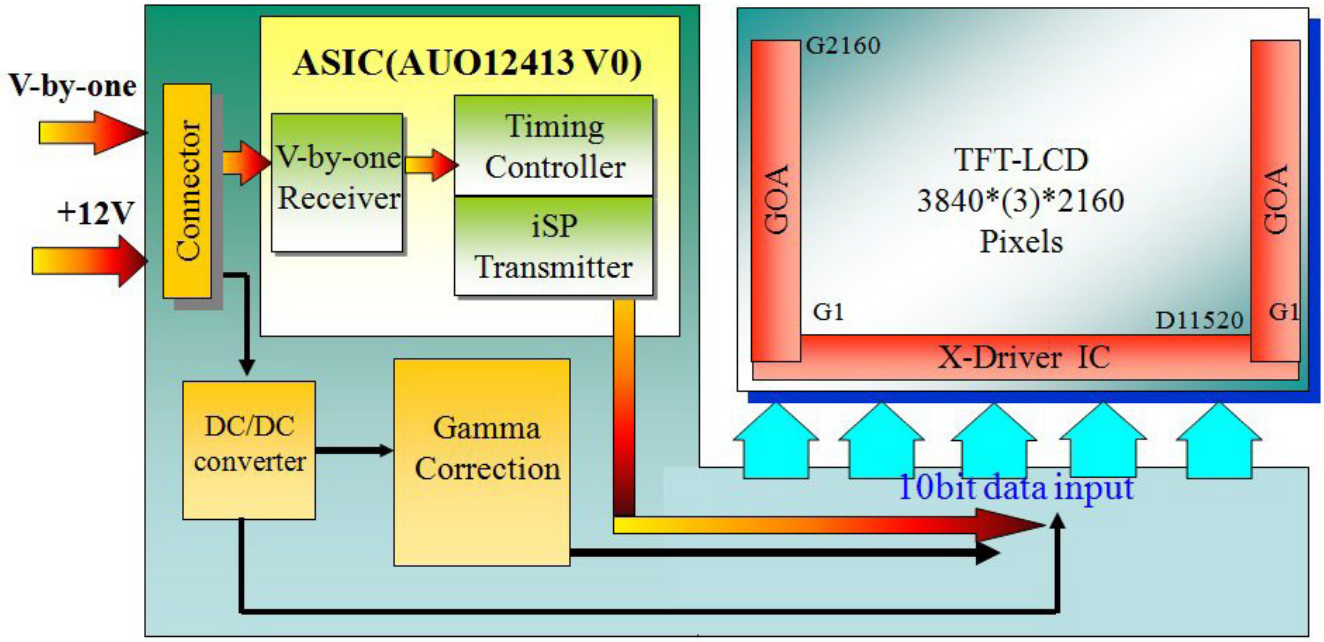
FC270070DSSWNGC3 is a 27" (27" diagonal) a-Si & transmissive type thin film transistor liquid crystal display (TFT-LCD) module with V by one interface. The module is composed of a TFT-LCD panel, driver circuit, and backlight unit.

1.2 TFT LCD MODULE SPECIFICATIONS

The following items are characteristics summary on the table under 25℃ condition :

Parameter	Specifications	Unit
Screen Size	27(diagonal)	inch
LCD Outline Dimension	656.9(H) x 399.9(V) x 25.8(D)	mm
LCD Active Area	596.16(H) x 335.34(V)	mm
Resolution	3840(H) x (R,G,B) x 2160(V)	Dots
Pixel Pitch	0.15525(H) x 0.15525(V)	mm
Pixel Arrangement	R.G.B. Vertical Stripe	
Display Mode	AHVA mode, Normally Black	
Display Colors	1.078 colors (8bit+Hi FRC)	
View direction	All	
Luminance, White	800	cd/m^2
LCD Interface	V by one	
Surface treatment	AR& AF(AS)Coating	
RoHS Compliance	Yes	

2. FUNCITONAL BLOCK DIAGRAM

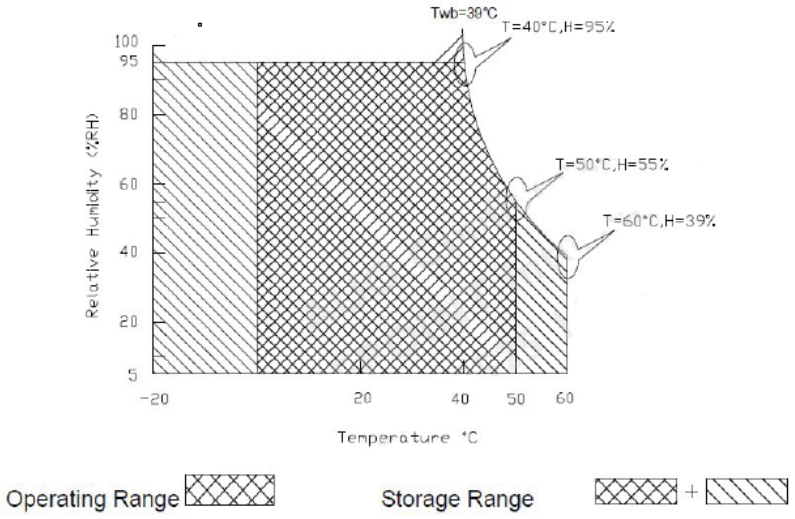


3.ABSOLUTE MAXIMUM RATINGS

3.1 ABSOLUTE RATINGS OF ENVIRONMENT

Parameter	Symbol	MIN.	MAX.	Unit	Remark
Operating Temperature	Top	0	50	°C	
Storage Temperature	Tst	-20	60	°C	
Operation Humidity	Hop	5	90	%RH	
Storage Humidity	Hst	5	90	%RH	

Note: Maximum Wet-Bulb should be 39°C and no condensation



3.2 ELECTRICAL ABSOLUTE RATINGS

Ta=25°C

Parameter	Symbol	MIN.	MAX.	Unit	Remark
Logic/LCD Drive Voltage	Vin	GND-0.3	14	V	

4. ELECTRICAL SPECIFCATIONS

4.1 ELECTRICAL CHARACTERISTICS

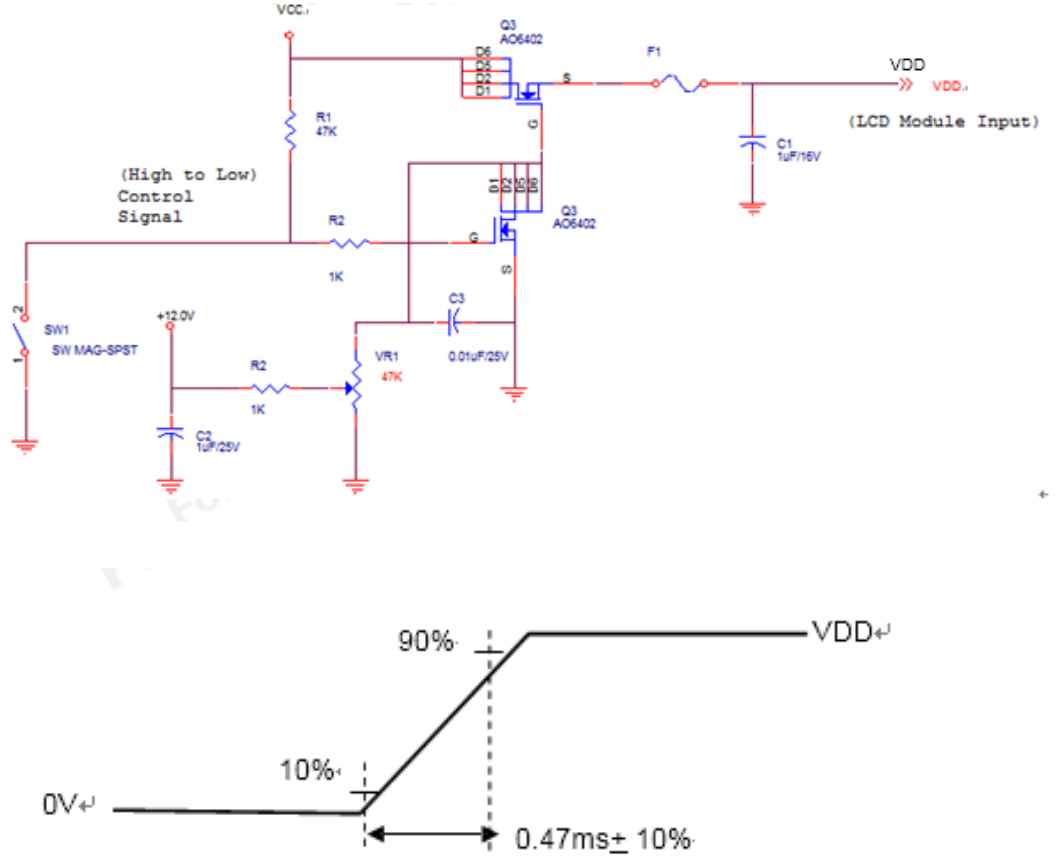
4.1.1 TFT LCD MODULE ELETRONICS SPECIFICATION

Input power specifications are shown as follows

Ta=25°C

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Power Supply Input voltage	VDD	10.8	12	13.2	V	
Power supply Input Current (RMS)	IDD	-	1.08	1.3	A	VDD= 12.0V, White pattern, fV=60Hz
Inrush Current	I_{Rush}	-	-	3	A	Note1
VDD Power Consumption	PDD	-	12.96	15.6	W	VDD= 12.0V , White pattern, fV=60Hz
Allowable VDD Ripple Voltage	VDDrp	-	-	VDD* 5%	[mV]	VDD= 12.0V, White pattern, fV=60Hz

Note1：Measurement conditions:



VDD rising time

4.1.2 BACKLIGHT UNIT SPECIFICATION

Following characteristics are measured under a stable condition using an inverter at 25°C(Room Temperature)

Item	Symbol	Min.	Typ.	Max.	Unit	Remark
Backlight Input Voltage	VDD	21.6	24	26.4	V	
Backlight Input Current	IVDD	-	2.05	2.46	A	100% PWM Duty
Backlight Power Consumption	PVDD	-	49.2	59.04	W	100% PWM Duty
Inrush Current	Irush LED	-	-	6	A	at rising time=470us
Dimming Frequency	FPWM	-	0.2	20	kHZ	
Swing Voltage		3	3.3	5.0	V	
Dimming Duty Cycle		10	-	100	%	
	LED Lifetime	50,000	-	-	Hrs	IF =70 mA, Ta = 25°C

Note 1: Ta means ambient temperature of TFT-LCD module
Note 2: VDD, PVDD, PVDD, Irush LED are defined for LED B/L.(100% duty of PWM dimming)
Note 3: If G270ZAN01.1 module is driven by high current or at high ambient temperature & humidity condition. The operating life will be reduced.
Note 4: The LED life-time is estimated data. And is defined when a single LED operated in room temperature, the estimated time to 50% degradation of initial luminous.
Note 5: Only one kind types for adjusting brightness: PWM.

4.2 SIGNAL CHARACTERISTICS

4.2.1 INTERFACE TIMING

Signal		Symbol	Min.	Typ.	Max.	Unit
Vertical Section	Period	Tv	2200	2250	2660	Th
	Active	Tdisp(v)	-	2160	-	Th
	Blanking	Tbp(v)+Tfp(v)+PWvs	40	90	500	Th
Horizontal Section	Period	Th	530	550	600	Tclk
	Active	Tdisp(h)	-	480	-	Tclk
	Blanking	Tbp(h)+Tfp(h)+PWhs	50	70	120	Tclk
Clock	Period	Tclk	15.15	13	12.98	ns
	Frequency	Freq.	66	74.25	77	MHz
Frame Rate	Frequency	1/Tv	45	60	63	Hz

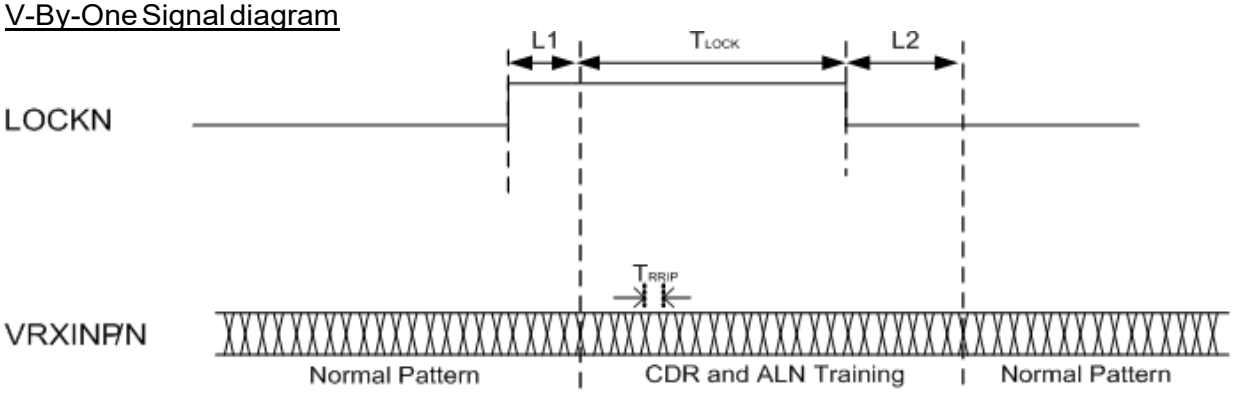
Note: DE mode only.

4.2.2 V-BY-ONE SPEC

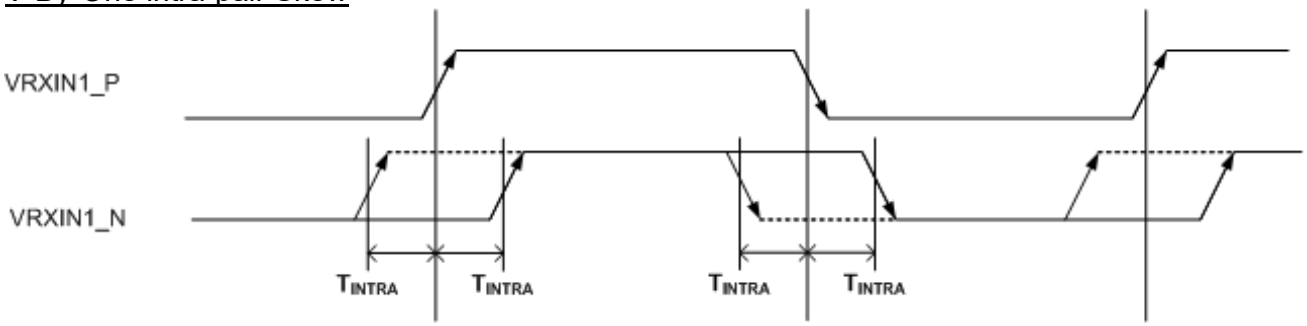
Item		Symbol	Min.	Typ.	Max.	Unit	Remark
V-by-one Interface	VRXINP/N input each bit Period	TRRIP	310	--	379	ps	1
	CDR training pattern time	TLOCK	--	500	--	us	1
	Latency from LOCKN 'HIGH' to clock training pattern	L1	0	--	--	us	1
	Latency from LOCKN 'LOW' to normal 8b10b data	L2	--	--	70	us	1
	CML Differential Input High Threshold	VRTH	+50			mV_{DC}	
	CML Differential Input Low Threshold	VRTL			-50	mV_{DC}	
	CML Common mode Bias Voltage	VRCT	0.8	0.9	1.0	mV_{DC}	
	Intra-pair skew	TINTRA	--	--	0.3	UI	2
	Inter-pair skew	TINTER	--	--	5	UI	3

Note: The V-By-One receiver spec is compliant to V-By-One HS standard version

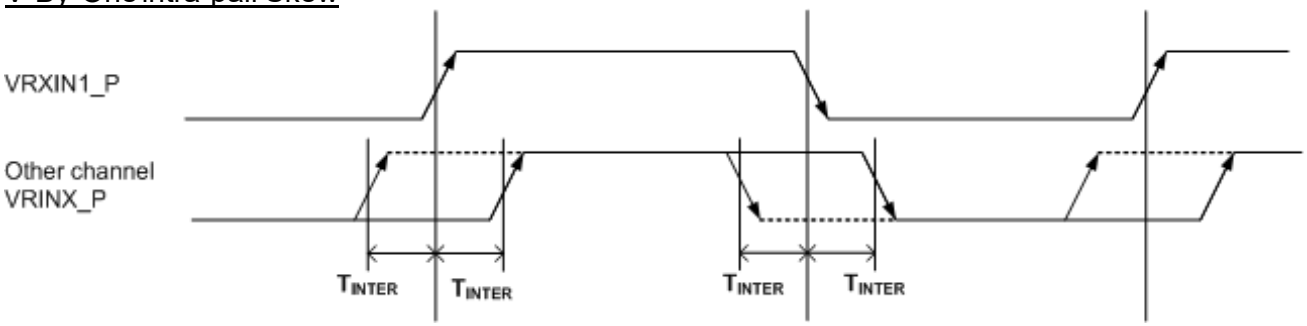
V-By-One Signal diagram



V-By-One intra-pair Skew

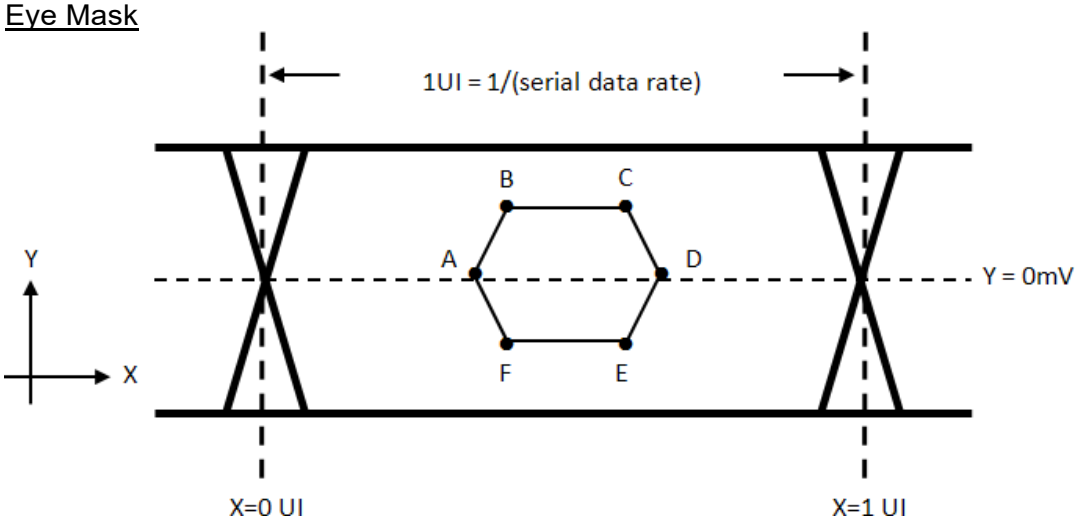


V-By-One intra-pair Skew



Item		Symbol	Min.	Typ.	Max.	Unit	Remark
V-by-one Interface	Eye diagram at receiver	A_X	--	0.25	--	UI	1
		A_Y	--	0	--	mV	
		B_X	--	0.3	--	UI	
		B_Y	--	50	--	mV	
		C_X	--	0.7	--	UI	
		C_Y	--	50	--	mV	
		D_X	--	0.75	--	UI	
		D_Y	--	0	--	mV	
		E_X	--	0.7	--	UI	
		E_Y	--	-50	--	mV	
		F_X	--	0.3	--	UI	
		F_Y	--	-50	--	mV	

Eye Mask



4.2.3 COLOR DATA INPUT REFERENCE

The brightness of each primary color is based on the 10bit gray scale data input for the color; the higher the Binary input, the brighter the color. The table below provides a reference for color versus data input.

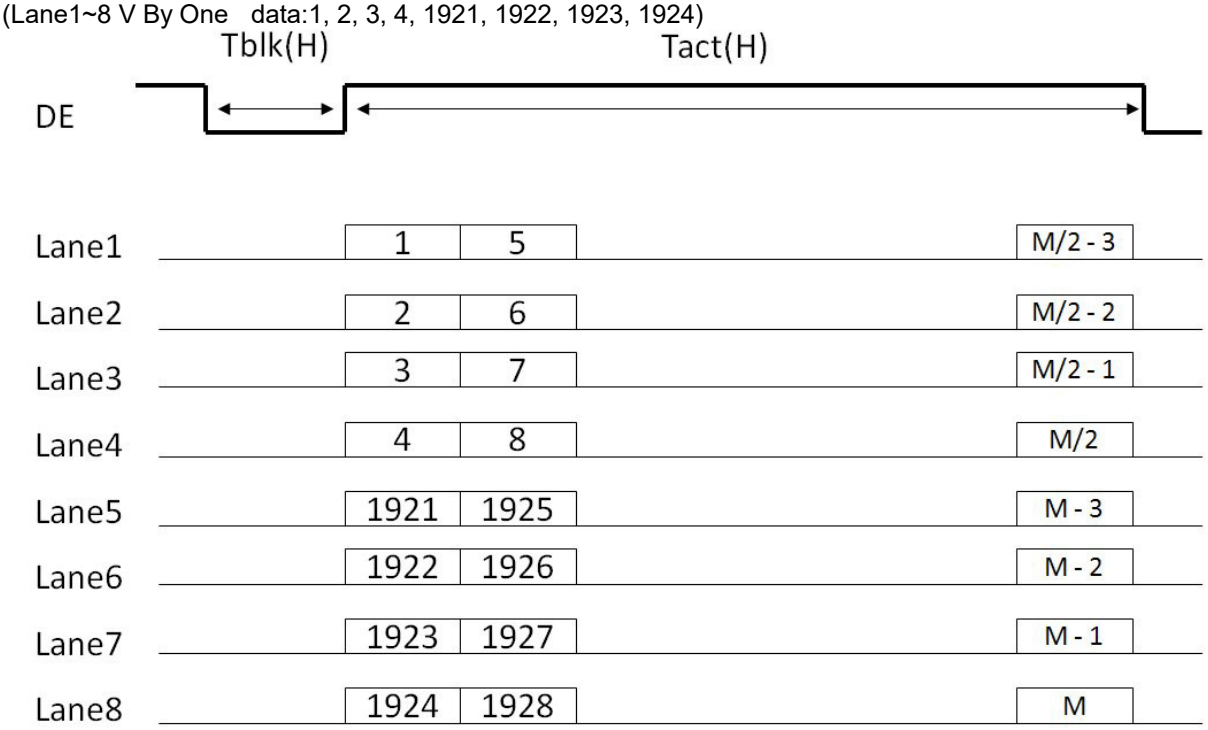
Color		Input color data																													
		RED										GREEN										BLUE									
		MSB									LSB	MSB									LSB	MSB									LSB
		R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Basic Color	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(0123)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue(1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R	RED(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(001)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	....																														
	RED(1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
G	Green(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	....																														
	Green(1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	Green(1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
B	Blue(000)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(001)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	....																														
	Blue(1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	Blue(1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

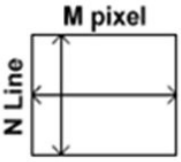
The Input Data Format

Mode	Packer input & Unpacker output		30bpp RGB /YCbCr444 (10bit)
4byte mode	Byte0	D[0]	R/Cr[2]
		D[1]	R/Cr[3]
		D[2]	R/Cr[4]
		D[3]	R/Cr[5]
		D[4]	R/Cr[6]
		D[5]	R/Cr[7]
		D[6]	R/Cr[8]
		D[7]	R/Cr[9]
	Byte1	D[8]	G/Y[2]
		D[9]	G/Y[3]
		D[10]	G/Y[4]
		D[11]	G/Y[5]
		D[12]	G/Y[6]
		D[13]	G/Y[7]
		D[14]	G/Y[8]
		D[15]	G/Y[9]
	Byte2	D[16]	B/Cb[2]
		D[17]	B/Cb[3]
		D[18]	B/Cb[4]
		D[19]	B/Cb[5]
		D[20]	B/Cb[6]
		D[21]	B/Cb[7]
		D[22]	B/Cb[8]
		D[23]	B/Cb[9]
	Byte3	D[24]	- -
		D[25]	- -
		D[26]	B/Cb[0]
		D[27]	B/Cb[1]
		D[28]	G/Y[0]
		D[29]	G/Y[1]
		D[30]	R/Cr[0]
		D[31]	R/Cr[1]

4.2.4 TIMING DIAGRAM

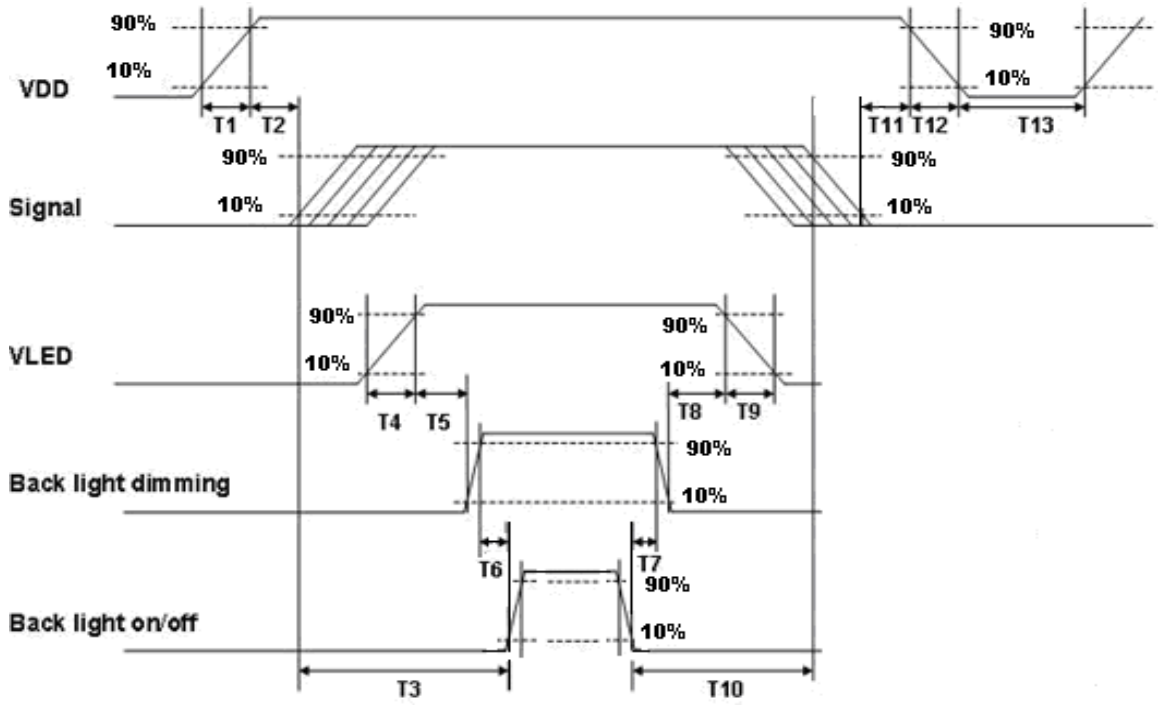
(Lane1~8 V By One data:1, 2, 3, 4, 1921, 1922, 1923, 1924)





4.2.5 POWER ON/OFF SEQUENCE

VDD power and lamp on/off sequence is as below. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.



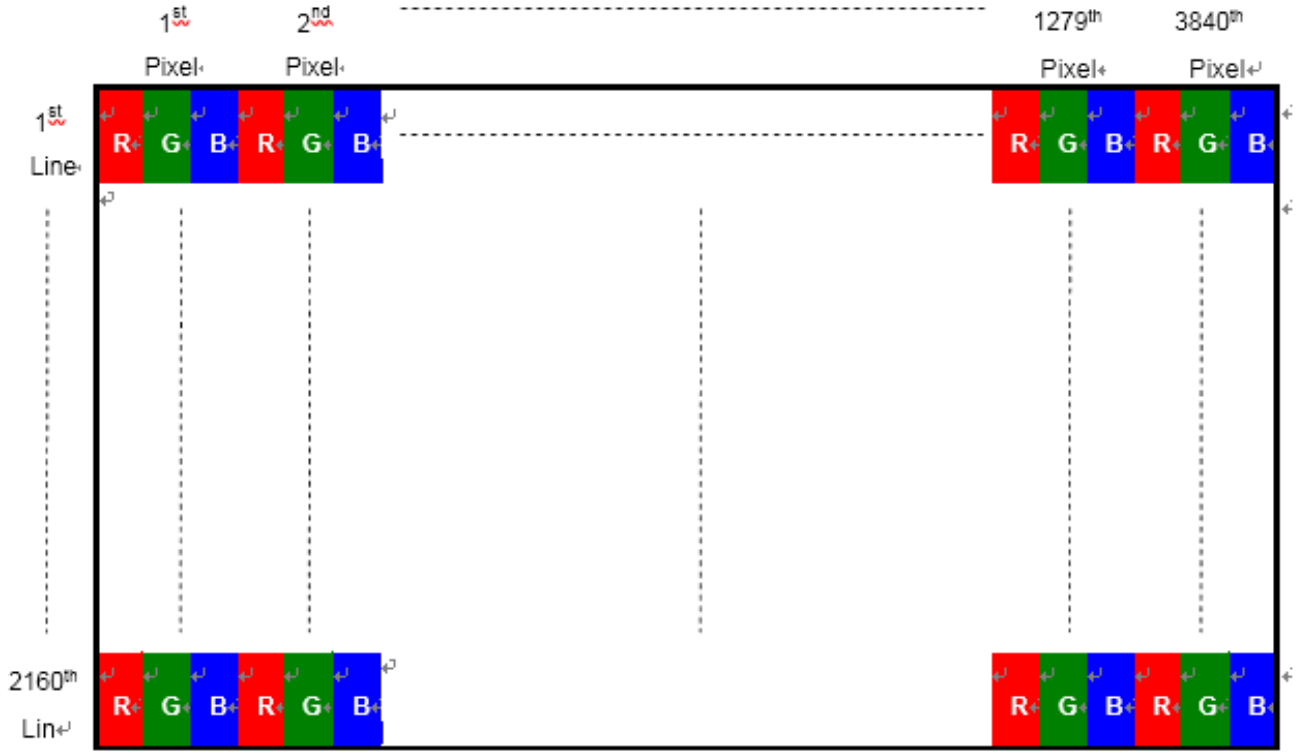
Power ON/OFF sequence timing

Parameter	Value				Remark
	Min.	Typ.	Max.	Units	
T1	0.5	-	10	ms	
T2	40	-	- *1	ms	
T3	200	-	--	ms	
T4	0.5	-	10	ms	
T5	10	-	-	ms	
T6	10	-	- *2	ms	
T7	0	-	-	ms	
T8	10	-	-	ms	
T9	-	-	10	ms	
T10	110	-	-	ms	
T11	0	16	50	ms	
T12	0		10	ms	
T13	1000	-	-	ms	

Note 1 (T2)：The maximum timing of VDD rising(90%) to HTPDN falling edge decided by customer system
Note 2 (T6)：voltage of VDD must decay smoothly after power-off.(customer system decide this value)

4.3 PIXEL FORMAT IMAGE

Following figure shows the relationship between input signal and LCD pixel format



4.4 INTERFACE CONNECTIONS

4.4.1 CN1 PIN DEFINITION

Pin No.	Symbol	Function	Note
1	VDD	Power input (+12V)	
2	VDD	Power input (+12V)	
3	VDD	Power input (+12V)	
4	VDD	Power input (+12V)	
5	VDD	Power input (+12V)	
6	VDD	Power input (+12V)	
7	VDD	Power input (+12V)	
8	VDD	Power input (+12V)	
9	NC	No Connection	
10	GND	Ground	
11	GND	Ground	
12	GND	Ground	
13	GND	Ground	
14	GND	Ground	
15	NC	No Connection	
16	NC	No Connection	
17	NC	No Connection	
18	NC	For internal use, no connection	
19	NC	For internal use, no connection	
20	NC	No Connection	
21	NC	No Connection	
22	NC	No Connection	
23	NC	No Connection	
24	NC	No Connection	
25	HTPDN	Vx1 HTPDN	
26	LOCKN	Vx1 LOCKN	
27	GND	Ground	
28	RX0N	Vx1 lane0	
29	RX0P	Vx1 lane0	
30	GND	Ground	
31	RX1N	Vx1 lane1	
32	RX1P	Vx1 lane1	
33	GND	Ground	
34	RX2N	Vx1 lane2	
35	RX2P	Vx1 lane2	
36	GND	Ground	
37	RX3N	Vx1 lane3	
38	RX3P	Vx1 lane3	
39	GND	Ground	
40	RX4N	Vx1 lane4	
41	RX4P	Vx1 lane4	
42	GND	Ground	
43	RX5N	Vx1 lane5	

44	RX5P	Vx1 lane5	
45	GND	Ground	
46	RX6N	Vx1 lane6	
47	RX6P	Vx1 lane6	
48	GND	Ground	
49	RX7N	Vx1 lane7	
50	RX7P	Vx1 lane7	
51	GND	Ground	

4.4.2 CN2 B/L PIN DEFINE

Pin No.	Symbol	Function	Note
1	VDD	Power +24V	
2	VDD	Power +24V	
3	VDD	Power +24V	
4	VDD	Power +24V	
5	VDD	Power +24V	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground	
9	GND	Ground	
10	GND	Ground	
11	NC	Do not connect	
12	EN	Enable (0V: disable, 2.5~5V: Enable)	
13	Dimming	PWM; duty 10%~ 100%	
14	NC	Do not connect	

5. OPTICAL SPECIFICATIONS

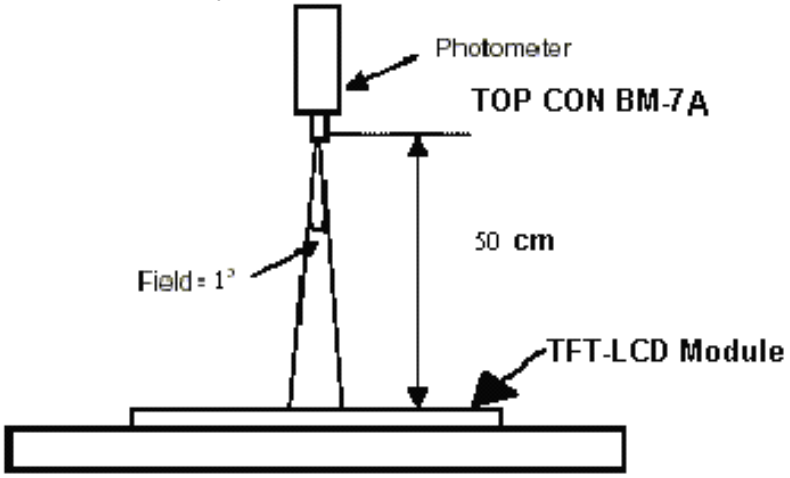
5.1 OPTICAL CHARACTERISTICS

Ta = 25°C

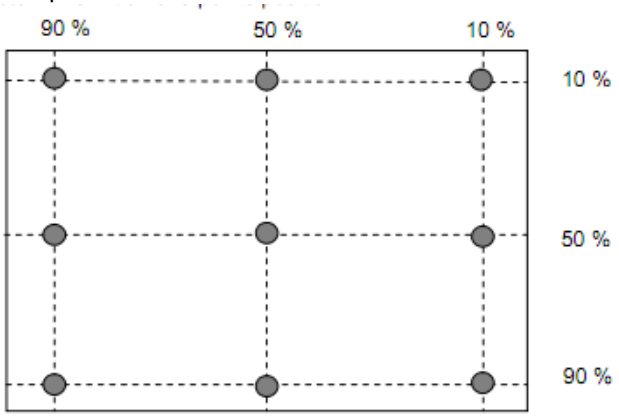
Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	θ_x+	Center CR≥10	75	89	--	deg.	Note 6
		θ_x-		75	89	--		
	Vertical	θ_Y+		70	89	--		
		θ_Y-		70	89	--		
Contrast Ratio		CR	at optimized viewing angle	700	1000	--		Note 4
Response time	Rise+ Fall	Tr+ Tf	Center θx=θy =0°	-	16	25	ms	Note 5
Uniformity		B-uni	θx=θy =0°	--	-	20	%	Note2,3
LCM Brightness		L	θx=θy =0°	640	800	--	cd/㎡	Note 1
Chromaticity		Wx	Center θx=θy =0°	0.283	0.313	0.343		
		Wy		0.299	0.329	0.359		

The following optical specifications shall be measured in a darkroom or equivalent state (ambient luminance ≤1 lux, and at room temperature). The operation temperature is 25°C±2°C. The measurement method is shown in Note1.

Note 1: The method of optical measurement:



Note 2: Definition of 9 points position



Note 3: Definition of luminance uniformity of 9 points.

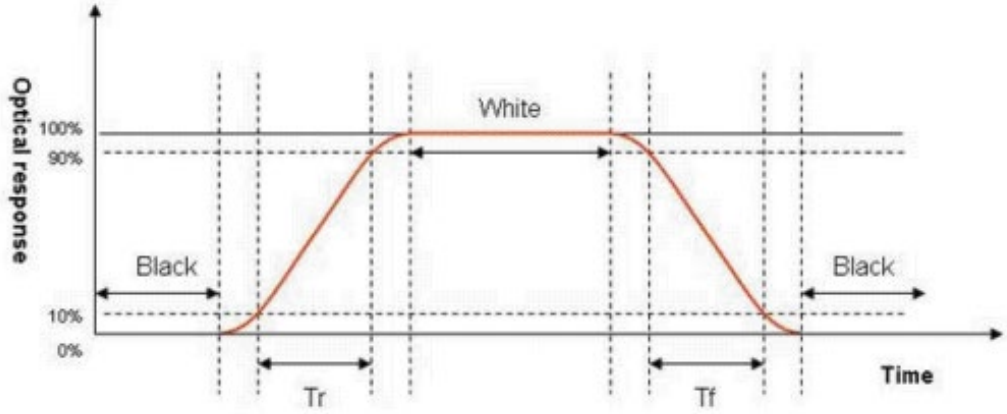
$$\delta_{w9} = \frac{\left|B_{max} \text{ or } B_{min} - B_{avg}\right|}{B_{avg}} \times 100\%$$

Note 4: Definition of contrast ratio (CR):

$$\text{contrast ratio CR} = \frac{\text{Brightness on the “White” state}}{\text{Brightness on the “Black” state}}$$

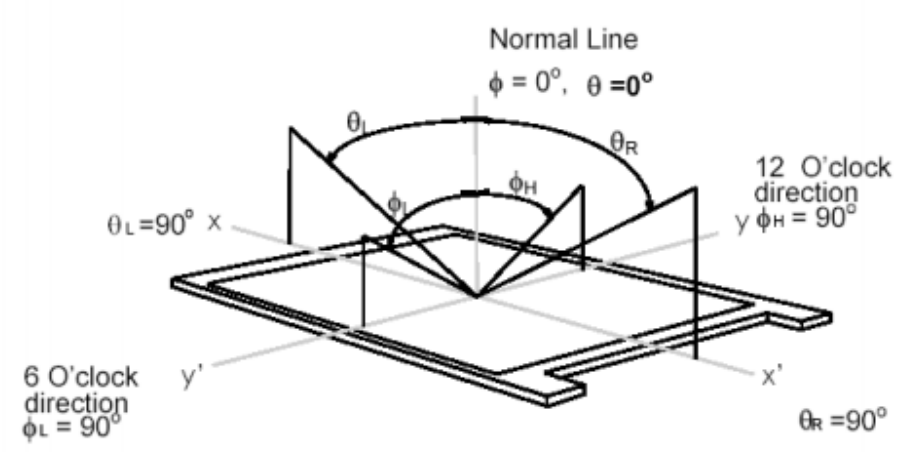
Note 5: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “White” to “Black” (falling time) and from “Black” to “White” (rising time), respectively. The response time interval is between 10% and 90% of amplitudes. Please refer to the figure as below



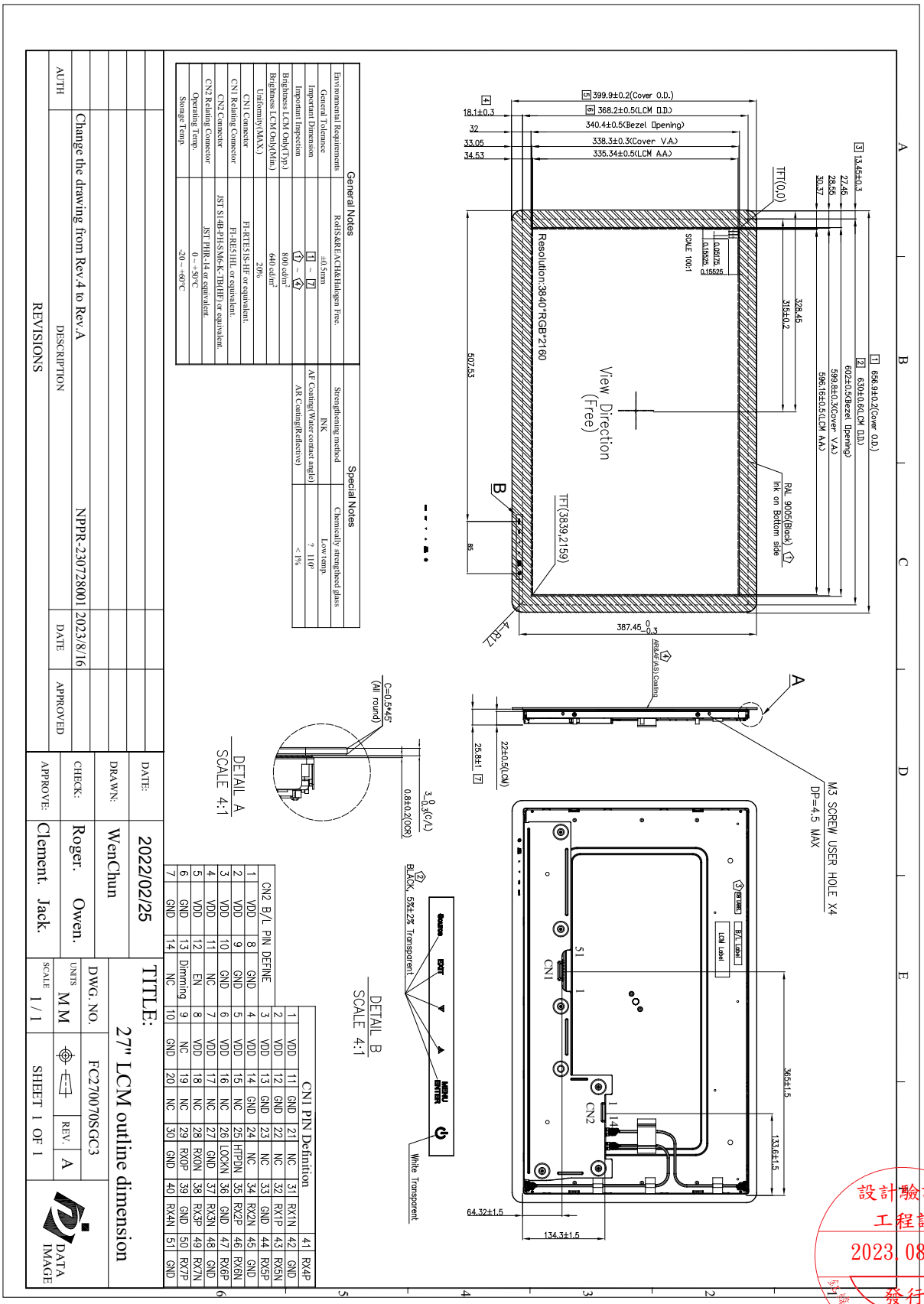
Note 6: Definition of viewing angle

Viewing angle is the measurement of contrast ratio □ 10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as below: 90° (θ) horizontal left and right, and 90° (Φ) vertical high (up) and low (down). The measurement direction is typically
perpendicular to the display surface with the screen rotated to its center to develop the desired measurement
viewing angle.



6. MECHANICAL SPECIFICATIONS

6.1 OUTLINE DRAWING



設計驗證
工程課
2023.08.15
發行
群燿科技開發股份有限公司

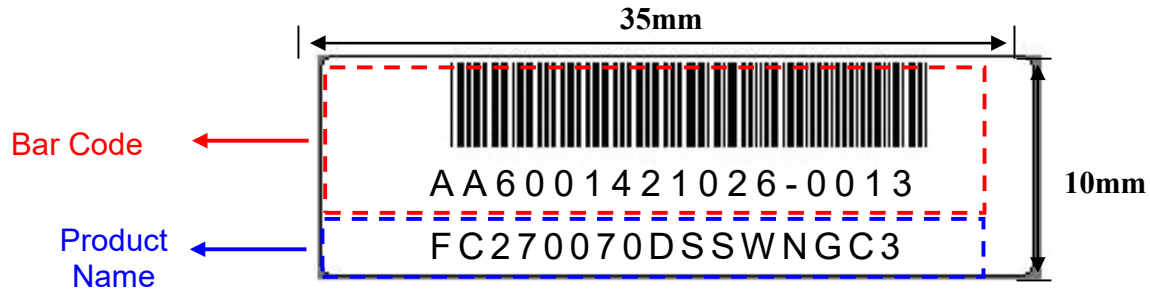
7. RELIABILITY TEST ITEM

Reliability Test Item & Level			Remark
No.	Test Item	Test Level	
1	High Temperature Storage Test	Ta=60°C,240hrs	IEC60068-2-2
2	Low Temperature Storage Test	Ta=-20°C,240hrs	IEC60068-2-1
3	High Temperature Operation Test	Ta=50°C,240hrs	IEC60068-2-2
4	Low Temperature Operation Test	Ta=0°C,240hrs	IEC60068-2-1
5	High Temperature and High Humidity (No operation)	T=50°C,80%RH,240hrs	IEC60068-2-3
6	Thermal Cycling Test (No operation)	-20°C /30min, 60/ °C 30min, 100 cycles	IEC60068-2-14
7	Vibration test (Package)	Frequency:10~55HZ Amplitude:1.5mm Sweep time:11min Test period:6Cycles for each direction of X,Y,Z	IEC60068-2-6
8	Drop test (Package)	Height :60cm 1 conner,3edges,6surfaces	IEC60068-2-32
9	Electrostatic Discharge Test	State: operating Location: LCM/TP surface Condition:150pf 330Ω Contact +/- 8kV Air +/-15kV Criteria: Class B	IEC61000-4-2

8. LCM PRODUCT LABEL DEFINE

8.1 SHIPPING LABLE

Product Label style:

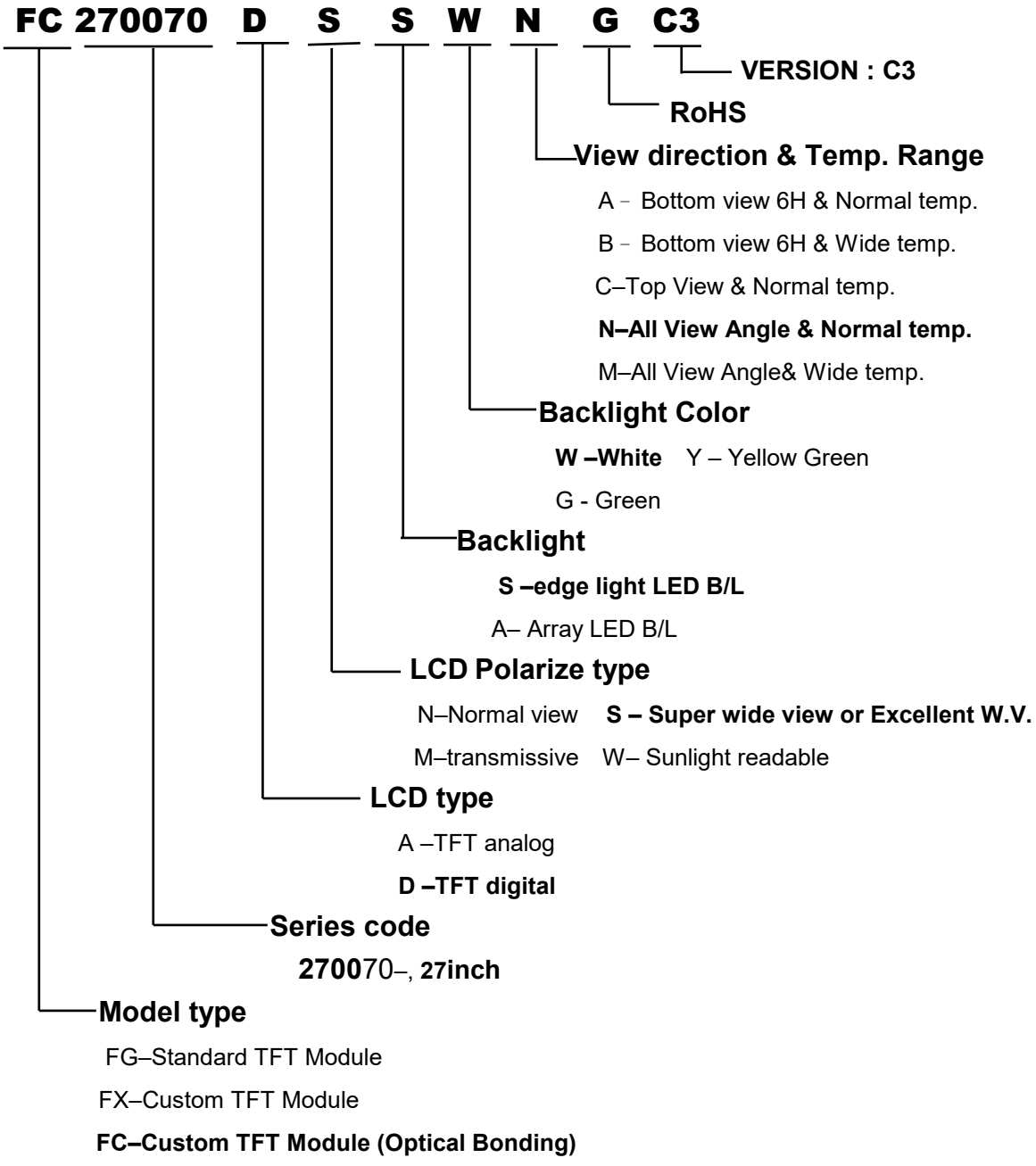


BarCode Define:

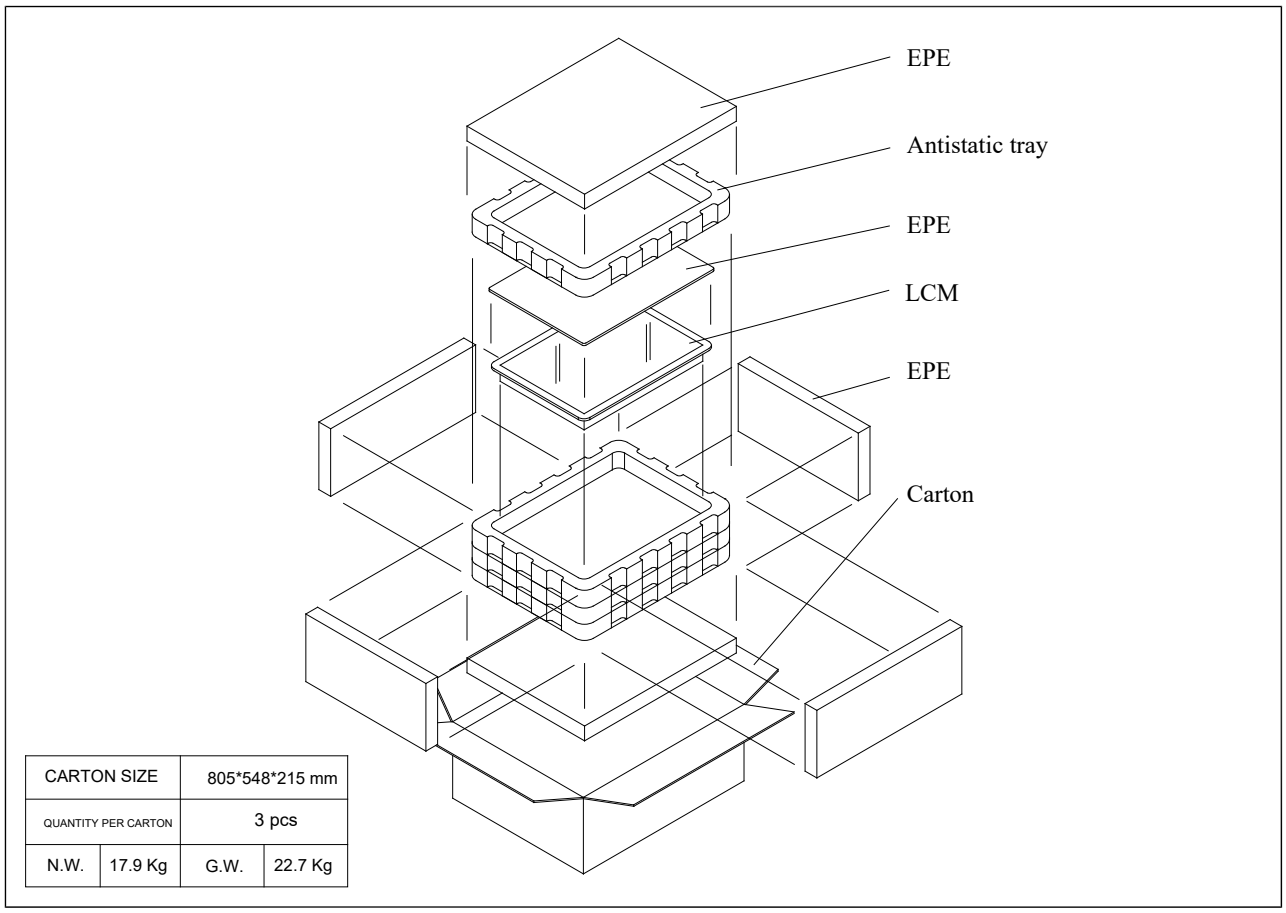
A A 6 0014 2 10 26-0013

- Serial number of the products
  Serial number starts from 0000
  Every work order is 10K at most
- Week of production
- Year of production
- Storage area
- Serial number of work order
  Serial number starts from 0000 each month
- Month of work order
- Year of work order
- The first 3 numbers of work order

Product Name Define:



8.2 CARTON PACKAGE



CARTON SIZE		805*548*215 mm	
QUANTITY PER CARTON		3 pcs	
N.W.	17.9 Kg	G.W.	22.7 Kg

9.Precaution

9.1 HANDLING PRECAUTIONS

(1). The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2). While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3). Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4). Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5). If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6). Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7). If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8). Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9). Do not disassemble the module.

(10). Do not pull or fold the LED wire.

(11). Pins of I/F connector should not be touched directly with bare hands.

9.2 STORAGE PRECAUTIONS

(1). High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2). It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3). It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

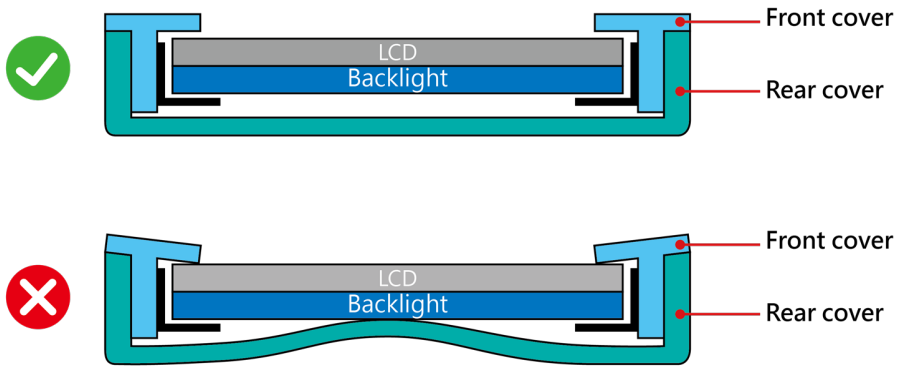
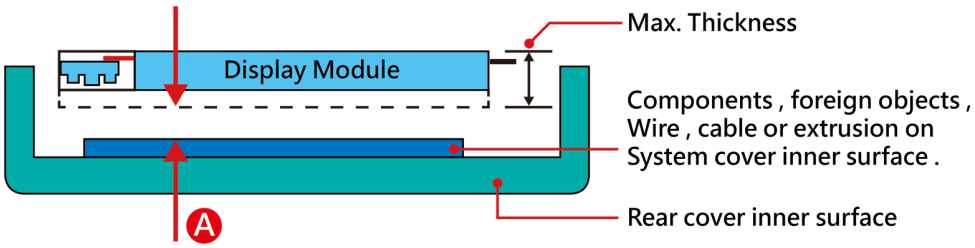
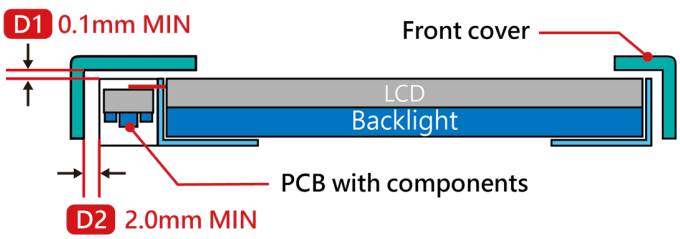
9.3 OPERATION PRECAUTIONS

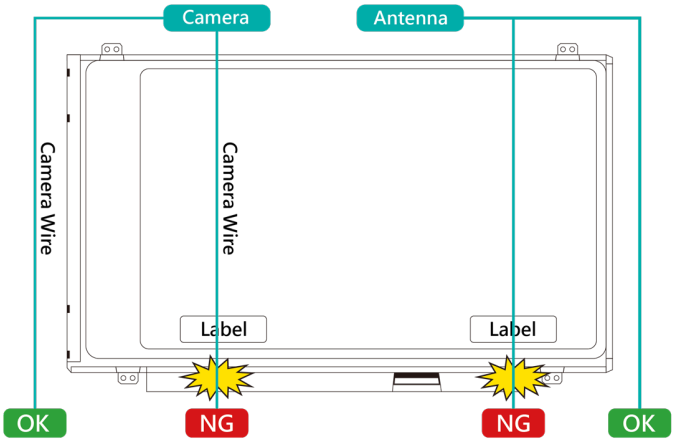
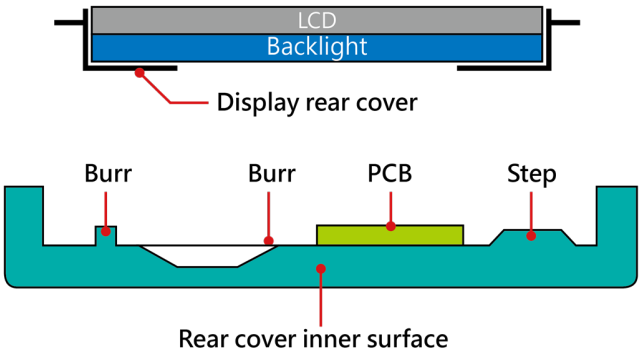
(1). Do not pull the I/F connector in or out while the module is operating.

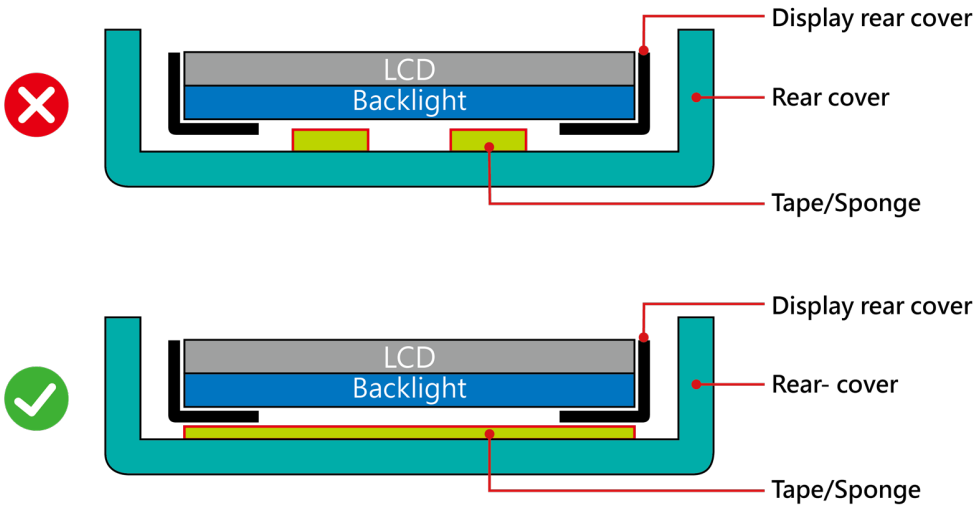
(2). Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

(3). The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the module or insert anything into the Backlight unit.

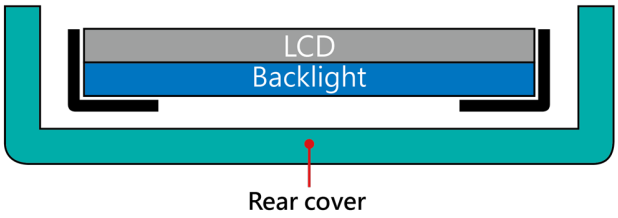
Appendix. Covers Design Guideline

A.	**Permanent deformation of front/rear covers after reliability test**
	
Definition	Front/rear covers may deform during reliability test. Permanent deformation of front/rear covers after reliability test should not interfere with display. Because it may cause issues such as pooling, abnormal display, white spot, and also cell crack.
B.	**Design gap A between display and any components on rear cover**
	
Definition	Gap A between display's maximum thickness boundary and rear cover inner surface components such as wire, cable, extrusion is needed for preventing from backpack or pogo test fail. Because zero gap or interference may cause stress concentration. Issues such as pooling, abnormal display, white spot, white spot and cell crack may occur. Flatness of display and rear cover should be taken into account for gap design.
C.	**Design gap D1 & D2 between front cover and PCB assembly**
	

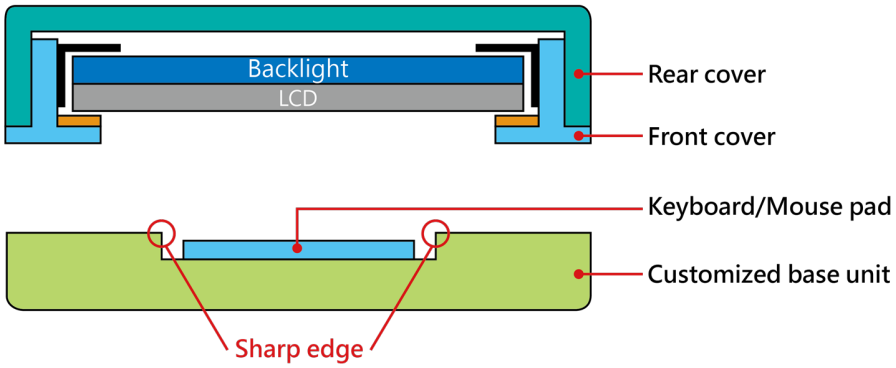
Definition	Gap D1 & D2 between front cover and LCD & front cover and PCBA are needed to prevent pooling or glass broken. Zero gap or interference such as burr and warpage from mold frame may cause pooling issue near front cover opening edge. This phenomenon is obvious during swing test, hinge test, knock test or during pooling inspection procedure. To remain sufficient gap, design with system rib higher than maximum display thickness is recommended.
D.	**Interference examination of camera's and antenna's cable**
	
Definition	Camera's and antenna's cable should not overlap with panel outline. Because issue such as abnormal display and white spot after backpack test, hinge test, twist test or pogo test may occur.
E.	**Rear cover inner surface examination**
	
Definition	Burr at logo edge, steps, protrusions or PCB may cause stress concentration. Whiter spot or glass broken issue may occur during reliability test.
F.	**Tape/sponge design on rear cover inner surface**



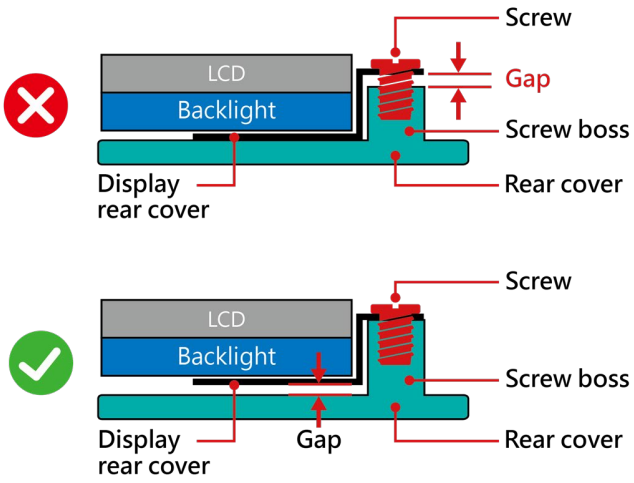
Definition	To prevent abnormal display and white spot after scuffing test, hinge test, pogo test, backpack test, tape/sponge should be well covered under rear cover. Because tape/sponge in separate location may act as pressure concentration location.
G.	**Material used for rear cover**



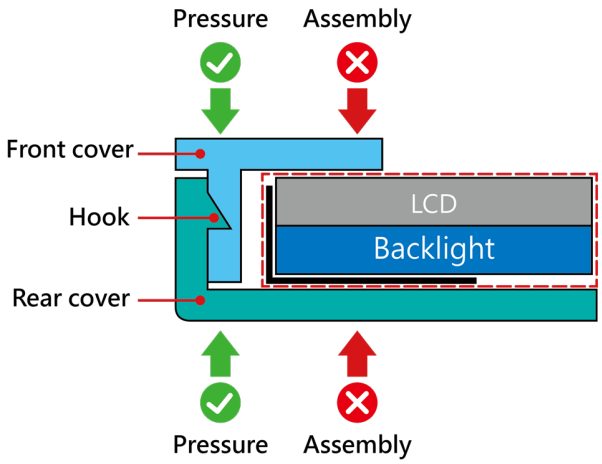
Definition	Rear cover material with high rigidity is needed to resist deformation during scuffing test, hinge test, pogo test or backpack test. Abnormal display, white spot, pooling issue may occur if low rigidity material is used. Pooling issue may occur because screw's boss positioning for module's bracket are deformed during open-close test. Solid structure design of system rear cover may also influence the rigidity of rear cover. The deformation of rear cover should not caused interference.
H.	**Customized base unit design near keyboard and mouse pad**



Definition	To prevent abnormal display and white spot after Scuffing test, hinge test, pogo test, backpack test, sharp edge design in keyboard surface may damage display during the test. We suggest to use slope edge design or to reduce the thickness difference of keyboard/mouse pad from the nearby surface.
I.	**Screw boss height design**

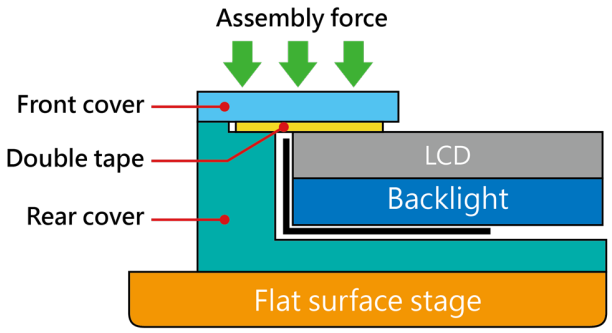


Definition	Screw boss height should be designed with respect to the height of bracket bottom surface to display bottom surface with flatness change of display it set. Because gap will exist between screw boss and bracket, if the screw boss height is smaller. As result while fastening screw, bracket will deformed and pooling issue may occur.
J.	**Assembly SOP examination for front cover with Hook design**



Definition	To prevent display crack during front cover assembly process with hook design, it is not recommended to press display or any location that related directly to the display.

L.	**Assembly SOP examination for front cover with Double tape design**



Definition	To prevent display crack during system front cover assembly process with double tape design, it is only allowed to give slight pressure (MAX 3 Kgf/50mm2) with large contact area. This can help to distribute the stress and prevent stress concentration. We also suggest putting the system on a flat surface stage to prevent unequal stress distribution during the assembly.