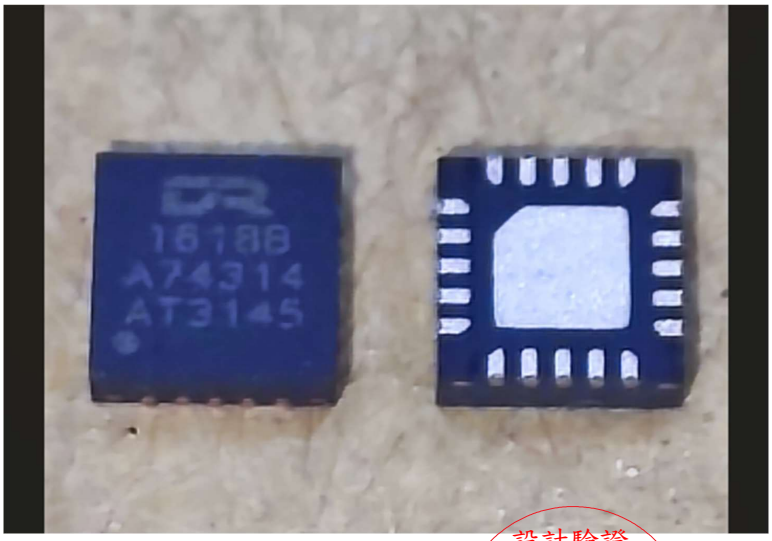

設計驗證
工程課
2023.10.12
發行
旺樂科技開發股份有限公司

承　　認　　書

品　　名：DR1618BQC

規　　格：USB TYPE-C® PORT PROTECTOR

SHORT-TO-VBUS OVERVOLTAGE AND IEC ESD PROTECTION

製 造 廠 商：DERUN MICROELECTRONICS

客　　戶：DIVA Laboratories. Ltd.

客 戶 料 號：3ADR1618B1Y (A0542)

適 用 機 種：

送 樣 日 期：2023-10-12

備　　註：物料說明 : IC (DR1618_QFN21,DERUN)

客 戶 承 認：

主　管	經　辦
	設計驗證 工程課 2023.10.12 發行 鈺偉科技開發股份有限公司

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PREPARED BY : Lange Chen

DR1618B: USB TYPE-C® PORT PROTECTOR

SHORT-TO-VBUS OVERVOLTAGE AND IEC ESD PROTECTION

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General Description

DR1618B provides an integrated single-chip protection solution for USB Type-C® connector. The solution of DR1618B includes Short-to-VBUS voltage protection for 4 channels, and a plus on 6 channels ESD protection.

USB Type-C® connector is well-known as a new generation USB interface. It enables flip-ability, and adapts to various advanced application ranging from USB 3.2, USB4, DisplayPort, Thunderbolt, up to 100W USB Power Delivery, and other Quick Charge specification.

With multiply pin assignments merged in a tiny USB Type-C® connector, each pin is closed to each other. Given any of the slightly slip connection or humidity, it will result the short in VBUS, CC line, and SBU. Once the VBUS voltage exceeds 5V, it possesses highly potential to destroy CC and SBU pin on the connector, which leads the malfunction on the product. Therefore, it is important to follow the USB Power Delivery specification in having VBUS voltage tolerance to 24V so as to prevent shorting issue.

DR1618B features to work as standalone IC and will not interfere any of product functionality. Over-voltage protection will be triggered when the voltage exceeds 5V. However, with DR1618B, it will serve as a protection IC to mitigate the over-voltage situation. In addition to the voltage protection function, DR1618B is integrated with IEC 61000-4-2 ESD protection on CC1, CC2, SBU1, SBU2, DP, DM so as to avoid using additional TVS diodes on the circuit.

Features

- 4-Channels of SHORT-TO-VBUS Overvoltage Protections (CC1, CC2, SBU1, SBU2): 24VDC Tolerance
- IEC 61000-4-2 ESD Protection: CC1, CC2, SBU1, SBU2, DP, DM pins
  - Contact discharge 9KV: CC1/CC2
  - Contact discharge 8KV: SBU1/SBU2
- IEC 61000-4-5 ±35V Surge Protection: CC1, CC2, SBU1, SBU2 pins
- Fast OVP Turnoff Time: 60ns
- CC1/2 600mA Switches for VCONN
- 3mm×3mm QFN-20L Package

Applications

- Notebooks/Laptop PC
- Tablets
- Monitors & TVs
- Docking Stations & Dongles
- Video Conference Systems
- Gaming Headsets
- Surveillance Cam

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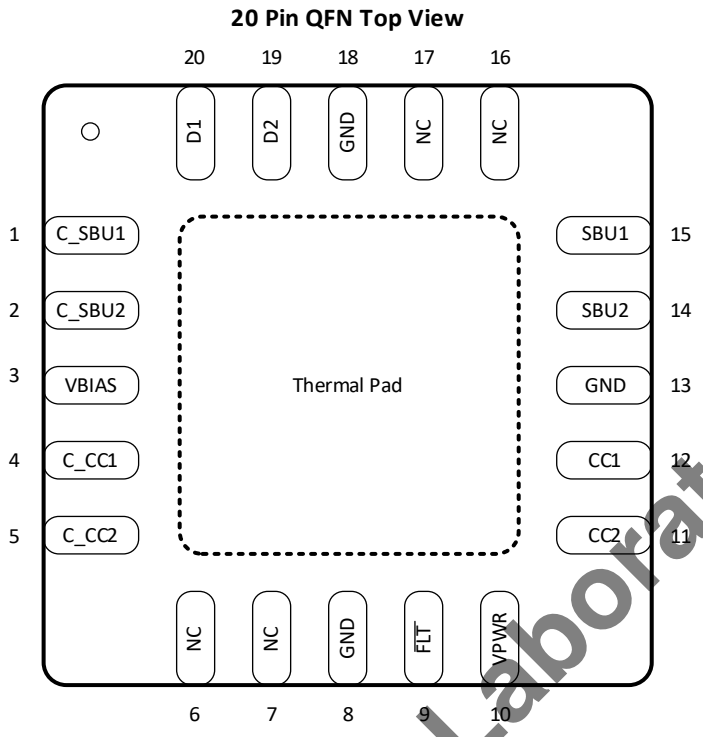
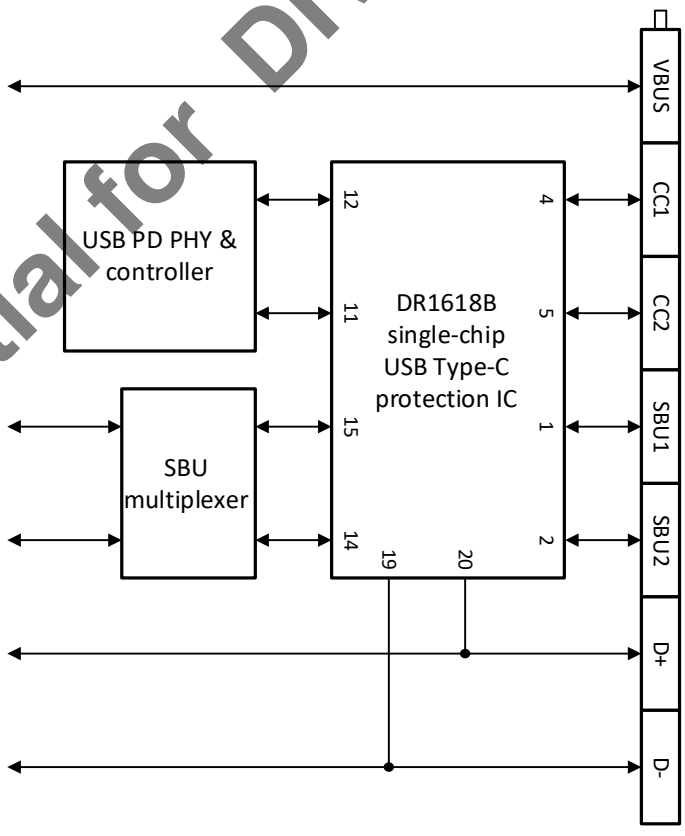
1. Pin Configuration



2. Simplified Application Circuit



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3. Pin Description

Pin No.	Pin Name	Type	Description
1	C_SBU1	I/O	Connector side of SBU1 OVP switch
2	C_SBU2	I/O	Connector side of SBU2 OVP switch
3	VBIAS	P	Place a 0.1uF capacitor on this pin to ground for ESD protection
4	C_CC1	I/O	Connector side of C_CC1 OVP switch
5	C_CC2	I/O	Connector side of C_CC2 OVP switch
6	NC	-	Unused pin. Connect to Ground or be floating
7	NC	-	Unused pin. Connect to Ground or be floating
8	GND	P	Ground pin. Connect to the system ground
9	/FLT	O	Fault flag. It goes low when protection is triggered
10	VPWR	P	Power supply input pin
11	CC2	I/O	Device side of CC2 OVP switch
12	CC1	I/O	Device side of CC1 OVP switch
13	GND	P	Ground pin. Connect to the system ground
14	SBU2	I/O	Device side of SBU2 OVP switch
15	SBU1	I/O	Device side of SBU1 OVP switch
16	NC	-	Unused pin. Connect to Ground or be floating
17	NC	-	Unused pin. Connect to Ground or be floating
18	GND	P	Ground pin. Connect to the system ground
19	D2	I/O	ESD protection device inside, connect to DM pin
20	D1	I/O	ESD protection device inside, connect to DP pin
-	E-PAD	P	Thermal pad and connected with chip ground. Must be connected to system ground plane on PCB.

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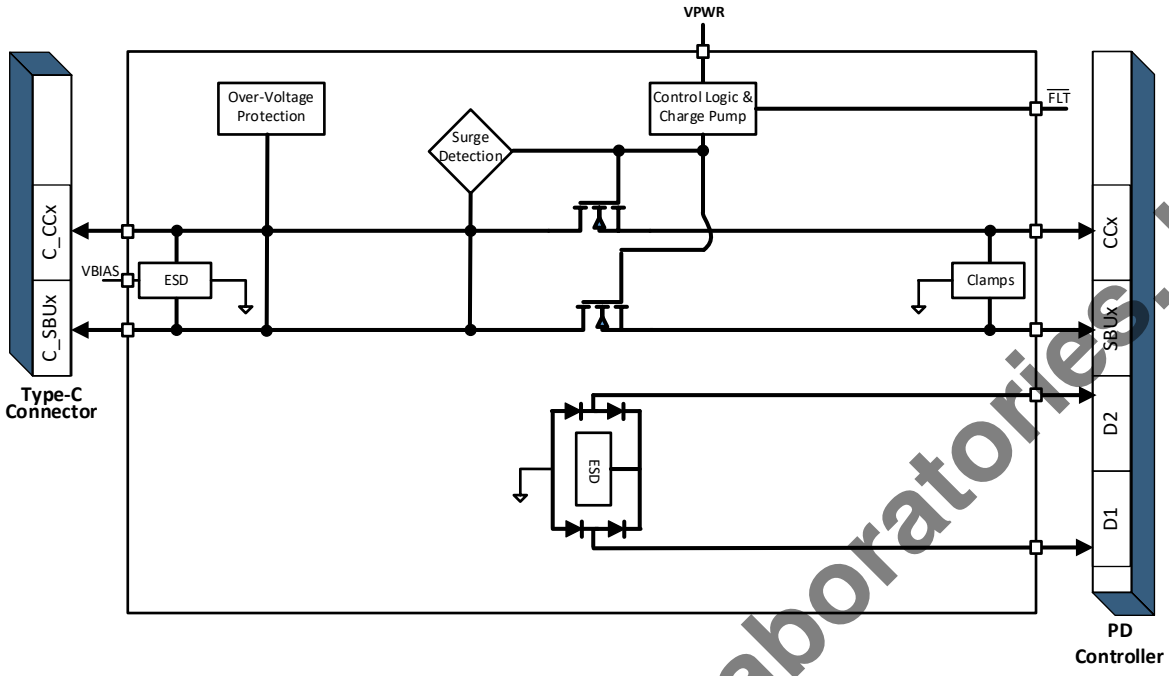
4. Block Diagram



5. Functional Description

(1) HV switches for CC/SBU Channels

DR1618B has four FET switches for both CCx and SBUx with OVP protection function. With smaller connector size and reduced pin pitch, USB Type-C® devices. When the VBUS voltage is increased to higher than 5V through the USB Power Delivery protocol, an improper unplugging of a USB Type-C® port may result in damage on CCx and SBUx related circuitry due to short-circuiting with VBUS. DR1618B is equipped with switch to function the protection accordingly with the voltage hit. The switch embedded is thoroughly design and will not cause any impact on USB PD communication for BMC data transmission. Moreover, Vconn voltage can be provided through the switch from C_CCx to CCx with extremely low voltage drop.

(2) High Voltage Protection

DR1618B provides user-friendly protection solution for your product in preventing unexpected short-circuiting to VBUS with high voltage strike. DR1618B solution integrates an internal circuitry for the C_CCx and C_SBUx pins that tolerates high voltages and ensures a protection of up to 24V-DC. When being struck by an unexpected short-circuiting to VBUS, it will have RLC elements on the interface with a ringing voltage up to 44V. In order to solve this problem effectively, it is crucial to add a capacitor on the VBIAS pin. Meanwhile, once DR1618B detect OVP circuit, it will turn off the switch to disconnect the C_CCx pin and CCx pin or C_SBUx pin to SBUx pin within a rapid period.

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(3) ESD and Surge Protection

As integrated circuit chipsets become more sensitive to the stress from electrostatic discharge (ESD) and other transient voltage surges, the circuit protection device becomes much more important. DR1618B integrates ESD protection device in accordance to IEC61000-4-2 requirement, DR1618B allows C_CCx or C_SBUx pins to pass at least of ±8KV contact discharge. Through this feature, system engineers can save PCB space and reduce external BOM costs when considering system ESD protection. In addition, the surge protection voltage of DR1618B can reach ±35V.

6. Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VPWR	-0.3	5.5	V
C_CC1, C_CC2, C_SBU1, C_SBU2	-0.3	24	V
CC1, CC2, SBU1, SBU2	-0.3	5.5	V
VBIAS	-0.3	24	V
/FLT	-0.3	5.5	V
D1, D2	-0.3	5.5	V
T_A, Ambient temperature when operating	-40	85	˚C
T_{STG}, Ambient temperature when storage	-40	150	˚C
θ_{JA}, thermal resistance, junction to ambient(1)		75.5	˚C/W
θ_{JC}, thermal resistance, junction to package(2)		44.9	˚C/W

Note.1 Dissipation on 2 layers PCB.
Note.2 Dissipation on 2 layers PCB with heat sink.

7. ESD Ratings

Parameter		Value	Unit
Human-Body model (HBM), JEDEC specification	C_CCx, C_SBUx	±8000	V
	Other Pins	±2000	V
Machine model (MM), JEDEC specification		±200	V
Charged-Device model (CDM), JEDEC specification		±500	V
IEC 61000-4-2, C_CC1, C_CC2	Contact discharge	±9000	V
IEC 61000-4-2, C_SBU1, C_SBU2	Contact discharge	±8000	V

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8. Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Unit
VPWR power supply range	2.7	3.3	5.0	V
C_CC1, C_CC2, CC1, CC2 voltage range	0		5.5	V
C_SBU1, C_SBU2, SBU1, SBU2 voltage range	0		4.0	V
VPWR capacitor value	0.47	1		uF
VBIAS capacitor value		0.1		uF
/FLT pull high resistance	2		200	KΩ

9. Electrical Characteristics

(T_A= 25˚C, VPWR= 3.3V, unless otherwise noted.)

Parameter	Test condition	Min.	Typ.	Max.	Unit
CC OVP Switches					
R_{ON_CC}	Resistance between connector and device side of CC OVP switches when it is on state.		390	465	mΩ
C_{ON_CC}	Capacitance between C_CCx to GND or CCx to GND when switch is on. Tested with 0V to 1.2V, f =400kHz.		130(1)		pF
V_{TH_OVP}	Threshold voltage to turn off the CC OVP switches. Increase voltage at C_CCx pin until /FLT goes low.	5.71	6	6.46	V
BW_{ON}	The -3dB frequency between C_CCx to CCx.		57(1)		MHz
V_{HV_CC}	The affordable voltage range at C_CCx when SHORT-TO-VBUS occurred. Tested by hot-plug C_CCx with 1 meter cable and place 30Ω resistor to GND at CCx.			24	V
V_{CLAMP_CC}	The clamp voltage at CCx when SHORT-TO-VBUS occurred. Tested with 30Ω load on CCx, hot-plug C_CCx with 24V-DC source.		5.5		V
SBU OVP Switches					
R_{ON_SBU}	Resistance between connector and device side of CC OVP switches when it is on state.		3	4.875	Ω
C_{ON_SBU}	Capacitance between C_CCx to GND or CCx to GND when switch is on.		9(1)		pF
V_{TH_OVP}	Threshold voltage to turn off the SBU OVP switches. Increase voltage at C_SBUx pin until /FLT goes low.	4.19	4.5	4.94	V

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Parameter	Test condition	Min.	Typ.	Max.	Unit
BW_{ON}	The -3dB frequency between C_SBUx to SBUx.		277(1)		MHz
V_{HV_SBU}	The affordable voltage range at C_SBUx when SHORT-TO-VBUS occurred. Tested by hot-plug C_SBUx with 1 meter cable and place 100nF capacitor in series with 30Ω resistor to GND at SBUx.			24	V
V_{CLAMP_SBU}	The clamp voltage at SBUx when SHORT-TO-VBUS occurred. Tested with 150nF in series with 40Ω resistor to GND at SBUx, hot-plug C_CCx with 24V-DC source.		5.5		V
VPWR					
UVLO	Increase VPWR voltage until OVP switches turned on.	2.1	2.3	2.5	V
Supply Current	Supply VPWR 3.3V(typ.) ~5V(max.), measure the current flow into VPWR.		110	155	uA
Leakage Current and I/O					
$I_{CC_LEAK_NOM}$	Force 3.6V at C_CCx pin, CCx is floated, measure the current flow into C_CCx pin. The current should be same if force 3.6V at CCx pin and C_CCx is left floating. VPWR= 3.3V.			3	uA
$I_{SBU_LEAK_NOM}$	Force 3.6V at C_SBUx pin, SBUx is floated, measure the current flow into C_SBUx pin. The current should be same if force 3.6V at SBUx pin and C_SBUx is left floating. VPWR= 3.3V.			3	uA
$I_{C_CC_LEAK_HV}$	Force 24V at C_CCx pin, CCx is 0V, measure the current flow into C_CCx pin.			1000	uA
$I_{C_SBU_LEAK_HV}$	Force 24V at C_SBUx pin, SBUx is 0V, measure the current flow into C_SBUx pin.			500	uA
$I_{CC_LEAK_HV}$	Force 24V at C_CCx pin, CCx is 0V, measure the current flow out of CCx pin.			3	uA
$I_{SBU_LEAK_HV}$	Force 24V at C_SBUx pin, SBUx is 0V, measure the current flow out of SBUx pin.			3	uA
I_{Dx_LEAK}	Force 3.6V at Dx pin and measure the current flow into Dx pin.			3	uA
V_{OL}	Force 3mA and measure the voltage level at /FLT pin			0.4	V
Timing					

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Parameter	Test condition	Min.	Typ.	Max.	Unit
t_{ON_SWITCH}	The time period between VPWR UVLO and switch FET turned on.		0.5	1.2	mS
t_{OVP_CC}	The time period between OVP event occurred at CCx and switch FET turned off.		60		nS
t_{OVP_SBU}	The time period between OVP event occurred at SBUx and switch FET turned off.		65		nS
$t_{OVP_CC_RECOVERY}$	The time period between OVP event removed at CCx and switch FET turned back to on.		160		uS
$t_{OVP_SBU_RECOVERY}$	The time period between OVP event removed at SBUx and switch FET turned back to on.		100		uS
t_{OVP_FLT}	The time period between OVP event occurred and /FLT pin goes to low state.		60		nS
$t_{OVP_FLT_RELEASE}$	The time period between OVP event removed and /FLT pin goes back to high state.		1		uS
$S.R._{MAX}$	The maximum allowable slew rate when the signal is transmitted on SBUx paths.			72(1)	V/uS

Note.1 Guaranteed by design.

10. Typical Operating Characteristics

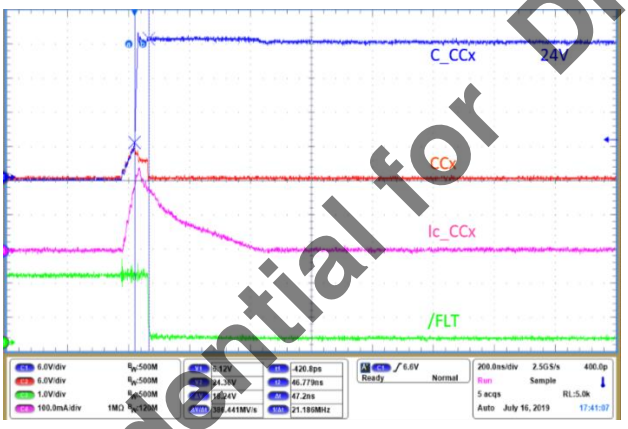

Fig.1 Hot-Plug with 24V at C_CC pin

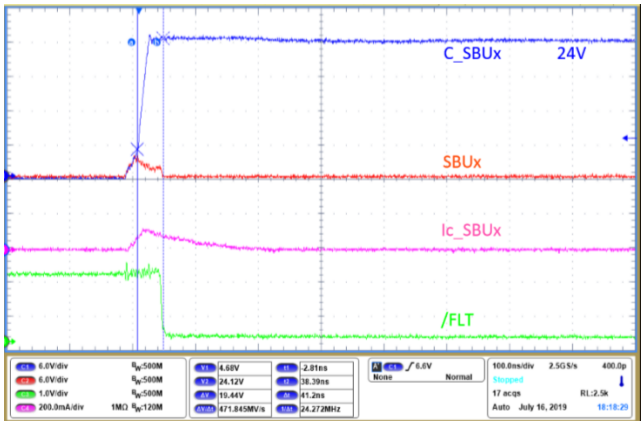

Fig.2 Hot-Plug with 24V at C_SBU pin

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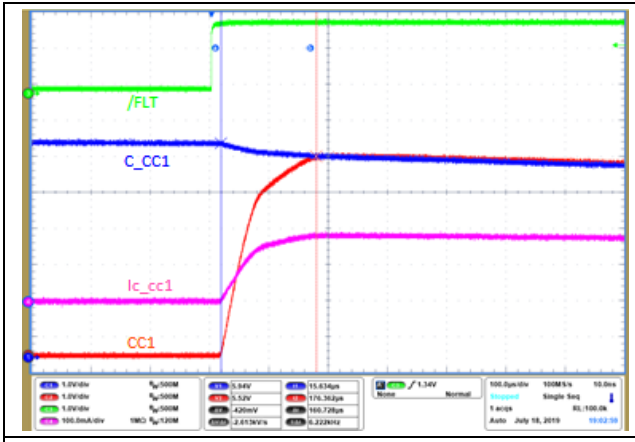

Fig.3 CC OVP recovery waveform(30Ω is added at CCx to GND)

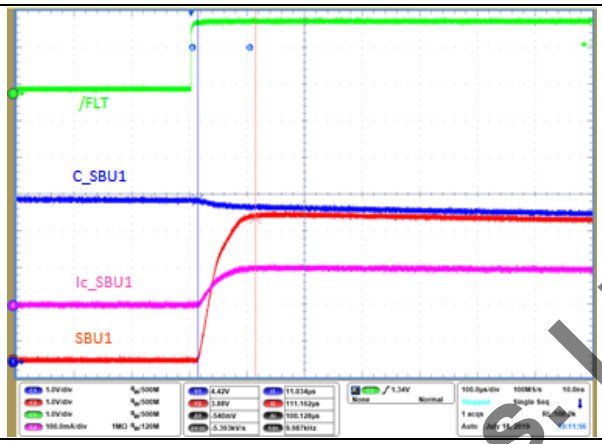

Fig.4 SBU OVP recovery waveform(30Ω is added at SBUx to GND)

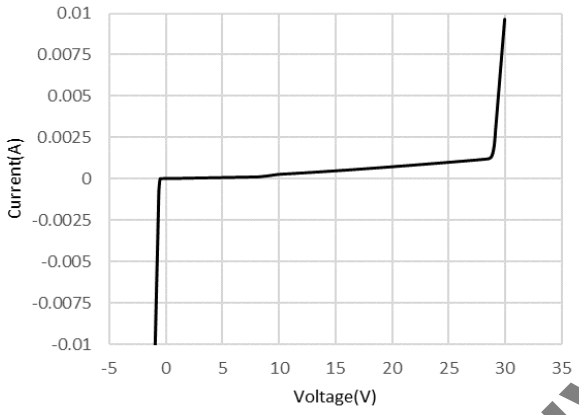

Fig.5 C_CC IV curve

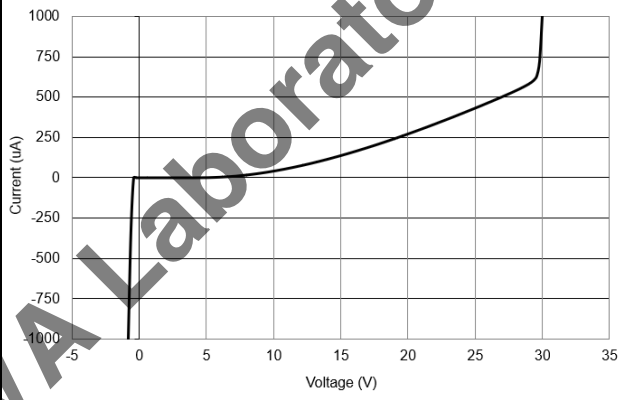

Fig.6 C_SBU IV curve

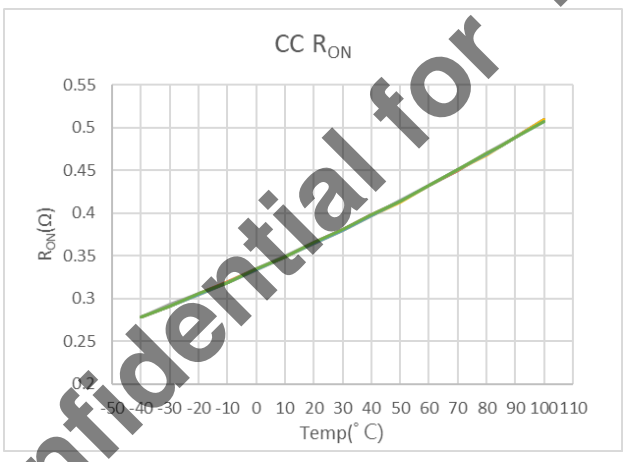

Fig.7 CC path R_{ON} vs Temperature

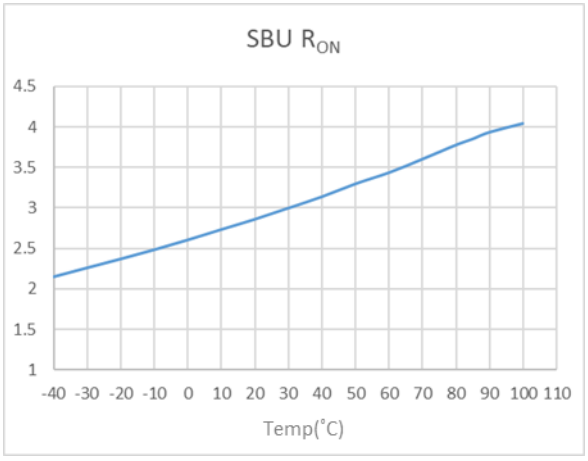

Fig.8 SBU path R_{ON} vs Temperature

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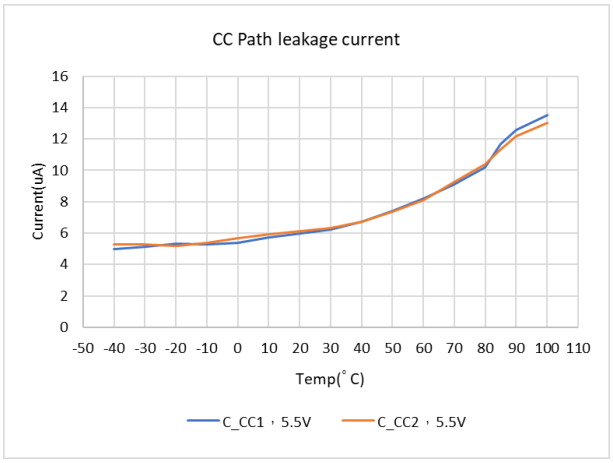

Fig.9 CC path leakage vs Temperature

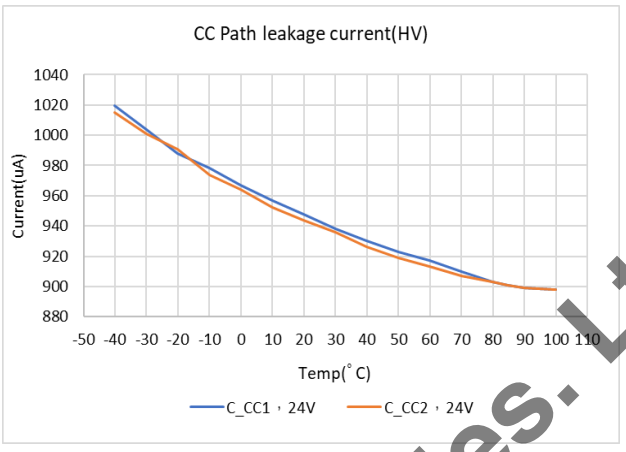

Fig.10 CC path leakage (HV) vs Temperature

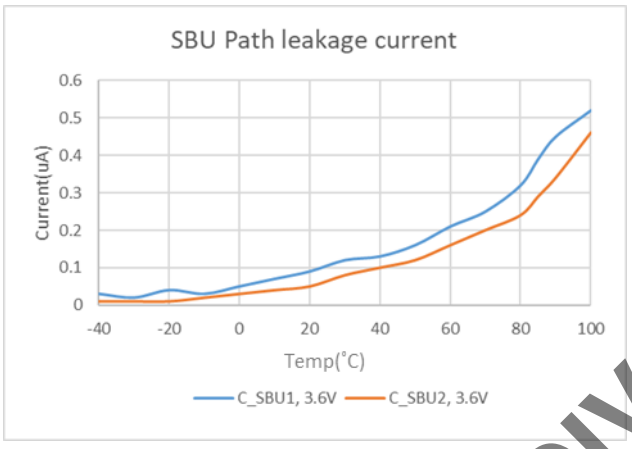

Fig.11 SBU path leakage vs Temperature

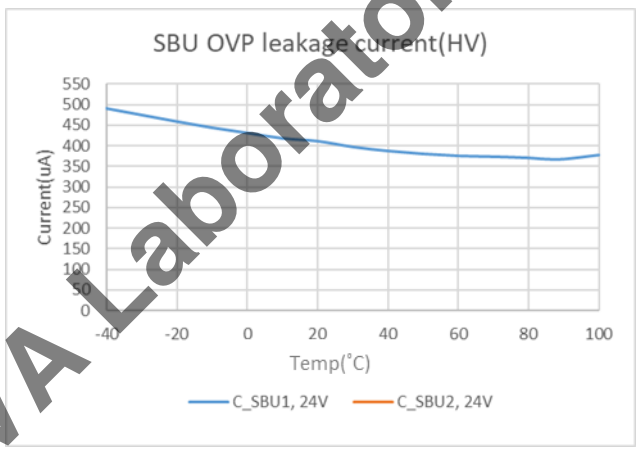

Fig.12 SBU path leakage (HV) vs Temperature

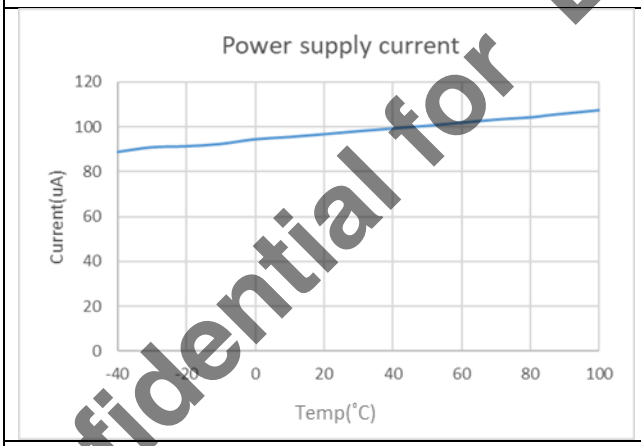

Fig.13 Power supply current (V_{PWR}= 5.5V)

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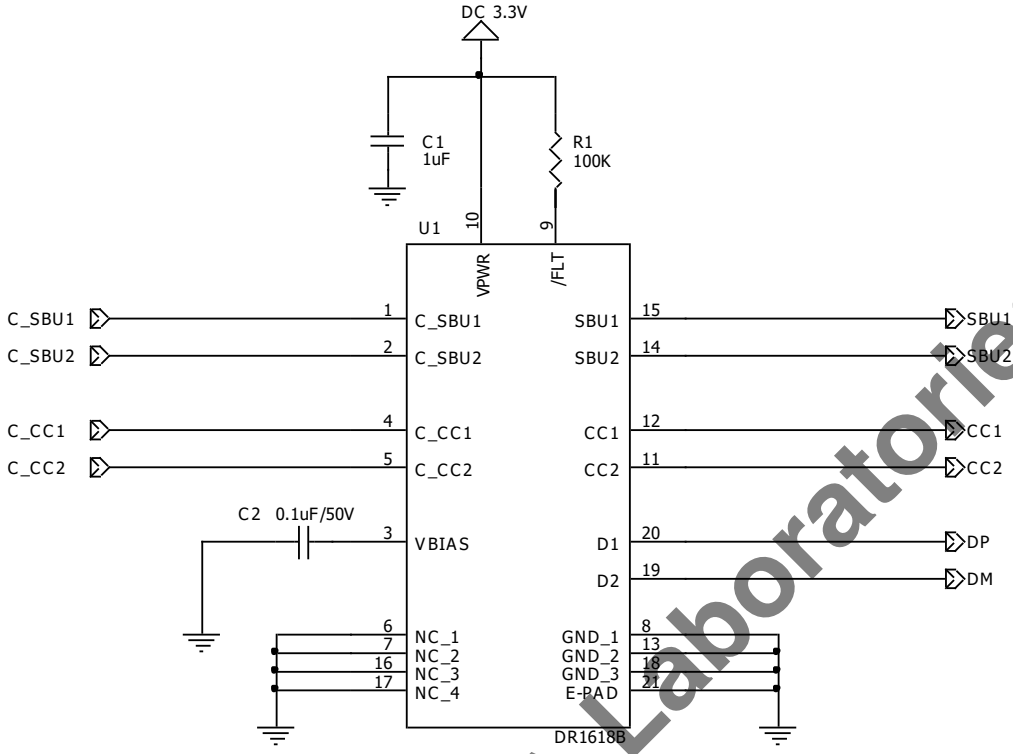
11. Typical Application Circuit



12. Application Information

Power Supply and Operation

When V_{PWR} is below V_{UVLO}, the CC1/CC2/SBU1/SBU2 switches are turned off. Once V_{PWR} goes above V_{ULVO}, DR1618B turns on the CCx/SBUx switches. DR1618B provides the immediately protections when C_CCx or C_SBUx short to high voltages, like VBUS. Also provides ESD protection to guarantee IEC61000-4-2 ESD specification. To achieve the quick protection, the slew rate of transmission signal needs to be constrained to below $S.R._{MAX}$. Basically, DR1618B only needs two external capacitors for normally operation. The switches status can be check in Figure.14.

INPUT			OUTPUT			
Power supply	C_CCx	C_SBUx	CC switch	SBU switch	CC Dead battery R_D	/FLT
V_{PWR}<UVLO	-	-	OFF	OFF	No Built-in	Hi-Z
V_{PWR}>UVLO	<OVP	<OVP	ON	ON		Hi-Z
	>OVP	<OVP	CCx OFF	ON		LOW (Fault Condition)
	<OVP	>OVP	ON	SBUx OFF		LOW (Fault Condition)

Fig.14 Control Logic Table

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Capacitors Selection

There are two capacitors required to make DR1618B operate properly, one for VPWR and one for VBIAS. It is recommended to place a 1uF capacitor closed to the VPWR pin. The voltage rating should be higher than the operation range of 5.0V(Max.). A 0.1uF capacitor is recommended to place as closed as possible to the VBIAS pin. The VBIAS capacitor improves protection performance when a SHORT-TO-VBUS event occurs. The suggested minimum requirement for the VBIAS capacitor is 50V. Since a forward diode is built internally from C_CCx/C_SBUx pins to the VBIAS pin, high voltage can be observed when SHORT-TO-VBUS occurs. The level may reach up to 40V when VBUS is at 20V. The recommended part number is listed in the table below.

Parameter	Size	Voltage Rating	Capacitance	Ref. Part Number
VBIAS Capacitor	0603	50V	0.1uF	GCM188R71H104KA57J

/FLT Operation

DR1618B provides an alerting function through /FLT pin. /FLT is an open drain structure within DR1618B. A pull-up resistor (R1 100K) is placed between the /FLT pin and a DC source voltage (VPWR) to provide and define the /FLT high level. Normally the best way to get DC source is to attach the device VPWR, and the suggested to use 2KΩ to 200KΩ ohm resistor. When the SHORT-TO-VBUS occurs and VBUS level is high enough to trigger over-voltage-protection, /FLT will be pulled to low state. Conversely, it will keep on high state on normal conditions.

Layout Guideline

To achieve good protection performance while maintaining good signal integrity. The PCB trace routing and component placement should be considered.

- Place C1 and C2 close to VPWR pin and VBIAS pin.
- Keep the signal traces as straight as possible and prevent sharp corner.

In addition, USB type-C has the pins other than the protected ones.

For the unprotected pins:

- Keep the traces of unprotected signals away from the protected pins and traces.

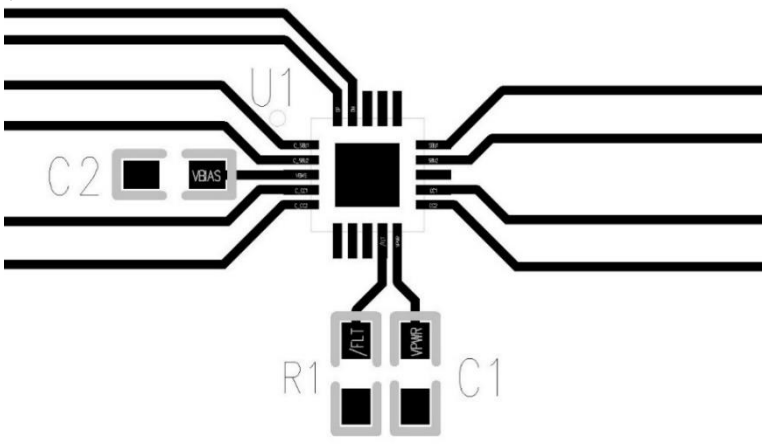

Fig.15 Reference of DR1618B PCB layout

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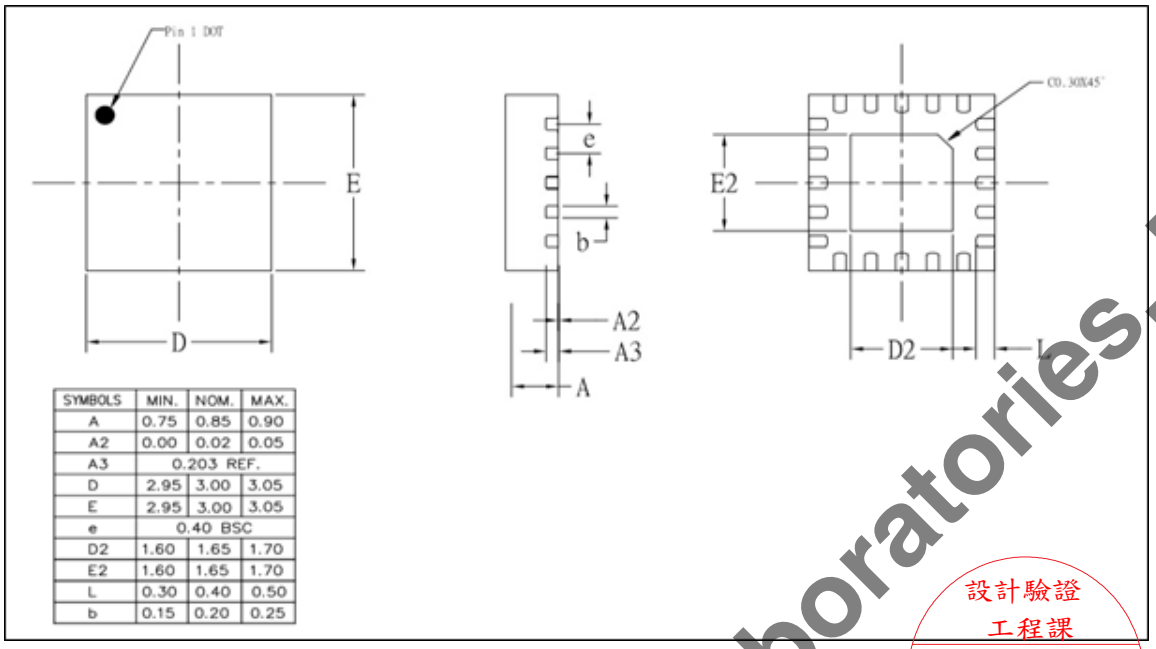
13. Package Outline



SYMBOLS	MIN.	NOM.	MAX.
A	0.75	0.85	0.90
A2	0.00	0.02	0.05
A3		0.203 REF.	
D	2.95	3.00	3.05
E	2.95	3.00	3.05
e		0.40 BSC	
D2	1.60	1.65	1.70
E2	1.60	1.65	1.70
L	0.30	0.40	0.50
b	0.15	0.20	0.25

14. Ordering Information

Part No.	Package	Package Type	MOQ
DR1618BQC	QFN-20L 3mm×3mm	Tape & Reel	5,000

15. Revision History

Version	Date	Revision Content
1.0	2021/6/28	Initial released
1.1	2022/7/18	Application updated

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