CH9904 BOOT ROM

FEATURES

- Wide Voltage Operation
  - Vcc: 1.8V to 5.5V
- Internally Organized:
  - CH9904, 8192 x 8 (64K bits)
- Two-wire Serial Interface
- Schmitt Trigger, Filtered Inputs for Noise Suppression
- Bidirectional Data Transfer Protocol
- 1 MHz (5V), 400 kHz (1.8V, 2.5V, 2.7V) Compatibility
- Write Enable Pin for ROM Write Enable
- 32-bytes Page Write Modes
- Partial Page Writes Allowed
- Self-timed Write Cycle (5 ms max)
- High-reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: 100 Years
- Operating Ambient Temperature: -40°C to +85°C
- 8-lead SOP Packages

GENERAL DESCRIPTIONS

The CH9904 provides 65536 bits of programmable read-only memory organized as 8192 words of 8 bits each. The device is specially configured only for the boot of Chrontel's Display Encoder/transmitter/receiver. The CH9904 is available in space-saving 8-pin SOP package and is accessed via a two-wire serial interface.

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Note: the above feature list is subject to change without notice. Please contact Chrontel for more information and current updates.

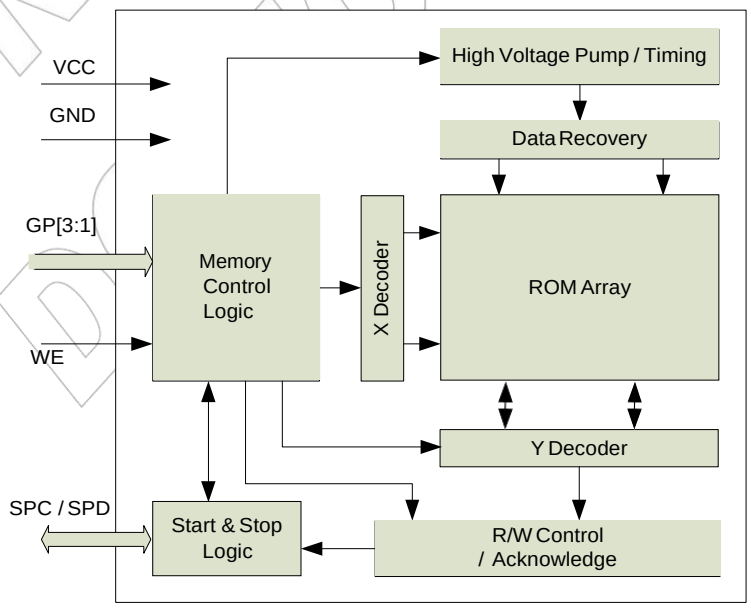

Figure 1: Functional Block Diagram

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1.1 PIN-OUT

1.2 Package Diagram

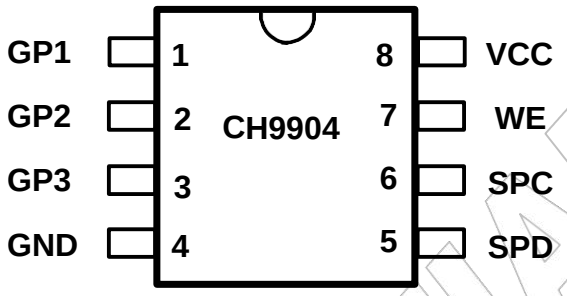

Figure 2: CH9904 Pin Assignment

1.3 Pin Description

Table 1: Pin Descriptions (SOP Package)

Pin #	Type	Symbol	Description
1,2,3	In	GP1-3	**General Configuration Input** The CH9904 uses the GP1-3 for hardware configuration These pins should be pull-up with 6.8K resistors.
5	I/O	SPD	**Serial Port Data Input/Output** This pin functions as the bi-directional data pin of the serial port and operates with inputs from 0 to VCC. Outputs are driven from 0 to VCC. This pin requires an external 4KΩ - 10 KΩ pull up resistor to VCC.
6	In	SPC	**Serial Port Clock Input** This pin functions as the clock output of the serial port and operates with output from 0 to VCC. This pin requires an external 4KΩ - 10KΩ pull up resistor to VCC.
7	In	WE	**Write Enable** The CH9904 has a Write Enable pin that provides hardware data Write enable. This pin enables the write operations when is connected to ground (GND). When this pin is connected to VCC, the write function is disabled.
4	Power	GND	**Power Ground**
8	Power	VCC	**Power Supply**

1.4 Memory Organization

Internally organized with 256 pages of 32 bytes each, the CH9904 requires a 13-bit data word address for random word addressing.

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2.1 FUNCTIONAL DESCRIPTION

CH9904 Boot ROM's operation follows the IIC protocol. The description of the transfer protocol is as follows:

The transfer sequence is initiated when a high-to-low transition of SPD occurs while SPC is high; this is the "START" condition. Transitions of address and data bits can only occur while SPC is low.

The transfer sequence is terminated when a low-to-high transition of SPD occurs while SPC is high; this is the "STOP" condition.

Upon receiving the first START condition, the Chrontel Boot ROM expects a Device Address Byte (DAB) from the master device. As specially configured for Chrontel's display device, the Device Address Byte of CH9904 Boot ROM is 0xAEh for serial port write and 0xAFh for serial port read. The data format of the DAB is shown below.

Device Address Byte (DAB)

B7	B6	B5	B4	B3	B2	B1	B0
1	0	1	0	1	1	1	R/W

After the DAB is received, the Chrontel Boot ROM expects a Data word Address Byte (RAB) from the master. The data format of the RAB is shown below.

Data word Address Bytes (RAB)

High Byte (RABH)

B7	B6	B5	B4	B3	B2	B1	B0
x	x	x	AR[12]	AR[11]	AR[10]	AR[9]	AR[8]

Low Byte (RABL)

B7	B6	B5	B4	B3	B2	B1	B0
AR[7]	AR[6]	AR[5]	AR[4]	AR[3]	AR[2]	AR[1]	AR[0]

'x' is the bit not cared. AR[12:0] is the data word address bytes that specifies the address of the data word to be accessed. The value of AR[12:0] will be loaded into the Data word Address of the CH9904 Boot ROM. The R/W access, which follows, will be directed to the data word specified by Data word Address Bytes.

2.2 Chrontel Boot ROM Write Cycle Protocol (R/W = 0)

An acknowledge is required for all data transfers. The acknowledge-related clock pulse is generated by the master-transmitter. The master-transmitter releases the SPD line (HIGH) during the acknowledge clock pulse. The slave-receiver must pull down the SPD line, during the acknowledge clock pulse, so that it remains LOW during the HIGH period of the clock pulse. Note that the resultant state of SPD is the wired-AND of data outputs from the transmitter and receiver. Figure 3 shows the acknowledge protocol.

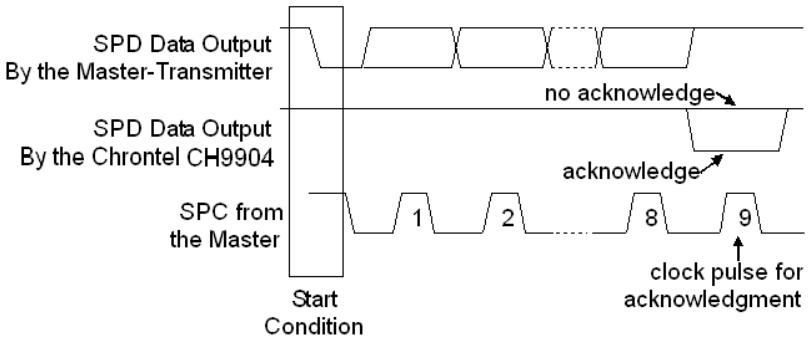

Figure 3: Acknowledge Protocol

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Byte Write Modes

Figure 4 represents two consecutive Byte Write cycles. The byte of information, following the Data word Address Byte (RAB), is the data to be written into the Data word Address specified by AR[12:0]. The serial interface bus will then enter the "Stop Condition" immediately after the acknowledge has been received. The cycle is then repeated for each subsequent write cycle.

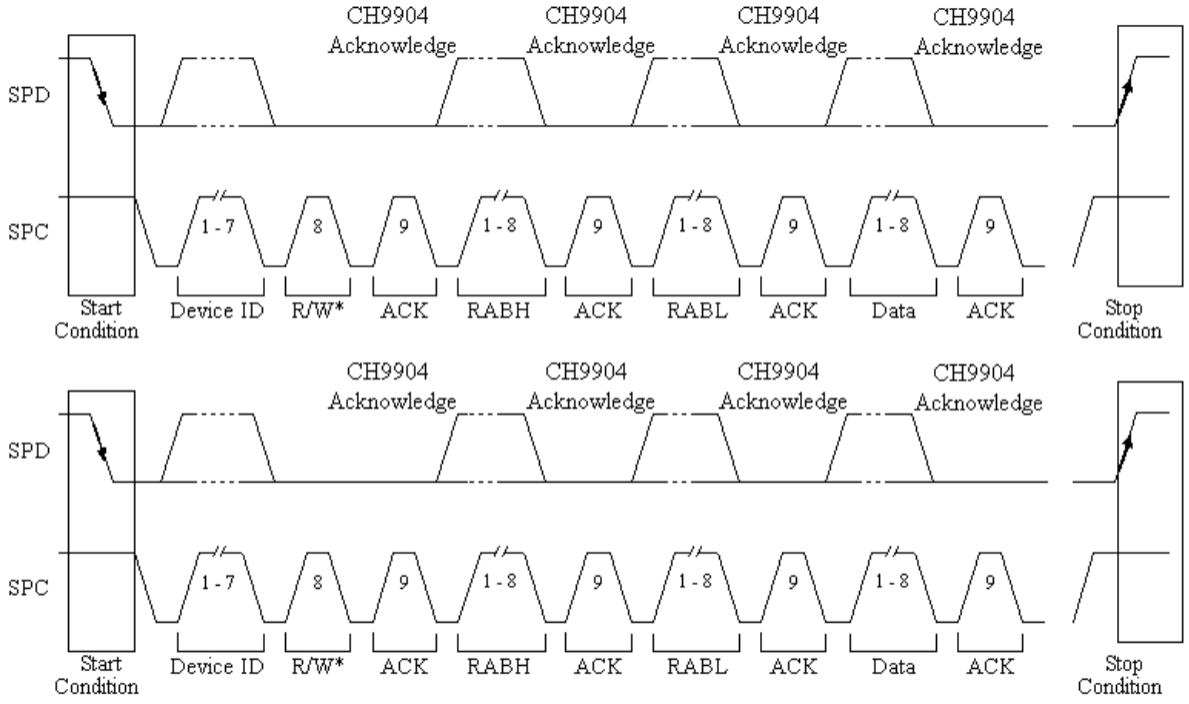

Figure 4: Byte Write Cycles (2 cycles)

Page Write Mode

The Page write cycle is shown in Figure 5. During the Page Write mode transfers, the Data word address pointer continues to increment for each data write cycle until AR[12:0] equal the last accessible Data word Address of the Boot ROM. The next byte of information represents a new auto-sequencing "Starting address", which is the address of the Data word to receive the next byte. The auto-sequencing then resumes based on this new "Starting address". The Auto-increment sequence can be terminated any time by either a "STOP" or "RESTART" condition. The write operation can be terminated with a "STOP" condition.

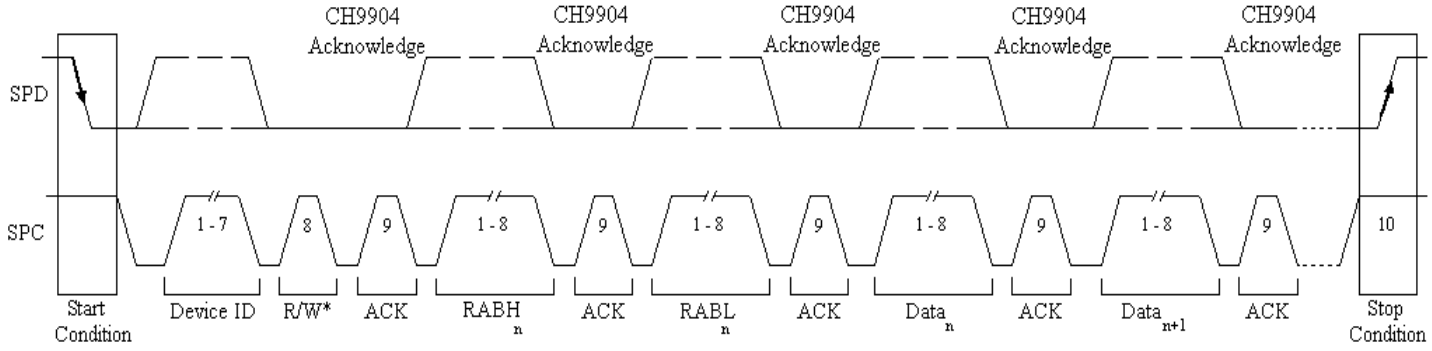

Figure 5: Page Write Cycle

2.3 Chrontel Boot ROM Read Cycle Protocol (R/W = 1)

The master-receiver must signal the end of data to the slave-transmitter by not generating an acknowledge on the last byte that was clocked out of the slave. The slave-transmitter Boot ROM will then release the data line to allow the master to generate either the STOP condition or the RESTART condition.

Current Address Read Mode

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained the Data word Address will wrap around and start from the first byte of the same page again while write is from the last byte of the current page.

Once the device address byte with the read/write select bit set to'1' is locked in and acknowledged by the CH9904 Boot ROM, the current address data word is serially clocked out, The Master does not respond with the acknowledge and generate the stop condition (Refer to Figure 6).

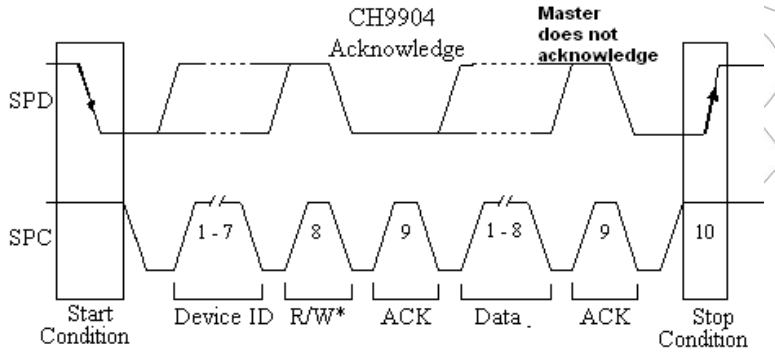

Figure 6: Current Address Read

Random Read Mode

To read the content of the Data words, the master device must first issue a "START" condition (or a "RESTART" condition). After the START condition, the first byte of data will be the DAB with R/W = 0. The second byte is the RAB with AR[12:0] containing the address of the Data word that the master device intends to read from. The master device must then issue a "RESTART" condition ("RESTART" = "START", without a previous "STOP" condition). The first byte of data, after the RESTART condition, is another DAB with R/W=1, indicating the master's intention to read data hereafter. The master then reads the next byte of data (the content of the Data word specified in the RAB). For Single-step mode, a "Stop" condition or "Restart" condition is sent out immediately after the acknowledge which indicates that the data has been read (Refer to Figure 7).

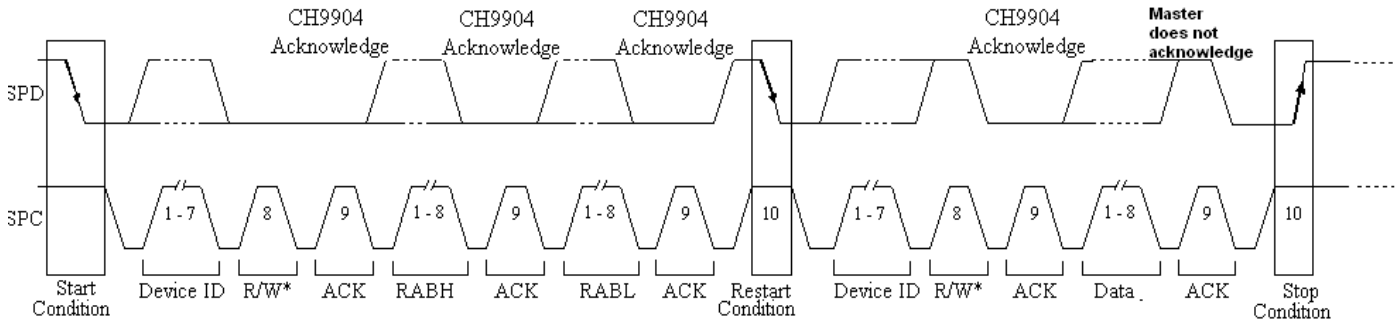

Figure 7: Random Read Cycles

Sequential Read Mode

For sequential read cycles, the Data word address is incremented automatically. This allows subsequent data bytes to be read from successive Data words without having to provide a second RAB.

Regarding the sequential read cycle, the address Data word continues to increment for each read cycle. The sequential reads are initialed by either current address read mode or random read mode. When AR[12:0] of the RAB has been incremented to the last accessible Data word address of the Boot ROM, the Data word Address will wrap around and start from 0x0000h again. The auto increment sequence can be terminated by either a "STOP" or "RESTART" condition. The read operation can be terminated with a "STOP" condition. Figure 8 shows an sequential read cycle terminated by a STOP condition.

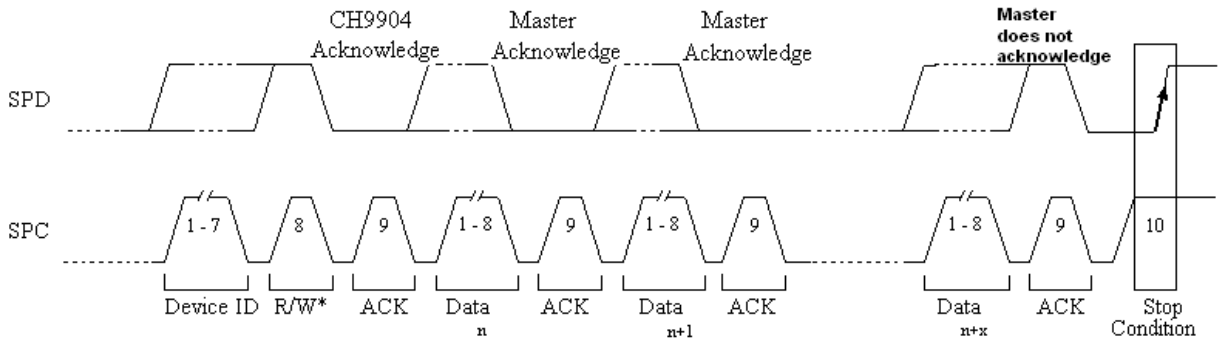

Figure 8: Sequential Read Cycles

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3.1 ELECTRICAL SPECIFICATIONS

3.2 Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units
	DC supply voltage	-0.3		6.5	V
	Input / Output voltage	GND-0.3		Vcc+0.3	V
T_{SC}	Analog output short circuit duration		Indefinite		Sec
T_{AMB}	Ambient operating temperature	-40		85	°C
T_{STOR}	Storage temperature	-65		150	°C
T_J	Junction temperature			150	°C
T_{VPS}	Vapor phase soldering (5 second)			260	°C
	Vapor phase soldering (11 second)			245	°C
	Vapor phase soldering (60 second)			225	°C

Note:
Stresses greater than those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions above those indicated under the normal operating condition of this specification is not recommended. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

3.3 DC Specifications

Applicable over recommended operating range from: T_{AMB} = -40°C to +85°C, Vcc = +1.8V to +5.5V (unless otherwise noted)

Symbol	Description	Min	Typ	Max	Units	Conditions
V_{CC}	Supply Voltage	+1.8		+5.5	V	
I_{CC1}	Supply Current V_{CC} = 5.0V	-	0.4	1.0	mA	Read at 100 kHz
I_{CC2}	Supply Current V_{CC} = 5.0V	-	2.0	3.0	mA	Write at 100 kHz
I_{SB}	Standby Current	-	-	1.0	µA	V_{IN} = V_{CC} or GND
I_{LI}	Input Leakage Current	-	-	3.0	µA	V_{IN} = V_{CC} or GND
I_{LO}	Output Leakage Current		0.05	3.0	mA	V_{OUT} = V_{CC} or GND
V_{IL}	Input Low Level	-0.3	-	V_{CC} x0.3	V	
V_{IH}	Input High Level	V_{CC} x 0.7		V_{CC} +0.3	V	
V_{OL1}	Output Low Level V_{CC} =5.0V			0.4	V	I_{OL} = 3.0 mA
V_{OL2}	Output Low Level V_{CC} =3.0V			0.4	V	I_{OL} = 2.1 mA
V_{OL3}	Output Low Level V_{CC} =1.8V			0.2	V	I_{OL} = 0.15 mA

3.4 AC Specifications

Application over recommended operating range from T_{AMB} = -40°C to +85°C, Vcc = +1.8V to +5.5V CL= 1 TTL Gate and 100pF (unless otherwise noted)

Symbol	Description	1.8V			5.0V			Units
		Min	Typ	Max	Min	Typ	Max	
f_{SCL}	Clock Frequency, SCL			400			1000	kHz
t_{LOW}	Clock Pulse Width Low	1.2			0.6			µs
t_{HIGH}	Clock Pulse Width High	0.6			0.4			µs
t_I	Noise Suppression Time			50			40	ns

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t_{AA}	Clock Low to Data Out Valid	0.05		0.9	0.05		0.55	µs
t_{BUF}	Time the Bus must be free before a new transmission ca start	1.2			0.5			µs
$t_{HD.STA}$	Start Hold Time	0.6			0.25			µs
$t_{SU.STA}$	Start Setup Time	0.6			0.25			µs
$t_{HD.DAT}$	Data In Hold Time	0			0			µs
$t_{SU.DAT}$	Data In Setup Time	100			100			ns
t_R	Inputs Rise Time (1)			0.3		0.3		µs
t_F	Input Fall Time (1)			300		100		ns
$t_{SU.STO}$	Stop Setup Time	0.6			0.25			µs
t_{DH}	Data Out Hold Time	50			50			ns
t_{WR}	Write Cycle Time			5		5		
Endurance	5.0V, 25°C, Byte Mode	1M						Write Cycles

Note

1. This parameter is characterized and is not 100% tested

2. AC measurement conditions:
R_L (connects to Vcc): 1.3 KΩ(2.5V, 5V), 10 KΩ(1.8V)
Input pulse voltage: 0.3Vcc to 0.7Vcc
Input rise and fall time:≤50 ns
Input and output timing reference voltage: 0.5 Vcc
The value of R_L should be connected according to the actual loading on the user's system.

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4.0 PACKAGE DIMENSIONS

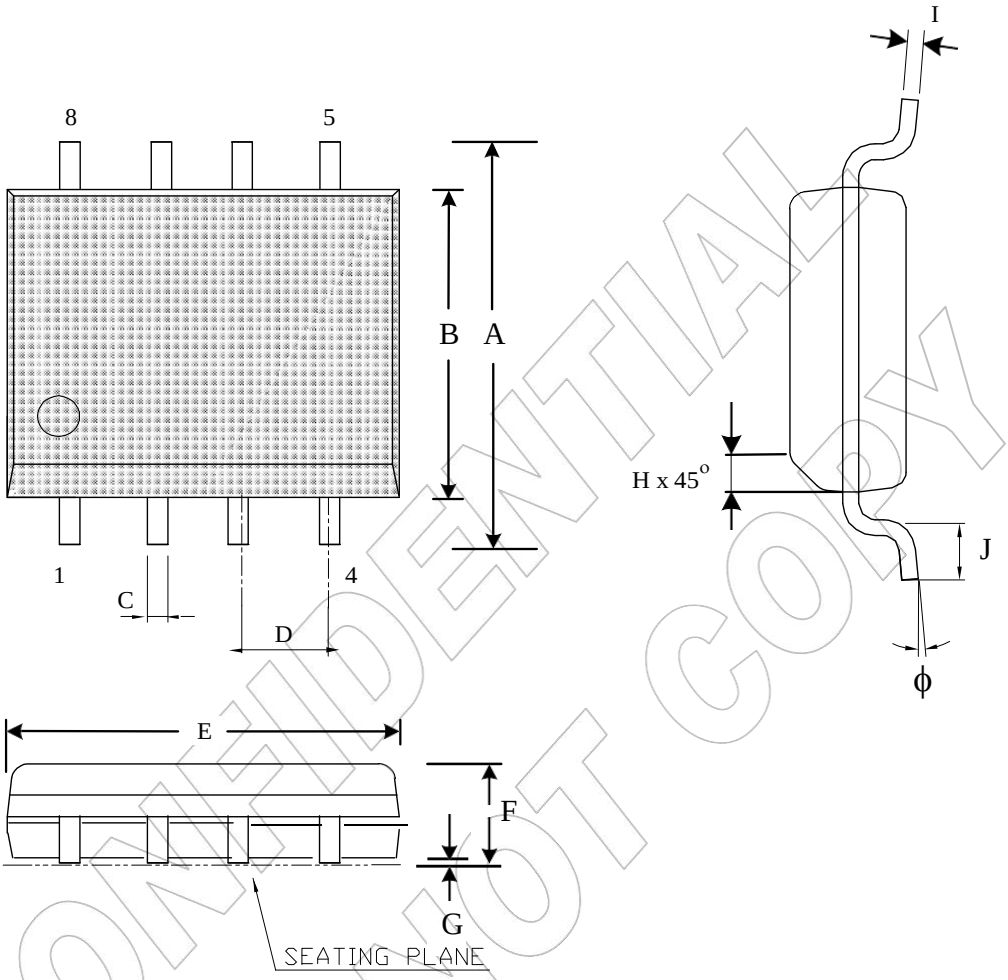

Figure 9: CH9904 SOP-8 Package

Table of Dimensions

No. of Leads		SYMBOL										
8		A	B	C	D	E	F	G	H	I	J	ϕ
Milli-meters	MIN	5.80	3.80	0.35	1.27 BSC	4.80	1.35	0.10	0.25	0.17	0.40	0°
	MAX	6.20	4.00	0.40		5.00	1.75	0.25	0.50	0.25	1.27	8°

Notes:
Conforms to JEDEC standard JESD-30 MO-220.

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5.0 Revision History

Rev. #	Date	Section	Description
1.0.0	07/08/2011	All	First Official Release
1.1.0	09/16/2011	1.2 and 3.2	Modified the Pin description and DC specification

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ORDERING INFORMATION			
Part Number	**Package Type**	**Operating Temperature Range**	**Minimum Order Quantity**
9904AMF	SOP-8, Lead-free	Industrial: -40 to 85°C	

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