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## APPROVAL SHEET

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| BRAND NAME: | **AMD (XILINX)** |
| PART NO.: | **XC7A15T-2CSG324C** |
| DESCRIPTION: | **#IC FPGA XC7A15T-2CSG324C**<br>**IC (XC7A15T-2CSG324C,FPGA,XILINX)** |
| COMPANY PART NO.: | **TY.7AD10.004**<br>**3AXC7A15T1Y** (A0543) |
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# Artix-7 FPGAs Data Sheet: DC and AC Switching Characteristics

DS181 (v1.27) February 10, 2022 **Product Specification**

## Introduction

Artix®-7 FPGAs are available in -3, -2, -1, -1LI, and -2L speed grades, with -3 having the highest performance. The Artix-7 FPGAs predominantly operate at a 1.0V core voltage. The -1LI and -2L devices are screened for lower maximum static power and can operate at lower core voltages for lower dynamic power than the -1 and -2 devices, respectively. The -1LI devices operate only at $V_{CCINT}$ = $V_{CCBRAM}$ = 0.95V and have the same speed specifications as the -1 speed grade. The -2L devices can operate at either of two $V_{CCINT}$ voltages, 0.9V and 1.0V and are screened for lower maximum static power. When operated at $V_{CCINT}$ = 1.0V, the speed specification of a -2L device is the same as the -2 speed grade. When operated at $V_{CCINT}$ = 0.9V, the -2L static and dynamic power is reduced.

Artix-7 FPGA DC and AC characteristics are specified in commercial, extended, industrial, expanded (-1Q), and military (-1M) temperature ranges. Except the operating temperature range or unless otherwise noted, all the DC and AC electrical parameters are the same for a particular speed grade (that is, the timing characteristics of a -1M speed grade military device are the same as for a -1C speed grade commercial device). However, only selected speed grades and/or devices are available in each temperature range. For example, -1M is only available in the defense-grade Artix-7Q family and -1Q is only available in XA Artix-7 FPGAs.

All supply voltage and junction temperature specifications are representative of worst-case conditions. The parameters included are common to popular designs and typical applications.

Available device and package combinations can be found in:

- *7 Series FPGAs Overview* (DS180)
- *Defense-Grade 7 Series FPGAs Overview* (DS185)
- *XA Artix-7 FPGAs Overview* (DS197)

This Artix-7 FPGA data sheet, part of an overall set of documentation on the 7 series FPGAs, is available on the Xilinx website at www.xilinx.com/documentation.

## DC Characteristics

*Table 1:* **Absolute Maximum Ratings(1)**

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| **FPGA Logic** | | | | |
| $V_{CCINT}$ | Internal supply voltage | –0.5 | 1.1 | V |
| $V_{CCAUX}$ | Auxiliary supply voltage | –0.5 | 2.0 | V |
| $V_{CCBRAM}$ | Supply voltage for the block RAM memories | –0.5 | 1.1 | V |
| $V_{CCO}$ | Output drivers supply voltage for HR I/O banks | –0.5 | 3.6 | V |
| $V_{REF}$ | Input reference voltage | –0.5 | 2.0 | V |
| $V_{IN}$(2)(3)(4) | I/O input voltage | –0.4 | $V_{CCO}$ + 0.55 | V |
| | I/O input voltage (when $V_{CCO}$ = 3.3V) for $V_{REF}$ and differential I/O standards except TMDS_33(5) | –0.4 | 2.625 | V |
| $V_{CCBATT}$ | Key memory battery backup supply | –0.5 | 2.0 | V |
| **GTP Transceiver** | | | | |
| $V_{MGTAVCC}$ | Analog supply voltage for the GTP transmitter and receiver circuits | –0.5 | 1.1 | V |
| $V_{MGTAVTT}$ | Analog supply voltage for the GTP transmitter and receiver termination circuits | –0.5 | 1.32 | V |
| $V_{MGTREFCLK}$ | Reference clock absolute input voltage | –0.5 | 1.32 | V |

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*Table 1:* **Absolute Maximum Ratings(1) *(Cont'd)***

| Symbol | Description | Min | Max | Units |
|---|---|---|---|---|
| $V_{IN}$ | Receiver (RXP/RXN) and Transmitter (TXP/TXN) absolute input voltage | –0.5 | 1.26 | V |
| $I_{DCIN-FLOAT}$ | DC input current for receiver input pins DC coupled RX termination = floating | – | 14 | mA |
| $I_{DCIN-MGTAVTT}$ | DC input current for receiver input pins DC coupled RX termination = $V_{MGTAVTT}$ | – | 12 | mA |
| $I_{DCIN-GND}$ | DC input current for receiver input pins DC coupled RX termination = GND | – | 6.5 | mA |
| $I_{DCOUT-FLOAT}$ | DC output current for transmitter pins DC coupled RX termination = floating | – | 14 | mA |
| $I_{DCOUT-MGTAVTT}$ | DC output current for transmitter pins DC coupled RX termination = $V_{MGTAVTT}$ | – | 12 | mA |
| **XADC** | | | | |
| $V_{CCADC}$ | XADC supply relative to GNDADC | –0.5 | 2.0 | V |
| $V_{REFP}$ | XADC reference input relative to GNDADC | –0.5 | 2.0 | V |
| **Temperature** | | | | |
| $T_{STG}$ | Storage temperature (ambient) | –65 | 150 | °C |
| $T_{SOL}$ | Maximum soldering temperature for Pb/Sn component bodies(6) | – | +220 | °C |
| | Maximum soldering temperature for Pb-free component bodies(6) | – | +260 | °C |
| $T_j$ | Maximum junction temperature(6) | – | +125 | °C |

**Notes:**

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.
2. The lower absolute voltage specification always applies.
3. For I/O operation, refer to *7 Series FPGAs SelectIO Resources User Guide* (UG471).
4. The maximum limit applies to DC signals. For maximum undershoot and overshoot AC specifications, see Table 4.
5. See Table 9 for TMDS_33 specifications.
6. For soldering guidelines and thermal considerations, see *7 Series FPGA Packaging and Pinout Specification* (UG475).

*Table 2:* **Recommended Operating Conditions(1)(2)**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| **FPGA Logic** | | | | | |
| $V_{CCINT}$(3) | For -3, -2, -2LE (1.0V), -1, -1Q, -1M devices: internal supply voltage | 0.95 | 1.00 | 1.05 | V |
| | For -1LI (0.95V) devices: internal supply voltage | 0.92 | 0.95 | 0.98 | V |
| | For -2LE (0.9V) devices: internal supply voltage | 0.87 | 0.90 | 0.93 | V |
| $V_{CCAUX}$ | Auxiliary supply voltage | 1.71 | 1.80 | 1.89 | V |
| $V_{CCBRAM}$(3) | For -3, -2, -2LE (1.0V), -2LE (0.9V), -1, -1Q, -1M devices: block RAM supply voltage | 0.95 | 1.00 | 1.05 | V |
| | For -1LI (0.95V) devices: block RAM supply voltage | 0.92 | 0.95 | 0.98 | V |
| $V_{CCO}$(4)(5) | Supply voltage for HR I/O banks | 1.14 | – | 3.465 | V |
| $V_{IN}$(6) | I/O input voltage | –0.20 | – | $V_{CCO}$ + 0.20 | V |
| | I/O input voltage (when $V_{CCO}$ = 3.3V) for $V_{REF}$ and differential I/O standards except TMDS_33(7) | –0.20 | – | 2.625 | V |
| $I_{IN}$(8) | Maximum current through any pin in a powered or unpowered bank when forward biasing the clamp diode. | – | – | 10 | mA |
| $V_{CCBATT}$(9) | Battery voltage | 1.0 | – | 1.89 | V |
| **GTP Transceiver** | | | | | |
| $V_{MGTAVCC}$(10) | Analog supply voltage for the GTP transmitter and receiver circuits | 0.97 | 1.0 | 1.03 | V |
| $V_{MGTAVTT}$(10) | Analog supply voltage for the GTP transmitter and receiver termination circuits | 1.17 | 1.2 | 1.23 | V |
| **XADC** | | | | | |

*Table 2:* **Recommended Operating Conditions(1)(2) *(Cont'd)***

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $V_{CCADC}$ | XADC supply relative to GNDADC | 1.71 | 1.80 | 1.89 | V |
| $V_{REFP}$ | Externally supplied reference voltage | 1.20 | 1.25 | 1.30 | V |
| **Temperature** | | | | | |
| $T_j$ | Junction temperature operating range for commercial (C) temperature devices | 0 | – | 85 | °C |
| | Junction temperature operating range for extended (E) temperature devices | 0 | – | 100 | °C |
| | Junction temperature operating range for industrial (I) temperature devices | –40 | – | 100 | °C |
| | Junction temperature operating range for expanded (Q) temperature devices | –40 | – | 125 | °C |
| | Junction temperature operating range for military (M) temperature devices | –55 | – | 125 | °C |

**Notes:**

1. All voltages are relative to ground.
2. For the design of the power distribution system consult *7 Series FPGAs PCB Design and Pin Planning Guide* (UG483).
3. If $V_{CCINT}$ and $V_{CCBRAM}$ are operating at the same voltage, $V_{CCINT}$ and $V_{CCBRAM}$ should be connected to the same supply.
4. Configuration data is retained even if $V_{CCO}$ drops to 0V.
5. Includes $V_{CCO}$ of 1.2V, 1.35V, 1.5V, 1.8V, 2.5V, and 3.3V at ±5%.
6. The lower absolute voltage specification always applies.
7. See Table 9 for TMDS_33 specifications.
8. A total of 200 mA per bank should not be exceeded.
9. $V_{CCBATT}$ is required only when using bitstream encryption. If battery is not used, connect $V_{CCBATT}$ to either ground or $V_{CCAUX}$.
10. Each voltage listed requires the filter circuit described in *7 Series FPGAs GTP Transceiver User Guide* (UG482).

*Table 3:* **DC Characteristics Over Recommended Operating Conditions**

| Symbol | Description | Min | Typ(1) | Max | Units |
|---|---|---|---|---|---|
| $V_{DRINT}$ | Data retention $V_{CCINT}$ voltage (below which configuration data might be lost) | 0.75 | – | – | V |
| $V_{DRI}$ | Data retention $V_{CCAUX}$ voltage (below which configuration data might be lost) | 1.5 | – | – | V |
| $I_{REF}$ | $V_{REF}$ leakage current per pin | – | – | 15 | µA |
| $I_L$ | Input or output leakage current per pin (sample-tested) | – | – | 15 | µA |
| $C_{IN}$(2) | Die input capacitance at the pad | – | – | 8 | pF |
| $I_{RPU}$ | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 3.3V | 90 | – | 330 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 2.5V | 68 | – | 250 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.8V | 34 | – | 220 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.5V | 23 | – | 150 | µA |
| | Pad pull-up (when selected) @ $V_{IN}$ = 0V, $V_{CCO}$ = 1.2V | 12 | – | 120 | µA |
| $I_{RPD}$ | Pad pull-down (when selected) @ $V_{IN}$ = 3.3V | 68 | – | 330 | µA |
| $I_{CCADC}$ | Analog supply current, analog circuits in powered up state | – | – | 25 | mA |
| $I_{BATT}$(3) | Battery supply current | – | – | 150 | nA |
| $R_{IN_TERM}$(4) | Thevenin equivalent resistance of programmable input termination to $V_{CCO}$/2 (UNTUNED_SPLIT_40) | 28 | 40 | 55 | Ω |
| | Thevenin equivalent resistance of programmable input termination to $V_{CCO}$/2 (UNTUNED_SPLIT_50) | 35 | 50 | 65 | Ω |
| | Thevenin equivalent resistance of programmable input termination to $V_{CCO}$/2 (UNTUNED_SPLIT_60) | 44 | 60 | 83 | Ω |

*Table 3:* **DC Characteristics Over Recommended Operating Conditions *(Cont'd)***

| Symbol | Description | Min | Typ[1] | Max | Units |
|---|---|---|---|---|---|
| n | Temperature diode ideality factor | – | 1.010 | – | – |
| r | Temperature diode series resistance | – | 2 | – | Ω |

**Notes:**

1. Typical values are specified at nominal voltage, 25°C.
2. This measurement represents the die capacitance at the pad, not including the package.
3. Maximum value specified for worst case process at 25°C.
4. Termination resistance to a $V_{CCO}/2$ level.

*Table 4:* **$V_{IN}$ Maximum Allowed AC Voltage Overshoot and Undershoot for HR I/O Banks[1][2]**

| AC Voltage Overshoot | % of UI @–55°C to 125°C | AC Voltage Undershoot | % of UI @–55°C to 125°C |
|---|---|---|---|
| $V_{CCO}$ + 0.55 | 100 | –0.40 | 100 |
| | | –0.45 | 61.7 |
| | | –0.50 | 25.8 |
| | | –0.55 | 11.0 |
| $V_{CCO}$ + 0.60 | 46.6 | –0.60 | 4.77 |
| $V_{CCO}$ + 0.65 | 21.2 | –0.65 | 2.10 |
| $V_{CCO}$ + 0.70 | 9.75 | –0.70 | 0.94 |
| $V_{CCO}$ + 0.75 | 4.55 | –0.75 | 0.43 |
| $V_{CCO}$ + 0.80 | 2.15 | –0.80 | 0.20 |
| $V_{CCO}$ + 0.85 | 1.02 | –0.85 | 0.09 |
| $V_{CCO}$ + 0.90 | 0.49 | –0.90 | 0.04 |
| $V_{CCO}$ + 0.95 | 0.24 | –0.95 | 0.02 |

**Notes:**

1. A total of 200 mA per bank should not be exceeded.
2. The peak voltage of the overshoot or undershoot, and the duration above $V_{CCO}$ + 0.20V or below GND – 0.20V, must not exceed the values in this table.

*Table 5:* **Typical Quiescent Supply Current**

| Symbol | Description | Device | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | | 0.95V | 0.9V | |
| | | | -3 | -2 | -2LE | -1 | -1LI | -2LE | |
| $I_{CCINTQ}$ | Quiescent $V_{CCINT}$ supply current | XC7A12T | 48 | 48 | 48 | 48 | 43 | 38 | mA |
| | | XC7A15T | 95 | 95 | 95 | 95 | 58 | 66 | mA |
| | | XC7A25T | 48 | 48 | 48 | 48 | 43 | 38 | mA |
| | | XC7A35T | 95 | 95 | 95 | 95 | 58 | 66 | mA |
| | | XC7A50T | 95 | 95 | 95 | 95 | 58 | 66 | mA |
| | | XC7A75T | 155 | 155 | 155 | 155 | 96 | 108 | mA |
| | | XC7A100T | 155 | 155 | 155 | 155 | 96 | 108 | mA |
| | | XC7A200T | 328 | 328 | 328 | 328 | 203 | 232 | mA |
| | | XA7A12T | N/A | 48 | N/A | 48 | N/A | N/A | mA |
| | | XA7A15T | N/A | 95 | N/A | 95 | N/A | N/A | mA |
| | | XA7A25T | N/A | 48 | N/A | 48 | N/A | N/A | mA |
| | | XA7A35T | N/A | 95 | N/A | 95 | N/A | N/A | mA |
| | | XA7A50T | N/A | 95 | N/A | 95 | N/A | N/A | mA |
| | | XA7A75T | N/A | 155 | N/A | 155 | N/A | N/A | mA |
| | | XA7A100T | N/A | 155 | N/A | 155 | N/A | N/A | mA |
| | | XQ7A50T | N/A | 95 | N/A | 95 | 58 | N/A | mA |
| | | XQ7A100T | N/A | 155 | N/A | 155 | 96 | N/A | mA |
| | | XQ7A200T | N/A | 328 | N/A | 328 | 203 | N/A | mA |
| $I_{CCOQ}$ | Quiescent $V_{CCO}$ supply current | XC7A12T | 1 | 1 | 1 | 1 | 1 | 1 | mA |
| | | XC7A15T | 1 | 1 | 1 | 1 | 1 | 1 | mA |
| | | XC7A25T | 1 | 1 | 1 | 1 | 1 | 1 | mA |
| | | XC7A35T | 1 | 1 | 1 | 1 | 1 | 1 | mA |
| | | XC7A50T | 1 | 1 | 1 | 1 | 1 | 1 | mA |
| | | XC7A75T | 4 | 4 | 4 | 4 | 4 | 4 | mA |
| | | XC7A100T | 4 | 4 | 4 | 4 | 4 | 4 | mA |
| | | XC7A200T | 5 | 5 | 5 | 5 | 5 | 5 | mA |
| | | XA7A12T | N/A | 1 | N/A | 1 | N/A | N/A | mA |
| | | XA7A15T | N/A | 1 | N/A | 1 | N/A | N/A | mA |
| | | XA7A25T | N/A | 1 | N/A | 1 | N/A | N/A | mA |
| | | XA7A35T | N/A | 1 | N/A | 1 | N/A | N/A | mA |
| | | XA7A50T | N/A | 1 | N/A | 1 | N/A | N/A | mA |
| | | XA7A75T | N/A | 4 | N/A | 4 | N/A | N/A | mA |
| | | XA7A100T | N/A | 4 | N/A | 4 | N/A | N/A | mA |
| | | XQ7A50T | N/A | 1 | N/A | 1 | 1 | N/A | mA |
| | | XQ7A100T | N/A | 4 | N/A | 4 | 4 | N/A | mA |
| | | XQ7A200T | N/A | 5 | N/A | 5 | 5 | N/A | mA |

*Table 5:* **Typical Quiescent Supply Current *(Cont'd)***

| Symbol | Description | Device | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | | 0.95V | 0.9V | |
| | | | -3 | -2 | -2LE | -1 | -1LI | -2LE | |
| $I_{CCAUXQ}$ | Quiescent $V_{CCAUX}$ supply current | XC7A12T | 13 | 13 | 13 | 13 | 13 | 13 | mA |
| | | XC7A15T | 22 | 22 | 22 | 22 | 19 | 22 | mA |
| | | XC7A25T | 13 | 13 | 13 | 13 | 13 | 13 | mA |
| | | XC7A35T | 22 | 22 | 22 | 22 | 19 | 22 | mA |
| | | XC7A50T | 22 | 22 | 22 | 22 | 19 | 22 | mA |
| | | XC7A75T | 36 | 36 | 36 | 36 | 32 | 36 | mA |
| | | XC7A100T | 36 | 36 | 36 | 36 | 32 | 36 | mA |
| | | XC7A200T | 73 | 73 | 73 | 73 | 65 | 73 | mA |
| | | XA7A12T | N/A | 13 | N/A | 13 | N/A | N/A | mA |
| | | XA7A15T | N/A | 22 | N/A | 22 | N/A | N/A | mA |
| | | XA7A25T | N/A | 13 | N/A | 13 | N/A | N/A | mA |
| | | XA7A35T | N/A | 22 | N/A | 22 | N/A | N/A | mA |
| | | XA7A50T | N/A | 22 | N/A | 22 | N/A | N/A | mA |
| | | XA7A75T | N/A | 36 | N/A | 36 | N/A | N/A | mA |
| | | XA7A100T | N/A | 36 | N/A | 36 | N/A | N/A | mA |
| | | XQ7A50T | N/A | 22 | N/A | 22 | 19 | N/A | mA |
| | | XQ7A100T | N/A | 36 | N/A | 36 | 32 | N/A | mA |
| | | XQ7A200T | N/A | 73 | N/A | 73 | 65 | N/A | mA |

*Table 5:* **Typical Quiescent Supply Current *(Cont'd)***

| Symbol | Description | Device | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | | 0.95V | 0.9V | |
| | | | -3 | -2 | -2LE | -1 | -1LI | -2LE | |
| $I_{CCBRAMQ}$ | Quiescent $V_{CCBRAM}$ supply current | XC7A12T | 1 | 1 | 1 | 1 | 1 | 1 | mA |
| | | XC7A15T | 2 | 2 | 2 | 2 | 1 | 2 | mA |
| | | XC7A25T | 1 | 1 | 1 | 1 | 1 | 1 | mA |
| | | XC7A35T | 2 | 2 | 2 | 2 | 1 | 2 | mA |
| | | XC7A50T | 2 | 2 | 2 | 2 | 1 | 2 | mA |
| | | XC7A75T | 4 | 4 | 4 | 4 | 2 | 4 | mA |
| | | XC7A100T | 4 | 4 | 4 | 4 | 2 | 4 | mA |
| | | XC7A200T | 11 | 11 | 11 | 11 | 6 | 11 | mA |
| | | XA7A12T | N/A | 1 | N/A | 1 | N/A | N/A | mA |
| | | XA7A15T | N/A | 2 | N/A | 2 | N/A | N/A | mA |
| | | XA7A25T | N/A | 1 | N/A | 1 | N/A | N/A | mA |
| | | XA7A35T | N/A | 2 | N/A | 2 | N/A | N/A | mA |
| | | XA7A50T | N/A | 2 | N/A | 2 | N/A | N/A | mA |
| | | XA7A75T | N/A | 4 | N/A | 4 | N/A | N/A | mA |
| | | XA7A100T | N/A | 4 | N/A | 4 | N/A | N/A | mA |
| | | XQ7A50T | N/A | 2 | N/A | 2 | 1 | N/A | mA |
| | | XQ7A100T | N/A | 4 | N/A | 4 | 2 | N/A | mA |
| | | XQ7A200T | N/A | 11 | N/A | 11 | 6 | N/A | mA |

**Notes:**

1. Typical values are specified at nominal voltage, 85°C junction temperature ($T_j$) with single-ended SelectIO resources.
2. Typical values are for blank configured devices with no output current loads, no active input pull-up resistors, all I/O pins are 3-state and floating.
3. Use the Xilinx Power Estimator (XPE) spreadsheet tool (download at http://www.xilinx.com/power) to estimate static power consumption for conditions other than those specified.

## Power-On/Off Power Supply Sequencing

The recommended power-on sequence is $V_{CCINT}$, $V_{CCBRAM}$, $V_{CCAUX}$, and $V_{CCO}$ to achieve minimum current draw and ensure that the I/Os are 3-stated at power-on. The recommended power-off sequence is the reverse of the power-on sequence. If $V_{CCINT}$ and $V_{CCBRAM}$ have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously. If $V_{CCAUX}$ and $V_{CCO}$ have the same recommended voltage levels then both can be powered by the same supply and ramped simultaneously.

For $V_{CCO}$ voltages of 3.3V in HR I/O banks and configuration bank 0:

- The voltage difference between $V_{CCO}$ and $V_{CCAUX}$ must not exceed 2.625V for longer than $T_{VCCO2VCCAUX}$ for each power-on/off cycle to maintain device reliability levels.
- The $T_{VCCO2VCCAUX}$ time can be allocated in any percentage between the power-on and power-off ramps.

The recommended power-on sequence to achieve minimum current draw for the GTP transceivers is $V_{CCINT}$, $V_{MGTAVCC}$, $V_{MGTAVTT}$ OR $V_{MGTAVCC}$, $V_{CCINT}$, $V_{MGTAVTT}$. Both $V_{MGTAVCC}$ and $V_{CCINT}$ can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to achieve minimum current draw.

If these recommended sequences are not met, current drawn from $V_{MGTAVTT}$ can be higher than specifications during power-up and power-down.

- When $V_{MGTAVTT}$ is powered before $V_{MGTAVCC}$ and $V_{MGTAVTT} - V_{MGTAVCC} > 150$ mV and $V_{MGTAVCC} < 0.7$V, the $V_{MGTAVTT}$ current draw can increase by 460 mA per transceiver during $V_{MGTAVCC}$ ramp up. The duration of the current draw can be up to 0.3 x $T_{MGTAVCC}$ (ramp time from GND to 90% of $V_{MGTAVCC}$). The reverse is true for power-down.
- When $V_{MGTAVTT}$ is powered before $V_{CCINT}$ and $V_{MGTAVTT} - V_{CCINT} > 150$ mV and $V_{CCINT} < 0.7$V, the $V_{MGTAVTT}$ current draw can increase by 50 mA per transceiver during $V_{CCINT}$ ramp up. The duration of the current draw can be up to 0.3 x $T_{VCCINT}$ (ramp time from GND to 90% of $V_{CCINT}$). The reverse is true for power-down.

There is no recommended sequence for supplies not shown.

Table 6 shows the minimum current, in addition to $I_{CCQ}$, that is required by Artix-7 devices for proper power-on and configuration. If the current minimums shown in Table 5 and Table 6 are met, the device powers on after all four supplies have passed through their power-on reset threshold voltages. The FPGA must not be configured until after $V_{CCINT}$ is applied.

Once initialized and configured, use the Xilinx Power Estimator (XPE) tools to estimate current drain on these supplies.

*Table 6:* **Power-On Current for Artix-7 Devices**

| Device | $I_{CCINTMIN}$ | $I_{CCAUXMIN}$ | $I_{CCOMIN}$ | $I_{CCBRAMMIN}$ | Units |
|---|---|---|---|---|---|
| XC7A12T | $I_{CCINTQ}$ + 120 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCBRAMQ}$ + 60 | mA |
| XC7A15T | $I_{CCINTQ}$ + 120 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCBRAMQ}$ + 60 | mA |
| XC7A25T | $I_{CCINTQ}$ + 120 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCBRAMQ}$ + 60 | mA |
| XC7A35T | $I_{CCINTQ}$ + 120 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCBRAMQ}$ + 60 | mA |
| XC7A50T | $I_{CCINTQ}$ + 120 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCBRAMQ}$ + 60 | mA |
| XC7A75T | $I_{CCINTQ}$ + 170 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCBRAMQ}$ + 60 | mA |
| XC7A100T | $I_{CCINTQ}$ + 170 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCBRAMQ}$ + 60 | mA |
| XC7A200T | $I_{CCINTQ}$ + 340 | $I_{CCAUXQ}$ + 50 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCBRAMQ}$ + 80 | mA |
| XA7A12T | $I_{CCINTQ}$ + 120 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCBRAMQ}$ + 60 | mA |
| XA7A15T | $I_{CCINTQ}$ + 120 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCBRAMQ}$ + 60 | mA |
| XA7A25T | $I_{CCINTQ}$ + 120 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCBRAMQ}$ + 60 | mA |
| XA7A35T | $I_{CCINTQ}$ + 120 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCBRAMQ}$ + 60 | mA |
| XA7A50T | $I_{CCINTQ}$ + 120 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCBRAMQ}$ + 60 | mA |
| XA7A75T | $I_{CCINTQ}$ + 170 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCBRAMQ}$ + 60 | mA |
| XA7A100T | $I_{CCINTQ}$ + 170 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCBRAMQ}$ + 60 | mA |
| XQ7A50T | $I_{CCINTQ}$ + 120 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCBRAMQ}$ + 60 | mA |

*Table 6:* **Power-On Current for Artix-7 Devices *(Cont'd)***

| Device | $I_{CCINTMIN}$ | $I_{CCAUXMIN}$ | $I_{CCOMIN}$ | $I_{CCBRAMMIN}$ | Units |
|---|---|---|---|---|---|
| XQ7A100T | $I_{CCINTQ}$ + 170 | $I_{CCAUXQ}$ + 40 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCBRAMQ}$ + 60 | mA |
| XQ7A200T | $I_{CCINTQ}$ + 340 | $I_{CCAUXQ}$ + 50 | $I_{CCOQ}$ + 40 mA per bank | $I_{CCBRAMQ}$ + 80 | mA |

*Table 7:* **Power Supply Ramp Time**

| Symbol | Description | Conditions | Min | Max | Units |
|---|---|---|---|---|---|
| $T_{VCCINT}$ | Ramp time from GND to 90% of $V_{CCINT}$ | | 0.2 | 50 | ms |
| $T_{VCCO}$ | Ramp time from GND to 90% of $V_{CCO}$ | | 0.2 | 50 | ms |
| $T_{VCCAUX}$ | Ramp time from GND to 90% of $V_{CCAUX}$ | | 0.2 | 50 | ms |
| $T_{VCCBRAM}$ | Ramp time from GND to 90% of $V_{CCBRAM}$ | | 0.2 | 50 | ms |
| $T_{VCCO2VCCAUX}$ | Allowed time per power cycle for $V_{CCO} - V_{CCAUX} > 2.625V$ | $T_J = 125°C$(1) | – | 300 | ms |
| | | $T_J = 100°C$(1) | – | 500 | |
| | | $T_J = 85°C$(1) | – | 800 | |
| $T_{MGTAVCC}$ | Ramp time from GND to 90% of $V_{MGTAVCC}$ | | 0.2 | 50 | ms |
| $T_{MGTAVTT}$ | Ramp time from GND to 90% of $V_{MGTAVTT}$ | | 0.2 | 50 | ms |

**Notes:**

1. Based on 240,000 power cycles with nominal $V_{CCO}$ of 3.3V or 36,500 power cycles with worst case $V_{CCO}$ of 3.465V.

## DC Input and Output Levels

Values for $V_{IL}$ and $V_{IH}$ are recommended input voltages. Values for $I_{OL}$ and $I_{OH}$ are guaranteed over the recommended operating conditions at the $V_{OL}$ and $V_{OH}$ test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at a minimum $V_{CCO}$ with the respective $V_{OL}$ and $V_{OH}$ voltage levels shown. Other standards are sample tested.

*Table 8:* **SelectIO DC Input and Output Levels**(1)(2)

| I/O Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ | $V_{OH}$ | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|
| | V, Min | V, Max | V, Min | V, Max | V, Max | V, Min | mA, Max | mA, Min |
| HSTL_I | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | 8.00 | –8.00 |
| HSTL_I_18 | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | 8.00 | –8.00 |
| HSTL_II | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | 16.00 | –16.00 |
| HSTL_II_18 | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | 16.00 | –16.00 |
| HSUL_12 | –0.300 | $V_{REF}$ – 0.130 | $V_{REF}$ + 0.130 | $V_{CCO}$ + 0.300 | 20% $V_{CCO}$ | 80% $V_{CCO}$ | 0.10 | –0.10 |
| LVCMOS12 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | Note 3 | Note 3 |
| LVCMOS15 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 25% $V_{CCO}$ | 75% $V_{CCO}$ | Note 4 | Note 4 |
| LVCMOS18 | –0.300 | 35% $V_{CCO}$ | 65% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 0.450 | $V_{CCO}$ – 0.450 | Note 5 | Note 5 |
| LVCMOS25 | –0.300 | 0.7 | 1.700 | $V_{CCO}$ + 0.300 | 0.400 | $V_{CCO}$ – 0.400 | Note 4 | Note 4 |
| LVCMOS33 | –0.300 | 0.8 | 2.000 | 3.450 | 0.400 | $V_{CCO}$ – 0.400 | Note 4 | Note 4 |
| LVTTL | –0.300 | 0.8 | 2.000 | 3.450 | 0.400 | 2.400 | Note 5 | Note 5 |
| MOBILE_DDR | –0.300 | 20% $V_{CCO}$ | 80% $V_{CCO}$ | $V_{CCO}$ + 0.300 | 10% $V_{CCO}$ | 90% $V_{CCO}$ | 0.10 | –0.10 |
| PCI33_3 | –0.400 | 30% $V_{CCO}$ | 50% $V_{CCO}$ | $V_{CCO}$ + 0.500 | 10% $V_{CCO}$ | 90% $V_{CCO}$ | 1.50 | –0.50 |
| SSTL135 | –0.300 | $V_{REF}$ – 0.090 | $V_{REF}$ + 0.090 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.150 | $V_{CCO}$/2 + 0.150 | 13.00 | –13.00 |
| SSTL135_R | –0.300 | $V_{REF}$ – 0.090 | $V_{REF}$ + 0.090 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.150 | $V_{CCO}$/2 + 0.150 | 8.90 | –8.90 |
| SSTL15 | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.175 | $V_{CCO}$/2 + 0.175 | 13.00 | –13.00 |

*Table 8:* **SelectIO DC Input and Output Levels(1)(2) *(Cont'd)***

| I/O Standard | $V_{IL}$ | | $V_{IH}$ | | $V_{OL}$ | $V_{OH}$ | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|
| | V, Min | V, Max | V, Min | V, Max | V, Max | V, Min | mA, Max | mA, Min |
| SSTL15_R | –0.300 | $V_{REF}$ – 0.100 | $V_{REF}$ + 0.100 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.175 | $V_{CCO}$/2 + 0.175 | 8.90 | –8.90 |
| SSTL18_I | –0.300 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.470 | $V_{CCO}$/2 + 0.470 | 8.00 | –8.00 |
| SSTL18_II | –0.300 | $V_{REF}$ – 0.125 | $V_{REF}$ + 0.125 | $V_{CCO}$ + 0.300 | $V_{CCO}$/2 – 0.600 | $V_{CCO}$/2 + 0.600 | 13.40 | –13.40 |

**Notes:**

1. Tested according to relevant specifications.
2. 3.3V and 2.5V standards are only supported in HR I/O banks.
3. Supported drive strengths of 4, 8, or 12 mA in HR I/O banks.
4. Supported drive strengths of 4, 8, 12, or 16 mA in HR I/O banks.
5. Supported drive strengths of 4, 8, 12, 16, or 24 mA in HR I/O banks.
6. For detailed interface specific DC voltage levels, see *7 Series FPGAs SelectIO Resources User Guide* (UG471).

*Table 9:* **Differential SelectIO DC Input and Output Levels**

| I/O Standard | $V_{ICM}$(1) | | | $V_{ID}$(2) | | | $V_{OCM}$(3) | | | $V_{OD}$(4) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | V, Min | V, Typ | V, Max | V, Min | V, Typ | V, Max | V, Min | V, Typ | V, Max | V, Min | V, Typ | V, Max |
| BLVDS_25 | 0.300 | 1.200 | 1.425 | 0.100 | – | – | – | 1.250 | – | Note 5 | | |
| MINI_LVDS_25 | 0.300 | 1.200 | $V_{CCAUX}$ | 0.200 | 0.400 | 0.600 | 1.000 | 1.200 | 1.400 | 0.300 | 0.450 | 0.600 |
| PPDS_25 | 0.200 | 0.900 | $V_{CCAUX}$ | 0.100 | 0.250 | 0.400 | 0.500 | 0.950 | 1.400 | 0.100 | 0.250 | 0.400 |
| RSDS_25 | 0.300 | 0.900 | 1.500 | 0.100 | 0.350 | 0.600 | 1.000 | 1.200 | 1.400 | 0.100 | 0.350 | 0.600 |
| TMDS_33 | 2.700 | 2.965 | 3.230 | 0.150 | 0.675 | 1.200 | $V_{CCO}$–0.405 | $V_{CCO}$–0.300 | $V_{CCO}$–0.190 | 0.400 | 0.600 | 0.800 |

**Notes:**

1. $V_{ICM}$ is the input common mode voltage.
2. $V_{ID}$ is the input differential voltage (Q – $\overline{Q}$).
3. $V_{OCM}$ is the output common mode voltage.
4. $V_{OD}$ is the output differential voltage (Q – $\overline{Q}$).
5. $V_{OD}$ for BLVDS will vary significantly depending on topology and loading.

*Table 10:* **Complementary Differential SelectIO DC Input and Output Levels**

| I/O Standard | $V_{ICM}$(1) | | | $V_{ID}$(2) | | $V_{OL}$(3) | $V_{OH}$(4) | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|---|
| | V, Min | V,Typ | V, Max | V,Min | V, Max | V, Max | V, Min | mA, Max | mA, Min |
| DIFF_HSTL_I | 0.300 | 0.750 | 1.125 | 0.100 | – | 0.400 | $V_{CCO}$–0.400 | 8.00 | –8.00 |
| DIFF_HSTL_I_18 | 0.300 | 0.900 | 1.425 | 0.100 | – | 0.400 | $V_{CCO}$–0.400 | 8.00 | –8.00 |
| DIFF_HSTL_II | 0.300 | 0.750 | 1.125 | 0.100 | – | 0.400 | $V_{CCO}$–0.400 | 16.00 | –16.00 |
| DIFF_HSTL_II_18 | 0.300 | 0.900 | 1.425 | 0.100 | – | 0.400 | $V_{CCO}$–0.400 | 16.00 | –16.00 |
| DIFF_HSUL_12 | 0.300 | 0.600 | 0.850 | 0.100 | – | 20% $V_{CCO}$ | 80% $V_{CCO}$ | 0.100 | –0.100 |
| DIFF_MOBILE_DDR | 0.300 | 0.900 | 1.425 | 0.100 | – | 10% $V_{CCO}$ | 90% $V_{CCO}$ | 0.100 | –0.100 |
| DIFF_SSTL135 | 0.300 | 0.675 | 1.000 | 0.100 | – | ($V_{CCO}$/2) – 0.150 | ($V_{CCO}$/2) + 0.150 | 13.0 | –13.0 |
| DIFF_SSTL135_R | 0.300 | 0.675 | 1.000 | 0.100 | – | ($V_{CCO}$/2) – 0.150 | ($V_{CCO}$/2) + 0.150 | 8.9 | –8.9 |
| DIFF_SSTL15 | 0.300 | 0.750 | 1.125 | 0.100 | – | ($V_{CCO}$/2) – 0.175 | ($V_{CCO}$/2) + 0.175 | 13.0 | –13.0 |
| DIFF_SSTL15_R | 0.300 | 0.750 | 1.125 | 0.100 | – | ($V_{CCO}$/2) – 0.175 | ($V_{CCO}$/2) + 0.175 | 8.9 | –8.9 |
| DIFF_SSTL18_I | 0.300 | 0.900 | 1.425 | 0.100 | – | ($V_{CCO}$/2) – 0.470 | ($V_{CCO}$/2) + 0.470 | 8.00 | –8.00 |

*Table 10:* **Complementary Differential SelectIO DC Input and Output Levels *(Cont'd)***

| I/O Standard | $V_{ICM}$[1] | | | $V_{ID}$[2] | | $V_{OL}$[3] | $V_{OH}$[4] | $I_{OL}$ | $I_{OH}$ |
|---|---|---|---|---|---|---|---|---|---|
| | V, Min | V,Typ | V, Max | V,Min | V, Max | V, Max | V, Min | mA, Max | mA, Min |
| DIFF_SSTL18_II | 0.300 | 0.900 | 1.425 | 0.100 | – | $(V_{CCO}/2) – 0.600$ | $(V_{CCO}/2) + 0.600$ | 13.4 | –13.4 |

**Notes:**

1. $V_{ICM}$ is the input common mode voltage.
2. $V_{ID}$ is the input differential voltage (Q – $\overline{Q}$).
3. $V_{OL}$ is the single-ended low-output voltage.
4. $V_{OH}$ is the single-ended high-output voltage.

## LVDS DC Specifications (LVDS_25)

*Table 11:* **LVDS_25 DC Specifications[1]**

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCO}$ | Supply Voltage | | 2.375 | 2.500 | 2.625 | V |
| $V_{OH}$ | Output High Voltage for Q and $\overline{Q}$ | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | – | – | 1.675 | V |
| $V_{OL}$ | Output Low Voltage for Q and $\overline{Q}$ | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 0.700 | – | – | V |
| $V_{ODIFF}$ | Differential Output Voltage:<br>(Q – $\overline{Q}$), Q = High<br>($\overline{Q}$ – Q), $\overline{Q}$ = High | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 247 | 350 | 600 | mV |
| $V_{OCM}$ | Output Common-Mode Voltage | $R_T$ = 100 Ω across Q and $\overline{Q}$ signals | 1.000 | 1.250 | 1.425 | V |
| $V_{IDIFF}$ | Differential Input Voltage:<br>(Q – $\overline{Q}$), Q = High<br>($\overline{Q}$ – Q), $\overline{Q}$ = High | | 100 | 350 | 600 | mV |
| $V_{ICM}$ | Input Common-Mode Voltage | | 0.300 | 1.200 | 1.500 | V |

**Notes:**

1. Differential inputs for LVDS_25 can be placed in banks with $V_{CCO}$ levels that are different from the required level for outputs. Consult the *7 Series FPGAs SelectIO Resources User Guide* (UG471) for more information.

## AC Switching Characteristics

All values represented in this data sheet are based on the speed specifications from the ISE® Design Suite and Vivado® Design Suite as outlined in Table 12.

*Table 12:* **Artix-7 FPGA Speed Specification Version By Device**

| Version In: | | Typical $V_{CCINT}$ | Device |
|---|---|---|---|
| ISE 14.7 | Vivado 2018.2 | (Table 2) | |
| N/A | 1.22 | 1.0V | XC7A12T, XC7A15T, XC7A25T, XC7A35T, XC7A50T, XC7A75T |
| N/A | 1.22 | 0.95V | XC7A12T, XC7A15T, XC7A25T, XC7A35T, XC7A50T, XC7A75T, XC7A100T, XC7A200T |
| N/A | 1.14 | 0.9V | XC7A12T, XC7A15T, XC7A25T, XC7A35T, XC7A50T, XC7A75T |
| 1.10 | 1.22 | 1.0V | XC7A100T, XC7A200T |
| 1.07 | 1.14 | 0.9V | XC7A100T, XC7A200T |
| N/A | 1.15 | 1.0V | XA7A12T, XA7A15T, XA725T, XA7A35T, XA7A50T, XA7A75T |
| 1.07 | 1.15 | 1.0V | XA7A100T |
| 1.06 | 1.11 | 1.0V | XQ7A100T, XQ7A200T |
| N/A | 1.11 | 1.0V | XQ7A50T |

Switching characteristics are specified on a per-speed-grade basis and can be designated as Advance, Preliminary, or Production. Each designation is defined as follows:

***Advance Product Specification***

These specifications are based on simulations only and are typically available soon after device design specifications are frozen. Although speed grades with this designation are considered relatively stable and conservative, some under-reporting might still occur.

***Preliminary Product Specification***

These specifications are based on complete ES (engineering sample) silicon characterization. Devices and speed grades with this designation are intended to give a better indication of the expected performance of production silicon. The probability of under-reporting delays is greatly reduced as compared to Advance data.

***Production Product Specification***

These specifications are released once enough production silicon of a particular device family member has been characterized to provide full correlation between specifications and devices over numerous production lots. There is no under-reporting of delays, and customers receive formal notification of any subsequent changes. Typically, the slowest speed grades transition to Production before faster speed grades.

### Testing of AC Switching Characteristics

Internal timing parameters are derived from measuring internal test patterns. All AC switching characteristics are representative of worst-case supply voltage and junction temperature conditions.

For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer and back-annotate to the simulation net list. Unless otherwise noted, values apply to all Artix-7 FPGAs.

## Speed Grade Designations

Since individual family members are produced at different times, the migration from one category to another depends completely on the status of the fabrication process for each device. Table 13 correlates the current status of each Artix-7 device on a per speed grade basis.

*Table 13:* **Artix-7 Device Speed Grade Designations**

| Device | Speed Grade Designations | | |
|---|---|---|---|
| | Advance | Preliminary | Production |
| XC7A12T | | | -3, -2, -2LE (1.0V), -1, -1LI (0.95V), and -2LE (0.9V) |
| XC7A15T | | | -3, -2, -2LE (1.0V), -1, -1LI (0.95V), and -2LE (0.9V) |
| XC7A25T | | | -3, -2, -2LE (1.0V), -1, -1LI (0.95V), and -2LE (0.9V) |
| XC7A35T | | | -3, -2, -2LE (1.0V), -1, -1LI (0.95V), and -2LE (0.9V) |
| XC7A50T | | | -3, -2, -2LE (1.0V), -1, -1LI (0.95V), and -2LE (0.9V) |
| XC7A75T | | | -3, -2, -2LE (1.0V), -1, -1LI (0.95V), and -2LE (0.9V) |
| XC7A100T | | | -3, -2, -2LE (1.0V), -1, -1LI (0.95V), and -2LE (0.9V) |
| XC7A200T | | | -3, -2, -2LE (1.0V), -1, -1LI (0.95V), and -2LE (0.9V) |
| XA7A12T | | | -2I, -1I, and -1Q |
| XA7A15T | | | -2I, -1I, and -1Q |
| XA7A25T | | | -2I, -1I, and -1Q |
| XA7A35T | | | -2I, -1I, and -1Q |
| XA7A50T | | | -2I, -1I, and -1Q |
| XA7A75T | | | -2I, -1I, and -1Q |
| XA7A100T | | | -2I, -1I, and -1Q |
| XQ7A50T | | | -2I, -1I, -1LI (0.95V), and -1M |
| XQ7A100T | | | -2I, -1I, -1LI (0.95V), and -1M |
| XQ7A200T | | | -2I, -1I, -1LI (0.95V), and -1M |

## Production Silicon and Software Status

In some cases, a particular family member (and speed grade) is released to production before a speed specification is released with the correct label (Advance, Preliminary, Production). Any labeling discrepancies are corrected in subsequent speed specification releases.

Table 14 lists the production released Artix-7 device, speed grade, and the minimum corresponding supported speed specification version and software revisions. The software and speed specifications listed are the minimum releases required for production. All subsequent releases of software and speed specifications are valid.

*Table 14:* **Artix-7 Device Production Software and Speed Specification Release**

| Device | Speed Grade | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 1.0V | | | | | | 0.95V | 0.9V |
| | -3 | -2 | -2LE | -1 | -1Q | -1M | -1LI | -2LE |
| XC7A12T | Vivado tools 2018.2 v1.22 | Vivado tools 2017.4 v1.20 | | | N/A | N/A | Vivado tools 2017.4 v1.20 | Vivado tools 2018.1 v1.14 |
| XC7A15T | Vivado tools 2014.4 v1.14 | | | | N/A | N/A | Vivado tools 2014.4 v1.14 | Vivado tools 2014.4 v1.10 |
| XC7A25T | Vivado tools 2018.2 v1.22 | Vivado tools 2017.4 v1.20 | | | N/A | N/A | Vivado tools 2017.4 v1.20 | Vivado tools 2018.1 v1.14 |
| XC7A35T | Vivado tools 2013.4 v1.11 | | | | N/A | N/A | Vivado tools 2014.4 v1.14 | Vivado tools 2013.4 v1.08 |

*Table 14:* **Artix-7 Device Production Software and Speed Specification Release *(Cont'd)***

| Device | Speed Grade | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | 1.0V | | | | | | 0.95V | 0.9V |
| | -3 | -2 | -2LE | -1 | -1Q | -1M | -1LI | -2LE |
| XC7A50T | Vivado tools 2013.4 v1.11 | | | | N/A | N/A | Vivado tools 2014.4 v1.14 | Vivado tools 2013.4 v1.08 |
| XC7A75T | Vivado tools 2013.3 v1.10 | | | | N/A | N/A | Vivado tools 2014.4 v1.14 | Vivado tools 2013.3 v1.07 |
| XC7A100T | ISE tools 14.4 or Vivado tools 2012.4 with the 14.4/2012.4 device pack v1.07 | | | | N/A | N/A | Vivado tools 2014.4 v1.14 | ISE tools 14.5 or Vivado tools 2013.1 v1.05 |
| XC7A200T | ISE tools 14.4 or Vivado tools 2012.4 with the 14.4/2012.4 device pack v1.07 | | | | N/A | N/A | Vivado tools 2014.4 v1.14 | |
| XA7A12T | N/A | Vivado tools 2018.1 v1.15 | N/A | Vivado tools 2018.1 v1.15 | | N/A | N/A | N/A |
| XA7A15T | N/A | Vivado tools 2014.4 v1.14 | N/A | Vivado tools 2014.4 v1.14 | | N/A | N/A | N/A |
| XA7A25T | N/A | Vivado tools 2018.1 v1.15 | N/A | Vivado tools 2018.1 v1.15 | | N/A | N/A | N/A |
| XA7A35T | N/A | Vivado tools 2014.1 v1.09 | N/A | Vivado tools 2014.1 v1.09 | | N/A | N/A | N/A |
| XA7A50T | N/A | Vivado tools 2014.1 v1.09 | N/A | Vivado tools 2014.1 v1.09 | | N/A | N/A | N/A |
| XA7A75T | N/A | Vivado tools 2014.1 v1.09 | N/A | Vivado tools 2014.1 v1.09 | | N/A | N/A | N/A |
| XA7A100T | N/A | ISE tools 14.5 or Vivado tools 2013.1 v1.05 | N/A | ISE tools 14.5 or Vivado tools 2013.1 v1.05 | ISE tools 14.6 or Vivado tools 2013.2 v1.06 | N/A | N/A | N/A |
| XQ7A50T | N/A | Vivado tools 2014.2 v1.08 | N/A | Vivado tools 2014.2 v1.08 | N/A | Vivado tools 2014.2 v1.08 | Vivado tools 2015.4 v1.11 | N/A |
| XQ7A100T | N/A | ISE tools 14.5 or Vivado tools 2013.1 v1.04 | N/A | ISE tools 14.5 or Vivado tools 2013.1 v1.04 | N/A | ISE tools 14.6 or Vivado tools 2013.2 v1.05 | Vivado tools 2015.4 v1.11 | N/A |
| XQ7A200T | N/A | ISE tools 14.5 or Vivado tools 2013.1 v1.04 | N/A | ISE tools 14.5 or Vivado tools 2013.1 v1.04 | N/A | ISE tools 14.6 or Vivado tools 2013.2 v1.05 | Vivado tools 2015.4 v1.11 | N/A |

### Selecting the Correct Speed Grade and Voltage in the Vivado Tools

It is important to select the correct device speed grade and voltage in the Vivado tools for the device that you are selecting.

To select the 1.0V speed specifications in the Vivado tools, select the **Artix-7**, **XA Artix-7**, or **Defense Grade Artix-7Q** sub-family, and then select the part name that is the device name followed by the package name followed by the speed grade. For example, select the **xc7a100tfgg676-3** part name for the XC7A100T device in the FGG676 package and -3 (1.0V) speed grade or select the **xc7a100tfgg676-2L** part name for the XC7A100T device in the FGG676 package and -2LE (1.0V) speed grade.

To select the -1LI (0.95V) speed specifications in the Vivado tools, select the **Artix-7** sub-family and then select the part name that is the device name followed by an "i" followed by the package name followed by the speed grade. For example, select the **xc7a100tifgg676-1L** part name for the XC7A100T device in the FGG676 package and -1LI (0.95V) speed grade. The -1LI (0.95V) speed specifications are not supported in the ISE tools.

To select the -2LE (0.9V) speed specifications in the Vivado tools, select the **Artix-7 Low Voltage** sub-family and then select the part name that is the device name followed by an "l" followed by the package name followed by the speed grade. For example, select the **xc7a100tlfgg676-2L** part name for the XC7A100T device in the FGG676 package and -2LE (0.9V) speed grade.

A similar part naming convention applies to the speed specifications selection in the ISE tools for supported devices. See Table 14 for the subset of 7 series FPGAs supported in the ISE tools.

## Performance Characteristics

This section provides the performance characteristics of some common functions and designs implemented in Artix-7 devices. The numbers reported here are worst-case values; they have all been fully characterized. These values are subject to the same guidelines as the AC Switching Characteristics, page 12.

*Table 15:* **Networking Applications Interface Performances**

| Description | Speed Grade | | | | | Units |
|---|---|---|---|---|---|---|
| | 1.0V | | | 0.95V | 0.9V | |
| | -3 | -2/-2LE | -1 | -1LI | -2LE | |
| SDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 8) | 680 | 680 | 600 | 600 | 600 | Mb/s |
| DDR LVDS transmitter (using OSERDES; DATA_WIDTH = 4 to 14) | 1250 | 1250 | 950 | 950 | 950 | Mb/s |
| SDR LVDS receiver (SFI-4.1)(1) | 680 | 680 | 600 | 600 | 600 | Mb/s |
| DDR LVDS receiver (SPI-4.2)(1) | 1250 | 1250 | 950 | 950 | 950 | Mb/s |

**Notes:**

1. LVDS receivers are typically bounded with certain applications where specific dynamic phase-alignment (DPA) algorithms dominate deterministic performance.

*Table 16:* **Maximum Physical Interface (PHY) Rate for Memory Interfaces IP available with the Memory Interface Generator(1)(2)**

| Memory Standard | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|
| | 1.0V | | | | 0.95V | 0.9V | |
| | -3 | -2/-2LE | -1 | -1Q/-1M | -1LI | -2LE | |
| **4:1 Memory Controllers** | | | | | | | |
| DDR3 | 1066(3) | 800 | 800 | 667 | 800 | 800 | Mb/s |
| DDR3L | 800 | 800 | 667 | N/A | 667 | 667 | Mb/s |
| DDR2 | 800 | 800 | 667 | 533 | 667 | 667 | Mb/s |
| **2:1 Memory Controllers** | | | | | | | |
| DDR3 | 800 | 700 | 620 | 620 | 620 | 620 | Mb/s |
| DDR3L | 800 | 700 | 620 | N/A | 620 | 620 | Mb/s |
| DDR2 | 800 | 700 | 620 | 533 | 620 | 620 | Mb/s |
| LPDDR2 | 667 | 667 | 533 | 400 | 533 | 533 | Mb/s |

**Notes:**

1. $V_{REF}$ tracking is required. For more information, see *7 Series FPGAs Memory Interface Solutions User Guide* (UG586).
2. When using the internal $V_{REF}$, the maximum data rate is 800 Mb/s (400 MHz).
3. The maximum PHY rate is 800 Mb/s in the CPG238 package.

## IOB Pad Input/Output/3-State

Table 17 summarizes the values of standard-specific data input delay adjustments, output delays terminating at pads (based on standard) and 3-state delays.

- $T_{IOPI}$ is described as the delay from IOB pad through the input buffer to the I-pin of an IOB pad. The delay varies depending on the capability of the SelectIO input buffer.
- $T_{IOOP}$ is described as the delay from the O pin to the IOB pad through the output buffer of an IOB pad. The delay varies depending on the capability of the SelectIO output buffer.
- $T_{IOTP}$ is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is disabled. The delay varies depending on the SelectIO capability of the output buffer. In HR I/O banks, the IN_TERM termination turn-on time is always faster than $T_{IOTP}$ when the INTERMDISABLE pin is used.

*Table 17:* **IOB High Range (HR) Switching Characteristics**

| I/O Standard | $T_{IOPI}$ | | | | | | $T_{IOOP}$ | | | | | | $T_{IOTP}$ | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | | | | Speed Grade | | | | | | Speed Grade | | | | | | |
| | 1.0V | | | | 0.95V | 0.9V | 1.0V | | | | 0.95V | 0.9V | 1.0V | | | | 0.95V | 0.9V | |
| | -3 | -2/ -2LE | -1 | -1Q/ -1M | -1LI | -2LE | -3 | -2/ -2LE | -1 | -1Q/ -1M | -1LI | -2LE | -3 | -2/ -2LE | -1 | -1Q/ -1M | -1LI | -2LE | |
| LVTTL_S4 | 1.26 | 1.34 | 1.41 | 1.53 | 1.41 | 1.58 | 3.80 | 3.93 | 4.18 | 4.18 | 4.18 | 4.41 | 3.82 | 3.96 | 4.20 | 4.20 | 4.20 | 4.05 | ns |
| LVTTL_S8 | 1.26 | 1.34 | 1.41 | 1.53 | 1.41 | 1.58 | 3.54 | 3.66 | 3.92 | 3.92 | 3.92 | 4.15 | 3.56 | 3.69 | 3.93 | 3.93 | 3.93 | 3.78 | ns |
| LVTTL_S12 | 1.26 | 1.34 | 1.41 | 1.53 | 1.41 | 1.58 | 3.52 | 3.65 | 3.90 | 3.90 | 3.90 | 4.13 | 3.54 | 3.68 | 3.91 | 3.91 | 3.91 | 3.77 | ns |
| LVTTL_S16 | 1.26 | 1.34 | 1.41 | 1.53 | 1.41 | 1.58 | 3.07 | 3.19 | 3.45 | 3.45 | 3.45 | 3.68 | 3.09 | 3.22 | 3.46 | 3.46 | 3.46 | 3.31 | ns |
| LVTTL_S24 | 1.26 | 1.34 | 1.41 | 1.53 | 1.41 | 1.58 | 3.29 | 3.41 | 3.67 | 3.67 | 3.67 | 3.90 | 3.31 | 3.44 | 3.68 | 3.68 | 3.68 | 3.53 | ns |
| LVTTL_F4 | 1.26 | 1.34 | 1.41 | 1.53 | 1.41 | 1.58 | 3.26 | 3.38 | 3.64 | 3.64 | 3.64 | 3.86 | 3.28 | 3.41 | 3.65 | 3.65 | 3.65 | 3.50 | ns |
| LVTTL_F8 | 1.26 | 1.34 | 1.41 | 1.53 | 1.41 | 1.58 | 2.74 | 2.87 | 3.12 | 3.12 | 3.12 | 3.35 | 2.76 | 2.90 | 3.13 | 3.13 | 3.13 | 2.99 | ns |
| LVTTL_F12 | 1.26 | 1.34 | 1.41 | 1.53 | 1.41 | 1.58 | 2.73 | 2.85 | 3.10 | 3.10 | 3.10 | 3.33 | 2.74 | 2.88 | 3.12 | 3.12 | 3.12 | 2.97 | ns |
| LVTTL_F16 | 1.26 | 1.34 | 1.41 | 1.53 | 1.41 | 1.58 | 2.56 | 2.68 | 2.93 | 2.93 | 2.93 | 3.16 | 2.57 | 2.71 | 2.95 | 2.95 | 2.95 | 2.80 | ns |
| LVTTL_F24 | 1.26 | 1.34 | 1.41 | 1.53 | 1.41 | 1.58 | 2.52 | 2.65 | 2.90 | 3.23 | 2.90 | 3.22 | 2.54 | 2.68 | 2.91 | 3.24 | 2.91 | 2.86 | ns |
| LVDS_25 | 0.73 | 0.81 | 0.88 | 0.89 | 0.88 | 0.90 | 1.29 | 1.41 | 1.67 | 1.67 | 1.67 | 1.86 | 1.31 | 1.44 | 1.68 | 1.68 | 1.68 | 1.50 | ns |
| MINI_LVDS_25 | 0.73 | 0.81 | 0.88 | 0.89 | 0.88 | 0.90 | 1.27 | 1.40 | 1.65 | 1.65 | 1.65 | 1.88 | 1.29 | 1.43 | 1.66 | 1.66 | 1.66 | 1.52 | ns |
| BLVDS_25 | 0.73 | 0.81 | 0.88 | 0.88 | 0.88 | 0.90 | 1.84 | 1.96 | 2.21 | 2.76 | 2.21 | 2.44 | 1.85 | 1.99 | 2.23 | 2.77 | 2.23 | 2.08 | ns |
| RSDS_25 (point to point) | 0.73 | 0.81 | 0.88 | 0.89 | 0.88 | 0.90 | 1.27 | 1.40 | 1.65 | 1.65 | 1.65 | 1.88 | 1.29 | 1.43 | 1.66 | 1.66 | 1.66 | 1.52 | ns |
| PPDS_25 | 0.73 | 0.81 | 0.88 | 0.89 | 0.88 | 0.90 | 1.29 | 1.41 | 1.67 | 1.67 | 1.67 | 1.88 | 1.31 | 1.44 | 1.68 | 1.68 | 1.68 | 1.52 | ns |
| TMDS_33 | 0.73 | 0.81 | 0.88 | 0.92 | 0.88 | 0.90 | 1.41 | 1.54 | 1.79 | 1.79 | 1.79 | 1.99 | 1.43 | 1.57 | 1.80 | 1.80 | 1.80 | 1.63 | ns |
| PCI33_3 | 1.24 | 1.32 | 1.39 | 1.52 | 1.39 | 1.57 | 3.10 | 3.22 | 3.48 | 3.48 | 3.48 | 3.71 | 3.12 | 3.25 | 3.49 | 3.49 | 3.49 | 3.34 | ns |
| HSUL_12_S | 0.67 | 0.75 | 0.82 | 0.88 | 0.82 | 0.87 | 1.81 | 1.93 | 2.18 | 2.18 | 2.18 | 2.41 | 1.82 | 1.96 | 2.20 | 2.20 | 2.20 | 2.05 | ns |
| HSUL_12_F | 0.67 | 0.75 | 0.82 | 0.88 | 0.82 | 0.87 | 1.29 | 1.41 | 1.67 | 1.67 | 1.67 | 1.90 | 1.31 | 1.44 | 1.68 | 1.68 | 1.68 | 1.53 | ns |
| DIFF_HSUL_ 12_S | 0.68 | 0.76 | 0.83 | 0.86 | 0.83 | 0.88 | 1.81 | 1.93 | 2.18 | 2.18 | 2.18 | 2.21 | 1.82 | 1.96 | 2.20 | 2.20 | 2.20 | 1.84 | ns |
| DIFF_HSUL_ 12_F | 0.68 | 0.76 | 0.83 | 0.86 | 0.83 | 0.88 | 1.29 | 1.41 | 1.67 | 1.67 | 1.67 | 1.79 | 1.31 | 1.44 | 1.68 | 1.68 | 1.68 | 1.42 | ns |
| MOBILE_ DDR_S | 0.76 | 0.84 | 0.91 | 0.91 | 0.91 | 0.96 | 1.68 | 1.80 | 2.06 | 2.06 | 2.06 | 2.24 | 1.70 | 1.83 | 2.07 | 2.07 | 2.07 | 1.88 | ns |
| MOBILE_ DDR_F | 0.76 | 0.84 | 0.91 | 0.91 | 0.91 | 0.96 | 1.38 | 1.51 | 1.76 | 1.76 | 1.76 | 1.97 | 1.40 | 1.54 | 1.77 | 1.77 | 1.77 | 1.61 | ns |
| DIFF_MOBILE_ DDR_S | 0.70 | 0.78 | 0.85 | 0.85 | 0.85 | 0.87 | 1.70 | 1.82 | 2.07 | 2.07 | 2.07 | 2.24 | 1.71 | 1.85 | 2.09 | 2.09 | 2.09 | 1.88 | ns |
| DIFF_MOBILE_ DDR_F | 0.70 | 0.78 | 0.85 | 0.85 | 0.85 | 0.87 | 1.45 | 1.57 | 1.82 | 1.82 | 1.82 | 2.00 | 1.46 | 1.60 | 1.84 | 1.84 | 1.84 | 1.64 | ns |

*Table 17:* **IOB High Range (HR) Switching Characteristics *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | | | | $T_{IOOP}$ | | | | | | $T_{IOTP}$ | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | | | | Speed Grade | | | | | | Speed Grade | | | | | | |
| | 1.0V | | | | 0.95V | 0.9V | 1.0V | | | | 0.95V | 0.9V | 1.0V | | | | 0.95V | 0.9V | |
| | -3 | -2/ -2LE | -1 | -1Q/ -1M | -1LI | -2LE | -3 | -2/ -2LE | -1 | -1Q/ -1M | -1LI | -2LE | -3 | -2/ -2LE | -1 | -1Q/ -1M | -1LI | -2LE | |
| HSTL_I_S | 0.67 | 0.75 | 0.82 | 0.86 | 0.82 | 0.87 | 1.62 | 1.74 | 1.99 | 1.99 | 1.99 | 2.19 | 1.63 | 1.77 | 2.01 | 2.01 | 2.01 | 1.83 | ns |
| HSTL_II_S | 0.65 | 0.73 | 0.80 | 0.86 | 0.80 | 0.85 | 1.41 | 1.54 | 1.79 | 1.79 | 1.79 | 1.99 | 1.43 | 1.57 | 1.80 | 1.81 | 1.80 | 1.63 | ns |
| HSTL_I_18_S | 0.67 | 0.75 | 0.82 | 0.88 | 0.82 | 0.87 | 1.29 | 1.41 | 1.67 | 1.67 | 1.67 | 1.86 | 1.31 | 1.44 | 1.68 | 1.68 | 1.68 | 1.50 | ns |
| HSTL_II_18_S | 0.66 | 0.75 | 0.81 | 0.88 | 0.81 | 0.87 | 1.41 | 1.54 | 1.79 | 1.79 | 1.79 | 1.97 | 1.43 | 1.57 | 1.80 | 1.80 | 1.80 | 1.61 | ns |
| DIFF_HSTL_I_S | 0.68 | 0.76 | 0.83 | 0.86 | 0.83 | 0.85 | 1.59 | 1.71 | 1.96 | 1.96 | 1.96 | 2.13 | 1.60 | 1.74 | 1.98 | 1.98 | 1.98 | 1.77 | ns |
| DIFF_HSTL_ II_S | 0.68 | 0.76 | 0.83 | 0.86 | 0.83 | 0.85 | 1.51 | 1.63 | 1.88 | 1.88 | 1.88 | 2.07 | 1.52 | 1.66 | 1.90 | 1.90 | 1.90 | 1.70 | ns |
| DIFF_HSTL_ I_18_S | 0.71 | 0.79 | 0.86 | 0.86 | 0.86 | 0.87 | 1.38 | 1.51 | 1.76 | 1.76 | 1.76 | 1.96 | 1.40 | 1.54 | 1.77 | 1.77 | 1.77 | 1.59 | ns |
| DIFF_HSTL_ II_18_S | 0.70 | 0.78 | 0.85 | 0.88 | 0.85 | 0.87 | 1.46 | 1.58 | 1.84 | 1.84 | 1.84 | 2.00 | 1.48 | 1.61 | 1.85 | 1.85 | 1.85 | 1.64 | ns |
| HSTL_I_F | 0.67 | 0.75 | 0.82 | 0.86 | 0.82 | 0.87 | 1.10 | 1.22 | 1.48 | 1.49 | 1.48 | 1.69 | 1.12 | 1.25 | 1.49 | 1.51 | 1.49 | 1.33 | ns |
| HSTL_II_F | 0.65 | 0.73 | 0.80 | 0.86 | 0.80 | 0.85 | 1.12 | 1.24 | 1.49 | 1.49 | 1.49 | 1.71 | 1.13 | 1.27 | 1.51 | 1.51 | 1.51 | 1.34 | ns |
| HSTL_I_18_F | 0.67 | 0.75 | 0.82 | 0.88 | 0.82 | 0.87 | 1.13 | 1.26 | 1.51 | 1.54 | 1.51 | 1.72 | 1.15 | 1.29 | 1.52 | 1.56 | 1.52 | 1.36 | ns |
| HSTL_II_18_F | 0.66 | 0.75 | 0.81 | 0.88 | 0.81 | 0.87 | 1.12 | 1.24 | 1.49 | 1.51 | 1.49 | 1.71 | 1.13 | 1.27 | 1.51 | 1.52 | 1.51 | 1.34 | ns |
| DIFF_HSTL_I_F | 0.68 | 0.76 | 0.83 | 0.86 | 0.83 | 0.85 | 1.18 | 1.30 | 1.56 | 1.56 | 1.56 | 1.77 | 1.20 | 1.33 | 1.57 | 1.57 | 1.57 | 1.41 | ns |
| DIFF_HSTL_ II_F | 0.68 | 0.76 | 0.83 | 0.86 | 0.83 | 0.85 | 1.21 | 1.33 | 1.59 | 1.59 | 1.59 | 1.77 | 1.23 | 1.36 | 1.60 | 1.60 | 1.60 | 1.41 | ns |
| DIFF_HSTL_ I_18_F | 0.71 | 0.79 | 0.86 | 0.86 | 0.86 | 0.87 | 1.21 | 1.33 | 1.59 | 1.59 | 1.59 | 1.77 | 1.23 | 1.36 | 1.60 | 1.60 | 1.60 | 1.41 | ns |
| DIFF_HSTL_ II_18_F | 0.70 | 0.78 | 0.85 | 0.88 | 0.85 | 0.87 | 1.21 | 1.33 | 1.59 | 1.59 | 1.59 | 1.77 | 1.23 | 1.36 | 1.60 | 1.60 | 1.60 | 1.41 | ns |
| LVCMOS33_S4 | 1.26 | 1.34 | 1.41 | 1.52 | 1.41 | 1.62 | 3.80 | 3.93 | 4.18 | 4.18 | 4.18 | 4.41 | 3.82 | 3.96 | 4.20 | 4.20 | 4.20 | 4.05 | ns |
| LVCMOS33_S8 | 1.26 | 1.34 | 1.41 | 1.52 | 1.41 | 1.62 | 3.52 | 3.65 | 3.90 | 3.90 | 3.90 | 4.13 | 3.54 | 3.68 | 3.91 | 3.91 | 3.91 | 3.77 | ns |
| LVCMOS33_S12 | 1.26 | 1.34 | 1.41 | 1.52 | 1.41 | 1.62 | 3.09 | 3.21 | 3.46 | 3.46 | 3.46 | 3.69 | 3.10 | 3.24 | 3.48 | 3.48 | 3.48 | 3.33 | ns |
| LVCMOS33_S16 | 1.26 | 1.34 | 1.41 | 1.52 | 1.41 | 1.62 | 3.40 | 3.52 | 3.77 | 3.78 | 3.77 | 4.00 | 3.42 | 3.55 | 3.79 | 3.79 | 3.79 | 3.64 | ns |
| LVCMOS33_F4 | 1.26 | 1.34 | 1.41 | 1.52 | 1.41 | 1.62 | 3.26 | 3.38 | 3.64 | 3.64 | 3.64 | 3.86 | 3.28 | 3.41 | 3.65 | 3.65 | 3.65 | 3.50 | ns |
| LVCMOS33_F8 | 1.26 | 1.34 | 1.41 | 1.52 | 1.41 | 1.62 | 2.74 | 2.87 | 3.12 | 3.12 | 3.12 | 3.35 | 2.76 | 2.90 | 3.13 | 3.13 | 3.13 | 2.99 | ns |
| LVCMOS33_F12 | 1.26 | 1.34 | 1.41 | 1.52 | 1.41 | 1.62 | 2.56 | 2.68 | 2.93 | 2.93 | 2.93 | 3.16 | 2.57 | 2.71 | 2.95 | 2.95 | 2.95 | 2.80 | ns |
| LVCMOS33_F16 | 1.26 | 1.34 | 1.41 | 1.52 | 1.41 | 1.62 | 2.56 | 2.68 | 2.93 | 3.06 | 2.93 | 3.16 | 2.57 | 2.71 | 2.95 | 3.07 | 2.95 | 2.80 | ns |
| LVCMOS25_S4 | 1.12 | 1.20 | 1.27 | 1.38 | 1.27 | 1.43 | 3.13 | 3.26 | 3.51 | 3.51 | 3.51 | 3.72 | 3.15 | 3.29 | 3.52 | 3.52 | 3.52 | 3.36 | ns |
| LVCMOS25_S8 | 1.12 | 1.20 | 1.27 | 1.38 | 1.27 | 1.43 | 2.88 | 3.01 | 3.26 | 3.26 | 3.26 | 3.49 | 2.90 | 3.04 | 3.27 | 3.27 | 3.27 | 3.13 | ns |
| LVCMOS25_S12 | 1.12 | 1.20 | 1.27 | 1.38 | 1.27 | 1.43 | 2.48 | 2.60 | 2.85 | 2.85 | 2.85 | 3.08 | 2.49 | 2.63 | 2.87 | 2.87 | 2.87 | 2.72 | ns |
| LVCMOS25_S16 | 1.12 | 1.20 | 1.27 | 1.38 | 1.27 | 1.43 | 2.82 | 2.94 | 3.20 | 3.20 | 3.20 | 3.43 | 2.84 | 2.97 | 3.21 | 3.21 | 3.21 | 3.06 | ns |
| LVCMOS25_F4 | 1.12 | 1.20 | 1.27 | 1.38 | 1.27 | 1.43 | 2.74 | 2.87 | 3.12 | 3.12 | 3.12 | 3.35 | 2.76 | 2.90 | 3.13 | 3.13 | 3.13 | 2.99 | ns |
| LVCMOS25_F8 | 1.12 | 1.20 | 1.27 | 1.38 | 1.27 | 1.43 | 2.18 | 2.30 | 2.56 | 2.56 | 2.56 | 2.79 | 2.20 | 2.33 | 2.57 | 2.57 | 2.57 | 2.42 | ns |
| LVCMOS25_F12 | 1.12 | 1.20 | 1.27 | 1.38 | 1.27 | 1.43 | 2.16 | 2.29 | 2.54 | 2.54 | 2.54 | 2.77 | 2.18 | 2.32 | 2.55 | 2.56 | 2.55 | 2.41 | ns |
| LVCMOS25_F16 | 1.12 | 1.20 | 1.27 | 1.38 | 1.27 | 1.43 | 2.01 | 2.13 | 2.39 | 2.63 | 2.39 | 2.61 | 2.03 | 2.16 | 2.40 | 2.65 | 2.40 | 2.25 | ns |
| LVCMOS18_S4 | 0.74 | 0.83 | 0.89 | 0.97 | 0.89 | 0.94 | 1.62 | 1.74 | 1.99 | 1.99 | 1.99 | 2.19 | 1.63 | 1.77 | 2.01 | 2.01 | 2.01 | 1.83 | ns |
| LVCMOS18_S8 | 0.74 | 0.83 | 0.89 | 0.97 | 0.89 | 0.94 | 2.18 | 2.30 | 2.56 | 2.56 | 2.56 | 2.79 | 2.20 | 2.33 | 2.57 | 2.57 | 2.57 | 2.42 | ns |
| LVCMOS18_S12 | 0.74 | 0.83 | 0.89 | 0.97 | 0.89 | 0.94 | 2.18 | 2.30 | 2.56 | 2.56 | 2.56 | 2.79 | 2.20 | 2.33 | 2.57 | 2.57 | 2.57 | 2.42 | ns |

*Table 17:* **IOB High Range (HR) Switching Characteristics *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | | | | $T_{IOOP}$ | | | | | | $T_{IOTP}$ | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | | | | Speed Grade | | | | | | Speed Grade | | | | | | |
| | 1.0V | | | | 0.95V | 0.9V | 1.0V | | | | 0.95V | 0.9V | 1.0V | | | | 0.95V | 0.9V | |
| | -3 | -2/ -2LE | -1 | -1Q/ -1M | -1LI | -2LE | -3 | -2/ -2LE | -1 | -1Q/ -1M | -1LI | -2LE | -3 | -2/ -2LE | -1 | -1Q/ -1M | -1LI | -2LE | |
| LVCMOS18_S16 | 0.74 | 0.83 | 0.89 | 0.97 | 0.89 | 0.94 | 1.52 | 1.65 | 1.90 | 1.90 | 1.90 | 2.13 | 1.54 | 1.68 | 1.91 | 1.91 | 1.91 | 1.77 | ns |
| LVCMOS18_S24 | 0.74 | 0.83 | 0.89 | 0.97 | 0.89 | 0.94 | 1.60 | 1.72 | 1.98 | 2.40 | 1.98 | 2.21 | 1.62 | 1.75 | 1.99 | 2.41 | 1.99 | 1.84 | ns |
| LVCMOS18_F4 | 0.74 | 0.83 | 0.89 | 0.97 | 0.89 | 0.94 | 1.45 | 1.57 | 1.82 | 1.82 | 1.82 | 2.05 | 1.46 | 1.60 | 1.84 | 1.84 | 1.84 | 1.69 | ns |
| LVCMOS18_F8 | 0.74 | 0.83 | 0.89 | 0.97 | 0.89 | 0.94 | 1.68 | 1.80 | 2.06 | 2.06 | 2.06 | 2.29 | 1.70 | 1.83 | 2.07 | 2.07 | 2.07 | 1.92 | ns |
| LVCMOS18_F12 | 0.74 | 0.83 | 0.89 | 0.97 | 0.89 | 0.94 | 1.68 | 1.80 | 2.06 | 2.06 | 2.06 | 2.29 | 1.70 | 1.83 | 2.07 | 2.07 | 2.07 | 1.92 | ns |
| LVCMOS18_F16 | 0.74 | 0.83 | 0.89 | 0.97 | 0.89 | 0.94 | 1.40 | 1.52 | 1.77 | 1.78 | 1.77 | 2.00 | 1.42 | 1.55 | 1.79 | 1.79 | 1.79 | 1.64 | ns |
| LVCMOS18_F24 | 0.74 | 0.83 | 0.89 | 0.97 | 0.89 | 0.94 | 1.34 | 1.46 | 1.71 | 2.28 | 1.71 | 1.94 | 1.35 | 1.49 | 1.73 | 2.29 | 1.73 | 1.58 | ns |
| LVCMOS15_S4 | 0.77 | 0.86 | 0.93 | 0.96 | 0.93 | 0.98 | 2.05 | 2.18 | 2.43 | 2.43 | 2.43 | 2.50 | 2.07 | 2.21 | 2.45 | 2.45 | 2.45 | 2.14 | ns |
| LVCMOS15_S8 | 0.77 | 0.86 | 0.93 | 0.96 | 0.93 | 0.98 | 2.09 | 2.21 | 2.46 | 2.46 | 2.46 | 2.69 | 2.10 | 2.24 | 2.48 | 2.48 | 2.48 | 2.33 | ns |
| LVCMOS15_S12 | 0.77 | 0.86 | 0.93 | 0.96 | 0.93 | 0.98 | 1.59 | 1.71 | 1.96 | 1.96 | 1.96 | 2.19 | 1.60 | 1.74 | 1.98 | 1.98 | 1.98 | 1.83 | ns |
| LVCMOS15_S16 | 0.77 | 0.86 | 0.93 | 0.96 | 0.93 | 0.98 | 1.59 | 1.71 | 1.96 | 1.96 | 1.96 | 2.19 | 1.60 | 1.74 | 1.98 | 1.98 | 1.98 | 1.83 | ns |
| LVCMOS15_F4 | 0.77 | 0.86 | 0.93 | 0.96 | 0.93 | 0.98 | 1.85 | 1.97 | 2.23 | 2.23 | 2.23 | 2.27 | 1.87 | 2.00 | 2.24 | 2.24 | 2.24 | 1.91 | ns |
| LVCMOS15_F8 | 0.77 | 0.86 | 0.93 | 0.96 | 0.93 | 0.98 | 1.60 | 1.72 | 1.98 | 1.98 | 1.98 | 2.21 | 1.62 | 1.75 | 1.99 | 1.99 | 1.99 | 1.84 | ns |
| LVCMOS15_F12 | 0.77 | 0.86 | 0.93 | 0.96 | 0.93 | 0.98 | 1.35 | 1.47 | 1.73 | 1.73 | 1.73 | 1.96 | 1.37 | 1.50 | 1.74 | 1.74 | 1.74 | 1.59 | ns |
| LVCMOS15_F16 | 0.77 | 0.86 | 0.93 | 0.96 | 0.93 | 0.98 | 1.34 | 1.46 | 1.71 | 2.07 | 1.71 | 1.94 | 1.35 | 1.49 | 1.73 | 2.09 | 1.73 | 1.58 | ns |
| LVCMOS12_S4 | 0.87 | 0.95 | 1.02 | 1.19 | 1.02 | 1.08 | 2.57 | 2.69 | 2.95 | 2.95 | 2.95 | 3.18 | 2.59 | 2.72 | 2.96 | 2.96 | 2.96 | 2.81 | ns |
| LVCMOS12_S8 | 0.87 | 0.95 | 1.02 | 1.19 | 1.02 | 1.08 | 2.09 | 2.21 | 2.46 | 2.46 | 2.46 | 2.69 | 2.10 | 2.24 | 2.48 | 2.48 | 2.48 | 2.33 | ns |
| LVCMOS12_S12 | 0.87 | 0.95 | 1.02 | 1.19 | 1.02 | 1.08 | 1.79 | 1.91 | 2.17 | 2.17 | 2.17 | 2.40 | 1.81 | 1.94 | 2.18 | 2.18 | 2.18 | 2.03 | ns |
| LVCMOS12_F4 | 0.87 | 0.95 | 1.02 | 1.19 | 1.02 | 1.08 | 1.98 | 2.10 | 2.35 | 2.35 | 2.35 | 2.58 | 1.99 | 2.13 | 2.37 | 2.37 | 2.37 | 2.22 | ns |
| LVCMOS12_F8 | 0.87 | 0.95 | 1.02 | 1.19 | 1.02 | 1.08 | 1.54 | 1.66 | 1.92 | 1.92 | 1.92 | 2.15 | 1.56 | 1.69 | 1.93 | 1.93 | 1.93 | 1.78 | ns |
| LVCMOS12_F12 | 0.87 | 0.95 | 1.02 | 1.19 | 1.02 | 1.08 | 1.38 | 1.51 | 1.76 | 1.76 | 1.76 | 1.97 | 1.40 | 1.54 | 1.77 | 1.77 | 1.77 | 1.61 | ns |
| SSTL135_S | 0.67 | 0.75 | 0.82 | 0.88 | 0.82 | 0.87 | 1.35 | 1.47 | 1.73 | 1.73 | 1.73 | 1.93 | 1.37 | 1.50 | 1.74 | 1.74 | 1.74 | 1.56 | ns |
| SSTL15_S | 0.60 | 0.68 | 0.75 | 0.75 | 0.75 | 0.80 | 1.30 | 1.43 | 1.68 | 1.71 | 1.68 | 1.88 | 1.32 | 1.46 | 1.69 | 1.73 | 1.69 | 1.52 | ns |
| SSTL18_I_S | 0.67 | 0.75 | 0.82 | 0.86 | 0.82 | 0.87 | 1.67 | 1.79 | 2.04 | 2.04 | 2.04 | 2.24 | 1.68 | 1.82 | 2.06 | 2.06 | 2.06 | 1.88 | ns |
| SSTL18_II_S | 0.67 | 0.75 | 0.82 | 0.88 | 0.82 | 0.85 | 1.31 | 1.43 | 1.68 | 1.68 | 1.68 | 1.91 | 1.32 | 1.46 | 1.70 | 1.70 | 1.70 | 1.55 | ns |
| DIFF_SSTL135_S | 0.68 | 0.76 | 0.83 | 0.88 | 0.83 | 0.87 | 1.35 | 1.47 | 1.73 | 1.73 | 1.73 | 1.93 | 1.37 | 1.50 | 1.74 | 1.74 | 1.74 | 1.56 | ns |
| DIFF_SSTL15_S | 0.68 | 0.76 | 0.83 | 0.88 | 0.83 | 0.87 | 1.30 | 1.43 | 1.68 | 1.71 | 1.68 | 1.88 | 1.32 | 1.46 | 1.69 | 1.73 | 1.69 | 1.52 | ns |
| DIFF_SSTL18_I_S | 0.71 | 0.79 | 0.86 | 0.88 | 0.86 | 0.87 | 1.68 | 1.80 | 2.06 | 2.06 | 2.06 | 2.24 | 1.70 | 1.83 | 2.07 | 2.07 | 2.07 | 1.88 | ns |
| DIFF_SSTL18_II_S | 0.71 | 0.79 | 0.86 | 0.88 | 0.86 | 0.87 | 1.38 | 1.51 | 1.76 | 1.76 | 1.76 | 1.94 | 1.40 | 1.54 | 1.77 | 1.77 | 1.77 | 1.58 | ns |

*Table 17:* **IOB High Range (HR) Switching Characteristics *(Cont'd)***

| I/O Standard | $T_{IOPI}$ | | | | | | $T_{IOOP}$ | | | | | | $T_{IOTP}$ | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Speed Grade | | | | | | Speed Grade | | | | | | Speed Grade | | | | | | |
| | 1.0V | | | | 0.95V | 0.9V | 1.0V | | | | 0.95V | 0.9V | 1.0V | | | | 0.95V | 0.9V | |
| | -3 | -2/ -2LE | -1 | -1Q/ -1M | -1LI | -2LE | -3 | -2/ -2LE | -1 | -1Q/ -1M | -1LI | -2LE | -3 | -2/ -2LE | -1 | -1Q/ -1M | -1LI | -2LE | |
| SSTL135_F | 0.67 | 0.75 | 0.82 | 0.88 | 0.82 | 0.87 | 1.12 | 1.24 | 1.49 | 1.49 | 1.49 | 1.71 | 1.13 | 1.27 | 1.51 | 1.51 | 1.51 | 1.34 | ns |
| SSTL15_F | 0.60 | 0.68 | 0.75 | 0.75 | 0.75 | 0.80 | 1.07 | 1.19 | 1.45 | 1.45 | 1.45 | 1.68 | 1.09 | 1.22 | 1.46 | 1.46 | 1.46 | 1.31 | ns |
| SSTL18_I_F | 0.67 | 0.75 | 0.82 | 0.86 | 0.82 | 0.87 | 1.12 | 1.24 | 1.49 | 1.53 | 1.49 | 1.72 | 1.13 | 1.27 | 1.51 | 1.54 | 1.51 | 1.36 | ns |
| SSTL18_II_F | 0.67 | 0.75 | 0.82 | 0.88 | 0.82 | 0.85 | 1.12 | 1.24 | 1.49 | 1.51 | 1.49 | 1.71 | 1.13 | 1.27 | 1.51 | 1.52 | 1.51 | 1.34 | ns |
| DIFF_SSTL135 _F | 0.68 | 0.76 | 0.83 | 0.88 | 0.83 | 0.87 | 1.12 | 1.24 | 1.49 | 1.49 | 1.49 | 1.71 | 1.13 | 1.27 | 1.51 | 1.51 | 1.51 | 1.34 | ns |
| DIFF_SSTL15_F | 0.68 | 0.76 | 0.83 | 0.88 | 0.83 | 0.87 | 1.07 | 1.19 | 1.45 | 1.45 | 1.45 | 1.68 | 1.09 | 1.22 | 1.46 | 1.46 | 1.46 | 1.31 | ns |
| DIFF_SSTL18_I _F | 0.71 | 0.79 | 0.86 | 0.88 | 0.86 | 0.87 | 1.23 | 1.35 | 1.60 | 1.60 | 1.60 | 1.80 | 1.24 | 1.38 | 1.62 | 1.62 | 1.62 | 1.44 | ns |
| DIFF_SSTL18_II _F | 0.71 | 0.79 | 0.86 | 0.88 | 0.86 | 0.87 | 1.21 | 1.33 | 1.59 | 1.59 | 1.59 | 1.79 | 1.23 | 1.36 | 1.60 | 1.60 | 1.60 | 1.42 | ns |

Table 18 specifies the values of $T_{IOTPHZ}$ and $T_{IOIBUFDISABLE}$. $T_{IOTPHZ}$ is described as the delay from the T pin to the IOB pad through the output buffer of an IOB pad, when 3-state is enabled (i.e., a high impedance state). $T_{IOIBUFDISABLE}$ is described as the IOB delay from IBUFDISABLE to O output. In HR I/O banks, the internal IN_TERM termination turn-off time is always faster than $T_{IOTPHZ}$ when the INTERMDISABLE pin is used.

*Table 18:* **IOB 3-state Output Switching Characteristics**

| Symbol | Description | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | 1.0V | | | | 0.95V | 0.9V | |
| | | -3 | -2/-2LE | -1 | -1Q/-1M | -1LI | -2LE | |
| $T_{IOTPHZ}$ | T input to pad high-impedance | 2.06 | 2.19 | 2.37 | 2.37 | 2.37 | 2.03 | ns |
| $T_{IOIBUFDISABLE}$ | IBUF turn-on time from IBUFDISABLE to O output | 2.11 | 2.30 | 2.60 | 2.60 | 2.60 | 2.17 | ns |

## I/O Standard Adjustment Measurement Methodology

### Input Delay Measurements

Table 19 shows the test setup parameters used for measuring input delay.

*Table 19:* **Input Delay Measurement Methodology**

| Description | I/O Standard Attribute | $V_L$ (1) | $V_H$ (1) | $V_{MEAS}$ (3)(5) | $V_{REF}$ (2)(4) |
|---|---|---|---|---|---|
| LVCMOS, 1.2V | LVCMOS12 | 0.1 | 1.1 | 0.6 | – |
| LVCMOS, 1.5V | LVCMOS15 | 0.1 | 1.4 | 0.75 | – |
| LVCMOS, 1.8V | LVCMOS18 | 0.1 | 1.7 | 0.9 | – |
| LVCMOS, 2.5V | LVCMOS25 | 0.1 | 2.4 | 1.25 | – |
| LVCMOS, 3.3V | LVCMOS33 | 0.1 | 3.2 | 1.65 | – |
| LVTTL, 3.3V | LVTTL | 0.1 | 3.2 | 1.65 | – |
| MOBILE_DDR, 1.8V | MOBILE_DDR | 0.1 | 1.7 | 0.9 | – |
| PCI33, 3.3V | PCI33_3 | 0.1 | 3.2 | 1.65 | – |
| HSTL (High-Speed Transceiver Logic), Class I, 1.2V | HSTL_I_12 | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | $V_{REF}$ | 0.60 |

*Table 19:* **Input Delay Measurement Methodology *(Cont'd)***

| Description | I/O Standard Attribute | $V_L$ (1) | $V_H$ (1) | $V_{MEAS}$ (3)(5) | $V_{REF}$ (2)(4) |
|---|---|---|---|---|---|
| HSTL, Class I & II, 1.5V | HSTL_I, HSTL_II | $V_{REF}$ – 0.65 | $V_{REF}$ + 0.65 | $V_{REF}$ | 0.75 |
| HSTL, Class I & II, 1.8V | HSTL_I_18, HSTL_II_18 | $V_{REF}$ – 0.8 | $V_{REF}$ + 0.8 | $V_{REF}$ | 0.90 |
| HSUL (High-Speed Unterminated Logic), 1.2V | HSUL_12 | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | $V_{REF}$ | 0.60 |
| SSTL (Stub Terminated Transceiver Logic), 1.2V | SSTL12 | $V_{REF}$ – 0.5 | $V_{REF}$ + 0.5 | $V_{REF}$ | 0.60 |
| SSTL, 1.35V | SSTL135, SSTL135_R | $V_{REF}$ – 0.575 | $V_{REF}$ + 0.575 | $V_{REF}$ | 0.675 |
| SSTL, 1.5V | SSTL15, SSTL15_R | $V_{REF}$ – 0.65 | $V_{REF}$ + 0.65 | $V_{REF}$ | 0.75 |
| SSTL, Class I & II, 1.8V | SSTL18_I, SSTL18_II | $V_{REF}$ – 0.8 | $V_{REF}$ + 0.8 | $V_{REF}$ | 0.90 |
| DIFF_MOBILE_DDR, 1.8V | DIFF_MOBILE_DDR | 0.9 – 0.125 | 0.9 + 0.125 | 0(5) | – |
| DIFF_HSTL, Class I, 1.2V | DIFF_HSTL_I_12 | 0.6 – 0.125 | 0.6 + 0.125 | 0(5) | – |
| DIFF_HSTL, Class I & II,1.5V | DIFF_HSTL_I, DIFF_HSTL_II | 0.75 – 0.125 | 0.75 + 0.125 | 0(5) | – |
| DIFF_HSTL, Class I & II, 1.8V | DIFF_HSTL_I_18, DIFF_HSTL_II_18 | 0.9 – 0.125 | 0.9 + 0.125 | 0(5) | – |
| DIFF_HSUL, 1.2V | DIFF_HSUL_12 | 0.6 – 0.125 | 0.6 + 0.125 | 0(5) | – |
| DIFF_SSTL135/DIFF_SSTL135_R, 1.35V | DIFF_SSTL135, DIFF_SSTL135_R | 0.675 – 0.125 | 0.675 + 0.125 | 0(5) | – |
| DIFF_SSTL15/DIFF_SSTL15_R, 1.5V | DIFF_SSTL15, DIFF_SSTL15_R | 0.75 – 0.125 | 0.75 + 0.125 | 0(5) | – |
| DIFF_SSTL18_I/DIFF_SSTL18_II, 1.8V | DIFF_SSTL18_I, DIFF_SSTL18_II | 0.9 – 0.125 | 0.9 + 0.125 | 0(5) | – |
| LVDS_25, 2.5V | LVDS_25 | 1.2 – 0.125 | 1.2 + 0.125 | 0(5) | – |
| BLVDS_25, 2.5V | BLVDS_25 | 1.25 – 0.125 | 1.25 + 0.125 | 0(5) | – |
| MINI_LVDS_25, 2.5V | MINI_LVDS_25 | 1.25 – 0.125 | 1.25 + 0.125 | 0(5) | – |
| PPDS_25 | PPDS_25 | 1.25 – 0.125 | 1.25 + 0.125 | 0(5) | – |
| RSDS_25 | RSDS_25 | 1.25 – 0.125 | 1.25 + 0.125 | 0(5) | – |
| TMDS_33 | TMDS_33 | 3 – 0.125 | 3 + 0.125 | 0(5) | – |

**Notes:**

1. Input waveform switches between $V_L$ and $V_H$.
2. Measurements are made at typical, minimum, and maximum $V_{REF}$ values. Reported delays reflect worst case of these measurements. $V_{REF}$ values listed are typical.
3. Input voltage level from which measurement starts.
4. This is an input voltage reference that bears no relation to the $V_{REF}$ / $V_{MEAS}$ parameters found in IBIS models and/or noted in Figure 1.
5. The value given is the differential input voltage.

### Output Delay Measurements

Output delays are measured with short output traces. Standard termination was used for all testing. The propagation delay of the trace is characterized separately and subtracted from the final measurement, and is therefore not included in the generalized test setups shown in Figure 1 and Figure 2.

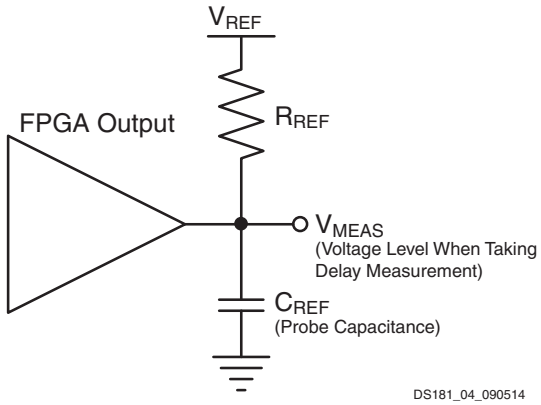



*Figure 1:* **Single-Ended Test Setup**

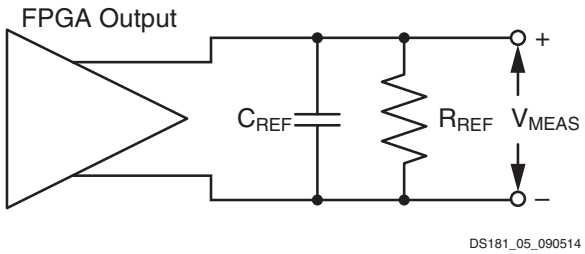



*Figure 2:* **Differential Test Setup**

Parameters $V_{REF}$, $R_{REF}$, $C_{REF}$, and $V_{MEAS}$ fully describe the test conditions for each I/O standard. The most accurate prediction of propagation delay in any given application can be obtained through IBIS simulation, using this method:

1. Simulate the output driver of choice into the generalized test setup using values from Table 20.
2. Record the time to $V_{MEAS}$.
3. Simulate the output driver of choice into the actual PCB trace and load using the appropriate IBIS model or capacitance value to represent the load.
4. Record the time to $V_{MEAS}$.
5. Compare the results of step 2 and step 4. The increase or decrease in delay yields the actual propagation delay of the PCB trace.

*Table 20:* **Output Delay Measurement Methodology**

| Description | I/O Standard Attribute | $R_{REF}$ (Ω) | $C_{REF}$[1] (pF) | $V_{MEAS}$ (V) | $V_{REF}$ (V) |
|---|---|---|---|---|---|
| LVCMOS, 1.2V | LVCMOS12 | 1M | 0 | 0.6 | 0 |
| LVCMOS, 1.5V | LVCMOS15 | 1M | 0 | 0.75 | 0 |
| LVCMOS, 1.8V | LVCMOS18 | 1M | 0 | 0.9 | 0 |
| LVCMOS, 2.5V | LVCMOS25 | 1M | 0 | 1.25 | 0 |
| LVCMOS, 3.3V | LVCMOS33 | 1M | 0 | 1.65 | 0 |
| LVTTL, 3.3V | LVTTL | 1M | 0 | 1.65 | 0 |
| PCI33, 3.3V | PCI33_3 | 25 | 10 | 1.65 | 0 |

*Table 20:* **Output Delay Measurement Methodology *(Cont'd)***

| Description | I/O Standard Attribute | $R_{REF}$ (Ω) | $C_{REF}$[1] (pF) | $V_{MEAS}$ (V) | $V_{REF}$ (V) |
|---|---|---|---|---|---|
| HSTL (High-Speed Transceiver Logic), Class I, 1.2V | HSTL_I_12 | 50 | 0 | $V_{REF}$ | 0.6 |
| HSTL, Class I, 1.5V | HSTL_I | 50 | 0 | $V_{REF}$ | 0.75 |
| HSTL, Class II, 1.5V | HSTL_II | 25 | 0 | $V_{REF}$ | 0.75 |
| HSTL, Class I, 1.8V | HSTL_I_18 | 50 | 0 | $V_{REF}$ | 0.9 |
| HSTL, Class II, 1.8V | HSTL_II_18 | 25 | 0 | $V_{REF}$ | 0.9 |
| HSUL (High-Speed Unterminated Logic), 1.2V | HSUL_12 | 50 | 0 | $V_{REF}$ | 0.6 |
| SSTL12, 1.2V | SSTL12 | 50 | 0 | $V_{REF}$ | 0.6 |
| SSTL135/SSTL135_R, 1.35V | SSTL135, SSTL135_R | 50 | 0 | $V_{REF}$ | 0.675 |
| SSTL15/SSTL15_R, 1.5V | SSTL15, SSTL15_R | 50 | 0 | $V_{REF}$ | 0.75 |
| SSTL (Stub Series Terminated Logic), Class I & Class II, 1.8V | SSTL18_I, SSTL18_II | 50 | 0 | $V_{REF}$ | 0.9 |
| DIFF_MOBILE_DDR, 1.8V | DIFF_MOBILE_DDR | 50 | 0 | $V_{REF}$ | 0.9 |
| DIFF_HSTL, Class I, 1.2V | DIFF_HSTL_I_12 | 50 | 0 | $V_{REF}$ | 0.6 |
| DIFF_HSTL, Class I & II, 1.5V | DIFF_HSTL_I, DIFF_HSTL_II | 50 | 0 | $V_{REF}$ | 0.75 |
| DIFF_HSTL, Class I & II, 1.8V | DIFF_HSTL_I_18, DIFF_HSTL_II_18 | 50 | 0 | $V_{REF}$ | 0.9 |
| DIFF_HSUL_12, 1.2V | DIFF_HSUL_12 | 50 | 0 | $V_{REF}$ | 0.6 |
| DIFF_SSTL135/DIFF_SSTL135_R, 1.35V | DIFF_SSTL135, DIFF_SSTL135_R | 50 | 0 | $V_{REF}$ | 0.675 |
| DIFF_SSTL15/DIFF_SSTL15_R, 1.5V | DIFF_SSTL15, DIFF_SSTL15_R | 50 | 0 | $V_{REF}$ | 0.75 |
| DIFF_SSTL18, Class I & II, 1.8V | DIFF_SSTL18_I, DIFF_SSTL18_II | 50 | 0 | $V_{REF}$ | 0.9 |
| LVDS, 2.5V | LVDS_25 | 100 | 0 | 0[2] | 0 |
| BLVDS (Bus LVDS), 2.5V | BLVDS_25 | 100 | 0 | 0[2] | 0 |
| Mini LVDS, 2.5V | MINI_LVDS_25 | 100 | 0 | 0[2] | 0 |
| PPDS_25 | PPDS_25 | 100 | 0 | 0[2] | 0 |
| RSDS_25 | RSDS_25 | 100 | 0 | 0[2] | 0 |
| TMDS_33 | TMDS_33 | 50 | 0 | 0[2] | 3.3 |

**Notes:**

1. $C_{REF}$ is the capacitance of the probe, nominally 0 pF.
2. The value given is the differential output voltage.

## Input/Output Logic Switching Characteristics

*Table 21:* **ILOGIC Switching Characteristics**

| Symbol | Description | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | 1.0V | | | | 0.95V | 0.9V | |
| | | -3 | -2/-2LE | -1 | -1Q/-1M | -1LI | -2LE | |
| **Setup/Hold** | | | | | | | | |
| $T_{ICE1CK}$/ $T_{ICKCE1}$ | CE1 pin setup/hold with respect to CLK | 0.48/0.02 | 0.54/0.02 | 0.76/0.02 | 0.76/0.02 | 0.76/0.02 | 0.50/–0.07 | ns |
| $T_{ISRCK}$/ $T_{ICKSR}$ | SR pin setup/hold with respect to CLK | 0.60/0.01 | 0.70/0.01 | 1.13/0.01 | 1.13/0.01 | 1.13/0.01 | 0.88/–0.35 | ns |
| $T_{IDOCK}$/ $T_{IOCKD}$ | D pin setup/hold with respect to CLK without Delay | 0.01/0.27 | 0.01/0.29 | 0.01/0.33 | 0.01/0.33 | 0.01/0.33 | 0.01/0.33 | ns |
| $T_{IDOCKD}$/ $T_{IOCKDD}$ | DDLY pin setup/hold with respect to CLK (using IDELAY) | 0.02/0.27 | 0.02/0.29 | 0.02/0.33 | 0.02/0.33 | 0.02/0.33 | 0.01/0.33 | ns |
| **Combinatorial** | | | | | | | | |
| $T_{IDI}$ | D pin to O pin propagation delay, no Delay | 0.11 | 0.11 | 0.13 | 0.13 | 0.13 | 0.14 | ns |
| $T_{IDID}$ | DDLY pin to O pin propagation delay (using IDELAY) | 0.11 | 0.12 | 0.14 | 0.14 | 0.14 | 0.15 | ns |
| **Sequential Delays** | | | | | | | | |
| $T_{IDLO}$ | D pin to Q1 pin using flip-flop as a latch without Delay | 0.41 | 0.44 | 0.51 | 0.51 | 0.51 | 0.54 | ns |
| $T_{IDLOD}$ | DDLY pin to Q1 pin using flip-flop as a latch (using IDELAY) | 0.41 | 0.44 | 0.51 | 0.51 | 0.51 | 0.55 | ns |
| $T_{ICKQ}$ | CLK to Q outputs | 0.53 | 0.57 | 0.66 | 0.66 | 0.66 | 0.71 | ns |
| $T_{RQ_ILOGIC}$ | SR pin to OQ/TQ out | 0.96 | 1.08 | 1.32 | 1.32 | 1.32 | 1.32 | ns |
| $T_{GSRQ_ILOGIC}$ | Global set/reset to Q outputs | 7.60 | 7.60 | 10.51 | 10.51 | 10.51 | 11.39 | ns |
| **Set/Reset** | | | | | | | | |
| $T_{RPW_ILOGIC}$ | Minimum pulse width, SR inputs | 0.61 | 0.72 | 0.72 | 0.72 | 0.72 | 0.72 | ns, Min |

*Table 22:* **OLOGIC Switching Characteristics**

| Symbol | Description | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | 1.0V | | | | 0.95V | 0.9V | |
| | | -3 | -2/-2LE | -1 | -1Q/-1M | -1LI | -2LE | |
| **Setup/Hold** | | | | | | | | |
| $T_{ODCK}$/ $T_{OCKD}$ | D1/D2 pins setup/hold with respect to CLK | 0.67/–0.11 | 0.71/–0.11 | 0.84/–0.11 | 0.84/–0.06 | 0.84/–0.11 | 0.64/0.03 | ns |
| $T_{OOCECK}$/ $T_{OCKOCE}$ | OCE pin setup/hold with respect to CLK | 0.32/0.58 | 0.34/0.58 | 0.51/0.58 | 0.51/0.58 | 0.51/0.58 | 0.28/0.01 | ns |
| $T_{OSRCK}$/ $T_{OCKSR}$ | SR pin setup/hold with respect to CLK | 0.37/0.21 | 0.44/0.21 | 0.80/0.21 | 0.80/0.21 | 0.80/0.21 | 0.62/–0.25 | ns |
| $T_{OTCK}$/ $T_{OCKT}$ | T1/T2 pins setup/hold with respect to CLK | 0.69/–0.14 | 0.73/–0.14 | 0.89/–0.14 | 0.89/–0.11 | 0.89/–0.14 | 0.66/0.02 | ns |
| $T_{OTCECK}$/ $T_{OCKTCE}$ | TCE pin setup/hold with respect to CLK | 0.32/0.01 | 0.34/0.01 | 0.51/0.01 | 0.51/0.10 | 0.51/0.01 | 0.24/0.05 | ns |

*Table 22:* **OLOGIC Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | 1.0V | | | | 0.95V | 0.9V | |
| | | -3 | -2/-2LE | -1 | -1Q/-1M | -1LI | -2LE | |
| **Combinatorial** | | | | | | | | |
| $T_{ODQ}$ | D1 to OQ out or T1 to TQ out | 0.83 | 0.96 | 1.16 | 1.16 | 1.16 | 1.36 | ns |
| **Sequential Delays** | | | | | | | | |
| $T_{OCKQ}$ | CLK to OQ/TQ out | 0.47 | 0.49 | 0.56 | 0.56 | 0.56 | 0.63 | ns |
| $T_{RQ_OLOGIC}$ | SR pin to OQ/TQ out | 0.72 | 0.80 | 0.95 | 0.95 | 0.95 | 1.12 | ns |
| $T_{GSRQ_OLOGIC}$ | Global set/reset to Q outputs | 7.60 | 7.60 | 10.51 | 10.51 | 10.51 | 11.39 | ns |
| **Set/Reset** | | | | | | | | |
| $T_{RPW_OLOGIC}$ | Minimum pulse width, SR inputs | 0.64 | 0.74 | 0.74 | 0.74 | 0.74 | 0.74 | ns, Min |

## Input Serializer/Deserializer Switching Characteristics

*Table 23:* **ISERDES Switching Characteristics**

| Symbol | Description | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | 1.0V | | | | 0.95V | 0.9V | |
| | | -3 | -2/-2LE | -1 | -1Q/-1M | -1LI | -2LE | |
| **Setup/Hold for Control Lines** | | | | | | | | |
| $T_{ISCCK_BITSLIP}$/ $T_{ISCKC_BITSLIP}$ | BITSLIP pin setup/hold with respect to CLKDIV | 0.01/0.14 | 0.02/0.15 | 0.02/0.17 | 0.02/0.17 | 0.02/0.17 | 0.02/0.21 | ns |
| $T_{ISCCK_CE}$ / $T_{ISCKC_CE}$(2) | CE pin setup/hold with respect to CLK (for CE1) | 0.45/–0.01 | 0.50/–0.01 | 0.72/–0.01 | 0.72/–0.01 | 0.72/–0.01 | 0.45/–0.11 | ns |
| $T_{ISCCK_CE2}$ / $T_{ISCKC_CE2}$(2) | CE pin setup/hold with respect to CLKDIV (for CE2) | –0.10/0.33 | –0.10/0.36 | –0.10/0.40 | –0.10/0.40 | –0.10/0.40 | –0.17/0.40 | ns |
| **Setup/Hold for Data Lines** | | | | | | | | |
| $T_{ISDCK_D}$ / $T_{ISCKD_D}$ | D pin setup/hold with respect to CLK | –0.02/0.12 | –0.02/0.14 | –0.02/0.17 | –0.02/0.17 | –0.02/0.17 | –0.04/0.19 | ns |
| $T_{ISDCK_DDLY}$ / $T_{ISCKD_DDLY}$ | DDLY pin setup/hold with respect to CLK (using IDELAY)(1) | –0.02/0.12 | –0.02/0.14 | –0.02/0.17 | –0.02/0.17 | –0.02/0.17 | –0.03/0.19 | ns |
| $T_{ISDCK_D_DDR}$ / $T_{ISCKD_D_DDR}$ | D pin setup/hold with respect to CLK at DDR mode | –0.02/0.12 | –0.02/0.14 | –0.02/0.17 | –0.02/0.17 | –0.02/0.17 | –0.04/0.19 | ns |
| $T_{ISDCK_DDLY_DDR}$/ $T_{ISCKD_DDLY_DDR}$ | DDLY pin setup/hold with respect to CLK at DDR mode (using IDELAY)(1) | 0.12/0.12 | 0.14/0.14 | 0.17/0.17 | 0.17/0.17 | 0.17/0.17 | 0.19/0.19 | ns |
| **Sequential Delays** | | | | | | | | |
| $T_{ISCKO_Q}$ | CLKDIV to out at Q pin | 0.53 | 0.54 | 0.66 | 0.66 | 0.66 | 0.67 | ns |
| **Propagation Delays** | | | | | | | | |
| $T_{ISDO_DO}$ | D input to DO output pin | 0.11 | 0.11 | 0.13 | 0.13 | 0.13 | 0.14 | ns |

**Notes:**

1. Recorded at 0 tap value.
2. $T_{ISCCK_CE2}$ and $T_{ISCKC_CE2}$ are reported as $T_{ISCCK_CE}$/$T_{ISCKC_CE}$ in the timing report.

## Output Serializer/Deserializer Switching Characteristics

*Table 24:* **OSERDES Switching Characteristics**

| Symbol | Description | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | 1.0V | | | | 0.95V | 0.9V | |
| | | -3 | -2/-2LE | -1 | -1Q/-1M | -1LI | -2LE | |
| **Setup/Hold** | | | | | | | | |
| $T_{OSDCK_D}$/ $T_{OSCKD_D}$ | D input setup/hold with respect to CLKDIV | 0.42/0.03 | 0.45/0.03 | 0.63/0.03 | 0.63/0.08 | 0.63/0.03 | 0.44/–0.02 | ns |
| $T_{OSDCK_T}$/ $T_{OSCKD_T}$(1) | T input setup/hold with respect to CLK | 0.69/–0.13 | 0.73/–0.13 | 0.88/–0.13 | 0.88/–0.13 | 0.88/–0.13 | 0.66/–0.25 | ns |
| $T_{OSDCK_T2}$/ $T_{OSCKD_T2}$(1) | T input setup/hold with respect to CLKDIV | 0.31/–0.13 | 0.34/–0.13 | 0.39/–0.13 | 0.39/–0.13 | 0.39/–0.13 | 0.46/–0.25 | ns |
| $T_{OSCCK_OCE}$/ $T_{OSCKC_OCE}$ | OCE input setup/hold with respect to CLK | 0.32/0.58 | 0.34/0.58 | 0.51/0.58 | 0.51/0.58 | 0.51/0.58 | 0.28/–0.04 | ns |
| $T_{OSCCK_S}$ | SR (reset) input setup with respect to CLKDIV | 0.47 | 0.52 | 0.85 | 0.85 | 0.85 | 0.70 | ns |
| $T_{OSCCK_TCE}$/ $T_{OSCKC_TCE}$ | TCE input setup/hold with respect to CLK | 0.32/0.01 | 0.34/0.01 | 0.51/0.01 | 0.51/0.10 | 0.51/0.01 | 0.24/0.00 | ns |
| **Sequential Delays** | | | | | | | | |
| $T_{OSCKO_OQ}$ | Clock to out from CLK to OQ | 0.40 | 0.42 | 0.48 | 0.48 | 0.48 | 0.54 | ns |
| $T_{OSCKO_TQ}$ | Clock to out from CLK to TQ | 0.47 | 0.49 | 0.56 | 0.56 | 0.56 | 0.63 | ns |
| **Combinatorial** | | | | | | | | |
| $T_{OSDO_TTQ}$ | T input to TQ Out | 0.83 | 0.92 | 1.11 | 1.11 | 1.11 | 1.18 | ns |

**Notes:**

1. $T_{OSDCK_T2}$ and $T_{OSCKD_T2}$ are reported as $T_{OSDCK_T}$/$T_{OSCKD_T}$ in the timing report.

## Input/Output Delay Switching Characteristics

*Table 25:* **Input/Output Delay Switching Characteristics**

| Symbol | Description | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | 1.0V | | | | 0.95V | 0.9V | |
| | | -3 | -2/-2LE | -1 | -1Q/-1M | -1LI | -2LE | |
| **IDELAYCTRL** | | | | | | | | |
| $T_{DLYCCO_RDY}$ | Reset to ready for IDELAYCTRL | 3.67 | 3.67 | 3.67 | 3.67 | 3.67 | 3.67 | µs |
| $F_{IDELAYCTRL_REF}$ | Attribute REFCLK frequency = 200.00(1) | 200.00 | 200.00 | 200.00 | 200.00 | 200.00 | 200.00 | MHz |
| | Attribute REFCLK frequency = 300.00(1) | 300.00 | 300.00 | 300.00 | 300.00 | 300.00 | 300.00 | MHz |
| | Attribute REFCLK frequency = 400.00(1) | 400.00 | 400.00 | N/A | N/A | N/A | N/A | MHz |
| IDELAYCTRL_REF_PRECISION | REFCLK precision | ±10 | ±10 | ±10 | ±10 | ±10 | ±10 | MHz |
| $T_{IDELAYCTRL_RPW}$ | Minimum Reset pulse width | 59.28 | 59.28 | 59.28 | 59.28 | 59.28 | 59.28 | ns |
| **IDELAY** | | | | | | | | |
| $T_{IDELAYRESOLUTION}$ | IDELAY chain delay resolution | 1/(32 x 2 x $F_{REF}$) | | | | | | µs |
| $T_{IDELAYPAT_JIT}$ | Pattern dependent period jitter in delay chain for clock pattern.(2) | 0 | 0 | 0 | 0 | 0 | 0 | ps per tap |
| | Pattern dependent period jitter in delay chain for random data pattern (PRBS 23)(3) | ±5 | ±5 | ±5 | ±5 | ±5 | ±5 | ps per tap |
| | Pattern dependent period jitter in delay chain for random data pattern (PRBS 23)(4) | ±9 | ±9 | ±9 | ±9 | ±9 | ±9 | ps per tap |
| $T_{IDELAY_CLK_MAX}$ | Maximum frequency of CLK input to IDELAY | 680.00 | 680.00 | 600.00 | 600.00 | 600.00 | 520.00 | MHz |
| $T_{IDCCK_CE}$ / $T_{IDCKC_CE}$ | CE pin setup/hold with respect to C for IDELAY | 0.12/0.11 | 0.16/0.13 | 0.21/0.16 | 0.21/0.16 | 0.21/0.16 | 0.14/0.16 | ns |
| $T_{IDCCK_INC}$/ $T_{IDCKC_INC}$ | INC pin setup/hold with respect to C for IDELAY | 0.12/0.16 | 0.14/0.18 | 0.16/0.22 | 0.16/0.23 | 0.16/0.22 | 0.10/0.23 | ns |
| $T_{IDCCK_RST}$/ $T_{IDCKC_RST}$ | RST pin setup/hold with respect to C for IDELAY | 0.15/0.09 | 0.16/0.11 | 0.18/0.14 | 0.18/0.14 | 0.18/0.14 | 0.22/0.19 | ns |
| $T_{IDDO_IDATAIN}$ | Propagation delay through IDELAY | Note 5 | Note 5 | Note 5 | Note 5 | Note 5 | Note 5 | ps |

**Notes:**

1. Average Tap Delay at 200 MHz = 78 ps, at 300 MHz = 52 ps, and at 400 MHz = 39 ps.
2. When HIGH_PERFORMANCE mode is set to TRUE or FALSE.
3. When HIGH_PERFORMANCE mode is set to TRUE.
4. When HIGH_PERFORMANCE mode is set to FALSE.
5. Delay depends on IDELAY tap setting. See the timing report for actual values.

*Table 26:* **IO_FIFO Switching Characteristics**

| Symbol | Description | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | 1.0V | | | | 0.95V | 0.9V | |
| | | -3 | -2/-2LE | -1 | -1Q/-1M | -1LI | -2LE | |
| **IO_FIFO Clock to Out Delays** | | | | | | | | |
| $T_{OFFCKO_DO}$ | RDCLK to Q outputs | 0.55 | 0.60 | 0.68 | 0.68 | 0.68 | 0.81 | ns |
| $T_{CKO_FLAGS}$ | Clock to IO_FIFO flags | 0.55 | 0.61 | 0.77 | 0.77 | 0.77 | 0.79 | ns |
| **Setup/Hold** | | | | | | | | |
| $T_{CCK_D}/T_{CKC_D}$ | D inputs to WRCLK | 0.47/0.02 | 0.51/0.02 | 0.58/0.02 | 0.58/0.18 | 0.58/0.02 | 0.76/0.09 | ns |
| $T_{IFFCCK_WREN}/T_{IFFCKC_WREN}$ | WREN to WRCLK | 0.42/–0.01 | 0.47/–0.01 | 0.53/–0.01 | 0.53/–0.01 | 0.53/–0.01 | 0.70/–0.05 | ns |
| $T_{OFFCCK_RDEN}/T_{OFFCKC_RDEN}$ | RDEN to RDCLK | 0.53/0.02 | 0.58/0.02 | 0.66/0.02 | 0.66/0.02 | 0.66/0.02 | 0.79/–0.02 | ns |
| **Minimum Pulse Width** | | | | | | | | |
| $T_{PWH_IO_FIFO}$ | RESET, RDCLK, WRCLK | 1.62 | 2.15 | 2.15 | 2.15 | 2.15 | 2.15 | ns |
| $T_{PWL_IO_FIFO}$ | RESET, RDCLK, WRCLK | 1.62 | 2.15 | 2.15 | 2.15 | 2.15 | 2.15 | ns |
| **Maximum Frequency** | | | | | | | | |
| $F_{MAX}$ | RDCLK and WRCLK | 266.67 | 200.00 | 200.00 | 200.00 | 200.00 | 200.00 | MHz |

## CLB Switching Characteristics

*Table 27:* **CLB Switching Characteristics**

| Symbol | Description | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | 1.0V | | | | 0.95V | 0.9V | |
| | | -3 | -2/-2LE | -1 | -1Q/-1M | -1LI | -2LE | |
| **Combinatorial Delays** | | | | | | | | |
| $T_{ILO}$ | An – Dn LUT address to A | 0.10 | 0.11 | 0.13 | 0.13 | 0.13 | 0.15 | ns, Max |
| $T_{ILO_2}$ | An – Dn LUT address to AMUX/CMUX | 0.27 | 0.30 | 0.36 | 0.36 | 0.36 | 0.41 | ns, Max |
| $T_{ILO_3}$ | An – Dn LUT address to BMUX_A | 0.42 | 0.46 | 0.55 | 0.55 | 0.55 | 0.65 | ns, Max |
| $T_{ITO}$ | An – Dn inputs to A – D Q outputs | 0.94 | 1.05 | 1.27 | 1.27 | 1.27 | 1.51 | ns, Max |
| $T_{AXA}$ | AX inputs to AMUX output | 0.62 | 0.69 | 0.84 | 0.84 | 0.84 | 1.01 | ns, Max |
| $T_{AXB}$ | AX inputs to BMUX output | 0.58 | 0.66 | 0.83 | 0.83 | 0.83 | 0.98 | ns, Max |
| $T_{AXC}$ | AX inputs to CMUX output | 0.60 | 0.68 | 0.82 | 0.82 | 0.82 | 0.98 | ns, Max |
| $T_{AXD}$ | AX inputs to DMUX output | 0.68 | 0.75 | 0.90 | 0.90 | 0.90 | 1.08 | ns, Max |
| $T_{BXB}$ | BX inputs to BMUX output | 0.51 | 0.57 | 0.69 | 0.69 | 0.69 | 0.82 | ns, Max |
| $T_{BXD}$ | BX inputs to DMUX output | 0.62 | 0.69 | 0.82 | 0.82 | 0.82 | 0.99 | ns, Max |
| $T_{CXC}$ | CX inputs to CMUX output | 0.42 | 0.48 | 0.58 | 0.58 | 0.58 | 0.69 | ns, Max |
| $T_{CXD}$ | CX inputs to DMUX output | 0.53 | 0.59 | 0.71 | 0.71 | 0.71 | 0.86 | ns, Max |
| $T_{DXD}$ | DX inputs to DMUX output | 0.52 | 0.58 | 0.70 | 0.70 | 0.70 | 0.84 | ns, Max |
| **Sequential Delays** | | | | | | | | |
| $T_{CKO}$ | Clock to AQ – DQ outputs | 0.40 | 0.44 | 0.53 | 0.53 | 0.53 | 0.62 | ns, Max |
| $T_{SHCKO}$ | Clock to AMUX – DMUX outputs | 0.47 | 0.53 | 0.66 | 0.66 | 0.66 | 0.73 | ns, Max |
| **Setup and Hold Times of CLB Flip-Flops Before/After Clock CLK** | | | | | | | | |
| $T_{AS}/T_{AH}$ | $A_N$ – $D_N$ input to CLK on A – D flip-flops | 0.07/0.12 | 0.09/0.14 | 0.11/0.18 | 0.11/0.28 | 0.11/0.18 | 0.11/0.22 | ns, Min |
| $T_{DICK}/T_{CKDI}$ | $A_X$ – $D_X$ input to CLK on A – D flip-flops | 0.06/0.19 | 0.07/0.21 | 0.09/0.26 | 0.09/0.35 | 0.09/0.26 | 0.09/0.33 | ns, Min |
| | $A_X$ – $D_X$ input through MUXs and/or carry logic to CLK on A – D flip-flops | 0.59/0.08 | 0.66/0.09 | 0.81/0.11 | 0.81/0.20 | 0.81/0.11 | 0.97/0.15 | ns, Min |
| $T_{CECK_CLB}/T_{CKCE_CLB}$ | CE input to CLK on A – D flip-flops | 0.15/0.00 | 0.17/0.00 | 0.21/0.01 | 0.21/0.13 | 0.21/0.01 | 0.34/–0.01 | ns, Min |
| $T_{SRCK}/T_{CKSR}$ | SR input to CLK on A – D flip-flops | 0.38/0.03 | 0.43/0.04 | 0.53/0.05 | 0.53/0.18 | 0.53/0.05 | 0.62/0.19 | ns, Min |
| **Set/Reset** | | | | | | | | |
| $T_{SRMIN}$ | SR input minimum pulse width | 0.52 | 0.78 | 1.04 | 1.04 | 1.04 | 0.95 | ns, Min |
| $T_{RQ}$ | Delay from SR input to AQ – DQ flip-flops | 0.53 | 0.59 | 0.71 | 0.71 | 0.71 | 0.83 | ns, Max |
| $T_{CEO}$ | Delay from CE input to AQ – DQ flip-flops | 0.52 | 0.58 | 0.70 | 0.70 | 0.70 | 0.83 | ns, Max |
| $F_{TOG}$ | Toggle frequency (for export control) | 1412 | 1286 | 1098 | 1098 | 1098 | 1098 | MHz |

## CLB Distributed RAM Switching Characteristics (SLICEM Only)

*Table 28:* **CLB Distributed RAM Switching Characteristics**

| Symbol | Description | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | 1.0V | | | | 0.95V | 0.9V | |
| | | -3 | -2/-2LE | -1 | -1Q/-1M | -1LI | -2LE | |
| **Sequential Delays** | | | | | | | | |
| $T_{SHCKO}$ | Clock to A – B outputs | 0.98 | 1.09 | 1.32 | 1.32 | 1.32 | 1.54 | ns, Max |
| $T_{SHCKO_1}$ | Clock to AMUX – BMUX outputs | 1.37 | 1.53 | 1.86 | 1.86 | 1.86 | 2.18 | ns, Max |
| **Setup and Hold Times Before/After Clock CLK** | | | | | | | | |
| $T_{DS_LRAM}$/ $T_{DH_LRAM}$ | A – D inputs to CLK | 0.54/0.28 | 0.60/0.30 | 0.72/0.35 | 0.72/0.37 | 0.72/0.35 | 0.96/0.40 | ns, Min |
| $T_{AS_LRAM}$/ $T_{AH_LRAM}$ | Address An inputs to clock | 0.27/0.55 | 0.30/0.60 | 0.37/0.70 | 0.37/0.71 | 0.37/0.70 | 0.43/0.71 | ns, Min |
| | Address An inputs through MUXs and/or carry logic to clock | 0.69/0.18 | 0.77/0.21 | 0.94/0.26 | 0.94/0.35 | 0.94/0.26 | 1.11/0.31 | ns, Min |
| $T_{WS_LRAM}$/ $T_{WH_LRAM}$ | WE input to clock | 0.38/0.10 | 0.43/0.12 | 0.53/0.17 | 0.53/0.17 | 0.53/0.17 | 0.62/0.13 | ns, Min |
| $T_{CECK_LRAM}$/ $T_{CKCE_LRAM}$ | CE input to CLK | 0.39/0.10 | 0.44/0.11 | 0.53/0.17 | 0.53/0.17 | 0.53/0.17 | 0.63/0.12 | ns, Min |
| **Clock CLK** | | | | | | | | |
| $T_{MPW_LRAM}$ | Minimum pulse width | 1.05 | 1.13 | 1.25 | 1.25 | 1.25 | 1.61 | ns, Min |
| $T_{MCP}$ | Minimum clock period | 2.10 | 2.26 | 2.50 | 2.50 | 2.50 | 3.21 | ns, Min |

**Notes:**

1. $T_{SHCKO}$ also represents the CLK to XMUX output. Refer to the timing report for the CLK to XMUX path.

## CLB Shift Register Switching Characteristics (SLICEM Only)

*Table 29:* **CLB Shift Register Switching Characteristics**

| Symbol | Description | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | 1.0V | | | | 0.95V | 0.9V | |
| | | -3 | -2/-2LE | -1 | -1Q/-1M | -1LI | -2LE | |
| **Sequential Delays** | | | | | | | | |
| $T_{REG}$ | Clock to A – D outputs | 1.19 | 1.33 | 1.61 | 1.61 | 1.61 | 1.89 | ns, Max |
| $T_{REG_MUX}$ | Clock to AMUX – DMUX output | 1.58 | 1.77 | 2.15 | 2.15 | 2.15 | 2.53 | ns, Max |
| $T_{REG_M31}$ | Clock to DMUX output via M31 output | 1.12 | 1.23 | 1.46 | 1.46 | 1.46 | 1.68 | ns, Max |
| **Setup and Hold Times Before/After Clock CLK** | | | | | | | | |
| $T_{WS_SHFREG}$/ $T_{WH_SHFREG}$ | WE input | 0.37/0.10 | 0.41/0.12 | 0.51/0.17 | 0.51/0.17 | 0.51/0.17 | 0.59/0.13 | ns, Min |
| $T_{CECK_SHFREG}$/ $T_{CKCE_SHFREG}$ | CE input to CLK | 0.37/0.10 | 0.42/0.11 | 0.52/0.17 | 0.52/0.17 | 0.52/0.17 | 0.60/0.12 | ns, Min |
| $T_{DS_SHFREG}$/ $T_{DH_SHFREG}$ | A – D inputs to CLK | 0.33/0.34 | 0.37/0.37 | 0.44/0.43 | 0.44/0.44 | 0.44/0.43 | 0.54/0.55 | ns, Min |
| **Clock CLK** | | | | | | | | |
| $T_{MPW_SHFREG}$ | Minimum pulse width | 0.77 | 0.86 | 0.98 | 0.98 | 0.98 | 1.22 | ns, Min |

## Block RAM and FIFO Switching Characteristics

*Table 30:* **Block RAM and FIFO Switching Characteristics**

| Symbol | Description | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | 1.0V | | | | 0.95V | 0.9V | |
| | | -3 | -2/-2LE | -1 | -1Q/-1M | -1LI | -2LE | |
| **Block RAM and FIFO Clock-to-Out Delays** | | | | | | | | |
| $T_{RCKO_DO}$ and $T_{RCKO_DO_REG}$[1] | Clock CLK to DOUT output (without output register)[2][3] | 1.85 | 2.13 | 2.46 | 2.46 | 2.46 | 2.87 | ns, Max |
| | Clock CLK to DOUT output (with output register)[4][5] | 0.64 | 0.74 | 0.89 | 0.89 | 0.89 | 1.02 | ns, Max |
| $T_{RCKO_DO_ECC}$ and $T_{RCKO_DO_ECC_REG}$ | Clock CLK to DOUT output with ECC (without output register)[2][3] | 2.77 | 3.04 | 3.84 | 3.84 | 3.84 | 5.30 | ns, Max |
| | Clock CLK to DOUT output with ECC (with output register)[4][5] | 0.73 | 0.81 | 0.94 | 0.94 | 0.94 | 1.11 | ns, Max |
| $T_{RCKO_DO_CASCOUT}$ and $T_{RCKO_DO_CASCOUT_REG}$ | Clock CLK to DOUT output with cascade (without output register)[2] | 2.61 | 2.88 | 3.30 | 3.30 | 3.30 | 3.76 | ns, Max |
| | Clock CLK to DOUT output with cascade (with output register)[4] | 1.16 | 1.28 | 1.46 | 1.46 | 1.46 | 1.56 | ns, Max |
| $T_{RCKO_FLAGS}$ | Clock CLK to FIFO flags outputs[6] | 0.76 | 0.87 | 1.05 | 1.05 | 1.05 | 1.14 | ns, Max |
| $T_{RCKO_POINTERS}$ | Clock CLK to FIFO pointers outputs[7] | 0.94 | 1.02 | 1.15 | 1.15 | 1.15 | 1.30 | ns, Max |
| $T_{RCKO_PARITY_ECC}$ | Clock CLK to ECCPARITY in ECC encode only mode | 0.78 | 0.85 | 0.94 | 0.94 | 0.94 | 1.10 | ns, Max |
| $T_{RCKO_SDBIT_ECC}$ and $T_{RCKO_SDBIT_ECC_REG}$ | Clock CLK to BITERR (without output register) | 2.56 | 2.81 | 3.55 | 3.55 | 3.55 | 4.90 | ns, Max |
| | Clock CLK to BITERR (with output register) | 0.68 | 0.76 | 0.89 | 0.89 | 0.89 | 1.05 | ns, Max |
| $T_{RCKO_RDADDR_ECC}$ and $T_{RCKO_RDADDR_ECC_REG}$ | Clock CLK to RDADDR output with ECC (without output register) | 0.75 | 0.88 | 1.07 | 1.07 | 1.07 | 1.15 | ns, Max |
| | Clock CLK to RDADDR output with ECC (with output register) | 0.84 | 0.93 | 1.08 | 1.08 | 1.08 | 1.29 | ns, Max |
| **Setup and Hold Times Before/After Clock CLK** | | | | | | | | |
| $T_{RCCK_ADDRA}$/ $T_{RCKC_ADDRA}$ | ADDR inputs[8] | 0.45/0.31 | 0.49/0.33 | 0.57/0.36 | 0.57/0.52 | 0.57/0.36 | 0.77/0.45 | ns, Min |
| $T_{RDCK_DI_WF_NC}$/ $T_{RCKD_DI_WF_NC}$ | Data input setup/hold time when block RAM is configured in WRITE_FIRST or NO_CHANGE mode[9] | 0.58/0.60 | 0.65/0.63 | 0.74/0.67 | 0.74/0.67 | 0.74/0.67 | 0.92/0.76 | ns, Min |
| $T_{RDCK_DI_RF}$/ $T_{RCKD_DI_RF}$ | Data input setup/hold time when block RAM is configured in READ_FIRST mode[9] | 0.20/0.29 | 0.22/0.34 | 0.25/0.41 | 0.25/0.50 | 0.25/0.41 | 0.29/0.38 | ns, Min |

*Table 30:* **Block RAM and FIFO Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | 1.0V | | | | 0.95V | 0.9V | |
| | | -3 | -2/-2LE | -1 | -1Q/-1M | -1LI | -2LE | |
| $T_{RDCK_DI_ECC}$/ $T_{RCKD_DI_ECC}$ | DIN inputs with block RAM ECC in standard mode(9) | 0.50/0.43 | 0.55/0.46 | 0.63/0.50 | 0.63/0.50 | 0.63/0.50 | 0.78/0.54 | ns, Min |
| $T_{RDCK_DI_ECCW}$/ $T_{RCKD_DI_ECCW}$ | DIN inputs with block RAM ECC encode only(9) | 0.93/0.43 | 1.02/0.46 | 1.17/0.50 | 1.17/0.50 | 1.17/0.50 | 1.38/0.48 | ns, Min |
| $T_{RDCK_DI_ECC_FIFO}$/ $T_{RCKD_DI_ECC_FIFO}$ | DIN inputs with FIFO ECC in standard mode(9) | 1.04/0.56 | 1.15/0.59 | 1.32/0.64 | 1.32/0.64 | 1.32/0.64 | 1.55/0.77 | ns, Min |
| $T_{RCCK_INJECTBITERR}$/ $T_{RCKC_INJECTBITERR}$ | Inject single/double bit error in ECC mode | 0.58/0.35 | 0.64/0.37 | 0.74/0.40 | 0.74/0.52 | 0.74/0.40 | 0.92/0.48 | ns, Min |
| $T_{RCCK_EN}$/$T_{RCKC_EN}$ | Block RAM enable (EN) input | 0.35/0.20 | 0.39/0.21 | 0.45/0.23 | 0.45/0.41 | 0.45/0.23 | 0.57/0.26 | ns, Min |
| $T_{RCCK_REGCE}$/ $T_{RCKC_REGCE}$ | CE input of output register | 0.24/0.15 | 0.29/0.15 | 0.36/0.16 | 0.36/0.39 | 0.36/0.16 | 0.40/0.19 | ns, Min |
| $T_{RCCK_RSTREG}$/ $T_{RCKC_RSTREG}$ | Synchronous RSTREG input | 0.29/0.07 | 0.32/0.07 | 0.35/0.07 | 0.35/0.17 | 0.35/0.07 | 0.41/0.07 | ns, Min |
| $T_{RCCK_RSTRAM}$/ $T_{RCKC_RSTRAM}$ | Synchronous RSTRAM input | 0.32/0.42 | 0.34/0.43 | 0.36/0.46 | 0.36/0.57 | 0.36/0.46 | 0.40/0.47 | ns, Min |
| $T_{RCCK_WEA}$/ $T_{RCKC_WEA}$ | Write enable (WE) input (block RAM only) | 0.44/0.18 | 0.48/0.19 | 0.54/0.20 | 0.54/0.42 | 0.54/0.20 | 0.64/0.23 | ns, Min |
| $T_{RCCK_WREN}$/ $T_{RCKC_WREN}$ | WREN FIFO inputs | 0.46/0.30 | 0.46/0.35 | 0.47/0.43 | 0.47/0.43 | 0.47/0.43 | 0.77/0.44 | ns, Min |
| $T_{RCCK_RDEN}$/ $T_{RCKC_RDEN}$ | RDEN FIFO inputs | 0.42/0.30 | 0.43/0.35 | 0.43/0.43 | 0.43/0.62 | 0.43/0.43 | 0.71/0.50 | ns, Min |
| **Reset Delays** | | | | | | | | |
| $T_{RCO_FLAGS}$ | Reset RST to FIFO flags/pointers(10) | 0.90 | 0.98 | 1.10 | 1.10 | 1.10 | 1.25 | ns, Max |
| $T_{RREC_RST}$/ $T_{RREM_RST}$ | FIFO reset recovery and removal timing(11) | 1.87/–0.81 | 2.07/–0.81 | 2.37/–0.81 | 2.37/–0.58 | 2.37/–0.81 | 2.44/–0.71 | ns, Max |
| **Maximum Frequency** | | | | | | | | |
| $F_{MAX_BRAM_WF_NC}$ | Block RAM (write first and no change modes) when not in SDP RF mode | 509.68 | 460.83 | 388.20 | 388.20 | 388.20 | 315.66 | MHz |
| $F_{MAX_BRAM_RF_PERFORMANCE}$ | Block RAM (read first, performance mode) when in SDP RF mode but no address overlap between port A and port B | 509.68 | 460.83 | 388.20 | 388.20 | 388.20 | 315.66 | MHz |
| $F_{MAX_BRAM_RF_DELAYED_WRITE}$ | Block RAM (read first, delayed write mode) when in SDP RF mode and there is possibility of overlap between port A and port B addresses | 447.63 | 404.53 | 339.67 | 339.67 | 339.67 | 268.96 | MHz |

*Table 30:* **Block RAM and FIFO Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | 1.0V | | | | 0.95V | 0.9V | |
| | | -3 | -2/-2LE | -1 | -1Q/-1M | -1LI | -2LE | |
| $F_{MAX_CAS_WF_NC}$ | Block RAM cascade (write first, no change mode) when cascade but not in RF mode | 467.07 | 418.59 | 345.78 | 345.78 | 345.78 | 273.30 | MHz |
| $F_{MAX_CAS_RF_PERFORMANCE}$ | Block RAM cascade (read first, performance mode) when in cascade with RF mode and no possibility of address overlap/one port is disabled | 467.07 | 418.59 | 345.78 | 345.78 | 345.78 | 273.30 | MHz |
| $F_{MAX_CAS_RF_DELAYED_WRITE}$ | When in cascade RF mode and there is a possibility of address overlap between port A and port B | 405.35 | 362.19 | 297.35 | 297.35 | 297.35 | 226.60 | MHz |
| $F_{MAX_FIFO}$ | FIFO in all modes without ECC | 509.68 | 460.83 | 388.20 | 388.20 | 388.20 | 315.66 | MHz |
| $F_{MAX_ECC}$ | Block RAM and FIFO in ECC configuration | 410.34 | 365.10 | 297.53 | 297.53 | 297.53 | 215.38 | MHz |

**Notes:**

1. The timing report shows all of these parameters as $T_{RCKO_DO}$.
2. $T_{RCKO_DOR}$ includes $T_{RCKO_DOW}$, $T_{RCKO_DOPR}$, and $T_{RCKO_DOPW}$ as well as the B port equivalent timing parameters.
3. These parameters also apply to synchronous FIFO with DO_REG = 0.
4. $T_{RCKO_DO}$ includes $T_{RCKO_DOP}$ as well as the B port equivalent timing parameters.
5. These parameters also apply to multirate (asynchronous) and synchronous FIFO with DO_REG = 1.
6. $T_{RCKO_FLAGS}$ includes the following parameters: $T_{RCKO_AEMPTY}$, $T_{RCKO_AFULL}$, $T_{RCKO_EMPTY}$, $T_{RCKO_FULL}$, $T_{RCKO_RDERR}$, $T_{RCKO_WRERR}$.
7. $T_{RCKO_POINTERS}$ includes both $T_{RCKO_RDCOUNT}$ and $T_{RCKO_WRCOUNT}$.
8. The ADDR setup and hold must be met when EN is asserted (even when WE is deasserted). Otherwise, block RAM data corruption is possible.
9. These parameters include both A and B inputs as well as the parity inputs of A and B.
10. $T_{RCO_FLAGS}$ includes the following flags: AEMPTY, AFULL, EMPTY, FULL, RDERR, WRERR, RDCOUNT, and WRCOUNT.
11. RDEN and WREN must be held Low prior to and during reset. The FIFO reset must be asserted for at least five positive clock edges of the slowest clock (WRCLK or RDCLK).

## DSP48E1 Switching Characteristics

*Table 31:* **DSP48E1 Switching Characteristics**

| Symbol | Description | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | 1.0V | | | | 0.95V | 0.9V | |
| | | -3 | -2/-2LE | -1 | -1Q/-1M | -1LI | -2LE | |
| **Setup and Hold Times of Data/Control Pins to the Input Register Clock** | | | | | | | | |
| $T_{DSPDCK_A_AREG}$/ $T_{DSPCKD_A_AREG}$ | A input to A register CLK | 0.26/ 0.12 | 0.30/ 0.13 | 0.37/ 0.14 | 0.37/ 0.28 | 0.37/ 0.14 | 0.45/ 0.14 | ns |
| $T_{DSPDCK_B_BREG}$/ $T_{DSPCKD_B_BREG}$ | B input to B register CLK | 0.33/ 0.15 | 0.38/ 0.16 | 0.45/ 0.18 | 0.45/ 0.25 | 0.45/ 0.18 | 0.60/ 0.19 | ns |
| $T_{DSPDCK_C_CREG}$/ $T_{DSPCKD_C_CREG}$ | C input to C register CLK | 0.17/ 0.17 | 0.20/ 0.19 | 0.24/ 0.21 | 0.24/ 0.26 | 0.24/ 0.21 | 0.34/ 0.29 | ns |
| $T_{DSPDCK_D_DREG}$/ $T_{DSPCKD_D_DREG}$ | D input to D register CLK | 0.25/ 0.25 | 0.32/ 0.27 | 0.42/ 0.27 | 0.42/ 0.42 | 0.42/ 0.27 | 0.54/ 0.23 | ns |
| $T_{DSPDCK_ACIN_AREG}$/ $T_{DSPCKD_ACIN_AREG}$ | ACIN input to A register CLK | 0.23/ 0.12 | 0.27/ 0.13 | 0.32/ 0.14 | 0.32/ 0.17 | 0.32/ 0.14 | 0.36/ 0.14 | ns |
| $T_{DSPDCK_BCIN_BREG}$/ $T_{DSPCKD_BCIN_BREG}$ | BCIN input to B register CLK | 0.25/ 0.15 | 0.29/ 0.16 | 0.36/ 0.18 | 0.36/ 0.18 | 0.36/ 0.18 | 0.41/ 0.19 | ns |
| **Setup and Hold Times of Data Pins to the Pipeline Register Clock** | | | | | | | | |
| $T_{DSPDCK_\{A, B\}_MREG_MULT}$/ $T_{DSPCKD_\{A, B\}_MREG_MULT}$ | {A, B} input to M register CLK using multiplier | 2.40/ –0.01 | 2.76/ –0.01 | 3.29/ –0.01 | 3.29/ –0.01 | 3.29/ –0.01 | 4.31/ –0.07 | ns |
| $T_{DSPDCK_\{A, D\}_ADREG}$/ $T_{DSPCKD_\{A, D\}_ADREG}$ | {A, D} input to AD register CLK | 1.29/ –0.02 | 1.48/ –0.02 | 1.76/ –0.02 | 1.76/ –0.02 | 1.76/ –0.02 | 2.29/ –0.27 | ns |
| **Setup and Hold Times of Data/Control Pins to the Output Register Clock** | | | | | | | | |
| $T_{DSPDCK_\{A, B\}_PREG_MULT}$/ $T_{DSPCKD_\{A, B\}_PREG_MULT}$ | {A, B} input to P register CLK using multiplier | 4.02/ –0.28 | 4.60/ –0.28 | 5.48/ –0.28 | 5.48/ –0.28 | 5.48/ –0.28 | 6.95/ –0.48 | ns |
| $T_{DSPDCK_D_PREG_MULT}$/ $T_{DSPCKD_D_PREG_MULT}$ | D input to P register CLK using multiplier | 3.93/ –0.73 | 4.50/ –0.73 | 5.35/ –0.73 | 5.35/ –0.73 | 5.35/ –0.73 | 6.73/ –1.68 | ns |
| $T_{DSPDCK_\{A, B\}_PREG}$/ $T_{DSPCKD_\{A, B\}_PREG}$ | A or B input to P register CLK not using multiplier | 1.73/ –0.28 | 1.98/ –0.28 | 2.35/ –0.28 | 2.35/ –0.28 | 2.35/ –0.28 | 2.80/ –0.48 | ns |
| $T_{DSPDCK_C_PREG}$/ $T_{DSPCKD_C_PREG}$ | C input to P register CLK not using multiplier | 1.54/ –0.26 | 1.76/ –0.26 | 2.10/ –0.26 | 2.10/ –0.26 | 2.10/ –0.26 | 2.54/ –0.45 | ns |
| $T_{DSPDCK_PCIN_PREG}$/ $T_{DSPCKD_PCIN_PREG}$ | PCIN input to P register CLK | 1.32/ –0.15 | 1.51/ –0.15 | 1.80/ –0.15 | 1.80/ –0.15 | 1.80/ –0.15 | 2.13/ –0.25 | ns |
| **Setup and Hold Times of the CE Pins** | | | | | | | | |
| $T_{DSPDCK_\{CEA;CEB\}_\{AREG;BREG\}}$/ $T_{DSPCKD_\{CEA;CEB\}_\{AREG;BREG\}}$ | {CEA; CEB} input to {A; B} register CLK | 0.35/ 0.06 | 0.42/ 0.08 | 0.52/ 0.11 | 0.52/ 0.11 | 0.52/ 0.11 | 0.64/ 0.11 | ns |
| $T_{DSPDCK_CEC_CREG}$/ $T_{DSPCKD_CEC_CREG}$ | CEC input to C register CLK | 0.28/ 0.10 | 0.34/ 0.11 | 0.42/ 0.13 | 0.42/ 0.13 | 0.42/ 0.13 | 0.49/ 0.16 | ns |
| $T_{DSPDCK_CED_DREG}$/ $T_{DSPCKD_CED_DREG}$ | CED input to D register CLK | 0.36/ –0.03 | 0.43/ –0.03 | 0.52/ –0.03 | 0.52/ –0.03 | 0.52/ –0.03 | 0.68/ 0.14 | ns |
| $T_{DSPDCK_CEM_MREG}$/ $T_{DSPCKD_CEM_MREG}$ | CEM input to M register CLK | 0.17/ 0.18 | 0.21/ 0.20 | 0.27/ 0.23 | 0.27/ 0.23 | 0.27/ 0.23 | 0.45/ 0.29 | ns |
| $T_{DSPDCK_CEP_PREG}$/ $T_{DSPCKD_CEP_PREG}$ | CEP input to P register CLK | 0.36/ 0.01 | 0.43/ 0.01 | 0.53/ 0.01 | 0.53/ 0.01 | 0.53/ 0.01 | 0.63/ 0.00 | ns |

*Table 31:* **DSP48E1 Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | 1.0V | | | | 0.95V | 0.9V | |
| | | -3 | -2/-2LE | -1 | -1Q/-1M | -1LI | -2LE | |
| **Setup and Hold Times of the RST Pins** | | | | | | | | |
| $T_{DSPDCK_\{RSTA;\ RSTB\}_\{AREG;\ BREG\}}$/ $T_{DSPCKD_\{RSTA;\ RSTB\}_\{AREG;\ BREG\}}$ | {RSTA, RSTB} input to {A, B} register CLK | 0.41/ 0.11 | 0.46/ 0.13 | 0.55/ 0.15 | 0.55/ 0.24 | 0.55/ 0.15 | 0.63/ 0.40 | ns |
| $T_{DSPDCK_RSTC_CREG}$/ $T_{DSPCKD_RSTC_CREG}$ | RSTC input to C register CLK | 0.07/ 0.10 | 0.08/ 0.11 | 0.09/ 0.12 | 0.09/ 0.25 | 0.09/ 0.12 | 0.13/ 0.11 | ns |
| $T_{DSPDCK_RSTD_DREG}$/ $T_{DSPCKD_RSTD_DREG}$ | RSTD input to D register CLK | 0.44/ 0.07 | 0.50/ 0.08 | 0.59/ 0.09 | 0.59/ 0.09 | 0.59/ 0.09 | 0.67/ 0.08 | ns |
| $T_{DSPDCK_RSTM_MREG}$/ $T_{DSPCKD_RSTM_MREG}$ | RSTM input to M register CLK | 0.21/ 0.22 | 0.23/ 0.24 | 0.27/ 0.28 | 0.27/ 0.28 | 0.27/ 0.28 | 0.28/ 0.35 | ns |
| $T_{DSPDCK_RSTP_PREG}$/ $T_{DSPCKD_RSTP_PREG}$ | RSTP input to P register CLK | 0.27/ 0.01 | 0.30/ 0.01 | 0.35/ 0.01 | 0.35/ 0.03 | 0.35/ 0.01 | 0.43/ 0.00 | ns |
| **Combinatorial Delays from Input Pins to Output Pins** | | | | | | | | |
| $T_{DSPDO_A_CARRYOUT_MULT}$ | A input to CARRYOUT output using multiplier | 3.79 | 4.35 | 5.18 | 5.18 | 5.18 | 6.61 | ns |
| $T_{DSPDO_D_P_MULT}$ | D input to P output using multiplier | 3.72 | 4.26 | 5.07 | 5.07 | 5.07 | 6.41 | ns |
| $T_{DSPDO_B_P}$ | B input to P output not using multiplier | 1.53 | 1.75 | 2.08 | 2.08 | 2.08 | 2.48 | ns |
| $T_{DSPDO_C_P}$ | C input to P output | 1.33 | 1.53 | 1.82 | 1.82 | 1.82 | 2.22 | ns |
| **Combinatorial Delays from Input Pins to Cascading Output Pins** | | | | | | | | |
| $T_{DSPDO_\{A;\ B\}_\{ACOUT;\ BCOUT\}}$ | {A, B} input to {ACOUT, BCOUT} output | 0.55 | 0.63 | 0.74 | 0.74 | 0.74 | 0.87 | ns |
| $T_{DSPDO_\{A,\ B\}_CARRYCASCOUT_MULT}$ | {A, B} input to CARRYCASCOUT output using multiplier | 4.06 | 4.65 | 5.54 | 5.54 | 5.54 | 7.03 | ns |
| $T_{DSPDO_D_CARRYCASCOUT_MULT}$ | D input to CARRYCASCOUT output using multiplier | 3.97 | 4.54 | 5.40 | 5.40 | 5.40 | 6.81 | ns |
| $T_{DSPDO_\{A,\ B\}_CARRYCASCOUT}$ | {A, B} input to CARRYCASCOUT output not using multiplier | 1.77 | 2.03 | 2.41 | 2.41 | 2.41 | 2.88 | ns |
| $T_{DSPDO_C_CARRYCASCOUT}$ | C input to CARRYCASCOUT output | 1.58 | 1.81 | 2.15 | 2.15 | 2.15 | 2.62 | ns |
| **Combinatorial Delays from Cascading Input Pins to All Output Pins** | | | | | | | | |
| $T_{DSPDO_ACIN_P_MULT}$ | ACIN input to P output using multiplier | 3.65 | 4.19 | 5.00 | 5.00 | 5.00 | 6.40 | ns |
| $T_{DSPDO_ACIN_P}$ | ACIN input to P output not using multiplier | 1.37 | 1.57 | 1.88 | 1.88 | 1.88 | 2.44 | ns |
| $T_{DSPDO_ACIN_ACOUT}$ | ACIN input to ACOUT output | 0.38 | 0.44 | 0.53 | 0.53 | 0.53 | 0.63 | ns |
| $T_{DSPDO_ACIN_CARRYCASCOUT_MULT}$ | ACIN input to CARRYCASCOUT output using multiplier | 3.90 | 4.47 | 5.33 | 5.33 | 5.33 | 6.79 | ns |
| $T_{DSPDO_ACIN_CARRYCASCOUT}$ | ACIN input to CARRYCASCOUT output not using multiplier | 1.61 | 1.85 | 2.21 | 2.21 | 2.21 | 2.84 | ns |
| $T_{DSPDO_PCIN_P}$ | PCIN input to P output | 1.11 | 1.28 | 1.52 | 1.52 | 1.52 | 1.82 | ns |
| $T_{DSPDO_PCIN_CARRYCASCOUT}$ | PCIN input to CARRYCASCOUT output | 1.36 | 1.56 | 1.85 | 1.85 | 1.85 | 2.21 | ns |

*Table 31:* **DSP48E1 Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | 1.0V | | | | 0.95V | 0.9V | |
| | | -3 | -2/-2LE | -1 | -1Q/-1M | -1LI | -2LE | |
| **Clock to Outs from Output Register Clock to Output Pins** | | | | | | | | |
| $T_{DSPCKO_P_PREG}$ | CLK PREG to P output | 0.33 | 0.37 | 0.44 | 0.44 | 0.44 | 0.54 | ns |
| $T_{DSPCKO_CARRYCASCOUT_PREG}$ | CLK PREG to CARRYCASCOUT output | 0.52 | 0.59 | 0.69 | 0.69 | 0.69 | 0.84 | ns |
| **Clock to Outs from Pipeline Register Clock to Output Pins** | | | | | | | | |
| $T_{DSPCKO_P_MREG}$ | CLK MREG to P output | 1.68 | 1.93 | 2.31 | 2.31 | 2.31 | 2.73 | ns |
| $T_{DSPCKO_CARRYCASCOUT_MREG}$ | CLK MREG to CARRYCASCOUT output | 1.92 | 2.21 | 2.64 | 2.64 | 2.64 | 3.12 | ns |
| $T_{DSPCKO_P_ADREG_MULT}$ | CLK ADREG to P output using multiplier | 2.72 | 3.10 | 3.69 | 3.69 | 3.69 | 4.60 | ns |
| $T_{DSPCKO_CARRYCASCOUT_ADREG_MULT}$ | CLK ADREG to CARRYCASCOUT output using multiplier | 2.96 | 3.38 | 4.02 | 4.02 | 4.02 | 4.99 | ns |
| **Clock to Outs from Input Register Clock to Output Pins** | | | | | | | | |
| $T_{DSPCKO_P_AREG_MULT}$ | CLK AREG to P output using multiplier | 3.94 | 4.51 | 5.37 | 5.37 | 5.37 | 6.84 | ns |
| $T_{DSPCKO_P_BREG}$ | CLK BREG to P output not using multiplier | 1.64 | 1.87 | 2.22 | 2.22 | 2.22 | 2.65 | ns |
| $T_{DSPCKO_P_CREG}$ | CLK CREG to P output not using multiplier | 1.69 | 1.93 | 2.30 | 2.30 | 2.30 | 2.81 | ns |
| $T_{DSPCKO_P_DREG_MULT}$ | CLK DREG to P output using multiplier | 3.91 | 4.48 | 5.32 | 5.32 | 5.32 | 6.77 | ns |
| **Clock to Outs from Input Register Clock to Cascading Output Pins** | | | | | | | | |
| $T_{DSPCKO_\{ACOUT;\ BCOUT\}_\{AREG;\ BREG\}}$ | CLK (ACOUT, BCOUT) to {A,B} register output | 0.64 | 0.73 | 0.87 | 0.87 | 0.87 | 1.02 | ns |
| $T_{DSPCKO_CARRYCASCOUT_\{AREG,\ BREG\}_MULT}$ | CLK (AREG, BREG) to CARRYCASCOUT output using multiplier | 4.19 | 4.79 | 5.70 | 5.70 | 5.70 | 7.24 | ns |
| $T_{DSPCKO_CARRYCASCOUT_\ BREG}$ | CLK BREG to CARRYCASCOUT output not using multiplier | 1.88 | 2.15 | 2.55 | 2.55 | 2.55 | 3.04 | ns |
| $T_{DSPCKO_CARRYCASCOUT_DREG_MULT}$ | CLK DREG to CARRYCASCOUT output using multiplier | 4.16 | 4.76 | 5.65 | 5.65 | 5.65 | 7.17 | ns |
| $T_{DSPCKO_CARRYCASCOUT_\ CREG}$ | CLK CREG to CARRYCASCOUT output | 1.94 | 2.21 | 2.63 | 2.63 | 2.63 | 3.20 | ns |
| **Maximum Frequency** | | | | | | | | |
| $F_{MAX}$ | With all registers used | 628.93 | 550.66 | 464.25 | 464.25 | 464.25 | 363.77 | MHz |
| $F_{MAX_PATDET}$ | With pattern detector | 531.63 | 465.77 | 392.93 | 392.93 | 392.93 | 310.08 | MHz |
| $F_{MAX_MULT_NOMREG}$ | Two register multiply without MREG | 349.28 | 305.62 | 257.47 | 257.47 | 257.47 | 210.44 | MHz |
| $F_{MAX_MULT_NOMREG_PATDET}$ | Two register multiply without MREG with pattern detect | 317.26 | 277.62 | 233.92 | 233.92 | 233.92 | 191.28 | MHz |
| $F_{MAX_PREADD_MULT_NOADREG}$ | Without ADREG | 397.30 | 346.26 | 290.44 | 290.44 | 290.44 | 223.26 | MHz |
| $F_{MAX_PREADD_MULT_NOADREG_PATDET}$ | Without ADREG with pattern detect | 397.30 | 346.26 | 290.44 | 290.44 | 290.44 | 223.26 | MHz |

*Table 31:* **DSP48E1 Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | 1.0V | | | | 0.95V | 0.9V | |
| | | -3 | -2/-2LE | -1 | -1Q/-1M | -1LI | -2LE | |
| $F_{MAX_NOPIPELINEREG}$ | Without pipeline registers (MREG, ADREG) | 260.01 | 227.01 | 190.69 | 190.69 | 190.69 | 150.13 | MHz |
| $F_{MAX_NOPIPELINEREG_PATDET}$ | Without pipeline registers (MREG, ADREG) with pattern detect | 241.72 | 211.15 | 177.43 | 177.43 | 177.43 | 140.10 | MHz |

## Clock Buffers and Networks

*Table 32:* **Global Clock Switching Characteristics (Including BUFGCTRL)**

| Symbol | Description | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | 1.0V | | | | 0.95V | 0.9V | |
| | | -3 | -2/-2LE | -1 | -1Q/-1M | -1LI | -2LE | |
| $T_{BCCCK_CE}$/ $T_{BCCKC_CE}$(1) | CE pins setup/hold | 0.12/0.39 | 0.13/0.40 | 0.16/0.41 | 0.16/0.83 | 0.16/0.41 | 0.31/0.67 | ns |
| $T_{BCCCK_S}$/ $T_{BCCKC_S}$(1) | S pins setup/hold | 0.12/0.39 | 0.13/0.40 | 0.16/0.41 | 0.16/0.83 | 0.16/0.41 | 0.31/0.67 | ns |
| $T_{BCCKO_O}$(2) | BUFGCTRL delay from I0/I1 to O | 0.08 | 0.09 | 0.10 | 0.10 | 0.10 | 0.14 | ns |
| **Maximum Frequency** | | | | | | | | |
| $F_{MAX_BUFG}$ | Global clock tree (BUFG) | 628.00 | 628.00 | 464.00 | 464.00 | 464.00 | 394.00 | MHz |

**Notes:**

1. $T_{BCCCK_CE}$ and $T_{BCCKC_CE}$ must be satisfied to assure glitch-free operation of the global clock when switching between clocks. These parameters do not apply to the BUFGMUX primitive that assures glitch-free operation. The other global clock setup and hold times are optional; only needing to be satisfied if device operation requires simulation matches on a cycle-for-cycle basis when switching between clocks.
2. $T_{BGCKO_O}$ (BUFG delay from I0 to O) values are the same as $T_{BCCKO_O}$ values.

*Table 33:* **Input/Output Clock Switching Characteristics (BUFIO)**

| Symbol | Description | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | 1.0V | | | | 0.95V | 0.9V | |
| | | -3 | -2/-2LE | -1 | -1Q/-1M | -1LI | -2LE | |
| $T_{BIOCKO_O}$ | Clock to out delay from I to O | 1.11 | 1.26 | 1.54 | 1.54 | 1.54 | 1.56 | ns |
| **Maximum Frequency** | | | | | | | | |
| $F_{MAX_BUFIO}$ | I/O clock tree (BUFIO) | 680.00 | 680.00 | 600.00 | 600.00 | 600.00 | 600.00 | MHz |

*Table 34:* **Regional Clock Buffer Switching Characteristics (BUFR)**

| Symbol | Description | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | 1.0V | | | | 0.95V | 0.9V | |
| | | -3 | -2/-2LE | -1 | -1Q/-1M | -1LI | -2LE | |
| $T_{BRCKO_O}$ | Clock to out delay from I to O | 0.64 | 0.76 | 0.99 | 0.99 | 0.99 | 1.24 | ns |
| $T_{BRCKO_O_BYP}$ | Clock to out delay from I to O with Divide Bypass attribute set | 0.34 | 0.39 | 0.52 | 0.52 | 0.52 | 0.72 | ns |
| $T_{BRDO_O}$ | Propagation delay from CLR to O | 0.81 | 0.85 | 1.09 | 1.09 | 1.09 | 0.96 | ns |

*Table 34:* **Regional Clock Buffer Switching Characteristics (BUFR) *(Cont'd)***

| Symbol | Description | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | 1.0V | | | | 0.95V | 0.9V | |
| | | -3 | -2/-2LE | -1 | -1Q/-1M | -1LI | -2LE | |
| **Maximum Frequency** | | | | | | | | |
| $F_{MAX_BUFR}$[1] | Regional clock tree (BUFR) | 420.00 | 375.00 | 315.00 | 315.00 | 315.00 | 315.00 | MHz |

**Notes:**

1. The maximum input frequency to the BUFR and BUFMR is the BUFIO $F_{MAX}$ frequency.

*Table 35:* **Horizontal Clock Buffer Switching Characteristics (BUFH)**

| Symbol | Description | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | 1.0V | | | | 0.95V | 0.9V | |
| | | -3 | -2/-2LE | -1 | -1Q/-1M | -1LI | -2LE | |
| $T_{BHCKO_O}$ | BUFH delay from I to O | 0.10 | 0.11 | 0.13 | 0.13 | 0.13 | 0.16 | ns |
| $T_{BHCCK_CE}$/ $T_{BHCKC_CE}$ | CE pin setup and hold | 0.19/0.13 | 0.22/0.15 | 0.28/0.21 | 0.28/0.42 | 0.28/0.21 | 0.35/0.25 | ns |
| **Maximum Frequency** | | | | | | | | |
| $F_{MAX_BUFH}$ | Horizontal clock buffer (BUFH) | 628.00 | 628.00 | 464.00 | 464.00 | 464.00 | 394.00 | MHz |

*Table 36:* **Duty Cycle Distortion and Clock-Tree Skew**

| Symbol | Description | Device | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | | 0.95V | 0.9V | |
| | | | -3 | -2/-2LE | -1 | -1Q/-1M | -1LI | -2LE | |
| $T_{DCD_CLK}$ | Global clock tree duty-cycle distortion[1] | All | 0.20 | 0.20 | 0.20 | N/A | 0.20 | 0.25 | ns |
| $T_{CKSKEW}$ | Global clock tree skew[2] | XC7A12T | 0.26 | 0.26 | 0.26 | N/A | 0.26 | 0.33 | ns |
| | | XC7A15T | 0.26 | 0.26 | 0.26 | N/A | 0.26 | 0.33 | ns |
| | | XC7A25T | 0.26 | 0.26 | 0.26 | N/A | 0.26 | 0.33 | ns |
| | | XC7A35T | 0.26 | 0.26 | 0.26 | N/A | 0.26 | 0.33 | ns |
| | | XC7A50T | 0.26 | 0.26 | 0.26 | N/A | 0.26 | 0.33 | ns |
| | | XC7A75T | 0.27 | 0.33 | 0.36 | N/A | 0.36 | 0.48 | ns |
| | | XC7A100T | 0.27 | 0.33 | 0.36 | N/A | 0.36 | 0.48 | ns |
| | | XC7A200T | 0.40 | 0.48 | 0.54 | N/A | 0.54 | 0.69 | ns |
| | | XA7A12T | N/A | 0.26 | 0.26 | 0.26 | N/A | N/A | ns |
| | | XA7A15T | N/A | 0.26 | 0.26 | 0.26 | N/A | N/A | ns |
| | | XA7A25T | N/A | 0.26 | 0.26 | 0.26 | N/A | N/A | ns |
| | | XA7A35T | N/A | 0.26 | 0.26 | 0.26 | N/A | N/A | ns |
| | | XA7A50T | N/A | 0.26 | 0.26 | 0.26 | N/A | N/A | ns |
| | | XA7A75T | N/A | 0.33 | 0.36 | 0.36 | N/A | N/A | ns |
| | | XA7A100T | N/A | 0.33 | 0.36 | 0.36 | N/A | N/A | ns |
| | | XQ7A50T | N/A | 0.26 | 0.26 | 0.26 | 0.26 | N/A | ns |
| | | XQ7A100T | N/A | 0.33 | 0.36 | 0.36 | 0.36 | N/A | ns |
| | | XQ7A200T | N/A | 0.48 | 0.54 | 0.54 | 0.54 | N/A | ns |
| $T_{DCD_BUFIO}$ | I/O clock tree duty cycle distortion | All | 0.14 | 0.14 | 0.14 | 0.14 | 0.14 | 0.14 | ns |

*Table 36:* **Duty Cycle Distortion and Clock-Tree Skew *(Cont'd)***

| Symbol | Description | Device | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | | 0.95V | 0.9V | |
| | | | -3 | -2/-2LE | -1 | -1Q/-1M | -1LI | -2LE | |
| $T_{BUFIOSKEW}$ | I/O clock tree skew across one clock region | All | 0.03 | 0.03 | 0.03 | 0.03 | 0.03 | 0.03 | ns |
| $T_{DCD_BUFR}$ | Regional clock tree duty cycle distortion | All | 0.18 | 0.18 | 0.18 | 0.18 | 0.18 | 0.18 | ns |

**Notes:**

1. These parameters represent the worst-case duty cycle distortion observable at the I/O flip flops. For all I/O standards, IBIS can be used to calculate any additional duty cycle distortion that might be caused by asymmetrical rise/fall times.
2. The $T_{CKSKEW}$ value represents the worst-case clock-tree skew observable between sequential I/O elements. Significantly less clock-tree skew exists for I/O registers that are close to each other and fed by the same or adjacent clock-tree branches. Use the Xilinx Timing Analyzer tools to evaluate clock skew specific to your application.

## MMCM Switching Characteristics

*Table 37:* **MMCM Specification**

| Symbol | Description | Speed Grade | | | | | Units |
|---|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.95V | 0.9V | |
| | | -3 | -2/-2LE | -1 | -1LI | -2LE | |
| $MMCM_F_{INMAX}$ | Maximum input clock frequency | 800.00 | 800.00 | 800.00 | 800.00 | 800.00 | MHz |
| $MMCM_F_{INMIN}$ | Minimum input clock frequency | 10.00 | 10.00 | 10.00 | 10.00 | 10.00 | MHz |
| $MMCM_F_{INJITTER}$ | Maximum input clock period jitter | < 20% of clock input period or 1 ns Max | | | | | |
| $MMCM_F_{INDUTY}$ | Allowable input duty cycle: 10—49 MHz | 25 | 25 | 25 | 25 | 25 | % |
| | Allowable input duty cycle: 50—199 MHz | 30 | 30 | 30 | 30 | 30 | % |
| | Allowable input duty cycle: 200—399 MHz | 35 | 35 | 35 | 35 | 35 | % |
| | Allowable input duty cycle: 400—499 MHz | 40 | 40 | 40 | 40 | 40 | % |
| | Allowable input duty cycle: > 500 MHz | 45 | 45 | 45 | 45 | 45 | % |
| $MMCM_F_{MIN_PSCLK}$ | Minimum dynamic phase-shift clock frequency | 0.01 | 0.01 | 0.01 | 0.01 | 0.01 | MHz |
| $MMCM_F_{MAX_PSCLK}$ | Maximum dynamic phase-shift clock frequency | 550.00 | 500.00 | 450.00 | 450.00 | 450.00 | MHz |
| $MMCM_F_{VCOMIN}$ | Minimum MMCM VCO frequency | 600.00 | 600.00 | 600.00 | 600.00 | 600.00 | MHz |
| $MMCM_F_{VCOMAX}$ | Maximum MMCM VCO frequency | 1600.00 | 1440.00 | 1200.00 | 1200.00 | 1200.00 | MHz |
| $MMCM_F_{BANDWIDTH}$ | Low MMCM bandwidth at typical(1) | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 | MHz |
| | High MMCM bandwidth at typical(1) | 4.00 | 4.00 | 4.00 | 4.00 | 4.00 | MHz |
| $MMCM_T_{STATPHAOFFSET}$ | Static phase offset of the MMCM outputs(2) | 0.12 | 0.12 | 0.12 | 0.12 | 0.12 | ns |
| $MMCM_T_{OUTJITTER}$ | MMCM output jitter | Note 3 | | | | | |
| $MMCM_T_{OUTDUTY}$ | MMCM output clock duty-cycle precision(4) | 0.20 | 0.20 | 0.20 | 0.20 | 0.25 | ns |
| $MMCM_T_{LOCKMAX}$ | MMCM maximum lock time | 100.00 | 100.00 | 100.00 | 100.00 | 100.00 | µs |
| $MMCM_F_{OUTMAX}$ | MMCM maximum output frequency | 800.00 | 800.00 | 800.00 | 800.00 | 800.00 | MHz |
| $MMCM_F_{OUTMIN}$ | MMCM minimum output frequency(5)(6) | 4.69 | 4.69 | 4.69 | 4.69 | 4.69 | MHz |

*Table 37:* **MMCM Specification *(Cont'd)***

| Symbol | Description | Speed Grade | | | | | Units |
|---|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.95V | 0.9V | |
| | | -3 | -2/-2LE | -1 | -1LI | -2LE | |
| MMCM_$T_{EXTFDVAR}$ | External clock feedback variation | < 20% of clock input period or 1 ns Max | | | | | |
| MMCM_$RST_{MINPULSE}$ | Minimum reset pulse width | 5.00 | 5.00 | 5.00 | 5.00 | 5.00 | ns |
| MMCM_$F_{PFDMAX}$ | Maximum frequency at the phase frequency detector | 550.00 | 500.00 | 450.00 | 450.00 | 450.00 | MHz |
| MMCM_$F_{PFDMIN}$ | Minimum frequency at the phase frequency detector | 10.00 | 10.00 | 10.00 | 10.00 | 10.00 | MHz |
| MMCM_$T_{FBDELAY}$ | Maximum delay in the feedback path | 3 ns Max or one CLKIN cycle | | | | | |
| **MMCM Switching Characteristics Setup and Hold** | | | | | | | |
| $T_{MMCMDCK_PSEN}$/ $T_{MMCMCKD_PSEN}$ | Setup and hold of phase-shift enable | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | ns |
| $T_{MMCMDCK_PSINCDEC}$/ $T_{MMCMCKD_PSINCDEC}$ | Setup and hold of phase-shift increment/decrement | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | 1.04/0.00 | ns |
| $T_{MMCMCKO_PSDONE}$ | Phase shift clock-to-out of PSDONE | 0.59 | 0.68 | 0.81 | 0.81 | 0.78 | ns |
| **Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK** | | | | | | | |
| $T_{MMCMDCK_DADDR}$/ $T_{MMCMCKD_DADDR}$ | DADDR setup/hold | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min |
| $T_{MMCMDCK_DI}$/ $T_{MMCMCKD_DI}$ | DI setup/hold | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min |
| $T_{MMCMDCK_DEN}$/ $T_{MMCMCKD_DEN}$ | DEN setup/hold | 1.76/0.00 | 1.97/0.00 | 2.29/0.00 | 2.29/0.00 | 2.40/0.00 | ns, Min |
| $T_{MMCMDCK_DWE}$/ $T_{MMCMCKD_DWE}$ | DWE setup/hold | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min |
| $T_{MMCMCKO_DRDY}$ | CLK to out of DRDY | 0.65 | 0.72 | 0.99 | 0.99 | 0.99 | ns, Max |
| $F_{DCK}$ | DCLK frequency | 200.00 | 200.00 | 200.00 | 200.00 | 100.00 | MHz, Max |

**Notes:**

1. The MMCM does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any MMCM outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard. See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}$/128 assuming output duty cycle is 50%.
6. When CLKOUT4_CASCADE = TRUE, MMCM_$F_{OUTMIN}$ is 0.036 MHz.

## PLL Switching Characteristics

*Table 38:* **PLL Specification**

| Symbol | Description | Speed Grade | | | | | Units |
|---|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.95V | 0.9V | |
| | | -3 | -2/-2LE | -1 | -1LI | -2LE | |
| PLL_$F_{INMAX}$ | Maximum input clock frequency | 800.00 | 800.00 | 800.00 | 800.00 | 800.00 | MHz |
| PLL_$F_{INMIN}$ | Minimum input clock frequency | 19.00 | 19.00 | 19.00 | 19.00 | 19.00 | MHz |
| PLL_$F_{INJITTER}$ | Maximum input clock period jitter | < 20% of clock input period or 1 ns Max | | | | | |
| PLL_$F_{INDUTY}$ | Allowable input duty cycle: 19—49 MHz | 25 | 25 | 25 | 25 | 25 | % |
| | Allowable input duty cycle: 50—199 MHz | 30 | 30 | 30 | 30 | 30 | % |
| | Allowable input duty cycle: 200—399 MHz | 35 | 35 | 35 | 35 | 35 | % |
| | Allowable input duty cycle: 400—499 MHz | 40 | 40 | 40 | 40 | 40 | % |
| | Allowable input duty cycle: >500 MHz | 45 | 45 | 45 | 45 | 45 | % |
| PLL_$F_{VCOMIN}$ | Minimum PLL VCO frequency | 800.00 | 800.00 | 800.00 | 800.00 | 800.00 | MHz |
| PLL_$F_{VCOMAX}$ | Maximum PLL VCO frequency | 2133.00 | 1866.00 | 1600.00 | 1600.00 | 1600.00 | MHz |
| PLL_$F_{BANDWIDTH}$ | Low PLL bandwidth at typical(1) | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 | MHz |
| | High PLL bandwidth at typical(1) | 4.00 | 4.00 | 4.00 | 4.00 | 4.00 | MHz |
| PLL_$T_{STATPHAOFFSET}$ | Static phase offset of the PLL outputs(2) | 0.12 | 0.12 | 0.12 | 0.12 | 0.12 | ns |
| PLL_$T_{OUTJITTER}$ | PLL output jitter | Note 3 | | | | | |
| PLL_$T_{OUTDUTY}$ | PLL output clock duty-cycle precision(4) | 0.20 | 0.20 | 0.20 | 0.20 | 0.25 | ns |
| PLL_$T_{LOCKMAX}$ | PLL maximum lock time | 100.00 | 100.00 | 100.00 | 100.00 | 100.00 | µs |
| PLL_$F_{OUTMAX}$ | PLL maximum output frequency | 800.00 | 800.00 | 800.00 | 800.00 | 800.00 | MHz |
| PLL_$F_{OUTMIN}$ | PLL minimum output frequency(5) | 6.25 | 6.25 | 6.25 | 6.25 | 6.25 | MHz |
| PLL_$T_{EXTFDVAR}$ | External clock feedback variation | < 20% of clock input period or 1 ns Max | | | | | |
| PLL_$RST_{MINPULSE}$ | Minimum reset pulse width | 5.00 | 5.00 | 5.00 | 5.00 | 5.00 | ns |
| PLL_$F_{PFDMAX}$ | Maximum frequency at the phase frequency detector | 550.00 | 500.00 | 450.00 | 450.00 | 450.00 | MHz |
| PLL_$F_{PFDMIN}$ | Minimum frequency at the phase frequency detector | 19.00 | 19.00 | 19.00 | 19.00 | 19.00 | MHz |
| PLL_$T_{FBDELAY}$ | Maximum delay in the feedback path | 3 ns Max or one CLKIN cycle | | | | | |
| **Dynamic Reconfiguration Port (DRP) for PLL Before and After DCLK** | | | | | | | |
| $T_{PLLDCK_DADDR}$/ $T_{PLLCKD_DADDR}$ | Setup and hold of D address | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min |
| $T_{PLLDCK_DI}$/ $T_{PLLCKD_DI}$ | Setup and hold of D input | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min |
| $T_{PLLDCK_DEN}$/ $T_{PLLCKD_DEN}$ | Setup and hold of D enable | 1.76/0.00 | 1.97/0.00 | 2.29/0.00 | 2.29/0.00 | 2.40/0.00 | ns, Min |
| $T_{PLLDCK_DWE}$/ $T_{PLLCKD_DWE}$ | Setup and hold of D write enable | 1.25/0.15 | 1.40/0.15 | 1.63/0.15 | 1.63/0.15 | 1.43/0.00 | ns, Min |
| $T_{PLLCKO_DRDY}$ | CLK to out of DRDY | 0.65 | 0.72 | 0.99 | 0.99 | 0.99 | ns, Max |

*Table 38:* **PLL Specification *(Cont'd)***

| Symbol | Description | Speed Grade | | | | | Units |
|---|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.95V | 0.9V | |
| | | -3 | -2/-2LE | -1 | -1LI | -2LE | |
| $F_{DCK}$ | DCLK frequency | 200.00 | 200.00 | 200.00 | 200.00 | 100.00 | MHz, Max |

**Notes:**

1. The PLL does not filter typical spread-spectrum input clocks because they are usually far below the bandwidth filter frequencies.
2. The static offset is measured between any PLL outputs with identical phase.
3. Values for this parameter are available in the Clocking Wizard. See http://www.xilinx.com/products/intellectual-property/clocking_wizard.htm.
4. Includes global clock buffer.
5. Calculated as $F_{VCO}/128$ assuming output duty cycle is 50%.

## Device Pin-to-Pin Output Parameter Guidelines

*Table 39:* **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Near Clock Region)(1)**

| Symbol | Description | Device | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | | 0.95V | 0.9V | |
| | | | -3 | -2/-2LE | -1 | -1M/-1Q | -1LI | -2LE | |
| SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM/PLL. | | | | | | | | | |
| $T_{ICKOF}$ | Clock-capable clock input and OUTFF at pins/banks closest to the BUFGs *without* MMCM/PLL (near clock region)(2) | XC7A12T | 4.97 | 5.55 | 6.44 | N/A | 6.44 | 7.38 | ns |
| | | XC7A15T | 5.10 | 5.70 | 6.61 | N/A | 6.61 | 7.56 | ns |
| | | XC7A25T | 4.97 | 5.55 | 6.44 | N/A | 6.44 | 7.38 | ns |
| | | XC7A35T | 5.10 | 5.70 | 6.61 | N/A | 6.61 | 7.56 | ns |
| | | XC7A50T | 5.10 | 5.70 | 6.61 | N/A | 6.61 | 7.56 | ns |
| | | XC7A75T | 5.14 | 5.74 | 6.72 | N/A | 6.72 | 7.62 | ns |
| | | XC7A100T | 5.14 | 5.74 | 6.72 | N/A | 6.72 | 7.62 | ns |
| | | XC7A200T | 5.47 | 6.11 | 7.16 | N/A | 7.16 | 8.08 | ns |
| | | XA7A12T | N/A | 5.55 | 6.44 | 6.44 | N/A | N/A | ns |
| | | XA7A15T | N/A | 5.70 | 6.61 | 6.61 | N/A | N/A | ns |
| | | XA7A25T | N/A | 5.55 | 6.44 | 6.44 | N/A | N/A | ns |
| | | XA7A35T | N/A | 5.70 | 6.61 | 6.61 | N/A | N/A | ns |
| | | XA7A50T | N/A | 5.70 | 6.61 | 6.61 | N/A | N/A | ns |
| | | XA7A75T | N/A | 5.74 | 6.72 | 6.72 | N/A | N/A | ns |
| | | XA7A100T | N/A | 5.74 | 6.72 | 6.72 | N/A | N/A | ns |
| | | XQ7A50T | N/A | 5.70 | 6.61 | 6.61 | 6.61 | N/A | ns |
| | | XQ7A100T | N/A | 5.74 | 6.72 | 6.72 | 6.72 | N/A | ns |
| | | XQ7A200T | N/A | 6.11 | 7.16 | 7.16 | 7.16 | N/A | ns |

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Refer to the Die Level Bank Numbering Overview section of *7 Series FPGA Packaging and Pinout Specification* (UG475).

*Table 40:* **Clock-Capable Clock Input to Output Delay Without MMCM/PLL (Far Clock Region)[1]**

| Symbol | Description | Device | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | | 0.95V | 0.9V | |
| | | | -3 | -2/-2LE | -1 | -1M/-1Q | -1LI | -2LE | |
| SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *without* MMCM/PLL. | | | | | | | | | |
| $T_{ICKOFFAR}$ | Clock-capable clock input and OUTFF at pins/banks farthest from the BUFGs *without* MMCM/PLL (far clock region)[2] | XC7A12T | 4.97 | 5.55 | 6.44 | N/A | 6.44 | 7.38 | ns |
| | | XC7A15T | 5.10 | 5.70 | 6.61 | N/A | 6.61 | 7.57 | ns |
| | | XC7A25T | 4.97 | 5.55 | 6.44 | N/A | 6.44 | 7.38 | ns |
| | | XC7A35T | 5.10 | 5.70 | 6.61 | N/A | 6.61 | 7.57 | ns |
| | | XC7A50T | 5.10 | 5.70 | 6.61 | N/A | 6.61 | 7.57 | ns |
| | | XC7A75T | 5.38 | 6.01 | 7.02 | N/A | 7.02 | 7.94 | ns |
| | | XC7A100T | 5.38 | 6.01 | 7.02 | N/A | 7.02 | 7.94 | ns |
| | | XC7A200T | 6.17 | 6.89 | 8.05 | N/A | 8.05 | 9.03 | ns |
| | | XA7A12T | N/A | 5.55 | 6.44 | 6.44 | N/A | N/A | ns |
| | | XA7A15T | N/A | 5.70 | 6.61 | 6.61 | N/A | N/A | ns |
| | | XA7A25T | N/A | 5.55 | 6.44 | 6.44 | N/A | N/A | ns |
| | | XA7A35T | N/A | 5.70 | 6.61 | 6.61 | N/A | N/A | ns |
| | | XA7A50T | N/A | 5.70 | 6.61 | 6.61 | N/A | N/A | ns |
| | | XA7A75T | N/A | 6.01 | 7.02 | 7.02 | N/A | N/A | ns |
| | | XA7A100T | N/A | 6.01 | 7.02 | 7.02 | N/A | N/A | ns |
| | | XQ7A50T | N/A | 5.70 | 6.61 | 6.61 | 6.61 | N/A | ns |
| | | XQ7A100T | N/A | 6.01 | 7.02 | 7.02 | 7.02 | N/A | ns |
| | | XQ7A200T | N/A | 6.89 | 8.05 | 8.05 | 8.05 | N/A | ns |

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Refer to the Die Level Bank Numbering Overview section of *7 Series FPGA Packaging and Pinout Specification* (UG475).

*Table 41:* **Clock-Capable Clock Input to Output Delay With MMCM**

| Symbol | Description | Device | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | | 0.95V | 0.9V | |
| | | | -3 | -2/-2LE | -1 | -1M/-1Q | -1LI | -2LE | |
| SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* MMCM. | | | | | | | | | |
| $T_{ICKOFMMCMCC}$ | Clock-capable clock input and OUTFF *with* MMCM | XC7A12T | 1.00 | 1.00 | 1.00 | N/A | 1.00 | 1.78 | ns |
| | | XC7A15T | 1.00 | 1.00 | 1.00 | N/A | 1.00 | 1.78 | ns |
| | | XC7A25T | 1.00 | 1.00 | 1.00 | N/A | 1.00 | 1.78 | ns |
| | | XC7A35T | 1.00 | 1.00 | 1.00 | N/A | 1.00 | 1.78 | ns |
| | | XC7A50T | 1.00 | 1.00 | 1.00 | N/A | 1.00 | 1.78 | ns |
| | | XC7A75T | 1.00 | 1.00 | 1.00 | N/A | 1.00 | 1.79 | ns |
| | | XC7A100T | 1.00 | 1.00 | 1.00 | N/A | 1.00 | 1.79 | ns |
| | | XC7A200T | 1.01 | 1.02 | 1.04 | N/A | 1.04 | 1.84 | ns |
| | | XA7A12T | N/A | 1.00 | 1.00 | 1.00 | N/A | N/A | ns |
| | | XA7A15T | N/A | 1.00 | 1.00 | 1.00 | N/A | N/A | ns |
| | | XA7A25T | N/A | 1.00 | 1.00 | 1.00 | N/A | N/A | ns |
| | | XA7A35T | N/A | 1.00 | 1.00 | 1.00 | N/A | N/A | ns |
| | | XA7A50T | N/A | 1.00 | 1.00 | 1.00 | N/A | N/A | ns |
| | | XA7A75T | N/A | 1.00 | 1.00 | 1.00 | N/A | N/A | ns |
| | | XA7A100T | N/A | 1.00 | 1.00 | 1.00 | N/A | N/A | ns |
| | | XQ7A50T | N/A | 1.00 | 1.00 | 1.00 | 1.00 | N/A | ns |
| | | XQ7A100T | N/A | 1.00 | 1.00 | 1.00 | 1.00 | N/A | ns |
| | | XQ7A200T | N/A | 1.02 | 1.04 | 1.04 | 1.04 | N/A | ns |

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. MMCM output jitter is already included in the timing calculation.

*Table 42:* **Clock-Capable Clock Input to Output Delay With PLL**

| Symbol | Description | Device | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | | 0.95V | 0.9V | |
| | | | -3 | -2/-2LE | -1 | -1M/-1Q | -1LI | -2LE | |
| SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, *with* PLL. | | | | | | | | | |
| $T_{ICKOFPLLCC}$ | Clock-capable clock input and OUTFF *with* PLL | XC7A12T | 0.83 | 0.83 | 0.83 | N/A | 0.83 | 1.38 | ns |
| | | XC7A15T | 0.82 | 0.82 | 0.82 | N/A | 0.82 | 1.39 | ns |
| | | XC7A25T | 0.83 | 0.83 | 0.83 | N/A | 0.83 | 1.38 | ns |
| | | XC7A35T | 0.82 | 0.82 | 0.82 | N/A | 0.82 | 1.39 | ns |
| | | XC7A50T | 0.82 | 0.82 | 0.82 | N/A | 0.82 | 1.39 | ns |
| | | XC7A75T | 0.82 | 0.82 | 0.82 | N/A | 0.82 | 1.40 | ns |
| | | XC7A100T | 0.82 | 0.82 | 0.82 | N/A | 0.82 | 1.40 | ns |
| | | XC7A200T | 0.81 | 0.81 | 0.81 | N/A | 0.81 | 1.45 | ns |
| | | XA7A12T | N/A | 0.83 | 0.83 | 0.83 | N/A | N/A | ns |
| | | XA7A15T | N/A | 0.82 | 0.82 | 0.82 | N/A | N/A | ns |
| | | XA7A25T | N/A | 0.83 | 0.83 | 0.83 | N/A | N/A | ns |
| | | XA7A35T | N/A | 0.82 | 0.82 | 0.82 | N/A | N/A | ns |
| | | XA7A50T | N/A | 0.82 | 0.82 | 0.82 | N/A | N/A | ns |
| | | XA7A75T | N/A | 0.82 | 0.82 | 0.82 | N/A | N/A | ns |
| | | XA7A100T | N/A | 0.82 | 0.82 | 0.82 | N/A | N/A | ns |
| | | XQ7A50T | N/A | 0.82 | 0.82 | 0.82 | 0.82 | N/A | ns |
| | | XQ7A100T | N/A | 0.82 | 0.82 | 0.82 | 0.82 | N/A | ns |
| | | XQ7A200T | N/A | 0.81 | 0.81 | 0.81 | 0.81 | N/A | ns |

**Notes:**

1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. PLL output jitter is already included in the timing calculation.

*Table 43:* **Pin-to-Pin, Clock-to-Out using BUFIO**

| Symbol | Description | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | 1.0V | | | | 0.95V | 0.9V | |
| | | -3 | -2/-2LE | -1 | -1M/-1Q | -1LI | -2LE | |
| SSTL15 Clock-Capable Clock Input to Output Delay using Output Flip-Flop, Fast Slew Rate, with BUFIO. | | | | | | | | |
| $T_{ICKOFCS}$ | Clock to out of I/O clock | 5.01 | 5.61 | 6.64 | 6.64 | 6.64 | 7.32 | ns |

## Device Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Values are expressed in nanoseconds unless otherwise noted.

*Table 44:* **Global Clock Input Setup and Hold Without MMCM/PLL with ZHOLD_DELAY on HR I/O Banks**

| Symbol | Description | Device | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | | 0.95V | 0.9V | |
| | | | -3 | -2/-2LE | -1 | -1M/-1Q | -1LI | -2LE | |
| Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1) | | | | | | | | | |
| $T_{PSFD}$/ $T_{PHFD}$ | Full delay (legacy delay or default delay) global clock input and IFF(2) without MMCM/PLL with ZHOLD_DELAY on HR I/O banks | XC7A12T | 2.49/–0.37 | 2.67/–0.37 | 3.12/–0.37 | N/A | 3.12/–0.37 | 5.13/–0.54 | ns |
| | | XC7A15T | 2.47/–0.29 | 2.65/–0.29 | 3.10/–0.29 | N/A | 3.10/–0.29 | 5.10/–0.44 | ns |
| | | XC7A25T | 2.49/–0.37 | 2.67/–0.37 | 3.12/–0.37 | N/A | 3.12/–0.37 | 5.13/–0.54 | ns |
| | | XC7A35T | 2.47/–0.29 | 2.65/–0.29 | 3.10/–0.29 | N/A | 3.10/–0.29 | 5.10/–0.44 | ns |
| | | XC7A50T | 2.47/–0.29 | 2.65/–0.29 | 3.10/–0.29 | N/A | 3.10/–0.29 | 5.10/–0.44 | ns |
| | | XC7A75T | 2.69/–0.34 | 2.89/–0.34 | 3.34/–0.34 | N/A | 3.34/–0.34 | 5.66/–0.51 | ns |
| | | XC7A100T | 2.69/–0.34 | 2.89/–0.34 | 3.34/–0.34 | N/A | 3.34/–0.34 | 5.66/–0.51 | ns |
| | | XC7A200T | 3.03/–0.36 | 3.27/–0.36 | 3.79/–0.36 | N/A | 3.79/–0.36 | 6.66/–0.55 | ns |
| | | XA7A12T | N/A | 2.67/–0.37 | 3.12/–0.37 | 3.12/–0.37 | N/A | N/A | ns |
| | | XA7A15T | N/A | 2.65/–0.29 | 3.10/–0.29 | 3.10/–0.29 | N/A | N/A | ns |
| | | XA7A25T | N/A | 2.67/–0.37 | 3.12/–0.37 | 3.12/–0.37 | N/A | N/A | ns |
| | | XA7A35T | N/A | 2.65/–0.29 | 3.10/–0.29 | 3.10/–0.29 | N/A | N/A | ns |
| | | XA7A50T | N/A | 2.65/–0.29 | 3.10/–0.29 | 3.10/–0.29 | N/A | N/A | ns |
| | | XA7A75T | N/A | 2.89/–0.34 | 3.34/–0.34 | 3.34/–0.34 | N/A | N/A | ns |
| | | XA7A100T | N/A | 2.89/–0.34 | 3.34/–0.34 | 3.34/–0.34 | N/A | N/A | ns |
| | | XQ7A50T | N/A | 2.65/–0.29 | 3.10/–0.29 | 3.10/–0.29 | 3.10/–0.29 | N/A | ns |
| | | XQ7A100T | N/A | 2.89/–0.34 | 3.34/–0.34 | 3.34/–0.34 | 3.34/–0.34 | N/A | ns |
| | | XQ7A200T | N/A | 3.27/–0.36 | 3.79/–0.36 | 3.79/–0.36 | 3.79/–0.36 | N/A | ns |

**Notes:**

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch.

*Table 45:* **Clock-Capable Clock Input Setup and Hold With MMCM**

| Symbol | Description | Device | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | | 0.95V | 0.9V | |
| | | | -3 | -2/-2LE | -1 | -1M/-1Q | -1LI | -2LE | |
| Input Setup and Hold Time Relative to Global Clock Input Signal for SSTL15 Standard.(1) | | | | | | | | | |
| $T_{PSMMCMCC}$/ $T_{PHMMCMCC}$ | No delay clock-capable clock input and IFF(2) with MMCM | XC7A12T | 2.37/–0.61 | 2.69/–0.61 | 3.21/–0.61 | N/A | 3.21/–0.61 | 2.00/–0.47 | ns |
| | | XC7A15T | 2.46/–0.62 | 2.80/–0.62 | 3.35/–0.62 | N/A | 3.35/–0.62 | 2.14/–0.48 | ns |
| | | XC7A25T | 2.37/–0.61 | 2.69/–0.61 | 3.21/–0.61 | N/A | 3.21/–0.61 | 2.00/–0.47 | ns |
| | | XC7A35T | 2.46/–0.62 | 2.80/–0.62 | 3.35/–0.62 | N/A | 3.35/–0.62 | 2.14/–0.48 | ns |
| | | XC7A50T | 2.46/–0.62 | 2.80/–0.62 | 3.35/–0.62 | N/A | 3.35/–0.62 | 2.14/–0.48 | ns |
| | | XC7A75T | 2.47/–0.62 | 2.81/–0.62 | 3.36/–0.62 | N/A | 3.36/–0.62 | 2.15/–0.48 | ns |
| | | XC7A100T | 2.47/–0.62 | 2.81/–0.62 | 3.36/–0.62 | N/A | 3.36/–0.62 | 2.15/–0.48 | ns |
| | | XC7A200T | 2.59/–0.63 | 2.95/–0.63 | 3.52/–0.63 | N/A | 3.52/–0.63 | 2.32/–0.51 | ns |
| | | XA7A12T | N/A | 2.69/–0.61 | 3.21/–0.61 | 3.21/–0.61 | N/A | N/A | ns |
| | | XA7A15T | N/A | 2.80/–0.62 | 3.35/–0.62 | 3.35/–0.62 | N/A | N/A | ns |
| | | XA7A25T | N/A | 2.69/–0.61 | 3.21/–0.61 | 3.21/–0.61 | N/A | N/A | ns |
| | | XA7A35T | N/A | 2.80/–0.62 | 3.35/–0.62 | 3.35/–0.62 | N/A | N/A | ns |
| | | XA7A50T | N/A | 2.80/–0.62 | 3.35/–0.62 | 3.35/–0.62 | N/A | N/A | ns |
| | | XA7A75T | N/A | 2.81/–0.62 | 3.36/–0.62 | 3.36/–0.62 | N/A | N/A | ns |
| | | XA7A100T | N/A | 2.81/–0.62 | 3.36/–0.62 | 3.36/–0.62 | N/A | N/A | ns |
| | | XQ7A50T | N/A | 2.80/–0.62 | 3.35/–0.62 | 3.35/–0.62 | 3.35/–0.62 | N/A | ns |
| | | XQ7A100T | N/A | 2.81/–0.62 | 3.36/–0.62 | 3.36/–0.62 | 3.36/–0.62 | N/A | ns |
| | | XQ7A200T | N/A | 2.95/–0.63 | 3.52/–0.63 | 3.52/–0.63 | 3.52/–0.63 | N/A | ns |

**Notes:**

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

*Table 46:* **Clock-Capable Clock Input Setup and Hold With PLL**

| Symbol | Description | Device | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | | 0.95V | 0.9V | |
| | | | -3 | -2/-2LE | -1 | -1M/-1Q | -1LI | -2LE | |
| Input Setup and Hold Time Relative to Clock-Capable Clock Input Signal for SSTL15 Standard.(1) | | | | | | | | | |
| $T_{PSPLLCC}$/ $T_{PHPLLCC}$ | No delay clock-capable clock input and IFF(2) with PLL | XC7A12T | 2.68/–0.19 | 3.04/–0.19 | 3.64/–0.19 | N/A | 3.64/–0.19 | 2.32/–0.57 | ns |
| | | XC7A15T | 2.77/–0.20 | 3.15/–0.20 | 3.77/–0.20 | N/A | 3.77/–0.20 | 2.46/–0.59 | ns |
| | | XC7A25T | 2.68/–0.19 | 3.04/–0.19 | 3.64/–0.19 | N/A | 3.64/–0.19 | 2.32/–0.57 | ns |
| | | XC7A35T | 2.77/–0.20 | 3.15/–0.20 | 3.77/–0.20 | N/A | 3.77/–0.20 | 2.46/–0.59 | ns |
| | | XC7A50T | 2.77/–0.20 | 3.15/–0.20 | 3.77/–0.20 | N/A | 3.77/–0.20 | 2.46/–0.59 | ns |
| | | XC7A75T | 2.78/–0.20 | 3.15/–0.20 | 3.78/–0.20 | N/A | 3.78/–0.20 | 2.47/–0.59 | ns |
| | | XC7A100T | 2.78/–0.20 | 3.15/–0.20 | 3.78/–0.20 | N/A | 3.78/–0.20 | 2.47/–0.59 | ns |
| | | XC7A200T | 2.91/–0.21 | 3.29/–0.21 | 3.94/–0.21 | N/A | 3.94/–0.21 | 2.64/–0.62 | ns |
| | | XA7A12T | N/A | 3.04/–0.19 | 3.64/–0.19 | 3.64/–0.19 | N/A | N/A | ns |
| | | XA7A15T | N/A | 3.15/–0.20 | 3.77/–0.20 | 3.77/–0.20 | N/A | N/A | ns |
| | | XA7A25T | N/A | 3.04/–0.19 | 3.64/–0.19 | 3.64/–0.19 | N/A | N/A | ns |
| | | XA7A35T | N/A | 3.15/–0.20 | 3.77/–0.20 | 3.77/–0.20 | N/A | N/A | ns |
| | | XA7A50T | N/A | 3.15/–0.20 | 3.77/–0.20 | 3.77/–0.20 | N/A | N/A | ns |
| | | XA7A75T | N/A | 3.15/–0.20 | 3.78/–0.20 | 3.78/–0.20 | N/A | N/A | ns |
| | | XA7A100T | N/A | 3.15/–0.20 | 3.78/–0.20 | 3.78/–0.20 | N/A | N/A | ns |
| | | XQ7A50T | N/A | 3.15/–0.20 | 3.77/–0.20 | 3.77/–0.20 | 3.77/–0.20 | N/A | ns |
| | | XQ7A100T | N/A | 3.15/–0.20 | 3.78/–0.20 | 3.78/–0.20 | 3.78/–0.20 | N/A | ns |
| | | XQ7A200T | N/A | 3.29/–0.21 | 3.94/–0.21 | 3.94/–0.21 | 3.94/–0.21 | N/A | ns |

**Notes:**

1. Setup and hold times are measured over worst case conditions (process, voltage, temperature). Setup time is measured relative to the global clock input signal using the slowest process, highest temperature, and lowest voltage. Hold time is measured relative to the global clock input signal using the fastest process, lowest temperature, and highest voltage.
2. IFF = Input flip-flop or latch
3. Use IBIS to determine any duty-cycle distortion incurred using various standards.

*Table 47:* **Data Input Setup and Hold Times Relative to a Forwarded Clock Input Pin Using BUFIO**

| Symbol | Description | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | 1.0V | | | | 0.95V | 0.9V | |
| | | -3 | -2/-2LE | -1 | -1M/-1Q | -1LI | -2LE | |
| Input Setup and Hold Time Relative to a Forwarded Clock Input Pin Using BUFIO for SSTL15 Standard. | | | | | | | | |
| $T_{PSCS}$/$T_{PHCS}$ | Setup and hold of I/O clock | –0.38/1.31 | –0.38/1.46 | –0.38/1.76 | –0.38/1.76 | –0.38/1.76 | –0.16/1.89 | ns |

*Table 48:* **Sample Window**

| Symbol | Description | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | 1.0V | | | | 0.95V | 0.9V | |
| | | -3 | -2/-2LE | -1 | -1M/-1Q | -1LI | -2LE | |
| $T_{SAMP}$ | Sampling error at receiver pins(1) | 0.59 | 0.64 | 0.70 | 0.70 | 0.70 | 0.70 | ns |

*Table 48:* **Sample Window *(Cont'd)***

| Symbol | Description | Speed Grade | | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | 1.0V | | | | 0.95V | 0.9V | |
| | | -3 | -2/-2LE | -1 | -1M/-1Q | -1LI | -2LE | |
| $T_{SAMP_BUFIO}$ | Sampling error at receiver pins using BUFIO[2] | 0.35 | 0.40 | 0.46 | 0.46 | 0.46 | 0.46 | ns |

**Notes:**

1. This parameter indicates the total sampling error of the Artix-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the MMCM to capture the DDR input registers' edges of operation. These measurements include:
   - CLK0 MMCM jitter
   - MMCM accuracy (phase offset)
   - MMCM phase shift resolution

   These measurements do not include package or clock tree skew.
2. This parameter indicates the total sampling error of the Artix-7 FPGAs DDR input registers, measured across voltage, temperature, and process. The characterization methodology uses the BUFIO clock network and IDELAY to capture the DDR input registers' edges of operation. These measurements do not include package or clock tree skew.

## Additional Package Parameter Guidelines

The parameters in this section provide the necessary values for calculating timing budgets for Artix-7 FPGA clock transmitter and receiver data-valid windows.

*Table 49:* **Package Skew**

| Symbol | Description | Device | Package | Value | Units |
|---|---|---|---|---|---|
| $T_{PKGSKEW}$ | Package skew[1] | XC7A12T | CPG238 | 55 | ps |
| | | | CSG325 | 76 | ps |
| | | XC7A15T | CPG236 | 48 | ps |
| | | | CSG324 | 104 | ps |
| | | | CSG325 | 142 | ps |
| | | | FTG256 | 98 | ps |
| | | | FGG484 | 97 | ps |
| | | XC7A25T | CPG238 | 55 | ps |
| | | | CSG325 | 76 | ps |
| | | XC7A35T | CPG236 | 48 | ps |
| | | | CSG324 | 104 | ps |
| | | | CSG325 | 142 | ps |
| | | | FTG256 | 98 | ps |
| | | | FGG484 | 97 | ps |
| | | XC7A50T | CPG236 | 48 | ps |
| | | | CSG324 | 104 | ps |
| | | | CSG325 | 142 | ps |
| | | | FTG256 | 98 | ps |
| | | | FGG484 | 97 | ps |
| | | XC7A75T | CSG324 | 113 | ps |
| | | | FTG256 | 120 | ps |
| | | | FGG484 | 144 | ps |
| | | | FGG676 | 153 | ps |

*Table 49:* **Package Skew *(Cont'd)***

| Symbol | Description | Device | Package | Value | Units |
|---|---|---|---|---|---|
| $T_{PKGSKEW}$ | Package skew(1) | XC7A100T | CSG324 | 113 | ps |
| | | | FTG256 | 120 | ps |
| | | | FGG484 | 144 | ps |
| | | | FGG676 | 153 | ps |
| | | XC7A200T | SBG484 | 111 | ps |
| | | | FBG484 | 109 | ps |
| | | | FBG676 | 121 | ps |
| | | | FFG1156 | 151 | ps |
| | | XA7A12T | CSG325 | 76 | ps |
| | | | CPG238 | 55 | ps |
| | | XA7A15T | CPG236 | 48 | ps |
| | | | CSG324 | 104 | ps |
| | | | CSG325 | 142 | ps |
| | | XA7A25T | CSG325 | 76 | ps |
| | | | CPG238 | 55 | ps |
| | | XA7A35T | CPG236 | 48 | ps |
| | | | CSG324 | 104 | ps |
| | | | CSG325 | 142 | ps |
| | | XA7A50T | CPG236 | 48 | ps |
| | | | CSG324 | 104 | ps |
| | | | CSG325 | 142 | ps |
| | | XA7A75T | CSG324 | 113 | ps |
| | | | FGG484 | 144 | ps |
| | | XA7A100T | CSG324 | 113 | ps |
| | | | FGG484 | 144 | ps |
| | | XQ7A50T | CS325 | 142 | ps |
| | | | FG484 | 97 | ps |
| | | XQ7A100T | CS324 | 113 | ps |
| | | | FG484 | 144 | ps |
| | | XQ7A200T | RS484 | 111 | ps |
| | | | RB484 | 109 | ps |
| | | | RB676 | 121 | ps |

**Notes:**

1. These values represent the worst-case skew between any two SelectIO resources in the package: shortest delay to longest delay from die pad to ball.
2. Package delay information is available for these device/package combinations. This information can be used to deskew the package.

# GTP Transceiver Specifications

## GTP Transceiver DC Input and Output Levels

Table 50 summarizes the DC output specifications of the GTP transceivers in Artix-7 FPGAs. Consult *7 Series FPGAs GTP Transceiver User Guide* (UG482) for further details.

*Table 50:* **GTP Transceiver DC Specifications**

| Symbol | DC Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $DV_{PPOUT}$ | Differential peak-to-peak output voltage(1) | Transmitter output swing is set to maximum setting | 1000 | – | – | mV |
| $V_{CMOUTDC}$ | DC common mode output voltage | Equation based | $V_{MGTAVTT} - DV_{PPOUT}/4$ | | | mV |
| $R_{OUT}$ | Differential output resistance | | – | 100 | – | Ω |
| $V_{CMOUTAC}$ | Common mode output voltage: AC coupled | | 1/2 $V_{MGTAVTT}$ | | | mV |
| $T_{OSKEW}$ | Transmitter output pair (TXP and TXN) intra-pair skew (FF, FB, SB packages) | | – | – | 10 | ps |
| | Transmitter output pair (TXP and TXN) intra-pair skew (FG, FT, CS, CP packages) | | – | – | 12 | ps |
| $DV_{PPIN}$ | Differential peak-to-peak input voltage | External AC coupled | 150 | – | 2000 | mV |
| $V_{IN}$ | Single-ended input voltage(2) | DC coupled $V_{MGTAVTT}$ = 1.2V | –200 | – | $V_{MGTAVTT}$ | mV |
| $V_{CMIN}$ | Common mode input voltage | DC coupled $V_{MGTAVTT}$ = 1.2V | – | 2/3 $V_{MGTAVTT}$ | – | mV |
| $R_{IN}$ | Differential input resistance | | – | 100 | – | Ω |
| $C_{EXT}$ | Recommended external AC coupling capacitor(3) | | – | 100 | – | nF |

**Notes:**

1. The output swing and preemphasis levels are programmable using the attributes discussed in *7 Series FPGAs GTP Transceiver User Guide* (UG482) and can result in values lower than reported in this table.
2. Voltage measured at the pin referenced to ground.
3. Other values can be used as appropriate to conform to specific protocols and standards.

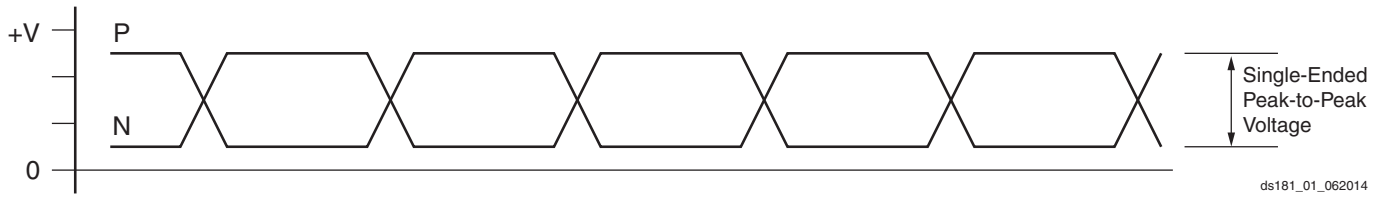



*Figure 3:* **Single-Ended Peak-to-Peak Voltage**

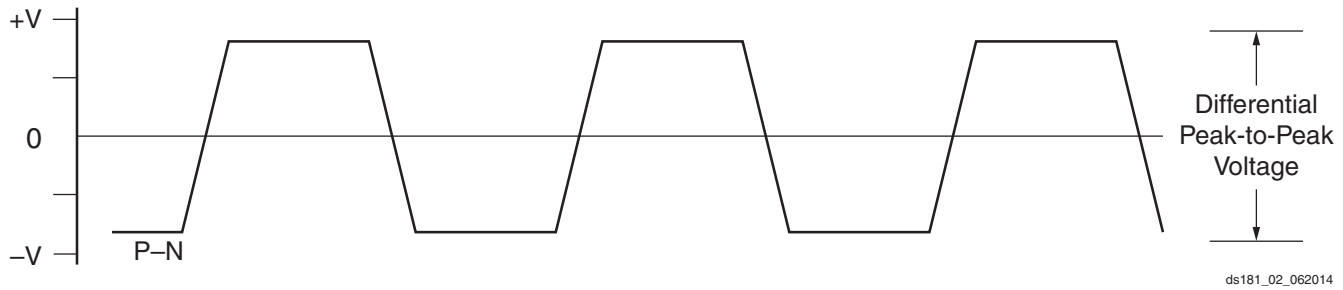



*Figure 4:* **Differential Peak-to-Peak Voltage**

***Note:*** In Figure 4, differential peak-to-peak voltage = single-ended peak-to-peak voltage x 2.

Table 51 summarizes the DC specifications of the clock input of the GTP transceiver. Consult *7 Series FPGAs GTP Transceiver User Guide* (UG482) for further details.

*Table 51:* **GTP Transceiver Clock DC Input Level Specification**

| Symbol | DC Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $V_{IDIFF}$ | Differential peak-to-peak input voltage | 350 | – | 2000 | mV |
| $R_{IN}$ | Differential input resistance | – | 100 | – | Ω |
| $C_{EXT}$ | Required external AC coupling capacitor | – | 100 | – | nF |

## GTP Transceiver Switching Characteristics

Consult *7 Series FPGAs GTP Transceiver User Guide* (UG482) for further information.

*Table 52:* **GTP Transceiver Performance**

| Symbol | Description | Output Divider | Speed Grade | | | | | | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | -3 (1.0V) | | -2 (1.0V) -2LE (1.0V) | | -1 (1.0V) -1LI (0.95V) -1Q (1.0V) -1M (1.0V) | | -2LE (0.9V) | | |
| | | | Package Type | | | | | | | | |
| | | | FF FB SB | FG FT CS CP | FF FB SB RB RS | FG FT CS CP | FF FB SB RB RS | FG FT CS CP | FF FB SB | FG FT CS CP | |
| $F_{GTPMAX}$ | Maximum GTP transceiver data rate | | 6.6 | 6.25 | 6.6 | 6.25 | 3.75 | 3.75 | 3.75 | 3.75 | Gb/s |
| $F_{GTPMIN}$ | Minimum GTP transceiver data rate | | 0.500 | 0.500 | 0.500 | 0.500 | 0.500 | 0.500 | 0.500 | 0.500 | Gb/s |
| $F_{GTPRANGE}$ | PLL line rate range | 1 | 3.2–6.6 | | 3.2–6.6 | | 3.2–3.75 | | 3.2–3.75 | | Gb/s |
| | | 2 | 1.6–3.3 | | 1.6–3.3 | | 1.6–3.2 | | 1.6–3.2 | | Gb/s |
| | | 4 | 0.8–1.65 | | 0.8–1.65 | | 0.8–1.6 | | 0.8–1.6 | | Gb/s |
| | | 8 | 0.5–0.825 | | 0.5–0.825 | | 0.5–0.8 | | 0.5–0.8 | | Gb/s |
| $F_{GTPPLLRANGE}$ | GTP transceiver PLL frequency range | | 1.6–3.3 | | 1.6–3.3 | | 1.6–3.3 | | 1.6–3.3 | | GHz |

*Table 53:* **GTP Transceiver Dynamic Reconfiguration Port (DRP) Switching Characteristics**

| Symbol | Description | Speed Grade | | | | | Units |
|---|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.95V | 0.9V | |
| | | -3 | -2/-2LE | -1 | -1LI | -2LE | |
| $F_{GTPDRPCLK}$ | GTPDRPCLK maximum frequency | 175 | 175 | 156 | 156 | 125 | MHz |

*Table 54:* **GTP Transceiver Reference Clock Switching Characteristics**

| Symbol | Description | Conditions | All Speed Grades | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $F_{GCLK}$ | Reference clock frequency range | | 60 | – | 660 | MHz |
| $T_{RCLK}$ | Reference clock rise time | 20% – 80% | – | 200 | – | ps |
| $T_{FCLK}$ | Reference clock fall time | 80% – 20% | – | 200 | – | ps |
| $T_{DCREF}$ | Reference clock duty cycle | Transceiver PLL only | 40 | – | 60 | % |

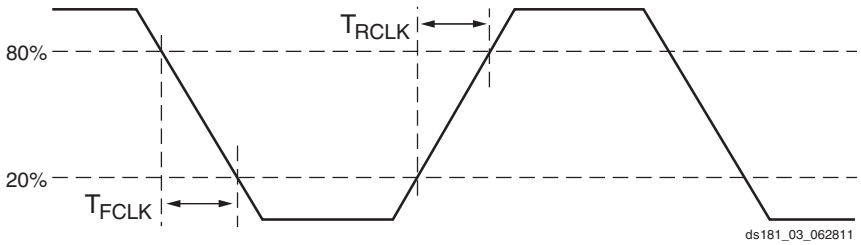



*Figure 5:* **Reference Clock Timing Parameters**

*Table 55:* **GTP Transceiver PLL/Lock Time Adaptation**

| Symbol | Description | Conditions | All Speed Grades | | | Units |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $T_{LOCK}$ | Initial PLL lock | | – | – | 1 | ms |
| $T_{DLOCK}$ | Clock recovery phase acquisition and adaptation time. | After the PLL is locked to the reference clock, this is the time it takes to lock the clock data recovery (CDR) to the data present at the input. | – | 50,000 | $2.3 \times 10^6$ | UI |

*Table 56:* **GTP Transceiver User Clock Switching Characteristics(1)**

| Symbol | Description | Conditions | Speed Grade | | | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | | 1.0V | | | 0.95V | 0.9V | |
| | | | -3 | -2/-2LE | -1 | -1LI | -2LE | |
| $F_{TXOUT}$ | TXOUTCLK maximum frequency | | 412.500 | 412.500 | 234.375 | 234.375 | 234.375 | MHz |
| $F_{RXOUT}$ | RXOUTCLK maximum frequency | | 412.500 | 412.500 | 234.375 | 234.375 | 234.375 | MHz |
| $F_{TXIN}$ | TXUSRCLK maximum frequency | 16-bit data path | 412.500 | 412.500 | 234.375 | 234.375 | 234.375 | MHz |
| $F_{RXIN}$ | RXUSRCLK maximum frequency | 16-bit data path | 412.500 | 412.500 | 234.375 | 234.375 | 234.375 | MHz |
| $F_{TXIN2}$ | TXUSRCLK2 maximum frequency | 16-bit data path | 412.500 | 412.500 | 234.375 | 234.375 | 234.375 | MHz |
| $F_{RXIN2}$ | RXUSRCLK2 maximum frequency | 16-bit data path | 412.500 | 412.500 | 234.375 | 234.375 | 234.375 | MHz |

**Notes:**

1. Clocking must be implemented as described in *7 Series FPGAs GTP Transceiver User Guide* (UG482).

*Table 57:* **GTP Transceiver Transmitter Switching Characteristics**

| Symbol | Description | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{GTPTX}$ | Serial data rate range | | 0.500 | – | $F_{GTPMAX}$ | Gb/s |
| $T_{RTX}$ | TX rise time | 20%–80% | – | 50 | – | ps |
| $T_{FTX}$ | TX fall time | 80%–20% | – | 50 | – | ps |
| $T_{LLSKEW}$ | TX lane-to-lane skew(1) | | – | – | 500 | ps |
| $V_{TXOOBVDPP}$ | Electrical idle amplitude | | – | – | 20 | mV |
| $T_{TXOOBTRANSITION}$ | Electrical idle transition time | | – | – | 140 | ns |
| $TJ_{6.6}$ | Total Jitter(2)(3) | 6.6 Gb/s | – | – | 0.30 | UI |
| $DJ_{6.6}$ | Deterministic Jitter(2)(3) | | – | – | 0.15 | UI |
| $TJ_{5.0}$ | Total Jitter(2)(3) | 5.0 Gb/s | – | – | 0.30 | UI |
| $DJ_{5.0}$ | Deterministic Jitter(2)(3) | | – | – | 0.15 | UI |
| $TJ_{4.25}$ | Total Jitter(2)(3) | 4.25 Gb/s | – | – | 0.30 | UI |
| $DJ_{4.25}$ | Deterministic Jitter(2)(3) | | – | – | 0.15 | UI |
| $TJ_{3.75}$ | Total Jitter(2)(3) | 3.75 Gb/s | – | – | 0.30 | UI |
| $DJ_{3.75}$ | Deterministic Jitter(2)(3) | | – | – | 0.15 | UI |
| $TJ_{3.2}$ | Total Jitter(2)(3) | 3.20 Gb/s(4) | – | – | 0.2 | UI |
| $DJ_{3.2}$ | Deterministic Jitter(2)(3) | | – | – | 0.1 | UI |
| $TJ_{3.2L}$ | Total Jitter(2)(3) | 3.20 Gb/s(5) | – | – | 0.32 | UI |
| $DJ_{3.2L}$ | Deterministic Jitter(2)(3) | | – | – | 0.16 | UI |
| $TJ_{2.5}$ | Total Jitter(2)(3) | 2.5 Gb/s(6) | – | – | 0.20 | UI |
| $DJ_{2.5}$ | Deterministic Jitter(2)(3) | | – | – | 0.08 | UI |
| $TJ_{1.25}$ | Total Jitter(2)(3) | 1.25 Gb/s(7) | – | – | 0.15 | UI |
| $DJ_{1.25}$ | Deterministic Jitter(2)(3) | | – | – | 0.06 | UI |
| $TJ_{500}$ | Total Jitter(2)(3) | 500 Mb/s | – | – | 0.1 | UI |
| $DJ_{500}$ | Deterministic Jitter(2)(3) | | – | – | 0.03 | UI |

**Notes:**

1. Using same REFCLK input with TX phase alignment enabled for up to four consecutive transmitters (one fully populated GTP Quad).
2. Using PLL[0/1]_FBDIV = 2, 20-bit internal data width. These values are NOT intended for protocol specific compliance determinations.
3. All jitter values are based on a bit-error ratio of $1e^{-12}$.
4. PLL frequency at 3.2 GHz and TXOUT_DIV = 2.
5. PLL frequency at 1.6 GHz and TXOUT_DIV = 1.
6. PLL frequency at 2.5 GHz and TXOUT_DIV = 2.
7. PLL frequency at 2.5 GHz and TXOUT_DIV = 4.

*Table 58:* **GTP Transceiver Receiver Switching Characteristics**

| Symbol | Description | | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $F_{GTPRX}$ | Serial data rate | RX oversampler not enabled | 0.500 | – | $F_{GTPMAX}$ | Gb/s |
| $T_{RXELECIDLE}$ | Time for RXELECIDLE to respond to loss or restoration of data | | – | 10 | – | ns |
| $RX_{OOBVDPP}$ | OOB detect threshold peak-to-peak | | 60 | – | 150 | mV |
| $RX_{SST}$ | Receiver spread-spectrum tracking(1) | Modulated @ 33 kHz | –5000 | – | 5000 | ppm |
| $RX_{RL}$ | Run length (CID) | | – | – | 512 | UI |
| $RX_{PPMTOL}$ | Data/REFCLK PPM offset tolerance | | –1250 | – | 1250 | ppm |
| **SJ Jitter Tolerance(2)** | | | | | | |
| $JT_SJ_{6.6}$ | Sinusoidal Jitter(3) | 6.6 Gb/s | 0.44 | – | – | UI |
| $JT_SJ_{5.0}$ | Sinusoidal Jitter(3) | 5.0 Gb/s | 0.44 | – | – | UI |
| $JT_SJ_{4.25}$ | Sinusoidal Jitter(3) | 4.25 Gb/s | 0.44 | – | – | UI |
| $JT_SJ_{3.75}$ | Sinusoidal Jitter(3) | 3.75 Gb/s | 0.44 | – | – | UI |
| $JT_SJ_{3.2}$ | Sinusoidal Jitter(3) | 3.2 Gb/s(4) | 0.45 | – | – | UI |
| $JT_SJ_{3.2L}$ | Sinusoidal Jitter(3) | 3.2 Gb/s(5) | 0.45 | – | – | UI |
| $JT_SJ_{2.5}$ | Sinusoidal Jitter(3) | 2.5 Gb/s(6) | 0.5 | – | – | UI |
| $JT_SJ_{1.25}$ | Sinusoidal Jitter(3) | 1.25 Gb/s(7) | 0.5 | – | – | UI |
| $JT_SJ_{500}$ | Sinusoidal Jitter(3) | 500 Mb/s | 0.4 | – | – | UI |
| **SJ Jitter Tolerance with Stressed Eye(2)** | | | | | | |
| $JT_TJSE_{3.2}$ | Total Jitter with Stressed Eye(8) | 3.2 Gb/s | 0.70 | – | – | UI |
| $JT_TJSE_{6.6}$ | | 6.6 Gb/s | 0.70 | – | – | UI |
| $JT_SJSE_{3.2}$ | Sinusoidal Jitter with Stressed Eye(8) | 3.2 Gb/s | 0.1 | – | – | UI |
| $JT_SJSE_{6.6}$ | | 6.6 Gb/s | 0.1 | – | – | UI |

**Notes:**

1. Using RXOUT_DIV = 1, 2, and 4.
2. All jitter values are based on a bit error ratio of $1e^{-12}$.
3. The frequency of the injected sinusoidal jitter is 10 MHz.
4. PLL frequency at 3.2 GHz and RXOUT_DIV = 2.
5. PLL frequency at 1.6 GHz and RXOUT_DIV = 1.
6. PLL frequency at 2.5 GHz and RXOUT_DIV = 2.
7. PLL frequency at 2.5 GHz and RXOUT_DIV = 4.
8. Composite jitter.

## GTP Transceiver Protocol Jitter Characteristics

For Table 59 through Table 63, the *7 Series FPGAs GTP Transceiver User Guide* (UG482) contains recommended settings for optimal usage of protocol specific characteristics.

*Table 59:* **Gigabit Ethernet Protocol Characteristics**

| Description | Line Rate (Mb/s) | Min | Max | Units |
|---|---|---|---|---|
| **Gigabit Ethernet Transmitter Jitter Generation** | | | | |
| Total transmitter jitter (T_TJ) | 1250 | – | 0.24 | UI |
| **Gigabit Ethernet Receiver High Frequency Jitter Tolerance** | | | | |
| Total receiver jitter tolerance | 1250 | 0.749 | – | UI |

*Table 60:* **XAUI Protocol Characteristics**

| Description | Line Rate (Mb/s) | Min | Max | Units |
|---|---|---|---|---|
| **XAUI Transmitter Jitter Generation** | | | | |
| Total transmitter jitter (T_TJ) | 3125 | – | 0.35 | UI |
| **XAUI Receiver High Frequency Jitter Tolerance** | | | | |
| Total receiver jitter tolerance | 3125 | 0.65 | – | UI |

*Table 61:* **PCI Express Protocol Characteristics(1)**

| Standard | Description | Line Rate (Mb/s) | Min | Max | Units |
|---|---|---|---|---|---|
| **PCI Express Transmitter Jitter Generation** | | | | | |
| PCI Express Gen 1 | Total transmitter jitter | 2500 | – | 0.25 | UI |
| PCI Express Gen 2 | Total transmitter jitter | 5000 | – | 0.25 | UI |
| **PCI Express Receiver High Frequency Jitter Tolerance** | | | | | |
| PCI Express Gen 1 | Total receiver jitter tolerance | 2500 | 0.65 | – | UI |
| PCI Express Gen 2(2) | Receiver inherent timing error | 5000 | 0.40 | – | UI |
| | Receiver inherent deterministic timing error | | 0.30 | – | UI |

**Notes:**

1. Tested per card electromechanical (CEM) methodology.
2. Using common REFCLK.

*Table 62:* **CEI-6G Protocol Characteristics**

| Description | Line Rate (Mb/s) | Interface | Min | Max | Units |
|---|---|---|---|---|---|
| **CEI-6G Transmitter Jitter Generation** | | | | | |
| Total transmitter jitter(1) | 4976–6375 | CEI-6G-SR | – | 0.3 | UI |
| **CEI-6G Receiver High Frequency Jitter Tolerance** | | | | | |
| Total receiver jitter tolerance(1) | 4976–6375 | CEI-6G-SR | 0.6 | – | UI |

**Notes:**

1. Tested at most commonly used line rate of 6250 Mb/s using 390.625 MHz reference clock.

*Table 63:* **CPRI Protocol Characteristics**

| Description | Line Rate (Mb/s) | Min | Max | Units |
|---|---|---|---|---|
| **CPRI Transmitter Jitter Generation** | | | | |
| Total transmitter jitter | 614.4 | – | 0.35 | UI |
| | 1228.8 | – | 0.35 | UI |
| | 2457.6 | – | 0.35 | UI |
| | 3072.0 | – | 0.35 | UI |
| | 4915.2 | – | 0.3 | UI |
| | 6144.0 | – | 0.3 | UI |
| **CPRI Receiver Frequency Jitter Tolerance** | | | | |
| Total receiver jitter tolerance | 614.4 | 0.65 | – | UI |
| | 1228.8 | 0.65 | – | UI |
| | 2457.6 | 0.65 | – | UI |
| | 3072.0 | 0.65 | – | UI |
| | 4915.2(1) | 0.60 | – | UI |
| | 6144.0(1) | 0.60 | – | UI |

**Notes:**
1. Tested to CEI-6G-SR.

## Integrated Interface Block for PCI Express Designs Switching Characteristics

More information and documentation on solutions for PCI Express designs can be found at:
www.xilinx.com/products/technology/pci-express.html

*Table 64:* **Maximum Performance for PCI Express Designs**

| Symbol | Description | Speed Grade | | | | | Units |
|---|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.95V | 0.9V | |
| | | -3 | -2/-2LE | -1 | -1LI | -2LE | |
| $F_{PIPECLK}$ | Pipe clock maximum frequency | 250.00 | 250.00 | 250.00 | 250.00 | 250.00 | MHz |
| $F_{USERCLK}$ | User clock maximum frequency | 250.00 | 250.00 | 250.00 | 250.00 | 250.00 | MHz |
| $F_{USERCLK2}$ | User clock 2 maximum frequency | 250.00 | 250.00 | 250.00 | 250.00 | 250.00 | MHz |
| $F_{DRPCLK}$ | DRP clock maximum frequency | 250.00 | 250.00 | 250.00 | 250.00 | 250.00 | MHz |

**Notes:**
1. Refer to PG054, *7 Series FPGAs Integrated Block for PCI Express Product Guide* for specific supported core configurations.

## XADC Specifications

*Table 65:* **XADC Specifications**

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CCADC}$ = 1.8V ± 5%, $V_{REFP}$ = 1.25V, $V_{REFN}$ = 0V, ADCCLK = 26 MHz, –55°C ≤ Tj ≤ 125°C, Typical values at $T_j$=+40°C | | | | | | |
| **ADC Accuracy**(1) | | | | | | |
| Resolution | | | 12 | – | – | Bits |
| Integral Nonlinearity(2) | INL | –40°C ≤ $T_j$ ≤ 100°C | – | – | ±2 | LSBs |
| | | –55°C ≤ $T_j$ < –40°C; 100°C < $T_j$ ≤ 125°C | – | – | ±3 | LSBs |
| Differential Nonlinearity | DNL | No missing codes, guaranteed monotonic | – | – | ±1 | LSBs |
| Offset Error | Unipolar | –40°C ≤ $T_j$ ≤ 100°C | – | – | ±8 | LSBs |
| | | –55°C ≤ $T_j$ < –40°C; 100°C < $T_j$ ≤ 125°C | – | – | ±12 | LSBs |
| | Bipolar | –55°C ≤ $T_j$ ≤ 125°C | – | – | ±4 | LSBs |
| Gain Error | | | – | – | ±0.5 | % |
| Offset Matching | | | – | – | 4 | LSBs |
| Gain Matching | | | – | – | 0.3 | % |
| Sample Rate | | | – | – | 1 | MS/s |
| Signal to Noise Ratio(2) | SNR | $F_{SAMPLE}$ = 500KS/s, $F_{IN}$ = 20 kHz | 60 | – | – | dB |
| RMS Code Noise | | External 1.25V reference | – | – | 2 | LSBs |
| | | On-chip reference | – | 3 | – | LSBs |
| Total Harmonic Distortion(2) | THD | $F_{SAMPLE}$ = 500KS/s, $F_{IN}$ = 20 kHz | 70 | – | – | dB |
| **Analog Inputs**(3) | | | | | | |
| ADC Input Ranges | | Unipolar operation | 0 | – | 1 | V |
| | | Bipolar operation | –0.5 | – | +0.5 | V |
| | | Unipolar common mode range (FS input) | 0 | – | +0.5 | V |
| | | Bipolar common mode range (FS input) | +0.5 | – | +0.6 | V |
| Maximum External Channel Input Ranges | | Adjacent analog channels set within these ranges should not corrupt measurements on adjacent channels | –0.1 | – | $V_{CCADC}$ | V |
| Auxiliary Channel Full Resolution Bandwidth | FRBW | | 250 | – | – | kHz |
| **On-Chip Sensors** | | | | | | |
| Temperature Sensor Error | | –40°C ≤ $T_j$ ≤ 100°C | – | – | ±4 | °C |
| | | –55°C ≤ $T_j$ < –40°C; 100°C < $T_j$ ≤ 125°C | – | – | ±6 | °C |
| Supply Sensor Error | | –40°C ≤ $T_j$ ≤ 100°C | – | – | ±1 | % |
| | | –55°C ≤ $T_j$ < –40°C; 100°C < $T_j$ ≤ 125°C | – | – | ±2 | % |
| **Conversion Rate**(4) | | | | | | |
| Conversion Time - Continuous | $t_{CONV}$ | Number of ADCCLK cycles | 26 | – | 32 | Cycles |
| Conversion Time - Event | $t_{CONV}$ | Number of CLK cycles | – | – | 21 | Cycles |
| DRP Clock Frequency | DCLK | DRP clock frequency | 8 | – | 250 | MHz |
| ADC Clock Frequency | ADCCLK | Derived from DCLK | 1 | – | 26 | MHz |
| DCLK Duty Cycle | | | 40 | – | 60 | % |

*Table 65:* **XADC Specifications *(Cont'd)***

| Parameter | Symbol | Comments/Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **XADC Reference**(5) | | | | | | |
| External Reference | $V_{REFP}$ | Externally supplied reference voltage | 1.20 | 1.25 | 1.30 | V |
| On-Chip Reference | | Ground $V_{REFP}$ pin to AGND, $-40°C \le T_j \le 100°C$ | 1.2375 | 1.25 | 1.2625 | V |
| | | Ground $V_{REFP}$ pin to AGND, $-55°C \le T_j < -40°C$; $100°C < T_j \le 125°C$ | 1.225 | 1.25 | 1.275 | V |

**Notes:**

1. Offset and gain errors are removed by enabling the XADC automatic gain calibration feature. The values are specified for when this feature is enabled.
2. Only specified for bitstream option XADCEnhancedLinearity = ON.
3. See the ADC chapter in the *7 Series FPGAs and Zynq-7000 SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter* (UG480) for a detailed description.
4. See the Timing chapter in the *7 Series FPGAs and Zynq-7000 SoC XADC Dual 12-Bit 1 MSPS Analog-to-Digital Converter* (UG480) for a detailed description.
5. Any variation in the reference voltage from the nominal $V_{REFP}$ = 1.25V and $V_{REFN}$ = 0V will result in a deviation from the ideal transfer function. This also impacts the accuracy of the internal sensor measurements (i.e., temperature and power supply). However, for external ratiometric type applications allowing reference to vary by ±4% is permitted.

## Configuration Switching Characteristics

*Table 66:* **Configuration Switching Characteristics**

| Symbol | Description | Speed Grade | | | | | Units |
|---|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.95V | 0.9V | |
| | | -3 | -2/-2LE | -1 | -1LI | -2LE | |
| **Power-up Timing Characteristics** | | | | | | | |
| $T_{PL}$(1) | Program latency | 5.00 | 5.00 | 5.00 | 5.00 | 5.00 | ms, Max |
| $T_{POR}$(1) | Power-on reset (50 ms ramp rate time) | 10/50 | 10/50 | 10/50 | 10/50 | 10/50 | ms, Min/Max |
| | Power-on reset (1 ms ramp rate time) | 10/35 | 10/35 | 10/35 | 10/35 | 10/35 | ms, Min/Max |
| $T_{PROGRAM}$ | Program pulse width | 250.00 | 250.00 | 250.00 | 250.00 | 250.00 | ns, Min |
| **CCLK Output (Master Mode)** | | | | | | | |
| $T_{ICCK}$ | Master CCLK output delay | 150.00 | 150.00 | 150.00 | 150.00 | 150.00 | ns, Min |
| $T_{MCCKL}$ | Master CCLK clock Low time duty cycle | 40/60 | 40/60 | 40/60 | 40/60 | 40/60 | %, Min/Max |
| $T_{MCCKH}$ | Master CCLK clock High time duty cycle | 40/60 | 40/60 | 40/60 | 40/60 | 40/60 | %, Min/Max |
| $F_{MCCK}$ | Master CCLK frequency | 100.00 | 100.00 | 100.00 | 100.00 | 70.00 | MHz, Max |
| | Master CCLK frequency for AES encrypted x16 | 50.00 | 50.00 | 50.00 | 50.00 | 35.00 | MHz, Max |
| $F_{MCCK_START}$ | Master CCLK frequency at start of configuration | 3.00 | 3.00 | 3.00 | 3.00 | 3.00 | MHz, Typ |
| $F_{MCCKTOL}$ | Frequency tolerance, master mode with respect to nominal CCLK | ±50 | ±50 | ±50 | ±50 | ±50 | %, Max |
| **CCLK Input (Slave Modes)** | | | | | | | |
| $T_{SCCKL}$ | Slave CCLK clock minimum Low time | 2.50 | 2.50 | 2.50 | 2.50 | 2.50 | ns, Min |
| $T_{SCCKH}$ | Slave CCLK clock minimum High time | 2.50 | 2.50 | 2.50 | 2.50 | 2.50 | ns, Min |
| $F_{SCCK}$ | Slave CCLK frequency | 100.00 | 100.00 | 100.00 | 100.00 | 70.00 | MHz, Max |
| **EMCCLK Input (Master Mode)** | | | | | | | |
| $T_{EMCCKL}$ | External master CCLK Low time | 2.50 | 2.50 | 2.50 | 2.50 | 2.50 | ns, Min |
| $T_{EMCCKH}$ | External master CCLK High time | 2.50 | 2.50 | 2.50 | 2.50 | 2.50 | ns, Min |
| $F_{EMCCK}$ | External master CCLK frequency | 100.00 | 100.00 | 100.00 | 100.00 | 70.00 | MHz, Max |

*Table 66:* **Configuration Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | | Units |
|---|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.95V | 0.9V | |
| | | -3 | -2/-2LE | -1 | -1LI | -2LE | |
| **Internal Configuration Access Port** | | | | | | | |
| $F_{ICAPCK}$ | Internal configuration access port (ICAPE2) clock frequency | 100.00 | 100.00 | 100.00 | 100.00 | 70.00 | MHz, Max |
| **Master/Slave Serial Mode Programming Switching** | | | | | | | |
| $T_{DCCK}$/ $T_{CCKD}$ | DIN setup/hold | 4.00/0.00 | 4.00/0.00 | 4.00/0.00 | 4.00/0.00 | 5.00/0.00 | ns, Min |
| $T_{CCO}$ | DOUT clock to out | 8.00 | 8.00 | 8.00 | 8.00 | 9.00 | ns, Max |
| **SelectMAP Mode Programming Switching** | | | | | | | |
| $T_{SMDCCK}$/ $T_{SMCCKD}$ | D[31:00] setup/hold | 4.00/0.00 | 4.00/0.00 | 4.00/0.00 | 4.00/0.00 | 4.50/0.00 | ns, Min |
| $T_{SMCSCCK}$/ $T_{SMCCKCS}$ | CSI_B setup/hold | 4.00/0.00 | 4.00/0.00 | 4.00/0.00 | 4.00/0.00 | 5.00/0.00 | ns, Min |
| $T_{SMWCCK}$/ $T_{SMCCKW}$ | RDWR_B setup/hold | 10.00/0.00 | 10.00/0.00 | 10.00/0.00 | 10.00/0.00 | 12.00/0.00 | ns, Min |
| $T_{SMCKCSO}$ | CSO_B clock to out (330 Ω pull-up resistor required) | 7.00 | 7.00 | 7.00 | 7.00 | 8.00 | ns, Max |
| $T_{SMCO}$ | D[31:00] clock to out in readback | 8.00 | 8.00 | 8.00 | 8.00 | 10.00 | ns, Max |
| $F_{RBCCK}$ | Readback frequency | 100.00 | 100.00 | 100.00 | 100.00 | 70.00 | MHz, Max |
| **Boundary-Scan Port Timing Specifications** | | | | | | | |
| $T_{TAPTCK}$/ $T_{TCKTAP}$ | TMS and TDI setup/hold | 3.00/2.00 | 3.00/2.00 | 3.00/2.00 | 3.00/2.00 | 3.00/2.00 | ns, Min |
| $T_{TCKTDO}$ | TCK falling edge to TDO output | 7.00 | 7.00 | 7.00 | 7.00 | 8.50 | ns, Max |
| $F_{TCK}$ | TCK frequency | 66.00 | 66.00 | 66.00 | 66.00 | 50.00 | MHz, Max |
| **BPI Flash Master Mode Programming Switching** | | | | | | | |
| $T_{BPICCO}$(2) | A[28:00], RS[1:0], FCS_B, FOE_B, FWE_B, ADV_B clock to out | 8.50 | 8.50 | 8.50 | 8.50 | 10.00 | ns, Max |
| $T_{BPIDCC}$/ $T_{BPICCD}$ | D[15:00] setup/hold | 4.00/0.00 | 4.00/0.00 | 4.00/0.00 | 4.00/0.00 | 4.50/0.00 | ns, Min |
| **SPI Flash Master Mode Programming Switching** | | | | | | | |
| $T_{SPIDCC}$/ $T_{SPICCD}$ | D[03:00] setup/hold | 3.00/0.00 | 3.00/0.00 | 3.00/0.00 | 3.00/0.00 | 3.00/0.00 | ns, Min |
| $T_{SPICCM}$ | MOSI clock to out | 8.00 | 8.00 | 8.00 | 8.00 | 9.00 | ns, Max |
| $T_{SPICCFC}$ | FCS_B clock to out | 8.00 | 8.00 | 8.00 | 8.00 | 9.00 | ns, Max |
| **STARTUPE2 Ports** | | | | | | | |
| $T_{USRCCLKO}$ | STARTUPE2 USRCCLKO input to CCLK output | 0.50/6.00 | 0.50/6.70 | 0.50/7.50 | 0.50/7.50 | 0.50/7.50 | ns, Min/Max |
| $F_{CFGMCLK}$ | STARTUPE2 CFGMCLK output frequency | 65.00 | 65.00 | 65.00 | 65.00 | 65.00 | MHz, Typ |
| $F_{CFGMCLKTOL}$ | STARTUPE2 CFGMCLK output frequency tolerance | ±50 | ±50 | ±50 | ±50 | ±50 | %, Max |

*Table 66:* **Configuration Switching Characteristics *(Cont'd)***

| Symbol | Description | Speed Grade | | | | | Units |
|---|---|---|---|---|---|---|---|
| | | 1.0V | | | 0.95V | 0.9V | |
| | | -3 | -2/-2LE | -1 | -1LI | -2LE | |
| **Device DNA Access Port** | | | | | | | |
| $F_{DNACK}$ | DNA access port (DNA_PORT) | 100.00 | 100.00 | 100.00 | 100.00 | 70.00 | MHz, Max |

**Notes:**

1. To support longer delays in configuration, use the design solutions described in *7 Series FPGA Configuration User Guide* (UG470).
2. Only during configuration, the last edge is determined by a weak pull-up/pull-down resistor in the I/O.

## eFUSE Programming Conditions

Table 67 lists the programming conditions specifically for eFUSE. For more information, see *7 Series FPGA Configuration User Guide* (UG470).

*Table 67:* **eFUSE Programming Conditions(1)**

| Symbol | Description | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $I_{FS}$ | $V_{CCAUX}$ supply current | – | – | 115 | mA |
| $T_j$ | Temperature range | 15 | – | 125 | °C |

**Notes:**

1. The FPGA must not be configured during eFUSE programming.

## Revision History

The following table shows the revision history for this document:

| Date | Version | Description |
|---|---|---|
| 09/26/2011 | 1.0 | Initial Xilinx release. |
| 11/07/2011 | 1.1 | Revised the $V_{OCM}$ specification in Table 11. Updated the AC Switching Characteristics based upon the ISE 13.3 software v1.02 speed specification throughout document including Table 13 and Table 14. Added MMCM_$T_{FBDELAY}$ while adding MMCM_ to the symbol names of a few specifications in Table 37 and PLL to the symbol names in Table 38. In Table 39 through Table 46, updated the pin-to-pin description with the SSTL15 standard. Updated units in Table 46. |
| 02/13/2012 | 1.2 | Updated the Artix-7 family of devices listed throughout the entire data sheet. Updated the AC Switching Characteristics based upon the ISE 13.4 software v1.03 for the -3, -2, and -1 speed grades and v1.00 for the -2L speed grade.<br>Updated summary description on page 1. In Table 2, revised $V_{CCO}$ for the 3.3V HR I/O banks and updated $T_j$. Updated the notes in Table 5. Added MGTAVCC and MGTAVTT power supply ramp times to Table 7. Rearranged Table 8, added Mobile_DDR, HSTL_I_18, HSTL_II_18, HSUL_12, SSTL135_R, SSTL15_R, and SSTL12 and removed DIFF_SSTL135, DIFF_SSTL18_I, DIFF_SSTL18_II, DIFF_HSTL_I, and DIFF_HSTL_II. Added Table 9 and Table 10. Revised the specifications in Table 11. Revised $V_{IN}$ in Table 50. Updated the eFUSE Programming Conditions section and removed the endurance table. Added the  table. Revised $F_{TXIN}$ and $F_{RXIN}$ in Table 56. Revised $I_{CCADC}$ and updated Note 1 in Table 65. Revised DDR LVDS transmitter data width in Table 15. Removed notes from Table 27 as they are no longer applicable. Updated specifications in Table 66. Updated Note 1 in Table 36. |

| Date | Version | Description |
|---|---|---|
| 06/01/2012 | 1.3 | Reorganized entire data sheet including adding Table 43 and Table 47.<br>Updated $T_{SOL}$ in Table 1. Updated $I_{BATT}$ and added $R_{IN_TERM}$ to Table 3. Updated Power-On/Off Power Supply Sequencing section with regards to GTP transceivers. In Table 8, updated many parameters including SSTL135 and SSTL135_R. Removed $V_{OX}$ column and added DIFF_HSUL_12 to Table 10. Updated $V_{OL}$ in Table 11. Updated Table 15 and removed notes 2 and 3. Updated Table 16.<br>Updated the AC Switching Characteristics based upon the ISE 14.1 software v1.03 for the -3, -2, -2L (1.0V), -1, and v1.01 for the -2L (0.9V) speed specifications throughout the document.<br>In Table 30, updated Reset Delays section including Note 10 and Note 11. In Table 56, replaced $F_{TXOUT}$ with $F_{GLK}$. Updated many of the XADC specifications in Table 65 and added Note 2. Updated and moved *Dynamic Reconfiguration Port (DRP) for MMCM Before and After DCLK* section from Table 66 to Table 37 and Table 38. |
| 09/20/2012 | 1.4 | In Table 1, updated the descriptions, changed $V_{IN}$ and Note 2, and added Note 4. In Table 2, changed descriptions and notes. Updated parameters in Table 3. Added Table 4. Revised the Power-On/Off Power Supply Sequencing section. Updated standards and specifications in Table 8, Table 9, and Table 10. Removed the XC7A350T device from data sheet.<br>Updated the AC Switching Characteristics section to the ISE 14.2 speed specifications throughout the document. Updated the IOB Pad Input/Output/3-State discussion and changed Table 18 by adding $T_{IOIBUFDISABLE}$. Removed many of the combinatorial delay specifications and $T_{CINCK}/T_{CKCIN}$ from Table 27.Changed $F_{PFDMAX}$ conditions in Table 37 and Table 38. Updated the GTP Transceiver Specifications section, moved the GTP Transceiver DC characteristics section to the overall DC Characteristics section, and added the GTP Transceiver Protocol Jitter Characteristics section. In Table 65, updated Note 1. In Table 66, updated $T_{POR}$. |
| 02/01/2013 | 1.5 | Updated the AC Switching Characteristics based upon the 14.4/2012.4 device pack for ISE 14.4 and Vivado 2012.4, both at v1.07 for the -3, -2, -2L (1.0V), -1 speed specifications, and v1.05 for the -2L (0.9V) speed specifications throughout the document. Production changes to Table 13 and Table 14 for -3, -2, -2L (1.0V), -1 speed specifications.<br>Revised $I_{DCIN}$ and $I_{DCOUT}$ and added Note 5 in Table 1. Added Note 2 to Table 2. Updated Table 5. Added minimum current specifications to Table 6. Removed SSTL12 and HSTL_I_12 from Table 8. Removed DIFF_SSTL12 from Table 10. Updated Table 13. Added a 2:1 memory controller section to Table 16. Updated Note 1 in Table 34. Revised Table 36. Updated Note 1 and Note 2 in Table 49.<br>Updated $D_{VPPIN}$ in Table 50. Updated $V_{IDIFF}$ in Table 51. Removed $T_{LOCK}$ and $T_{PHASE}$ and revised $F_{GCLK}$ in Table 54. Updated $T_{DLOCK}$ in Table 55. Updated Table 56. In Table 57, updated $T_{RTX}$, $T_{FTX}$, $V_{TXOOBVDPP}$ , and revised Note 1 through Note 7. In Table 58, updated $RX_{SST}$ and $RX_{PPMTOL}$ and revised Note 4 through Note 7. In Table 63, revised and added Note 1.<br>Revised the maximum external channel input ranges in Table 65. In Table 66, revised $F_{MCCK}$ and added the Internal Configuration Access Port section. |
| 04/17/2013 | 1.6 | Updated the AC Switching Characteristics based upon v1.07 of the ISE 14.5 and Vivado 2013.1 for the -3, -2, -2L (1.0V), and -1 speed specifications, and v1.05 for the -2L (0.9V) speed specifications. Production changes to Table 13 and Table 14 for -2L (0.9V) speed specifications.<br>In Table 1, revised $V_{IN}$ (I/O input voltage) to match values in Table 4 and combined Note 4 with old Note 5 and then added new Note 5. Revised $V_{IN}$ description, removed Note 10, and added Note 7 in Table 2. Updated first 3 rows in Table 4. Also revised PCI33_3 voltage minimum in Table 8 to match values in Table 1 and Table 4. Added Note 1 to Table 11. Removed Note 1 from Table 14. Updated Table 16 title. Throughout the data sheet (Table 28, Table 29, and Table 44) removed the obvious note “A Zero “0” Hold Time listing indicates no hold time or a negative hold time.” |
| 09/04/2013 | 1.7 | Added new Artix-7 devices (XC7A35T, XC7A50T, and XC7A75T) throughout. In Table 1, updated $I_{DCIN}$ and $I_{DCOUT}$ for cases when floating, at $V_{MGTAVTT}$, or GND. Added back Note 1 to Table 14. Added CPG package to Table 50 and Table 52. |
| 11/27/2013 | 1.8 | Added automotive and expanded temperature range Artix-7 devices throughout. Added -1M and -1Q speed grades throughout. Added reference to *7 Series FPGAs Overview*, *Defense-Grade 7 Series FPGAs Overview*, and *XA Artix-7 FPGAs Overview* in Introduction. In Table 2, added junction temperature operating ranges for expanded (Q) and military (M) devices, and added Note 3. In Table 3, removed commercial (C), industrial (I), and extended (E) from descriptions of $R_{IN_TERM}$. Updated temperature ranges in Table 4. Removed notes from Table 6. Added $T_J$ = 125°C to Conditions column for $T_{VCCO2VCCAUX}$ in Table 7. In AC Switching Characteristics, updated first paragraph, added Table 12, and added -1Q/-1M speed grades to other tables in this section. In Table 52, added RB and RS packages, and updated $F_{GTPMAX}$. In Table 65, updated ADC Accuracy, On-Chip Sensors, XADC Reference sections and notes. Added $T_{USRCCLKO}$ and $F_{DNACK}$ to Table 66. |

| Date | Version | Description |
|---|---|---|
| 01/07/2014 | 1.9 | In Table 13, promoted all XC7A75T speed grades from Advance to Production and all XQ7A50T speed grades from Preliminary to Advance. In Table 14, inserted “Vivado tools 2013.3” for the production XC7A75T speed grades. |
| 01/23/2014 | 1.10 | Updated the AC Switching Characteristics based upon ISE 14.7 and Vivado 2013.4. Updated Note 5 in Table 2. Removed pad pull-down @ $V_{IN}$ = 1.8V for $I_{RPD}$ in Table 3. Added Note 2 to Table 4. Removed XQ7A50T fromTable 12, Table 13, and Table 14. In Table 13, changed speed grades for XA Artix-7 FPGAs and defense-grade Artix-7Q family from -2 to -2I and -1 to -1I, and moved all speed grades of XA7A100T, and -1I and -2I speed grades of XQ7A100T from Preliminary to Production. In Table 14, updated production software for XA7A100T and XQ7A100T. Added HSUL_12_F, DIFF_HSUL_12_F, MOBILE_DDR_S, MOBILE_DDR_F, DIFF_MOBILE_DDR_S, and DIFF_MOBILE_DDR_F to Table 17. Removed introductory text in Device Pin-to-Pin Output Parameter Guidelines. |
| 03/04/2014 | 1.11 | Updated Note 2 in Table 4. In Table 13, moved XQ7A100T -1M speed grade from Preliminary to Production. In Table 14, added production software for XQ7A100T -1M speed grade. |
| 03/28/2014 | 1.12 | In Table 5, added $I_{CCINTQ}$, $I_{CCOQ}$, $I_{CCAUXQ}$, and $I_{CCBRAMQ}$ values for XC7A35T, XC7A50T, XA7A35T, XA7A50T, and XQ7A50T devices. In Table 6, added power-on current values for XC7A35T, XC7A50T, XA7A35T, XA7A50T, and XQ7A50T devices. In Table 12, added row for XC7A35T, XC7A50T, and XC7A75T devices. In Table 13, moved all speed grades of XC7A35T and XC7A50T devices from Advance to Production, and added XQ7A50T. In Table 14, added XQ7A50T and production software for XC7A35T and XC7A50T -3, -2, -2L (1.0V), -1, and -2L (0.9V) speed grades. For $F_{IDELAYCTRL_REF}$ in Table 25, updated REFCLK frequency of 300 MHz, added REFCLK frequency of 400 MHz, and updated Note 1. In Table 36, added $T_{CKSKEW}$ data for XC7A35T and XC7A50T devices. In Table 39, updated $T_{ICKOF}$ data for -1 and -2L (0.9V) speed grades of XC7A35T and XC7A50T devices. In Table 40, updated $T_{ICKOFFAR}$ data for -1 and -2L (0.9V) speed grades of XC7A35T and XC7A50T devices. In Table 41, added $T_{ICKOFMMCMCC}$ data for -2L (0.9V) speed grade of XC7A35T and XC7A50T devices. In Table 42, added $T_{ICKOFPLLCC}$ data for -2L (0.9V) speed grade of XC7A35T and XC7A50T devices. In Table 44, updated $T_{PSFD}/T_{PHFD}$ data for -2/-2L, -1, and -2L (0.9V) speed grades of XC7A35T and XC7A50T devices. In Table 45, updated $T_{PSMMCMCC}/T_{PHMMCMCC}$ data for -1 and -2L (0.9V) speed grades of XC7A35T and XC7A50T devices. In Table 46, updated $T_{PSPLLCC}/T_{PHPLLCC}$ data for -1 and -2L (0.9V) speed grades of XC7A35T and XC7A50T devices. In Table 49, added package skew values for XC7A35T, XC7A50T, XA7A35T, XA7A50T, and XQ7A50T devices. |
| 05/13/2014 | 1.13 | In AC Switching Characteristics, updated to Vivado 2014.1. In Table 12, updated Vivado 2014.1 version numbers and consolidated rows. In Table 13, moved all XA7A75T speed grades from Advance to Preliminary and all XQ7A200T speed grades from Preliminary to Production. In Table 14, added production software for XQ7A200T -2, -1, and -1M speed grades. Added timing data for XA7A35T, XA7A50T, XA7A75T, and XQ7A50T devices to Table 39, Table 40, Table 41, Table 42, Table 44, Table 45, and Table 46. |
| 07/01/2014 | 1.14 | Updated Note 2 in Table 4 per the customer notice XCN14014: *7 Series FPGA and Zynq-7000 AP SoC I/O Undershoot Voltage Data Sheet Update*. In Power-On/Off Power Supply Sequencing, added sentence about there being no recommended sequence for supplies not shown. In AC Switching Characteristics, updated to Vivado 2014.2. In Table 12, added row for XQ7A50T. In Table 13, moved all XQ7A50T speed grades from Advance to Production. In Table 14, added production software for XQ7A50T -2, -1, and -1M speed grades. In Table 36, added $T_{CKSKEW}$ values for XA7A35T, XA7A50T, and XQ7A50T. Updated description of $T_{ICKOF}$ in Table 39 and added Note 2. Updated description of $T_{ICKOFFAR}$ in Table 40 and added Note 2. In Table 50, moved $DV_{PPOUT}$ value of 1000 mV from Max to Min column, updated $V_{IN}$ DC parameter description, and added Note 2. Added “peak-to-peak” to labels in Figure 3 and Figure 4. Added note after Figure 4. Added Note 1 to Table 64. In Table 66, replaced USRCCLK Output with STARTUPE2 Ports and added $F_{CFGMCLK}$ and $F_{CFGMCLKTOL}$. |
| 09/23/2014 | 1.15 | Removed 3.3V as descriptor of HR I/O banks throughout. Updated Note 3 in Table 5. In Table 13, moved all XA7A35T and XA7A50T speed grades from Advance to Production, and all XA7A75T speed grades from Preliminary to Production. In Table 14, added production software for XA7A35T, XA7A50T, and XA7A75T -2, -1, and -1Q speed grades, and removed Note 2. Added I/O Standard Adjustment Measurement Methodology. |
| 10/09/2014 | 1.16 | Added XC7A15T and XA7A15T devices. Added -1LI speed grade throughout. Updated Introduction. Added -1LI (0.95V) to description of $V_{CCINT}$ and $V_{CCBRAM}$ in Table 2. Updated Note 1 and added Note 2 to Table 14. |

| Date | Version | Description |
|---|---|---|
| 11/19/2014 | 1.17 | Replaced -2L speed grade with -2LE throughout. Updated descriptions of $V_{CCINT}$ and $V_{CCBRAM}$ in Table 2. Updated the AC Switching Characteristics based upon Vivado 2014.4. In Table 12, updated Vivado software version and added a row for $V_{CCINT}$ = 0.95V. In Table 13, moved all speed grades for all devices from Advance to Production. In Table 14, added Vivado 2014.4 software version to -1LI (0.95V) speed grade column for commercial devices and applicable speed grades for XC7A15T and XA7A15T devices, and removed table notes. Added Selecting the Correct Speed Grade and Voltage in the Vivado Tools. In Table 16, moved LPDDR2 row to end of 2:1 Memory Controllers section. Updated speed grade heading row in Table 52. |
| 03/18/2015 | 1.18 | In Table 11, changed maximum $V_{ICM}$ value from 1.425V to 1.500V. Removed LVDS 1.8V standard from Table 19 and Table 20. Removed minimum sample rate specification from Table 65. |
| 09/24/2015 | 1.19 | Updated first paragraph in Introduction. Assigned quiescent supply currents to -1LI speed grade Artix-7Q devices in Table 5. In Table 14, changed -1LI speed grade Artix-7Q device cells from N/A to blank and added Note 1. Removed DIFF_SSTL12 standard from Table 19 and Table 20. Changed -1LI speed grade Artix-7Q device cells from N/A to blank in Table 36, Table 39, Table 40, Table 41, Table 42, Table 44, Table 45, and Table 46. Added SBV484, FBV484, FBV676, and FFV1156 packages to Table 49. Removed Pb-free G suffix from packages in Table 50 and Table 52. |
| 11/24/2015 | 1.20 | In AC Switching Characteristics, updated to Vivado 2015.4. In Table 13, added -1LI (0.95V) speed grade to Production column for XQ7A50T, XQ7A100T, and XQ7A200T. In Table 14, removed table note and added Vivado 2015.4 software version to -1LI (0.95V) speed grade column for XQ7A50T, XQ7A100T, and XQ7A200T. In Table 36, added $T_{CKSKEW}$ for XQ7A50T, XQ7A100T, and XQ7A200T at -1LI (0.95V) speed grade. Updated device pin-to-pin output parameter tables (Table 39 to Table 42) and input parameter tables (Table 44 to Table 46) for XQ7A50T, XQ7A100T, and XQ7A200T at -1LI (0.95V) speed grade. |
| 09/27/2016 | 1.21 | Added XC7A12T and XC7A25T devices. Updated the AC Switching Characteristics based upon Vivado 2016.3. In Table 19, updated $V_{MEAS}$ values for LVCMOS 3.3V, LVTTL 3.3V, and PCI33 3.3V, and removed note 1. Removed LVDCI_15, HSLVDCI_15, LVDCI_15, and HSLVDCI_18 I/O standards from Table 20. |
| 04/13/2017 | 1.22 | Added 1.35V to Note 5 in Table 2. Updated the AC Switching Characteristics based upon Vivado 2016.4. In Table 13, added -2LE (0.9V) speed grade to Advance column for XC7A12T and XC7A25T. In Table 25, changed $T_{IDELAYRESOLUTION}$ units from ps to µs. In Table 36, updated $T_{CKSKEW}$ for XC7A12T and XC7A25T devices at -2LE (0.9V) speed grade. Updated device pin-to-pin output parameter tables (Table 39 to Table 42) and input parameter tables (Table 44 to Table 46) for XC7A12T and XC7A25T devices at -2LE (0.9V) speed grade. Removed SBV484, FBV484, FBV676, and FFV1156 packages from Table 49 per the customer notice XCN16022: *Cross-ship of Lead-free Bump and Substrates in Lead-free (FFG/FBG/SBG) Packages*. |
| 12/21/2017 | 1.23 | Updated the AC Switching Characteristics based upon Vivado 2017.4. For XC7A12T and XC7A25T in Table 13, moved -3 and -2LE (0.9V) speed grades to Preliminary column and -2, -1, and -1LI (0.95V) speed grades to Production column. In Table 14, added Vivado 2017.4 software version to -2, -2LE, -1, and -1LI (0.95V) speed grade columns for XC7A12T and XC7A25T. In Table 44, updated $T_{PSFD}$/ $T_{PHFD}$ for XC7A12T and XC7A25T at -3, -2/-2LE, -1 and -1LI (0.95V) speed grades. In Table 46, updated $T_{PSPLLCC}$ for XC7A12T and XC7A25T at -1 and -1LI (0.95V) speed grades. In Table 49, added package skew values for XC7A12T and XC7A25T. |
| 04/04/2018 | 1.24 | Added XA7A12T and XA7A25T devices. Updated the AC Switching Characteristics based upon Vivado 2018.1. In Table 13, for XC7A12T and XC7A25T moved -2LE (0.9V) speed grade to Production column and added XA7A12T and XA7A25T with -2I, -1I, and -1Q speed grades in Production column. Added Note 3 to Table 16. |
| 06/18/2018 | 1.25 | Updated the AC Switching Characteristics based upon Vivado 2018.2. In Table 13, for XC7A12T and XC7A25T moved -3 speed grade to Production. In Table 14, added Vivado 2018.2 software version to -3 speed grade for XC7A12T and XC7A25T and removed note. |
| 03/23/2021 | 1.26 | Replaced D with DDLY in description of $T_{ISDCK_DDLY_DDR}$/$T_{ISCKD_DDLY_DDR}$ in Table 23. |
| 02/10/2022 | 1.27 | Added -2LE (1.0V) speed grade for XC7A12T and XC7A25T devices to Table 13. |

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AUTOMOTIVE PRODUCTS (IDENTIFIED AS "XA" IN THE PART NUMBER) ARE NOT WARRANTED FOR USE IN THE DEPLOYMENT OF AIRBAGS OR FOR USE IN APPLICATIONS THAT AFFECT CONTROL OF A VEHICLE ("SAFETY APPLICATION") UNLESS THERE IS A SAFETY CONCEPT OR REDUNDANCY FEATURE CONSISTENT WITH THE ISO 26262 AUTOMOTIVE SAFETY STANDARD ("SAFETY DESIGN"). CUSTOMER SHALL, PRIOR TO USING OR DISTRIBUTING ANY SYSTEMS THAT INCORPORATE PRODUCTS, THOROUGHLY TEST SUCH SYSTEMS FOR SAFETY PURPOSES. USE OF PRODUCTS IN A SAFETY APPLICATION WITHOUT A SAFETY DESIGN IS FULLY AT THE RISK OF CUSTOMER, SUBJECT ONLY TO APPLICABLE LAWS AND REGULATIONS GOVERNING LIMITATIONS ON PRODUCT LIABILITY.

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XMP058 (v1.27) March 30, 2023

# REACH Position & POP Statement: EU Regulation (EC) Number 1907/2006

## Background

The Regulation, Evaluation, Authorization, and Restriction of Chemicals (REACH) is a European Community Regulation related to the safe use and identification of chemicals (Regulation (EC) Number 1907/2006).
REACH entered into force on June 1, 2007 with the aim of improving the protection of human health and the environment through better and earlier identification of the intrinsic properties of chemical substances. REACH was aimed at streamlining and improving former European Union chemical legislation by replacing approximately 40 individual pieces of legislation and harmonizing with the remaining legislation. The new legislative framework under REACH shifts responsibility for the control and safety of chemicals from government authorities to industry and created the European Chemicals Agency to act as a central coordinator.

Xilinx packaged devices are delivered in compliance with the following requirements for hazardous substances, and all noted exceptions would be listed here.

| Regulations | Comment | Remark |
|---|---|---|
| (EU) 2019/1021 Annex I | Comply with the conditions limit of list of substances of Annex I | There are a total of 27 substances listed in Part A of Annex I according to EU published Regulation (EU) 2019/1021 of the European Parliament and of the Council of 4 JUL. 2020 on persistent organic pollutants. https://echa.europa.eu/list-of-substances-subject-to-pops-regulation |

## Xilinx Responsibilities

Xilinx is a supplier of “articles” as defined in REACH. The “substances” contained in these articles are not intended to be released under normal or reasonably foreseeable conditions of use.
Xilinx will continue to monitor REACH developments and will comply with any applicable requirements. As Substances of Very High Concern (SVHCs) are added to Annex XIV of the Regulation (Authorization List), Xilinx will assess whether both of the following conditions are met:
1. The substance is present in the articles in quantities over one (1) ton per year
2. The substances are present in Xilinx® devices, development products and packing material above a concentration level of 0.1% w/w
Xilinx shall comply with the requirements of Article 7(2) and Article 33 of the Regulation, as necessary.
For informational purposes, Xilinx has contacted its material and manufacturing vendors who have confirmed to Xilinx that Xilinx devices, development products, and packing material do not intentionally contain SVHCs above a concentration level of 0.1% w/w. However, regarding 4,4'-isopropylidenediphenol (Bisphenol A), some suppliers of substrate materials have reported Bisphenol A as a raw polymer ingredient of <0.3wt%. With regard to 2-methyl-1-(4-methylthiophenyl)-2-morpholinopropan-1-one, some suppliers of substrate materials have reported it is used for Photoinitiator as <1.5wt% in the concentration level. However, it does comply with Substrate:<0.1wt%(w/w) These substances are contained in the material as a small residue in the molecular form and cannot be released under normal conditions. With regard to lead, certain legacy devices utilize solder paste and solder balls containing 37% lead. In addition, Xilinx is compliant with the substance restrictions listed in REACH Annex XVII that limits the use of certain substances for specific uses.
Further information on REACH can be obtained at:
https://echa.europa.eu/regulations/reach/understanding-reach
https://echa.europa.eu/candidate-list-obligations

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Table 1: Candidate List of SVHCs defines the substances published by the European Chemicals Agency (ECHA) on the current Candidate List. Xilinx devices, development products, and packing material do not intentionally contain SVHCs above a concentration level of 0.1% w/w, except as noted in Items 76, 170, and 204.

**Table 1: Candidate List of SVHCs**

| Item | Substance Name | EC Number | CAS No. |
|---|---|---|---|
| 1 | 4,4'- Diaminodiphenylmethane (MDA) | 202-974-4 | 101-77-9 |
| 2 | 5-tert-butyl-2,4,6-trinitro-m-xylene (musk xylene) | 201-329-4 | 81-15-2 |
| 3 | Alkanes, C10-13, chloro (Short Chain Chlorinated Paraffins) | 287-476-5 | 85535-84-8 |
| 4 | Anthracene | 204-371-1 | 120-12-7 |
| 5 | Benzyl butyl phthalate | 201-622-7 | 85-68-7 |
| 6 | Bis (2-ethyl(hexyl)phthalate) (DEHP) | 204-211-0 | 117-81-7 |
| 7 | Bis (tributyltin) oxide (TBTO) | 200-268-0 | 56-35-9 |
| 8 | Diarsenic pentaoxide | 215-116-9 | 1303-28-2 |
| 9 | Diarsenic trioxide | 215-481-4 | 1327-53-3 |
| 10 | Dibutyl phthalate (DBP) | 201-557-4 | 84-74-2 |
| 11 | Hexabromocyclododecane (HBCDD) and all major diastereoisomers identifield (α - HBCDD, β-HBCDD, γ -HBCDD) | 247-148-4, 221-695-9 | 134237-50-6, 134237-51-7, 134237-52-8 |
| 12 | Lead hydrogen arsenate | 232-064-2 | 7784-40-9 |
| 13 | Sodium dichromate | 234-190-3 | 7789-12-0, 10588-01-9 |
| 14 | Triethyl arsenate | 427-700-2 | 15606-95-8 |
| 15 | 2,4-Dinitrotoluene | 204-450-0 | 121-14-2 |
| 16 | Anthracene oil | 292-602-7 | 90640-80-5 |
| 17 | Anthracene oil, anthracene-low | 292-604-8 | 90640-82-7 |
| 18 | Anthracene oil, anthracene paste | 292-603-2 | 90640-81-6 |
| 19 | Anthracene oil, anthracene paste, anthracene fraction | 295-275-9 | 91995-15-2 |
| 20 | Anthracene oil, anthracene paste, distillation lights | 295-278-5 | 91995-17-4 |
| 21 | Di isobutyl phthalate (DIBP) | 201-553-2 | 84-69-5 |
| 22 | Lead chromate | 231-846-0 | 7758-97-6 |
| 23 | Lead chromate molybdate sulphate red (C.I. Pigment Red 104) | 235-759-9 | 12656-85-8 |
| 24 | Lead sulfochromate yellow (C.I. Pigment Yellow 34) | 215-693-7 | 1344-37-2 |


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**Table 1: Candidate List of SVHCs (Cont'd)**

| Item | Substance name | EC Number | CAS No. |
|---|---|---|---|
| 25 | Coal tar pitch, high temperature | 266-028-2 | 65996-93-2 |
| 26 | Tris (2-chloroethyl) phosphate | 204-118-5 | 115-96-8 |
| 27 | Acrylamide | 201-173-7 | 79-06-1 |
| 28 | Trichloroethylene | 201-167-4 | 79-01-6 |
| 29 | Boric acid | 233-139-2<br>(234-343-4) | 10043-35-3<br>(1113-50-1) |
| 30 | Disodium tetraborate, anhydrous | 215-540-4 | 1330-43-4,<br>(anhydrous)<br>12179-04-3,<br>(pentahydrate)<br>1303-96-4,<br>(decahydrate) |
| 31 | Tetraboron disodium heptaoxide, hydrate | 235-541-3 | 12267-73-1 |
| 32 | Potassium dichromate | 231-906-6 | 7778-50-9 |
| 33 | Ammonium dichromate | 232-143-1 | 7789-09-5 |
| 34 | Potassium chromate | 232-140-5 | 7789-00-6 |
| 35 | Sodium chromate | 231-889-5 | 7775-11-3 |
| 36 | Cobalt(II) sulphate | 233-334-2 | 10124-43-3 |
| 37 | Cobalt(II) dinitrate | 233-402-1 | 10141-05-6 |
| 38 | Cobalt(II) carbonate | 208-169-4 | 513-79-1 |
| 39 | Cobalt(II) diacetate | 200-755-8 | 71-48-7 |
| 40 | 2-Methoxyethanol | 203-713-7 | 109-86-4 |
| 41 | 2-Ethoxyethanol | 203-804-1 | 110-80-5 |
| 42 | Chromium trioxide | 215-607-8 | 1333-82-0 |
| 43 | Chromic acid,<br>Oligomers of chromic acid and dichromic acid,<br>Dichromic acid | 231-801-5<br>-<br>236-881-5 | 7738-94-5<br>-<br>13530-68-2 |
| 44 | 2-Ethoxyethyl acetate | 203-839-2 | 111-15-9 |
| 45 | Strontium chromate | 232-142-6 | 7789-06-2 |
| 46 | 1,2-Benzenedicarboxylic acid, di-C7-11-branched and linear alkyl esters | 271-084-6 | 68515-42-4 |
| 47 | Hydrazine | 206-114-9 | 302-01-2,<br>7803-57-8 |
| 48 | 1-Methyl-2-pyrrolidone | 212-828-1 | 872-50-4 |


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**Table 1: Candidate List of SVHCs (Cont'd)**

| Item | Substance name | EC Number | CAS No. |
|---|---|---|---|
| 49 | 1,2,3-Trichloropropane | 202-486-1 | 96-18-4 |
| 50 | 1,2-Benzenedicarboxylic acid, di-C6-8-branched alkyl esters, C7-rich | 276-158-1 | 71888-89-6 |
| 51 | Cobalt dichloride | 231-589-4 | 7646-79-9 |
| 52 | N,N-dimethylacetamide | 204-826-4 | 127-19-5 |
| 53 | Lead azide – Lead diazide | 236-542-1 | 13424-46-9 |
| 54 | Lead styphnate | 236-542-1 | 15345-44-0 |
| 55 | 2,2'-dichloro-4,4'-methylenedianiline (MOCA) | 202-918-9 | 101-14-4 |
| 56 | Phenolphthalein | 201-004-7 | 77-09-8 |
| 57 | Lead dipicrate | 229-335-2 | 6477-64-1 |
| 58 | Aluminosilicate Refractory Ceramic Fibres (RCF) - are fibres covered by index number 650-017-00-8 in Annex VI, part 3, table 3.1 of Regulation (EC) No 1272/2008 of the European Parliament and of the Council of 16 December 2008 on classification, labelling and packaging of substances and mixtures, and fulfil the three following conditions: a) oxides of aluminium and silicon are the main components present (in the fibres) within variable concentration ranges b) fibres have a length weighted geometric mean diameter less two standard geometric errors of 6 or less micrometres (µm) c) alkaline oxide and alkali earth oxide (Na2O+K2O+CaO+MgO+BaO) content less or equal to 18% by weight | - | Extracted from: 650-017-00-8 |
| 59 | Zirconia Aluminosilicate Refractory Ceramic Fibres (Zr-RCF) - are fibres covered by index number 650-017-00-8 in Annex VI, part 3, table 3.1 of Regulation (EC) No 1272/2008 of the European Parliament and of the Council of 16 December 2008 on classification, labelling and packaging of substances and mixtures, and fulfil the three following conditions: a) oxides of aluminium, silicon and zirconium are the main components present (in the fibres) within variable concentration ranges b) fibres have a length weighted geometric mean diameter less two standard geometric errors of 6 or less micrometres (µm). c) alkaline oxide and alkali earth oxide (Na2O+K2O+CaO+MgO+BaO) content less or equal to 18% by weight | - | Extracted from: 650-017-00-8 |
| 60 | Bis(2-methoxyethyl)ether | 203-924-4 | 111-96-6 |
| 61 | 1,2-Dichloroethane | 203-458-1 | 107-06-2 |
| 62 | Dichromium tris(chromate) | 246-356-2 | 24613-89-6 |
| 63 | Potassium hydroxyoctaoxodizincatedichromate | 234-329-8 | 11103-86-9 |
| 64 | Pentazinc chromate octahydroxide | 256-418-0 | 49663-84-5 |
| 65 | Formaldehyde, oligomeric reaction products with aniline (technical MDA) | 500-036-1 | 25214-70-4 |
| 66 | Bis(2-methoxyethyl) phthalate | 204-212-6 | 117-82-6 |
| 67 | Arsenic acid | 231-901-9 | 7778-39-4 |


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**Table 1: Candidate List of SVHCs (Cont'd)**

| Item | Substance name | EC Number | CAS No. |
|---|---|---|---|
| 68 | Calcium arsenate | 231-904-5 | 7778-44-1 |
| 69 | Trilead diarsenate | 222-979-5 | 3687-31-8 |
| 70 | 2-Methoxyaniline; o-Anisidine | 201-963-1 | 90-04-0 |
| 71 | 4-(1,1,3,3-tetramethylbutyl)phenol, (4-tert-Octylphenol) | 205-507-9 | 140-66-9 |
| 72 | [4-[4,4'-bis(dimethylamino) benzhydrylidene]cyclohexa-2,5-dien-1-ylidene]dimethylammonium chloride (C.I. Basic Violet 3) | 208-953-6 | 548-62-9 |
| 73 | [4-[[4-anilino-1-naphthyl][4-(dimethylamino)phenyl]methylene]cyclohexa-2,5-dien-1-ylidene] dimethylammonium chloride (C.I. Basic Blue 26) | 219-943-6 | 2580-56-5 |
| 74 | N,N,N',N'-tetramethyl-4,4'-methylenedianiline (Michler's base) | 202-959-2 | 101-61-1 |
| 75 | β-TGIC (1,3,5-tris[(2S and 2R)-2,3-epoxypropyl]-1,3,5-triazine-2,4,6-(1H,3H,5H)-trione) | 423-400-0 | 59653-74-6 |
| 76 | Diboron trioxide<br>Note: Diboron Trioxide is a raw ingredient used in the manufacture of the glass material used in capacitors. The substance is completely transformed and is not present in the final glass article of the capacitor and so is not required to be declared in REACH. However, the material is declared on the capacitor MDDS per JEITA recommendation due to glass has no CAS #. | 215-125-8 | 1303-86-2 |
| 77 | a,a-Bis[4-(dimethylamino)phenyl]-4 (phenylamino)naphthalene-1-methanol (C.I. Solvent Blue 4) | 229-851-8 | 6786-83-0 |
| 78 | 1,2-bis(2-methoxyethoxy)ethane (TEGDME triglyme) | 203-977-3 | 112-49-2 |
| 79 | 4,4'-bis(dimethylamino)-4''-(methylamino)trityl alcohol | 209-218-2 | 561-41-1 |
| 80 | TGIC (1,3,5-tris(oxiranylmethyl)-1,3,5-triazine-2,4,6(1H,3H,5H)-trione) | 219-514-3 | 2451-62-9 |
| 81 | Formamide | 200-842-0 | 75-12-7 |
| 82 | 4,4'-bis(dimethylamino)benzophenone (Michler's ketone) | 202-027-5 | 90-94-8 |
| 83 | Lead(II) bis(methanesulfonate) | 401-750-5 | 17570-76-2 |
| 84 | 1,2-dimethoxyethane ethylene glycol dimethyl ether (EGDME) | 203-794-9 | 110-71-4 |
| 85 | Pyrochlore, antimony lead yellow | 232-382-1 | 8012-00-8 |
| 86 | 6-methoxy-m-toluidine (p-cresidine) | 204-419-1 | 120-71-8 |
| 87 | Henicosafluoroundecanoic acid | 218-165-4 | 2058-94-8 |
| 88 | Hexahydromethylphthalic anhydride [1], Hexahydro-4-methylphthalic anhydride [2], Hexahydro-1-methylphthalic anhydride [3], Hexahydro-3-methylphthalic anhydride [4] [The individual isomers [2], [3] and [4] (including their cis- and trans- stereo isomeric forms) and all possible combinations of the isomers [1] are covered by this entry] | 247-094-1, 243-072-0, 256-356-4, 260-566-1 | 25550-51-0, 19438-60-9, 48122-14-1, 57110-29-9 |
| 89 | Cyclohexane-1,2-dicarboxylic anhydride [1], cis-cyclohexane-1,2-dicarboxylic anhydride [2], trans-cyclohexane-1,2-dicarboxylic anhydride [3] [The individual cis- [2] and trans- [3] isomer substances and all possible combinations of the cis- and trans-isomers [1] are covered by this entry] | 201-604-9, 236-086-3, 238-009-9 | 85-42-7, 13149-00-3, 14166-21-3 |
| 90 | Dibutyltin dichloride (DBTC) | 211-670-0 | 683-18-1 |


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**Table 1: Candidate List of SVHCs (Cont'd)**

| Item | Substance name | EC Number | CAS No. |
|---|---|---|---|
| 91 | Lead bis(tetrafluoroborate) | 237-486-0 | 13814-96-5 |
| 92 | Lead dinitrate | 233-245-9 | 10099-74-8 |
| 93 | Silicic acid, lead salt | 234-363-3 | 11120-22-2 |
| 94 | 4-Aminoazobenzene | 200-453-6 | 60-09-3 |
| 95 | Lead titanium zirconium oxide | 235-727-4 | 12626-81-2 |
| 96 | Lead monoxide (lead oxide) | 215-267-0 | 1317-36-8 |
| 97 | o-Toluidine | 202-429-0 | 95-53-4 |
| 98 | 3-ethyl-2-methyl-2-(3-methylbutyl)-1,3-oxazolidine | 421-150-7 | 143860-04-2 |
| 99 | Silicic acid (H2Si2O5), barium salt (1:1), lead-doped [with lead (Pb) content above the applicable generic concentration limit for 'toxicity for reproduction' Repr. 1A (CLP) or category 1 (DSD); the substance is a member of the group entry of lead compounds, with index number 082-001-00-6 in Regulation (EC) No 1272/2008] | 272-271-5 | 68784-75-8 |
| 100 | Trilead bis(carbonate)dihydroxide | 215-290-6 | 1319-46-6 |
| 101 | Furan | 203-727-3 | 110-00-9 |
| 102 | N,N-dimethylformamide | 200-679-5 | 68-12-2 |
| 103 | 4-(1,1,3,3-tetramethylbutyl)phenol, ethoxylated [covering well-defined substances and UVCB substances, polymers and homologues] | - | - |
| 104 | 4-Nonylphenol, branched and linear [substances with a linear and/or branched alkyl chain with a carbon number of 9 covalently bound in position 4 to phenol, covering also UVCB- and well-defined substances which include any of the individual isomers or a combination thereof] | - | - |
| 105 | 4,4'-methylenedi-o-toluidine | 212-658-8 | 838-88-0 |
| 106 | Diethyl sulphate | 200-589-6 | 64-67-5 |
| 107 | Dimethyl sulphate | 201-058-1 | 77-78-1 |
| 108 | Lead oxide sulfate | 234-853-7 | 12036-76-9 |
| 109 | Lead titanium trioxide | 235-038-9 | 12060-00-3 |
| 110 | Acetic acid, lead salt, basic | 257-175-3 | 51404-69-4 |
| 111 | [Phthalato(2-)]dioxotrilead | 273-688-5 | 69011-06-9 |
| 112 | Bis(pentabromophenyl) ether (decabromodiphenyl ether; DecaBDE) | 214-604-9 | 1163-19-5 |
| 113 | N-methylacetamide | 201-182-6 | 79-16-3 |
| 114 | Dinoseb (6-sec-butyl-2,4-dinitrophenol) | 201-861-7 | 88-85-7 |


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**Table 1: Candidate List of SVHCs (Cont'd)**

| Item | Substance name | EC Number | CAS No. |
|---|---|---|---|
| 115 | 1,2-Diethoxyethane | 211-076-1 | 629-14-1 |
| 116 | Tetralead trioxide sulphate | 235-380-9 | 12202-17-4 |
| 117 | N-pentyl-isopentylphthalate | - | 776297-69-9 |
| 118 | Dioxobis(stearato)trilead | 235-702-8 | 12578-12-0 |
| 119 | Tetraethyllead | 201-075-4 | 78-00-2 |
| 120 | Pentalead tetraoxide sulphate | 235-067-7 | 12065-90-6 |
| 121 | Pentacosafluorotridecanoic acid | 276-745-2 | 72629-94-8 |
| 122 | Tricosafluorododecanoic acid | 206-203-2 | 307-55-1 |
| 123 | Heptacosafluorotetradecanoic acid | 206-803-4 | 376-06-7 |
| 124 | 1-bromopropane (n-propyl bromide) | 203-445-0 | 106-94-5 |
| 125 | Methoxyacetic acid | 210-894-6 | 625-45-6 |
| 126 | 4-methyl-m-phenylenediamine (toluene-2,4-diamine) | 202-453-1 | 95-80-7 |
| 127 | Methyloxirane (Propylene oxide) | 200-879-2 | 75-56-9 |
| 128 | Trilead dioxide phosphonate | 235-252-2 | 12141-20-7 |
| 129 | o-aminoazotoluene | 202-591-2 | 97-56-3 |
| 130 | 1,2-Benzenedicarboxylic acid, dipentylester, branched and linear | 284-032-2 | 84777-06-0 |
| 131 | 4,4'-oxydianiline and its salts | 202-977-0 | 101-80-4 |
| 132 | Orange lead (lead tetroxide) | 215-235-6 | 1314-41-6 |
| 133 | Biphenyl-4-ylamine | 202-177-1 | 92-67-1 |
| 134 | Diisopentylphthalate | 210-088-4 | 605-50-5 |
| 135 | Fatty acids, C16-18, lead salts | 292-966-7 | 91031-62-8 |
| 136 | Diazene-1,2-dicarboxamide (C,C'-azodi(formamide)) | 204-650-8 | 123-77-3 |
| 137 | Sulfurous acid, lead salt, dibasic | 263-467-1 | 62229-08-7 |
| 138 | Lead cyanamidate | 244-073-9 | 20837-86-9 |
| 139 | Cadmium | 231-152-8 | 7440-43-9 |
| 140 | Cadmium oxide | 215-146-2 | 1306-19-0 |

**Table 1: Candidate List of SVHCs (Cont'd)**

| Item | Substance name | EC Number | CAS No. |
|---|---|---|---|
| 141 | Ammonium pentadecafluorooctanoate | 223-320-4 | 3825-26-1 |
| 142 | Pentadecafluorooctanoic acid | 206-397-9 | 335-67-1 |
| 143 | Dipentyl phthalate | 205-017-9 | 131-18-0 |
| 144 | 4-Nonylphenol, branched and linear, ethoxylated | - | - |
| 145 | Cadmium Sulphide | 215-147-8 | 1306-23-6 |
| 146 | Diphexyl Phytalate | 201-559-5 | 84-75-3 |
| 147 | Disodium 3,3'-[[1,1'-biphenyl]-4,4'-diylbis(azo)]bis(4-aminonaphthalene-1-sulphonate) (C.I. Direct Red 28) | 209-358-4 | 573-58-0 |
| 148 | Disodium 4-amino-3-[[4'-[(2,4-diaminophenyl)azo][1,1'-biphenyl]-4-yl]azo] -5-hydroxy-6-(phenylazo)naphthalene-2,7-disulphonate (C.I. Direct Black 38) | 217-710-3 | 1937-37-7 |
| 149 | imidazolidine-2-thione; 2-imidazoline-2-thiol | 202-506-9 | 96-45-7 |
| 150 | Lead di(acetate) | 206-104-4 | 301-04-2 |
| 151 | Trixylyl phosphate | 246-677-8 | 25155-23-1 |
| 152 | 1,2-Benzenedicarboxylic acid, dihexyl ester, branched and linear | 271-093-5 | 68515-50-4 |
| 153 | Sodium perborate; perboric acid, sodium salt | 239-172-9, 234-390-0 | - |
| 154 | Sodium peroxometaborate | 231-556-4 | 7632-04-4 |
| 155 | Cadmium chloride | 233-296-7 | 10108-64-2 |
| 156 | 2-benzotriazol-2-yl-4,6-di-tert-butylphenol (UV-320) | 223-346-6 | 3846-71-7 |
| 157 | 2-ethylhexyl 10-ethyl-4,4-dioctyl-7-oxo-8-oxa-3,5-dithia-4-stannatetradecanoate (DOTE) | 239-622-4 | 15571-58-1 |
| 158 | Reaction mass of 2-ethylhexyl 10-ethyl-4,4-dioctyl-7-oxo-8-oxa-3,5-dithia-4-stannatetradecanoate and 2-ethylhexyl 10-ethyl-4-[[2-[(2-ethylhexyl)oxy]-2-oxoethyl]thio]-4-octyl-7-oxo-8-oxa-3,5-dithia-4-stannatetradecanoate (reaction mass of DOTE and MOTE) | - | - |
| 159 | 2-(2H-benzotriazol-2-yl)-4,6-ditertpentylphenol (UV-328) | 247-384-8 | 25973-55-1 |
| 160 | Cadmium Fluoride | 232-222-0 | 7790-79-6 |
| 161 | Cadmium Sulphate | 233-331-6 | 10124-36-4, 31119-53-6 |
| 162 | 1,2-benzenedicarboxylic acid, di-C6-10-alkyl esters; 1,2-benzenedicarboxylic acid, mixed decyl and hexyl and octyl diesters with ≥ 0.3% of dihexyl phthalate (EC No. 201-559-5) | 271-094-0 272-013-1 | 68515-51-5 68648-93-1 |
| 163 | 5-sec-butyl-2-(2,4-dimethylcyclohex-3-en-1-yl)-5-methyl-1,3-dioxane [1], 5-sec-butyl-2-(4,6-dimethylcyclohex-3-en-1-yl)-5-methyl-1,3-dioxane [2] [covering any of the individual stereoisomers of [1] and [2] or any combination thereof] | - | - |



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**Table 1: Candidate List of SVHCs (Cont'd)**

| Item | Substance name | EC Number | CAS No. |
|---|---|---|---|
| 164 | 1,3-propanesultone | 214-317-9 | 1120-71-4 |
| 165 | 2,4-di-tert-butyl-6-(5-chlorobenzotriazol-2-yl)phenol | 223-383-8 | 3864-99-1 |
| 166 | 2-(2H-benzotriazol-2-yl)-4-(tert-butyl)-6-(sec-butyl)phenol | 253-037-1 | 36437-37-3 |
| 167 | Nitrobenzene | 202-716-0 | 98-95-3 |
| 168 | Perfluorononan-1-oic acid and its sodium and ammonium salts | -<br>206-801-3<br>- | 375-95-1<br>21049-39-8<br>4149-60-4 |
| 169 | Benzo[def]chrysene | 200-028-5 | 50-32-8 |
| 170 | 4,4'-isopropylidenediphenol (Bisphenol A)<br>Note: Some suppliers of substrate materials have reported Bisphenol A as a raw polymer ingredient of <0.3wt%. This substance is contained in the material as a small residue in the molecular form and can not be released under normal conditions. | 201-245-8 | 80-05-7 |
| 171 | 4-Heptylphenol, branched and linear | - | - |
| 172 | Nonadecafluorodecanoic acid (PFDA) and its sodium and ammonium salts. This entry has the following member substances: | | |
| | Nonadecafluorodecanoic acid | 206-400-3 | 335-76-2 |
| | Ammonium nonadecafluorodecanoate | 221-470-5 | 3108-42-7 |
| | Decanoic acid, nonadecafluoro-, sodium salt | - | 3830-45-3 |
| 173 | p-(1,1-dimethylpropyl)phenol | 201-280-9 | 80-46-6 |
| 174 | Perfluorohexane-1-sulfonic acid and its salts (PFHxS) | - | - |
| 175 | Reaction products of 1,3,4-thiadiazolidine-2,5-dithione, formaldehyde and 4-heptylphenol, branched and linear (RP-HP) | - | - |
| 176 | Dodecachloropentacyclo[12.2.1.16,9.02,13.05,10]octadeca-7,15-diene ("Dechlorane Plus"™) | - | - |
| 177 | Chrysene | 205-923-4 | 218-01-9,<br>1719-03-5 |
| 178 | Cadmium nitrate | 233-710-6 | 10022-68-1,<br>10325-94-7 |
| 179 | Cadmium hydroxide | 244-168-5 | 21041-95-2 |
| 180 | Cadmium carbonate | 208-168-9 | 513-78-0 |
| 181 | Benz[a]anthracene | 200-280-6 | 56-55-3,<br>1718-53-2 |
| 182 | Octamethylcyclotetrasiloxane (D4) | 209-136-7 | 556-67-2 |
| 183 | Decamethylcyclopentasiloxane (D5) | 208-764-9 | 541-02-6 |
| 184 | Dodecamethylcyclohexasiloxane (D6) | 208-762-8 | 540-97-6 |
| 185 | Lead | 231-100-4 | 7439-92-1 |

**Table 1: Candidate List of SVHCs (Cont'd)**

| Item | Substance name | EC Number | CAS No. |
|---|---|---|---|
| 186 | Disodium octaborate | 234-541-0 | 12008-41-2 |
| 187 | Benzo[ghi]perylene | 205-883-8 | 191-24-2 |
| 188 | Terphenyl hydrogenated | 262-967-7 | 61788-32-7 |
| 189 | Ethylenediamine (EDA) | 203-468-6 | 107-15-3 |
| 190 | Benzene-1,2,4-tricarboxylic acid 1,2 anhydride (trimellitic anhydride) (TMA) | 209-008-0 | 552-30-7 |
| 191 | Dicyclohexyl phthalate (DCHP) | 201-545-9 | 84-61-7 |
| 192 | 2,2-bis(4'-hydroxyphenyl)-4-methylpentane | 401-720-1 | 6807-17-6 |
| 193 | Benzo[k]fluoranthene | 205-916-6 | 207-08-9 |
| 194 | Fluoranthene | 205-912-4 | 206-44-0 |
| 195 | Phenanthrene | 201-581-5 | 85-01-8 |
| 196 | Pyrene | 204-927-3 | 129-00-0 |
| 197 | 1,7,7-trimethyl-3-(phenylmethylene)bicyclo[2.2.1]heptan-2-one | 239-139-9 | 15087-24-8 |
| 198 | 2-methoxyethyl acetate | 203-772-9 | 110-49-6 |
| 199 | Tris(4-nonylphenyl, branched and linear) phosphite (TNPP) with ≥ 0.1% w/w of 4-nonylphenol, branched and linear (4-NP) | - | - |
| 200 | 2,3,3,3-tetrafluoro-2-(heptafluoropropoxy)propionic acid, its salts and its acyl halides (covering any of their individual isomers and combinations thereof) | - | - |
| 201 | 4-tert-butylphenol | 202-679-0 | 98-54-4 |
| 202 | Perfluorobutane sulfonic acid (PFBS) and its salts | - | - |
| 203 | Diisohexyl phthalate | 276-090-2 | 71850-09-4 |
| 204 | 2-methyl-1-(4-methylthiophenyl)-2-morpholinopropan-1-one<br>Note: With regard to 2-methyl-1-(4-methylthiophenyl)-2-morpholinopropan-1-one, some suppliers of substrate materials have reported it is used for Photoinitiator as <1.5wt% in the Concentration level. However does comply with Substrate:<0.1wt%(w/w) These substances are contained in the material as a small residue in the molecular form and cannot be released under normal conditions | 400-600-6 | 71868-10-5 |
| 205 | 2-benzyl-2-dimethylamino-4'-morpholinobutyrophenone | 404-360-3 | 119313-12-1 |
| 206 | Dibutylbis(pentane-2,4-dionato-O,O')tin | 22673-19-4 | 245-152-0 |
| 207 | butyl 4-hydroxybenzoate | 94-26-8 | 202-318-7 |
| 208 | 2-methylimidazole | 693-98-1 | 211-765-7 |
| 209 | 1-vinylimidazole | 1072-63-5 | 214-012-0 |
| 210 | bis(2-(2-methoxyethoxy)ethyl) ether | 205-594-7 | 143-24-8 |



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| Item | Substance name | EC Number | CAS No. |
|---|---|---|---|
| 211 | Dioctyltin dilaurate, stannane, dioctyl-, bis(coco acyloxy) derivs., and any other stannane, dioctyl-, bis(fatty acyloxy) derivs. wherein C12 is the predominant carbon number of the fatty acyloxy moiety | - | - |
| 212 | 1,4-dioxane | 204-661-8 | 123-91-1 |
| 213 | 2,2-bis(bromomethyl)propane-1,3-diol (BMP); 2,2-dimethylpropan-1-ol, tribromo derivative/3-bromo-2,2-bis(bromomethyl)-1-propanol (TBNPA); 2,3-dibromo-1-propanol (2,3-DBPA) | 221-967-7 | 3296-90-0<br>36483-57-5<br>1522-92-5<br>96-13-9 |
| 214 | 2-(4-tert-butylbenzyl)propionaldehyde and its individual stereoisomers | 799-970-2 | - |
| 215 | 4,4'-(1-methylpropylidene)bisphenol | 201-025-1 | 77-40-7 |
| 216 | glutaral | 203-856-5 | 111-30-8 |
| 217 | Medium-chain chlorinated paraffins (MCCP) [UVCB substances consisting of more than or equal to 80% linear chloroalkanes with carbon chain lengths within the range from C14 to C17] | 799-971-8 | - |
| 218 | Orthoboric acid, sodium salt | 237-560-2 | 13840-56-7 |
| 219 | Phenol, alkylation products (mainly in para position) with C12-rich branched or linear alkyl chains from oligomerisation, covering any individual isomers and/ or combinations thereof (PDDP) | 799-972-3 | - |
| 220 | 6,6'-di-tert-butyl-2,2'-methylenedi-p-cresol | 204-327-1 | 119-47-1 |
| 221 | tris(2-methoxyethoxy)vinylsilane | 213-934-0 | 1067-53-4 |
| 222 | (±)-1,7,7-trimethyl-3-[(4-methylphenyl)methylene]bicyclo[2.2.1]heptan-2-one covering any of the individual isomers and/or combinations thereof (4-MBC) | - | - |
| 223 | S-(tricyclo(5.2.1.02,6)deca-3-en-8(or 9)-yl O-(isopropyl or isobutyl or 2-ethylhexyl) O-(isopropyl or isobutyl or 2-ethylhexyl) phosphorodithioate | 401-850-9 | 255881-94-8 |
| 224 | N-(hydroxymethyl)acrylamide | 213-103-2 | 924-42-5 |
| 225 | 1,1'-[ethane-1,2-diylbisoxy]bis[2,4,6-tribromobenzene] | 253-692-3 | 37853-59-1 |
| 226 | 2,2',6,6'-tetrabromo-4,4'-isopropylidenediphenol | 201-236-9 | 79-94-7 |
| 227 | 4,4'-sulphonyldiphenol | 201-250-5 | 80-09-1 |
| 228 | Barium diboron tetraoxide | 237-222-4 | 13701-59-2 |
| 229 | Bis(2-ethylhexyl) tetrabromophthalate covering any of the individual isomers and/or combinations thereof | - | - |
| 230 | Isobutyl 4-hydroxybenzoate | 224-208-8 | 4247-02-3 |
| 231 | Melamine | 203-615-4 | 108-78-1 |
| 232 | Perfluoroheptanoic acid and its salts | - | - |



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| | | | |
|---|---|---|---|
| 233 | reaction mass of 2,2,3,3,5,5,6,6-octafluoro-4-(1,1,1,2,3,3,3-heptafluoropropan-2-yl)morpholine and 2,2,3,3,5,5,6,6-octafluoro-4-(heptafluoropropyl)morpholine | 473-390-7 | - |

## References

Questions in relation to this REACH statement to Technical Support: http://www.xilinx.com/support/service-portal/contact-support.html

## Revision History

The following table shows the revision history for this document.

| Date | Version | Description of Revisions |
|---|---|---|
| 03/02/10 | 1.0 | Initial Xilinx release. Created from REACH Position Statement (Rev 2.0) dated July, 2009. |
| 07/06/10 | 1.1 | Added items 30 through to 38 to Table 1 |
| 02/25/11 | 1.2 | Added items 39 through to 46 in Table 1 |
| 05/20/11 | 1.3 | Expand applicability of statement to Xilinx development products |
| 08/19/11 | 1.4 | 1. Revise Xilinx position from importer to supplier<br>2. Re-ordered list of SVHCs chronologically<br>3. Added items 47 through to 53 in Table 1<br>4. Expand applicability of statement to packing material<br>5. Include statement of compliance to restrictions listed in REACH Annex XVII<br>6. Update Xilinx contact details |
| 02/06/12 | 1.5 | Added items 54 through to 73 in Table 1. |
| 07/06/12 | 1.6 | 1. Add the word “intentionally” in para. 4 of Xilinx responsibilities In Table 1<br>2. Consolidate entries of aluminosilicate refractory ceramic fibres (Al- RCF) and zirconia aluminosilicate refractory ceramic fibres (ZrAl- RCF).<br>3. Add 13 items 72 through to 84. |
| 03/08/13 | 1.7 | Add 54 items 85 through to 138 |
| 08/20/13 | 1.8 | Add 6 items 138 through to 144 |
| 01/02/14 | 1.9 | Add 7 items 144 to 151 |
| 07/19/14 | 1.10 | Add 4 items 152 to 155 |
| 02/06/15 | 1.11 | Add 6 items 156 to 161. Remove %W/W column as text in Xilinx Responsibilities covers the intent of the content in this column. |
| 08/14/15 | 1.12 | Add 2 items 162 to 163. Update Technical Support Link |



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| | | |
|---|---|---|
| 02/05/16 | 1.13 | Add 5 items 164 to 168 |
| 08/12/16 | 1.14 | Add 1 item 169 |
| 01/25/17 | 1.15 | Add 4 items 170 to 173 |
| 07/11/17 | 1.16 | Add 1 item 174 |
| 3/15/2018 | 1.17 | 1. Updated REACH link<br>2. Added notes for item 76 & item 170.<br>3. Added item 175 to 181. |
| 9/27/2018 | 1.18 | Add Candidate List obligations.<br>Add note for Lead.<br>Add item 182 to 191. |
| 3/22/2019 | 1.19 | Add items 192 to 197 to Candidate List for 15 January 2019 SVHC |
| 9/27/2019 | 1.20 | Add items 198 to 201 to Candidate List |
| 2/28/2020 | 1.21 | Add items 202 to 205 to Candidate List |
| 8/31/2020 | 1.22 | Add note for (#204) 2-methyl-1-(4-methylthiophenyl)-2-morpholinopropan-1-one<br>Add items 206 to 209 to Candidate List. |
| 4/8/2021 | 1.23 | Added items 210 to 211. (19th Jan 2021, European Chemicals Agency (ECHA) published the 24th batch of SVHC Candidate List) |
| 11/25/2021 | 1.24 | Added items 212 to 219. (8th July 2021, European Chemicals Agency (ECHA) published the 24th batch of SVHC Candidate List) |
| 3/23/2022 | 1.25 | Added items 220 to 223. (17th January 2022, European Chemicals Agency (ECHA) published the 24th batch of SVHC Candidate List) |
| 3/23/2023 | 1.26 | Added items 224 (10th July 2022, European Chemicals Agency (ECHA) |
| 3/30/3023 | 1.27 | Added items 225 to 233 (17th January 2023, European Chemicals Agency (ECHA) |

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## 7 Series FPGA Ordering Information

Table 12 shows the speed and temperature grades available in the different device families. Some devices might not be available in every speed and temperature grade.

*Table 12:* **7 Series Speed Grade and Temperature Ranges**

| Device Family | Devices | Speed Grade, Temperature Range, and Operating Voltage | | | |
|---|---|---|---|---|---|
| | | Commercial (C) 0°C to +85°C | Extended (E) 0°C to +100°C | Industrial (I) –40°C to +100°C | Expanded (Q) –40°C to +125°C |
| Spartan-7 | All | -2C (1.0V) | | -2I (1.0V) | |
| | | -1C (1.0V) | | -1I (1.0V) | -1Q (1.0V) |
| | | | | -1LI (0.95V) | |
| Artix-7 | All | | -3E (1.0V) | | |
| | | -2C (1.0V) | | -2I (1.0V) | |
| | | | -2LE (1.0V or 0.9V) | | |
| | | -1C (1.0V) | | -1I (1.0V) | |
| | | | | -1LI (0.95V) | |
| Kintex-7 | XC7K70T | | -3E (1.0V) | | |
| | | -2C (1.0V) | | -2I (1.0V) | |
| | | | -2LE (1.0V or 0.9V) | | |
| | | -1C (1.0V) | | -1I (1.0V) | |
| | XC7K160T XC7K325T XC7K355T XC7K410T XC7K420T XC7K480T | | -3E (1.0V) | | |
| | | -2C (1.0V) | | -2I (1.0V) | |
| | | | -2LE (1.0V or 0.9V) | -2LI (0.95V) | |
| | | -1C (1.0V) | | -1I (1.0V) | |
| Virtex-7 T | XC7V585T | | -3E (1.0V) | | |
| | | -2C (1.0V) | | -2I (1.0V) | |
| | | | -2LE (1.0V) | | |
| | | -1C (1.0V) | | -1I (1.0V) | |
| | XC7V2000T | -2C (1.0V) | | | |
| | | | -2GE (1.0V) | | |
| | | | -2LE (1.0V) | | |
| | | -1C (1.0V) | | -1I (1.0V) | |
| Virtex-7 XT | XC7VX330T XC7VX415T XC7VX485T XC7VX550T XC7VX690T | | -3E (1.0V) | | |
| | | -2C (1.0V) | | -2I (1.0V) | |
| | | | -2LE (1.0V) | | |
| | | -1C (1.0V) | | -1I (1.0V) | |
| | XC7VX980T | -2C (1.0V) | | | |
| | | | -2LE (1.0V) | | |
| | | -1C (1.0V) | | -1I (1.0V) | |
| | XC7VX1140T | -2C (1.0V) | | | |
| | | | -2GE (1.0V) | | |
| | | | -2LE (1.0V) | | |
| | | -1C (1.0V) | | -1I (1.0V) | |
| Virtex-7 HT | All | -2C (1.0V) | | | |
| | | | -2GE (1.0V) | | |
| | | | -2LE (1.0V) | | |
| | | -1C (1.0V) | | | |

The Spartan-7 FPGA ordering information is shown in Figure 1. Refer to the Package Marking section of UG475, *7 Series FPGAs Packaging and Pinout* for a more detailed explanation of the device markings.

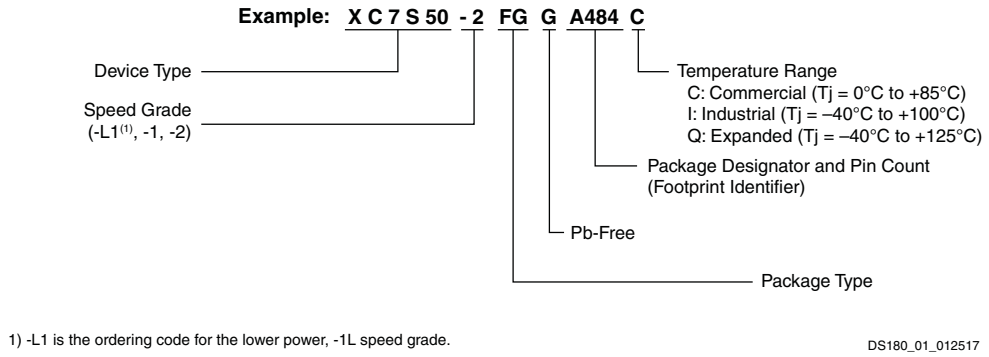



*Figure 1:* **Spartan-7 FPGA Ordering Information**

The Artix-7, Kintex-7, and Virtex-7 FPGA ordering information, shown in Figure 2, applies to all packages including Pb-Free. Refer to the Package Marking section of UG475, *7 Series FPGAs Packaging and Pinout* for a more detailed explanation of the device markings.

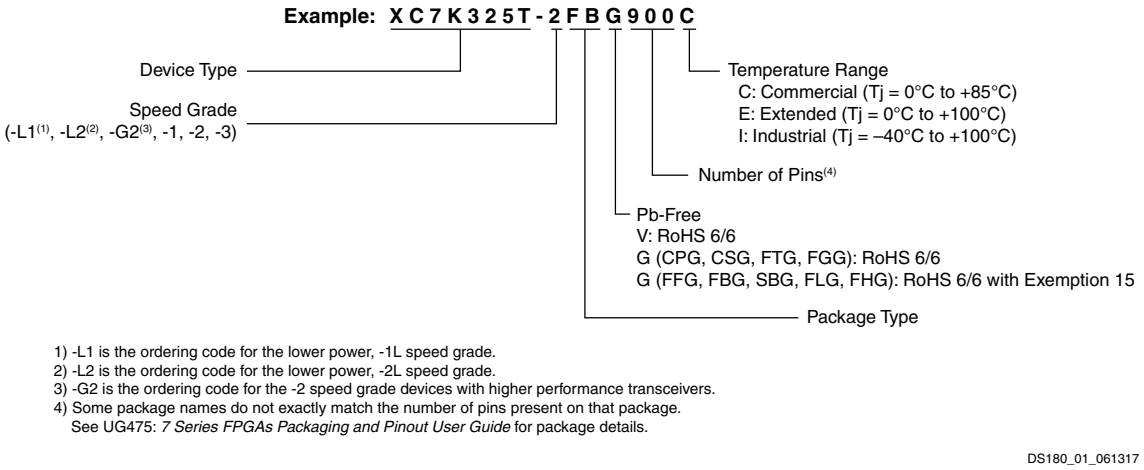



*Figure 2:* **Artix-7, Kintex-7, and Virtex-7 FPGA Ordering Information**

Chapter 6

# Package Marking

## Introduction

All 7 series devices (Spartan®-7, Artix®-7, Kintex®-7, and Virtex®-7 FPGAs) have package top-markings similar to the examples shown in Figure 6-1, Figure 6-2, Figure 6-3, and Figure 6-4. The markings are explained in Table 6-1.

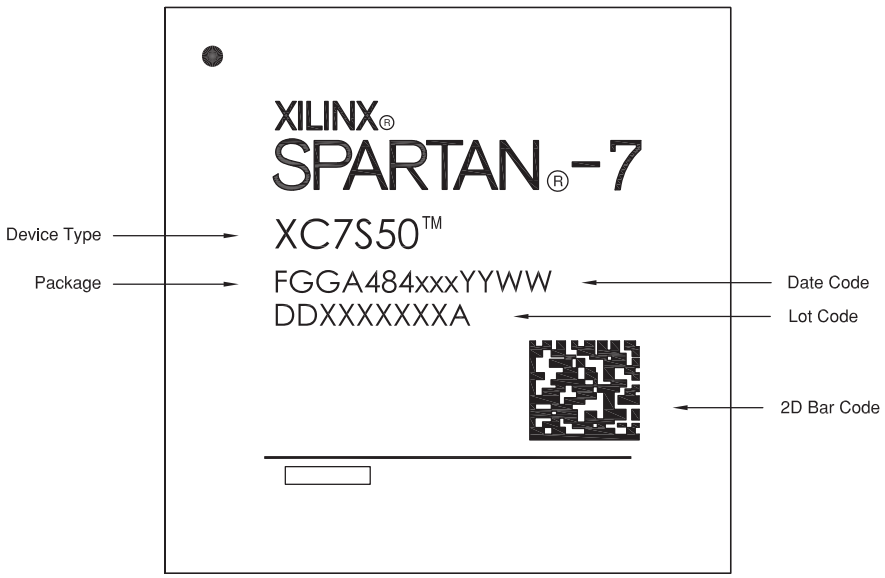



*Figure 6-1:* **Spartan-7 Device Package Marking**

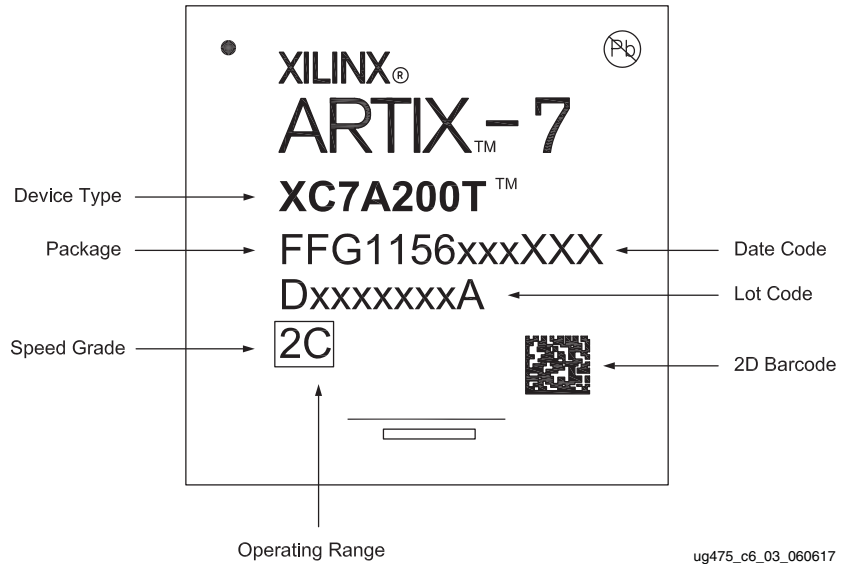



*Figure 6-2:* **Artix-7 Device Package Marking**




*Figure 6-3:* **Kintex-7 Device Package Marking**




*Figure 6-4:* **Virtex-7 Device Package Marking**

*Table 6-1:* **Xilinx Device Marking Definition—Example**

| Item | Definition |
|---|---|
| Xilinx Logo | Xilinx logo, Xilinx name with trademark, and trademark-registered status. |
| Pb-free Character | For FFG, FBG, or SBG packages, a Pb-free character is marked in the upper right corner of the device to denote that the device is manufactured using a lead-free material set as described in *Cross-ship of Lead-free Bump and Substrates in Lead-free (FFG/FBG/SBG) Packages* (XCN16022). |
| Family Brand Logo | Device family name with trademark and trademark-registered status. This line is optional and could appear blank. |
| 1st Line | Device type. |
| 2nd Line | Package code, circuit design revision, the location code for the wafer fab, the geometry code, and date code.<br>A *G* (or V) in the third letter of a package code indicates a Pb-free RoHS compliant package. For more details on Xilinx Pb-Free and RoHS Compliant Products, see: www.xilinx.com/pbfree. |
| 3rd Line | Ten alphanumeric characters for Assembly, Lot, and Step information. The last digit is usually an *A* or an *M* if a stepping version does not exist. |

*Table 6-1:* **Xilinx Device Marking Definition—Example *(Cont'd)***

| Item | Definition | |
|---|---|---|
| 4th Line | When marked, this line describes the device speed grade and temperature range. For more information on the ordering codes, see the *7 Series FPGAs Overview* (DS180).<br>Other variations for the 4th line: | |
| | L2E | The *L2E* indicates a -2LE device. The -2LE speed grade offers reduced maximum power consumption. Artix-7 and Kintex-7 FPGAs are capable of operating at lower core voltage. The E is for the extended temperature operating range. For more information, see the specific device data sheets at: 7 series FPGAs. |
| | 1C xxxx | The *xxxx* indicates the SCD for the device. An SCD is a special ordering code that is not always marked in the device top mark. |
| | 1C ES | The addition of an *ES* indicates an Engineering Sample. |
| | This line is not marked on some devices. Refer to the bar code for device speed grade and temperature range information. | |
| Bar Code | A device-specific bar code is marked on each device. Refer to the *FAQ: Top Marking Change for 7 Series, UltraScale, and UltraScale+ Products* (XTP424). | |