DATA IMAGE CORPORATION
PRODUCT SPECIFICATION
MODEL NO.: FC310500DSSWNG01

☐ Preliminary Specification
■ Approval Specification

2AAD617003T(T0203)

Customer :
APPROVED BY

設計驗證
工程課
2023.10.27
發行
鈺鐘科技開發股份有限公司

SIGNATURE **DATE**

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Issued Date	Revision
20/OCT/23’	A

2. RECORD OF REVISION

Rev	Date	Item	Page	Comment	Source
1	02/AUG/21'	All	All	Initial Preliminary	ESR1007018
2	17/NOV/21'	All	All	Modify Part No. from FC310500DSSWBG01 to FC310500DSSWNG01	ESR1007018
3	02/MAY/22'	6.1	22	Modify Outline Drawing from Rev. 1 to 2 2)Remove peeling tape & Change Notes to Table Notes	ECR110-M40001
4	05/AUG/22'	1.2 6.1	4 22	Modify LCD Outline Dimension Modify Outline Drawing from Rev. 2 to 3 3)Modify cover lens outline and icon dimensions	NPDO-2418
A	20/OCT/23'	6.1 8.2	22 26	Modify Outline Drawing from Rev.3 to A A) Change the drawing from Rev.3 to Rev. A. Add CARTON PACKAGE Release Rev: A for production.	NPPR-230728002
				在這裡輸入文字	

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1. GENERAL DESCRIPTION

1.1 OVERVIEW

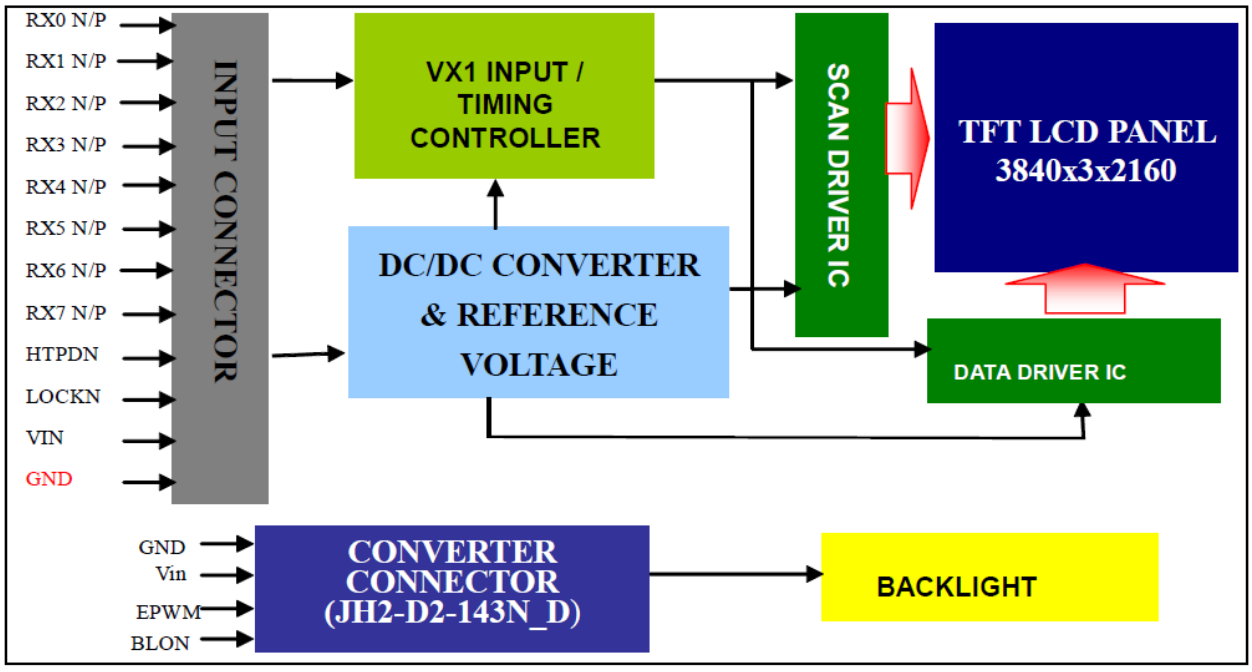
FC310500DSSWBG01 is a 31.5” (31.5” diagonal) a-Si & transmissive type thin film transistor liquid crystal display (TFT-LCD) module with RGB interface The module is composed of a TFT-LCD panel, driver circuit, and backlight unit.

1.2 TFT LCD MODULE SPECIFICATIONS

The following items are characteristics summary on the table under 25℃ condition :

Parameter	Specifications	Unit
Screen Size	31.5(diagonal)	inch
LCD Outline Dimension	751.4(H) x 448.65(V) x 28.2Max(D)	mm
LCD Active Area	697.31(H) x 392.23(V)	mm
Resolution	3840(H) x RGB x 2160(V)	
Pixel Pitch	0.181(H) x 0.181(V)	mm
Pixel Arrangement	RGB vertical stripe	
Display Mode	Normally Black	
Display Colors	1.073G	
View direction	All	
Luminance, White	800	cd/m^2
LCD Interface	RGB	
Surface treatment	AR+AF Coating	
RoHS Compliance	Yes	

2. FUNCITONAL BLOCK DIAGRAM

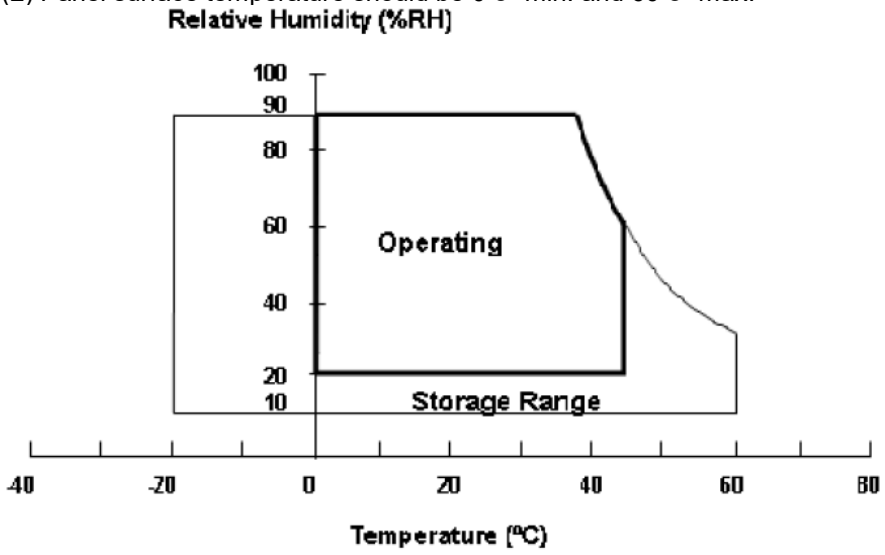


3.ABSOLUTE MAXIMUM RATINGS

3.1 ABSOLUTE RATINGS OF ENVIRONMENT

Parameter	Symbol	MIN.	MAX.	Unit	Remark
Operating temperature	TOP	0	45	°C	
Storage temperature	TST	-20	60	°C	

Note (1)
(a) 90 %RH Max..
(b) Wet-bulb temperature should be 39 ℃ Max.
(c) No condensation.
Note (2) Panel surface temperature should be 0℃ min. and 60℃ max.



3.2 ELECTRICAL ABSOLUTE RATINGS

Parameter	Symbol	MIN.	MAX.	Unit	Remark
Power Supply Voltage	VCCS	-0.3	13.5	V	Note1
Logic Input Voltage	VIN	-0.3	3.6	V	
LED Forward Current Per Input Pin	IF	-	20	mA	Note1,2 Duty=100%

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.
Note (2) Specified values are for input pin of LED light bar at Ta=25±2 ℃ (Refer to 4.3.3 and 4.3.4 for further information).

4. ELECTRICAL SPECIFCATIONS

4.1 ELECTRICAL CHARACTERISTICS

4.1.1 TFT LCD MODULE ELETRONICS SPECIFICATION

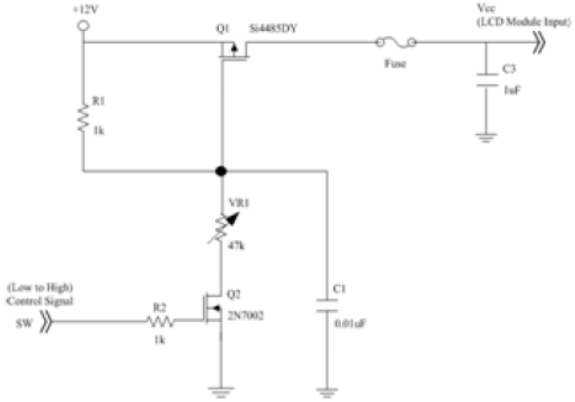
Ta=25°C

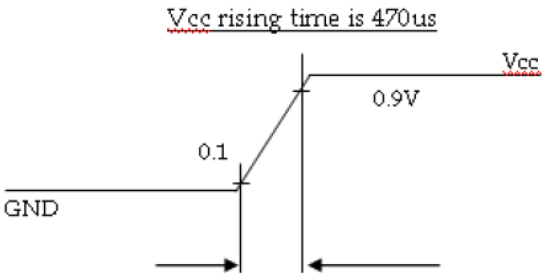
Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
Power Supply Voltage		VCC	10.8	12	13.2	V	Note1
Rush Current		IRUSH	-	-	2.6	A	Note2
Power Consumption	White Pattern	PT	-	17.4	19.8	W	Note3
	Black Pattern	PT	-	9.96	12.24	W	Note3
	Horizontal Stripe	PT	-	16.8	19.2	W	Note3
Power Supply Current	White Pattern	-	-	1.45	1.65	A	Note3
	Black Pattern	-	-	0.83	1.02	A	Note3
	Horizontal Stripe	-	-	1.4	1.6	A	Note3

V-by-One HS	Differential Input High Threshold Voltage	VLVTH	-	-	+50	mV	
	Differential Input Low Threshold Voltage	VLVTL	-50	-	-	mV	
	Differential Input Resistor	RRIN	80	100	120	ohm	
CMOS interface	Input High Threshold Voltage	VIH	2.7	-	3.3	V	
	Input Low Threshold Voltage	VIL	0	-	0.7	V	

Note (1) The module should be always operated within the above ranges. The ripple voltage should be controlled under 10 % of Vcc (Typ.)

Note (2) Measurement Conditions





Note (3) The specified power supply current is under the conditions at Vcc = 12 V, Ta = 25 ± 2 ºC, Fr = 60Hz, whereas a power dissipation check pattern below is displayed.

a. White Pattern



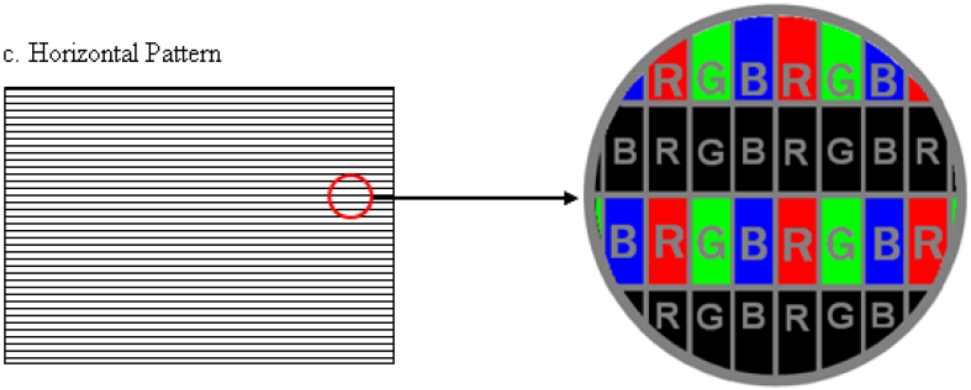
Active Area

b. Black Pattern

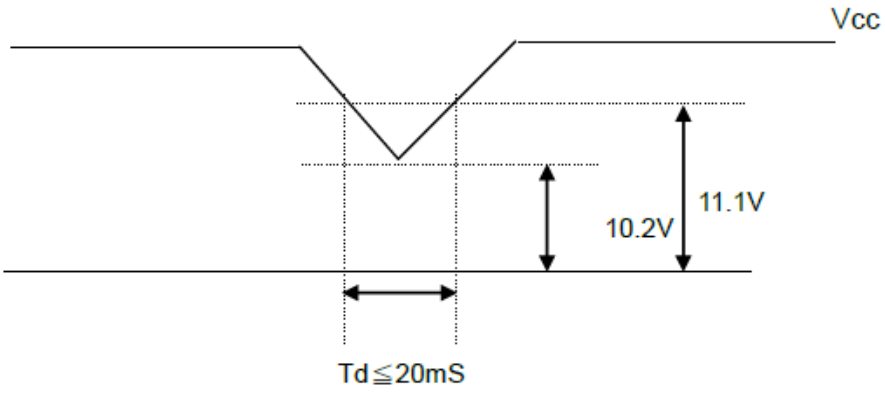


Active Area

c. Horizontal Pattern



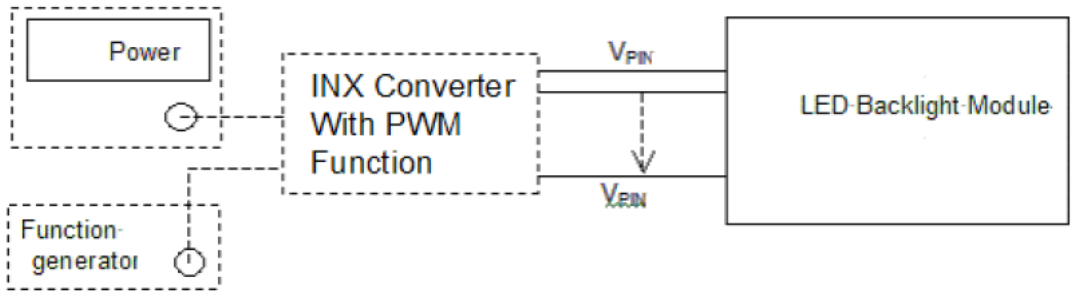
Vcc Power Dip Condition



4.1.2 BACKLIGHT UNIT SPECIFICATION

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED voltage	V_F	37.7	41.6	44.2	V	Note1 Duty=100%, IPIN=(145)mA
LED current	I_F	--	145	--	mA	Note1,2 Duty=100%
LED power consumption	P	--	96.5	102.5	W	Note1 Duty=100%, IPIN=(145)mA
LED Life Time		30,000	--	--	Hour	Note 3

Note (1) LED light bar input voltage and current are measured by utilizing a true RMS multimeter as shown below:
Note (2) PBL = IPIN × VPIN × (16) input pins.
Note (3) The lifetime of LED is estimated data and defined as the time when LED packages continue to operate under the conditions at Ta = 25 ±2 ℃ and I= (145) mA (per chip) until the brightness becomes ≦ 50% of its original value. Operating LED under high temperature environment will reduce life time and lead to color shift.
Note (4) The module must be operated with constant driving current.
Note (5) If converter has PWM function, the PWM Frequency setting must be equal to 200Hz.

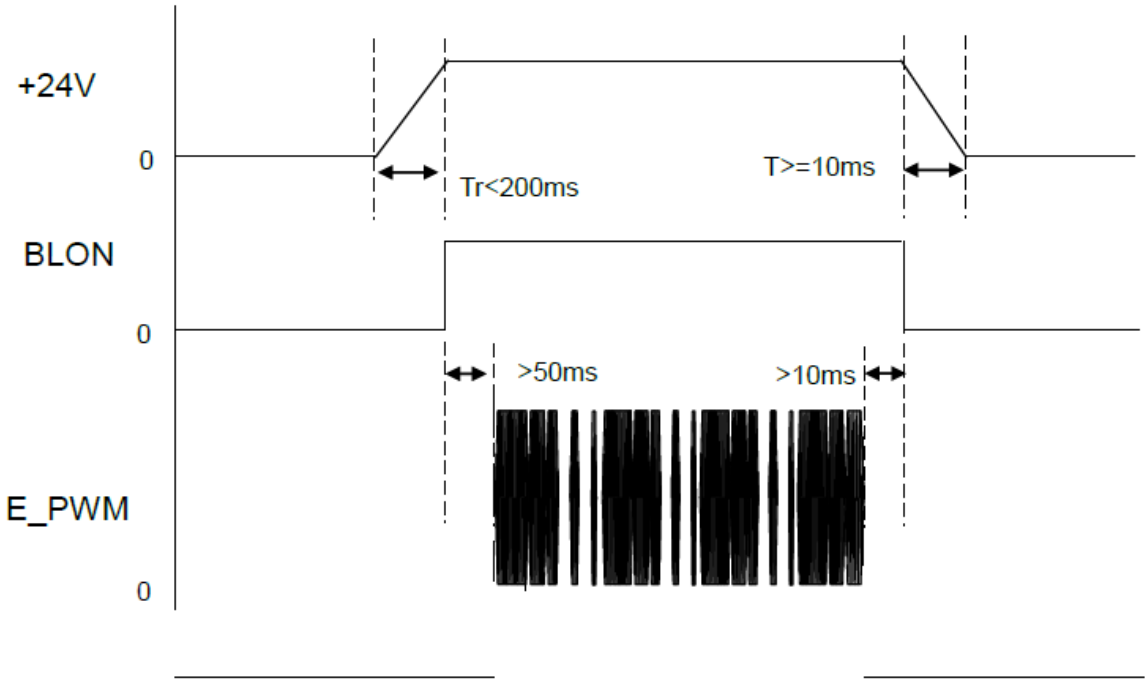


4.1.3 CONVERTER ELECTRICAL CHARACTERISTICS

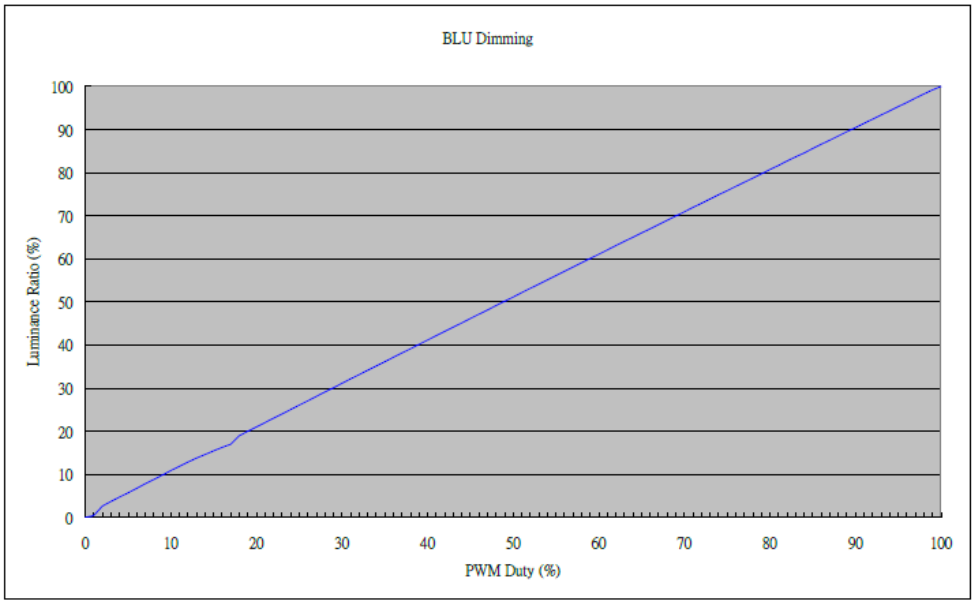
Ta=25°C

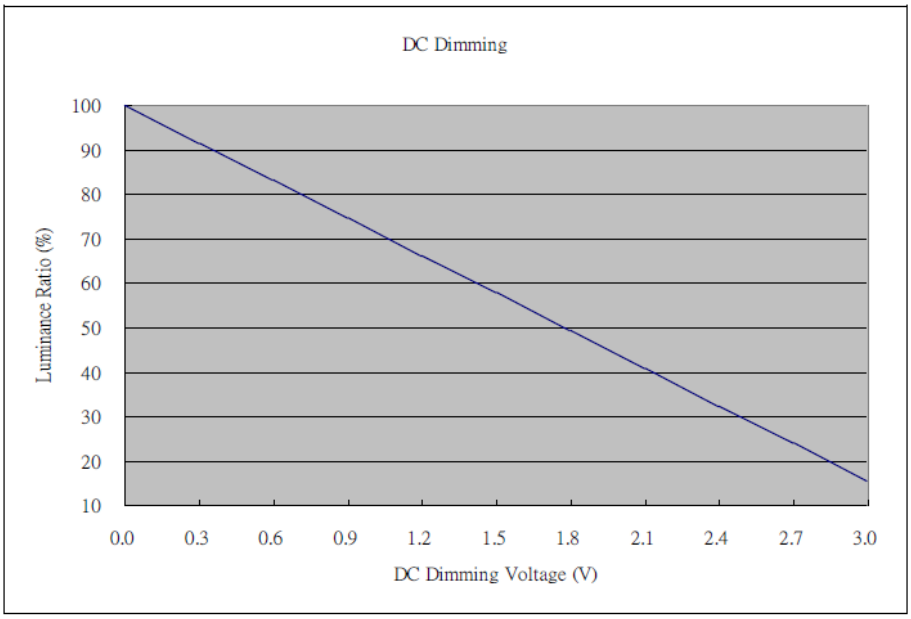
Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
Converter Power Supply Voltage		V_i	21.6	24.0	26.4	V	(Duty 100%)
Converter Power Supply Current		I_i	-	4.2	5	A	@ Vi = 24V (Duty 100%)
Input Power Consumption		P_O	-	100.8	120	W	@ Vi = 24V (Duty 100%)
BL Control Level	Backlight on	BLON	2	3.3	5	V	
	Backlight off		0	0	0.15	V	
SEL Control Level	SEL High Level	SEL	2	3.3	5	V	DC_Dimming
	SEL Low Level		0	0	0.15	V	PWM Dimming
PWM Control Level	PWM High Level	E_PWM	2	3.3	5	V	Positive Dimming
	PWM Low Level		0	0	0.15	V	
DC Control Level	High Level	DC_Dimming	-	-	0	V	Negative dimming
	Low Level		3	-	-	V	
PWM Control Duty Ratio			5	-	100	%	f_{PWM} =200Hz
PWM Control Frequency		f_{PWM}	100	200	20K	Hz	Note1

Note (1) The minimum PWM control duty ratio will be 20% when PWM control frequency is operated in 20KHz.
Power sequence and control signal timing are shown in the following figure



Note： While system is turned ON or OFF, the power sequences must follow as below descriptions
Turn ON sequence: Vi(+24V) → BLON → E_PWM signal
Turn OFF sequence: E_PWM signal → BLON → Vi(+24V)
The definition of T_r : the time period of 10%*V_i to 90%*V_i
The definition of T_f : the time period of 90%*V_i to 10%*V_i
The following chart is the BLU Dimming for your reference.


BLU Dimming
Luminance Ratio (%)
100
90
80
70
60
50
40
30
20
10
0
0
10
20
30
40
50
60
70
80
90
100
PWM Duty (%)


DC Dimming
Luminance Ratio (%)
100
90
80
70
60
50
40
30
20
10
0.0
0.3
0.6
0.9
1.2
1.5
1.8
2.1
2.4
2.7
3.0
DC Dimming Voltage (V)

4.2 SIGNAL CHARACTERISTICS

4.2.1 DISPLAY TIMING SPECIFICATION

The input signal timing specifications are shown as the following table and timing diagram.

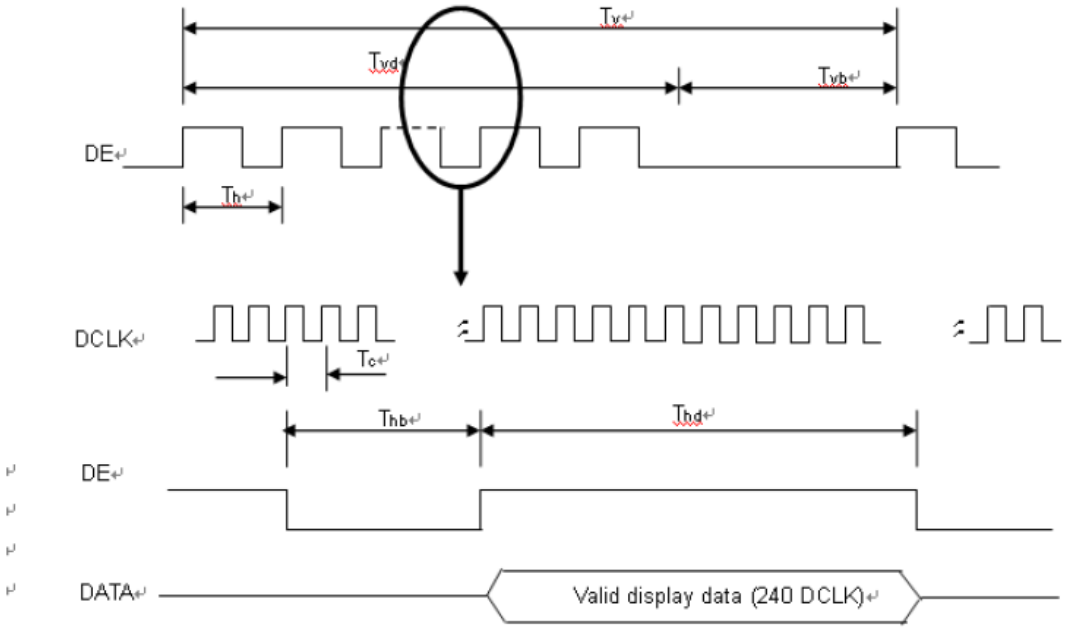
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Remark
V by One	Frequency	Fc	70	74.25	80	MHz	Note1
	Intra-Pair skew		-0.3	-	0.3	UI	Note2
	Inter-Pair skew		-5	-	5	UI	Note3
	Spread spectrum modulation range	Fclkin_mod	F_{clkin}-0.5%	-	F_{clkin}+0.5%	MHz	Note4
	Spread spectrum modulation frequency	F_{SSM}	-	-	30	KHz	Note4
Vertical Display Term	Frame Rate	Fr	48	60	62.5	Hz	Note5,6
	Total	Tv	2200	2250	2790	Th	Tv=Tvd+Tvb Note7
	Active Display	Tvd	2160	2160	2160	Th	
	Blank	Tvb	40	90	630	Th	
Horizontal Display Term	Total	Th	530	550	570	Tc	Th=Thd+Thb
	Active Display	Thd	480	480	480	Tc	
	Blank	Thb	50	70	90	Tc	

Note (1) Please make sure the range of pixel clock has follow the below equation:

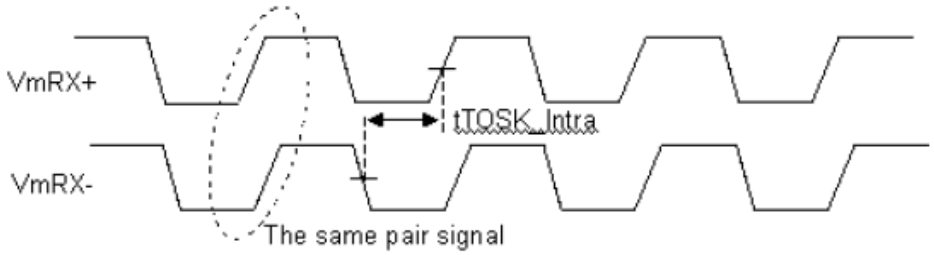
Fclkin(max) ≧ Fr × Tv × Th

Fr × Tv × Th ≧ Fclkin (min)

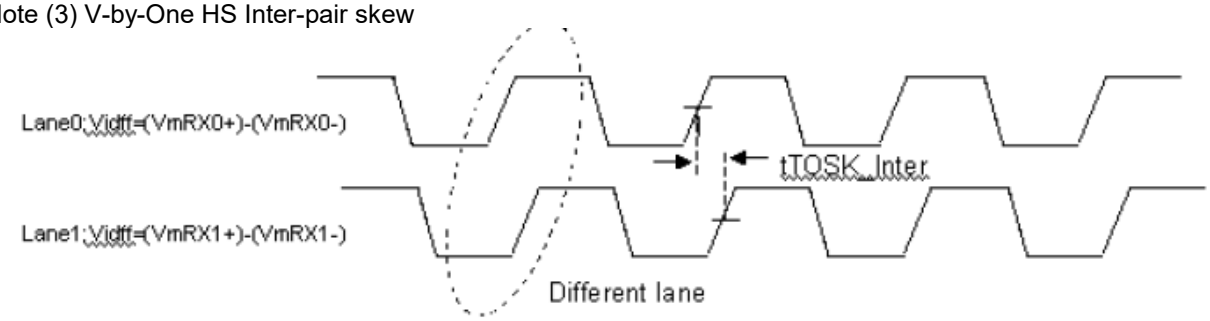
INPUT SIGNAL TIMING DIAGRAM



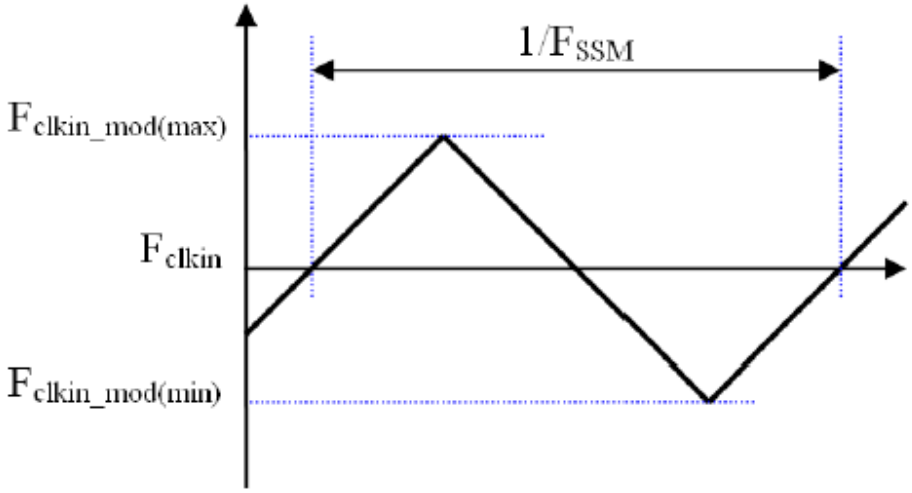
Note (2) V-by-One HS Intra-pair skew



Note (3) V-by-One HS Inter-pair skew

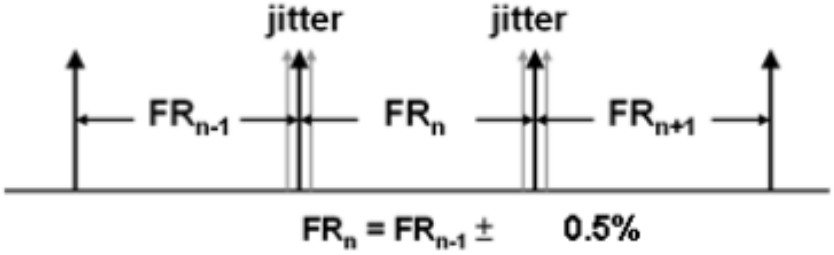


Note (4) The SSCG (Spread spectrum clock generator) is defined as below figures.



Note (5) The frame-to-frame jitter of the input frame rate is defined as the above figures. FRn = FRn-1 ± 0.5%.

Note (6) The setup of the frame rate jitter > 0.5% may result in the cosmetic LED backlight symptom and the electric function is affected.



Note (7) The Tv(Tvd+Tvb) must be integer, otherwise, this module would operate abnormally.

4.2.2 V BY ONE INPUT SIGNAL TIMING DIAGRAM

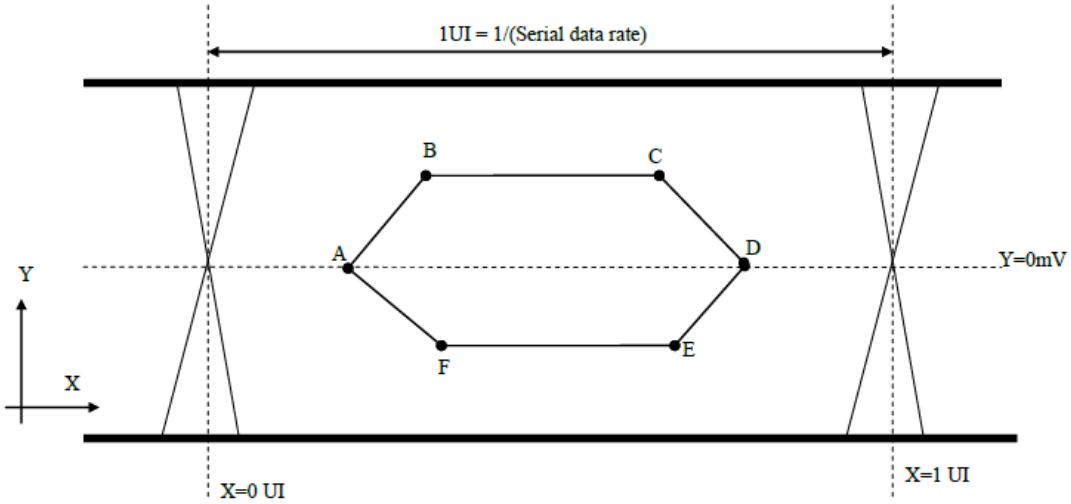


Table 1 Eye Mask Specification

	X [UI]	Y [mV]	Note
A	0.25	0	Note1
B	0.3	50	Note1
C	0.7	50	Note1
D	0.75	0	Note1
E	0.7	-50	Note1
F	0.3	-50	Note1

Note (1) Input levels of V-by-One HS signals are comes from “V-by-One HS Stander Ver.1.4”

4.2.3 BYTE LENGTH AND COLOR MAPPING OF V-BY-ONE HS

Packer input & Unpacker output		30bpp RGB (10bit)
Byte 0	D[0]	R[2]
	D[1]	R[3]
	D[2]	R[4]
	D[3]	R[5]
	D[4]	R[5]
	D[4]	R[6]
	D[5]	R[7]
	D[6]	R[8]
	D[7]	R[9]
Byte 1	D[8]	G[2]
	D[9]	G[3]
	D[10]	G[4]
	D[11]	G[5]
	D[12]	G[6]
	D[13]	G[7]
	D[14]	G[8]
	D[15]	G[9]
Byte 2	D[16]	B[2]
	D[17]	B[3]
	D[18]	B[4]
	D[19]	B[5]
	D[20]	B[6]
	D[21]	B[7]
	D[22]	B[8]
	D[23]	B[9]

Byte 3	D[24]	X
	D[25]	X
	D[26]	B[0]
	D[27]	B[1]
	D[28]	G[0]
	D[29]	G[1]
	D[30]	R[0]
	D[31]	R[1]

4.2.4 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 10-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																													
		Red										Green										BLUE									
		R9	R8	G7	G6	R5	R4	R3	R2	R1	R0	G9	G8	G7	G6	G5	G4	G3	G2	G1	G0	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
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	Red(1021)	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1022)	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1023)	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
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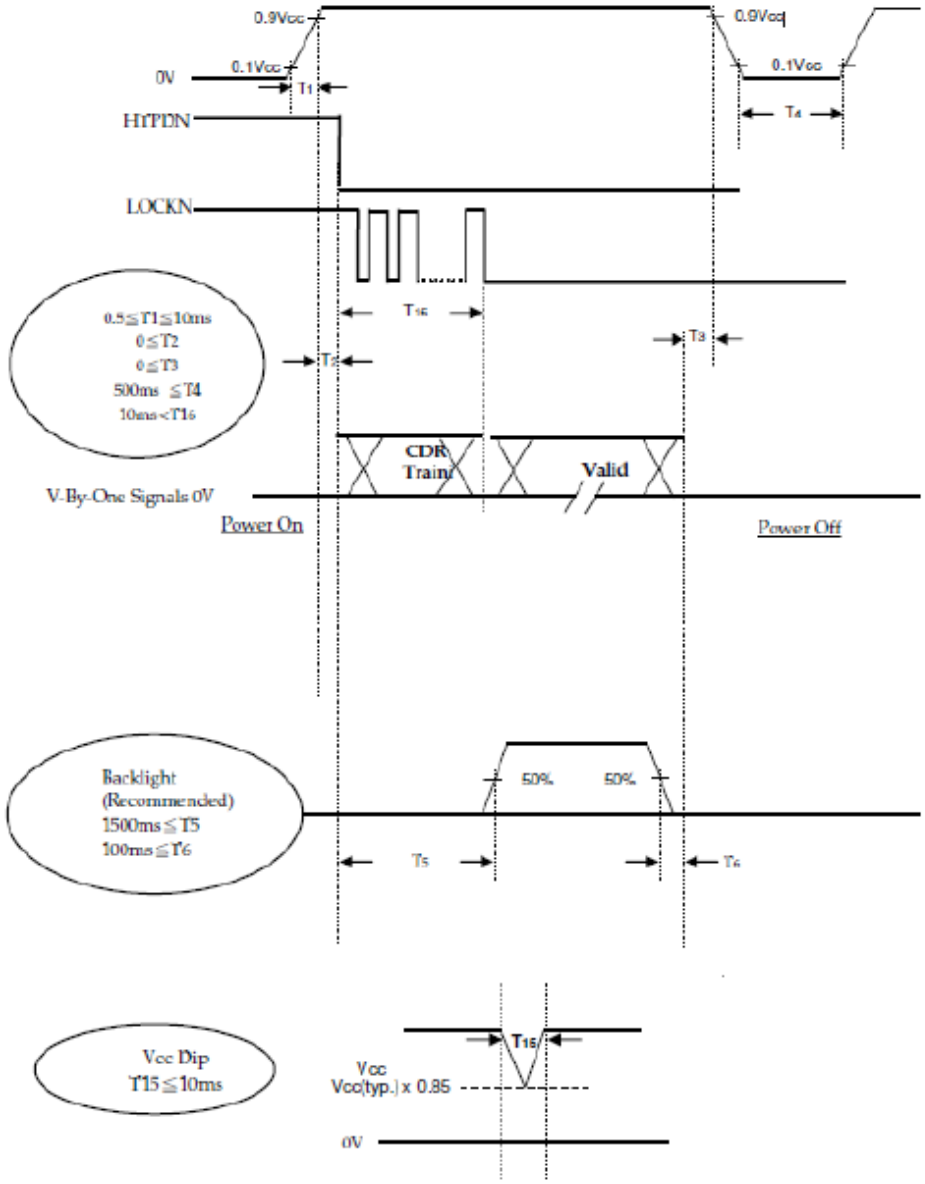
	Green(1021)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
	Green(1022)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	Green(1023)	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(1021)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1
	Blue(1022)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	Blue(1023)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

Note (1) 0: Low Level Voltage, 1: High Level Voltage

4.2.5 POWER ON OFF SEQUENCE

(Ta = 25 ± 2 ºC)

To prevent a latch-up or DC operation of LCD module, the power on/off sequence should be as the diagram below.



Note (1) The supply voltage of the external system for the module input should follow the definition of Vcc.

Note (2) Apply the LED voltage within the LCD operation range. When the backlight turns on before the LCD operation or the LCD turns off before the backlight turns off, the display may momentarily become abnormal screen..

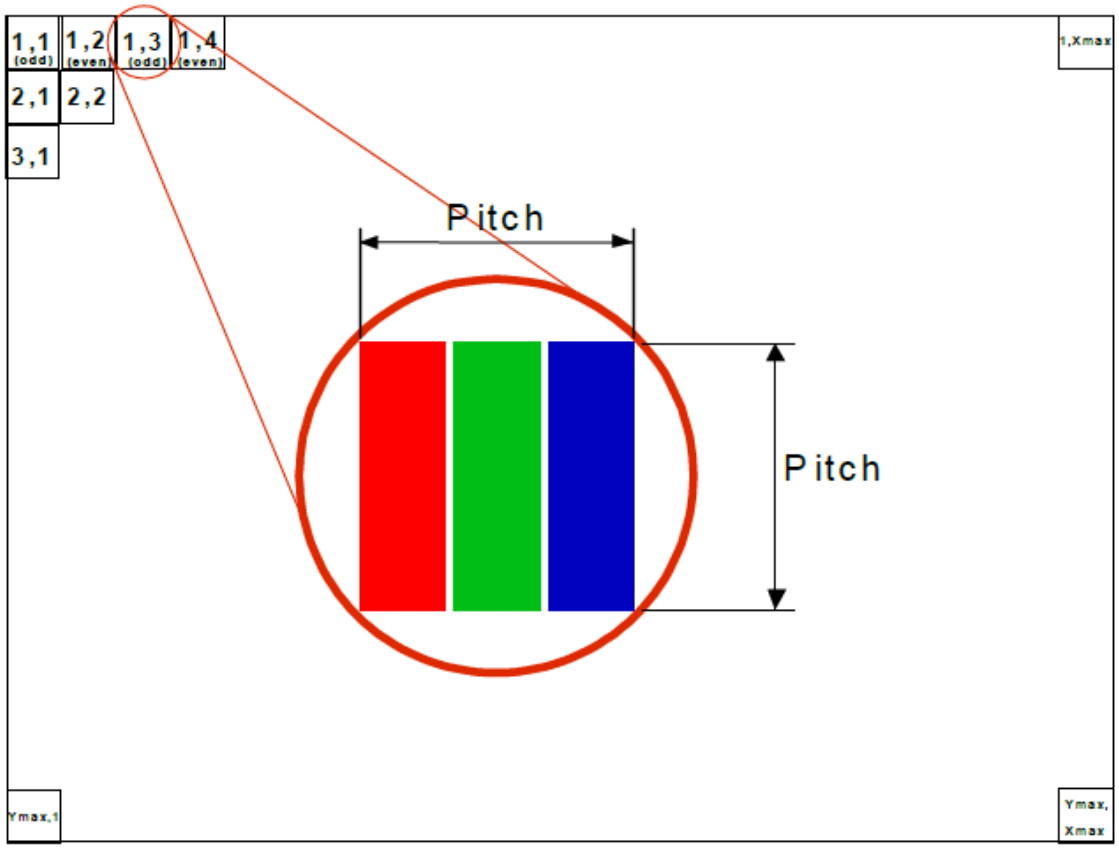
Note (3) In case of Vcc is in off level, please keep the level of input signals on the low or high impedance. If T2<0, that maybe cause electrical overstress failure.

Note (4) T4 should be measured after the module has been fully discharged between power off and on period..

Note (5) Interface signal shall not be kept at high impedance when the power is on

Note (6) Vcc must decay smoothly when power-off

4.3 PIXEL FORMAT IMAGE



4.4 INTERFACE CONNECTIONS

4.4.1 CN1 PIN ASSIGNMENT

Pin No.	Symbol	Description	Note
1	Vin	Power input (+12V)	
2	Vin	Power input (+12V)	
3	Vin	Power input (+12V)	
4	Vin	Power input (+12V)	
5	Vin	Power input (+12V)	
6	Vin	Power input (+12V)	
7	Vin	Power input (+12V)	
8	Vin	Power input (+12V)	
9	NC	No Connection	Note2
10	GND	Ground	
11	GND	Ground	
12	GND	Ground	
13	GND	Ground	
14	GND	Ground	
15	NC	No Connection	Note2
16	NC	No Connection	Note2
17	NC	No Connection	Note2
18	NC	No Connection	Note2
19	NC	No Connection	Note2
20	NC	No Connection	Note2
21	NC	No Connection	Note2
22	NC	No Connection	Note2
23	NC	No Connection	Note2
24	NC	No Connection	
25	HTPDN	Hot plug detect output, Open drain.	
26	LOCKN	Lock detect output, Open drain.	
27	GND	Ground	
28	RX0N	Pixel Negative Vby One differential data input in area A. Lan 0	Note1
29	RX0P	Pixel Positive Vby One differential data input in area A. Lan 0	
30	GND	Ground	
31	RX1N	Pixel Negative Vby One differential data input in area A. Lan 1	Note1
32	RX1P	Pixel Positive Vby One differential data input in area A. Lan 1	
33	GND	Ground	
34	RX2N	Pixel Negative Vby One differential data input in area A. Lan 2	Note1
35	RX2P	Pixel Positive Vby One differential data input in area A. Lan 2	
36	GND	Ground	
37	RX3N	Pixel Negative Vby One differential data input in area A. Lan 3	Note1
38	RX3P	Pixel Positive Vby One differential data input in area A. Lan 3	
39	GND	Ground	
40	RX4N	Pixel Negative Vby One differential data input in area A. Lan 4	Note1

41	RX4P	Pixel Positive Vby One differential data input in area A. Lan 4	
42	GND	Ground	
43	RX5N	Pixel Negative Vby One differential data input in area A. Lan 5	Note1
44	RX5P	Pixel Positive Vby One differential data input in area A. Lan 5	
45	GND	Ground	
46	RX6N	Pixel Negative Vby One differential data input in area A. Lan 6	Note1
47	RX6P	Pixel Positive Vby One differential data input in area A. Lan 6	
48	GND	Ground	
49	RX7N	Pixel Negative Vby One differential data input in area A. Lan 7	Note1
50	RX7P	Pixel Positive Vby One differential data input in area A. Lan 7	
51	GND	Ground	

4.4.2 CN2 PIN ASSIGNMENT

Pin No.	Symbol	Description	Note
1	VBL	+24 V	
2	VBL	+24 V	
3	VBL	+24 V	
4	VBL	+24 V	
5	VBL	+24 V	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground	
9	GND	Ground	
10	GND	Ground	
11	DC_Dimming	DC Dimming (Hi: $3V_{DC}$, Lo:$0V_{DC}$)	
12	BLON	BL ON/OFF (ON:3.3V, OFF:0V)	
13	SEL	DC_Dimming : Hi 3.3V; PWM_Dimming : Lo 0V	
14	E_PWM	External PWM Control (Hi Level: 3.3V, Lo Level: 0V)	

Connector information

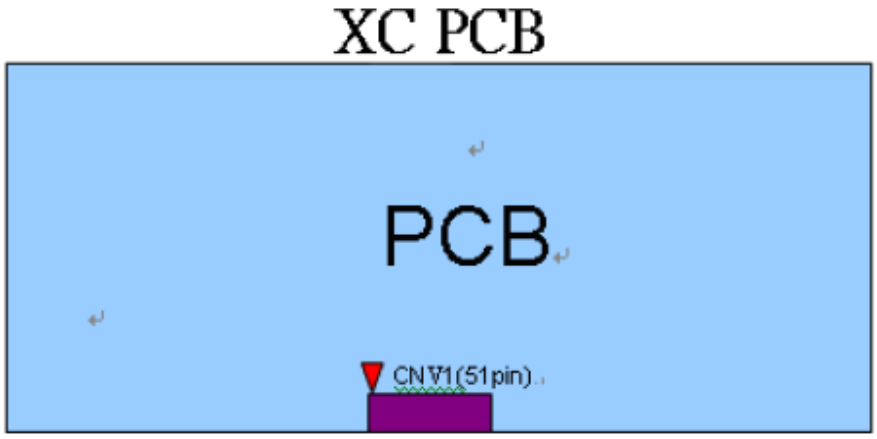
Item	Description
Manufacturer	FCN/ P-TWO
Type part number	FCN: WF23-402-5133 P-TWO: 187059-51221
User's Mating housing part number	JAE: FI-RE51HL

*Notice: There would be compatible issues if not using the indicated connectors in the matching list.

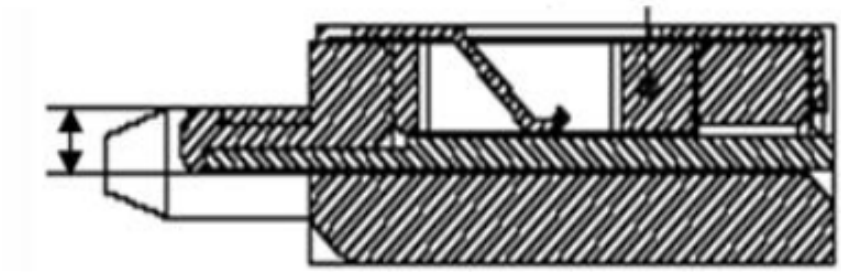
Note (1) V-by-One$_{OR}$HS Data Mapping

Lan	Data Stream
Lan 0	1, 9, 17, ..., 3825, 3833
Lan 1	2, 10, 18, ..., 3826, 3834
Lan 2	3, 11, 19, ..., 3827, 3835
Lan 3	4, 12, 20, ..., 3828, 3836
Lan 4	5, 13, 21, ..., 3829, 3837
Lan 5	6, 14, 22, ..., 3830, 3838
Lan 6	7, 15, 23, ..., 3831, 3839
Lan 7	8, 16, 24, ..., 3832, 3840

Note (2) Reserved for internal use. Please leave it open.
Note (3) V-by-One$_{OR}$HS connector pin order defined as following:



Note (4) V-by-One connector mating dimension range request is 0.93mm~1.0mm as below:



5. OPTICAL SPECIFICATIONS

5.1OPTICAL CHARACTERISTICS

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remarks
Viewing Angle	Horizontal	θ_x+	Center CR≥10	160	178	--	deg	Note 1,4
		θ_x-		160	178	--		
	Vertical	θ_Y+		160	178	--		
		θ_Y-		160	178	--		
Contrast Ratio		CR	at optimized viewing angle	1000	1250	--		Note 1,3
Response time	Rise+ Fall	Tr+ Tf	Center θx=θy =0°	-	16	--	ms	Note 1,6
Uniformity		B-uni	θx=θy =0°	75	--	--	%	Note1,5
Brightness		L	θx=θy =0°	640	800	--	cd/㎡	Note 1,2
Chromaticity		Wx	Center θx=θy =0°	Typ -0.05	0.313	Typ +0.05		Note 1,7
		Wy			0.329			
Image sticking		tis	2 hours			2	Sec	Note 8

The following optical specifications shall be measured in a darkroom or equivalent state (ambient luminance≤1 lux, and at room temperature). The operation temperature is 25°C±2°C. The measurement method is shown in Note 1.

Note 1: The method of optical measurement:

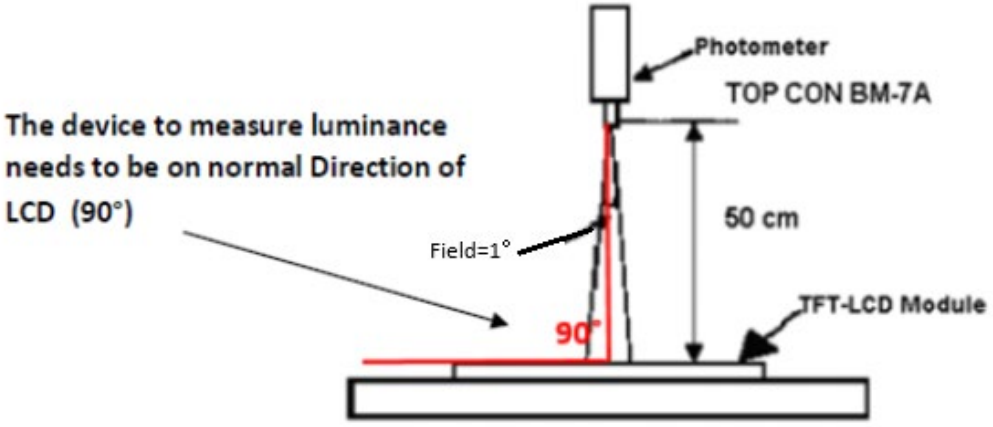


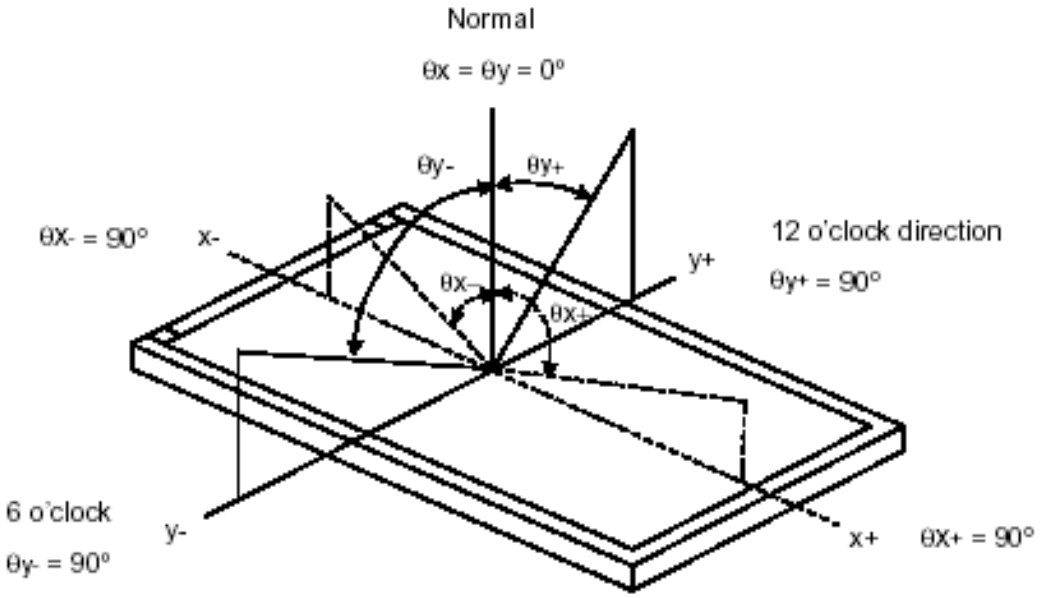
Image1: The method of optical measurement

Note 2: Measured at the center area of the panel and at the viewing angle of the θx=θy =0°

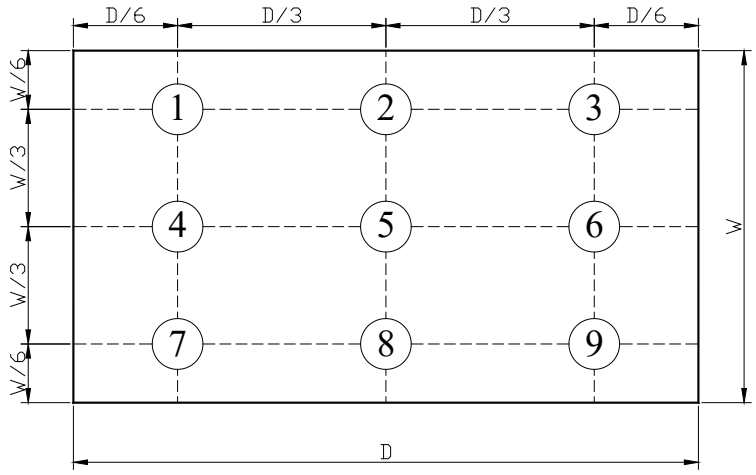
Note 3: Definition of Contrast Ratio (CR):

$$CR = \frac{\text{Luminance with all pixels in white state}}{\text{Luminance with all pixels in Black state}}$$

Note 4: Definition of Viewing Angle



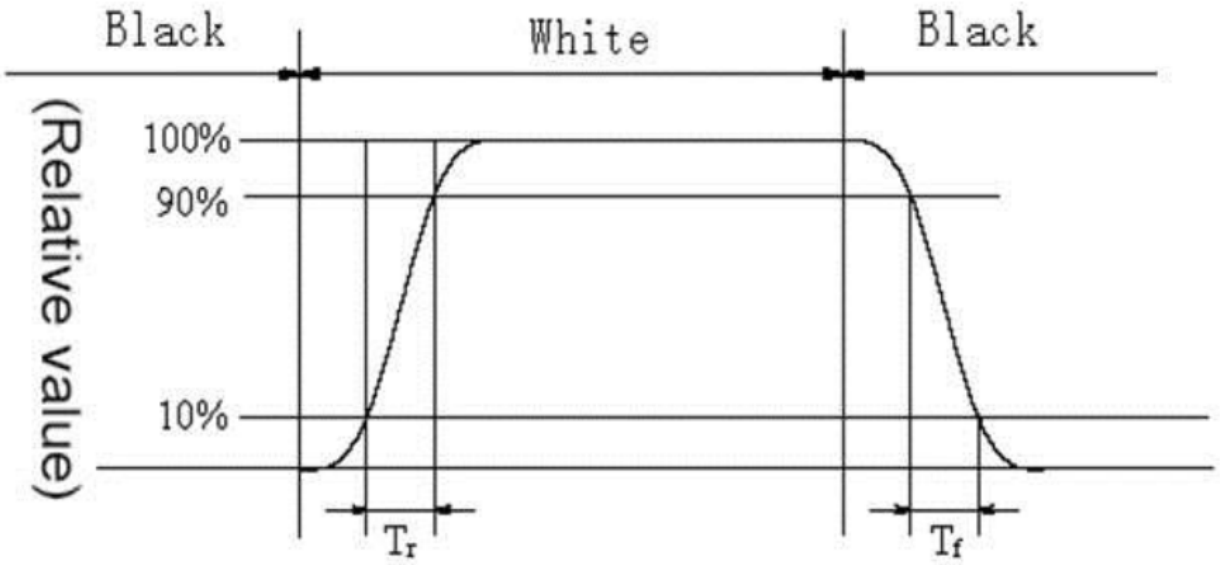
Note 5: Definition of Brightness Uniformity (B-uni):



$$\text{B-uni} = \frac{\text{Minimum luminance of 9 points}}{\text{Maximum luminance of 9points}} \quad \text{(Note 5).}$$

Note 6: Definition of Response Time:

The Response Time is set initially by defining the “Rising Time (Tr)” and the “Falling Time (Tf)” respectively. Tr and Tf are defined as following figure.



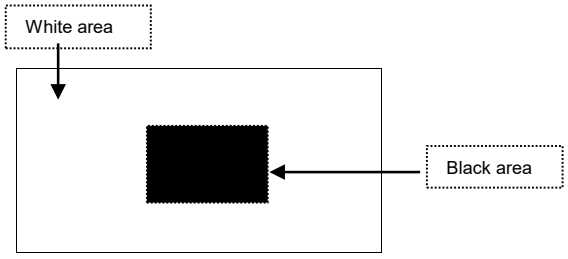
Note 7: Definition of Chromaticity:

The color coordinates (x_W,y_W) are obtained with all pixels in the viewing field at white, red, green, and blue states, respectively.

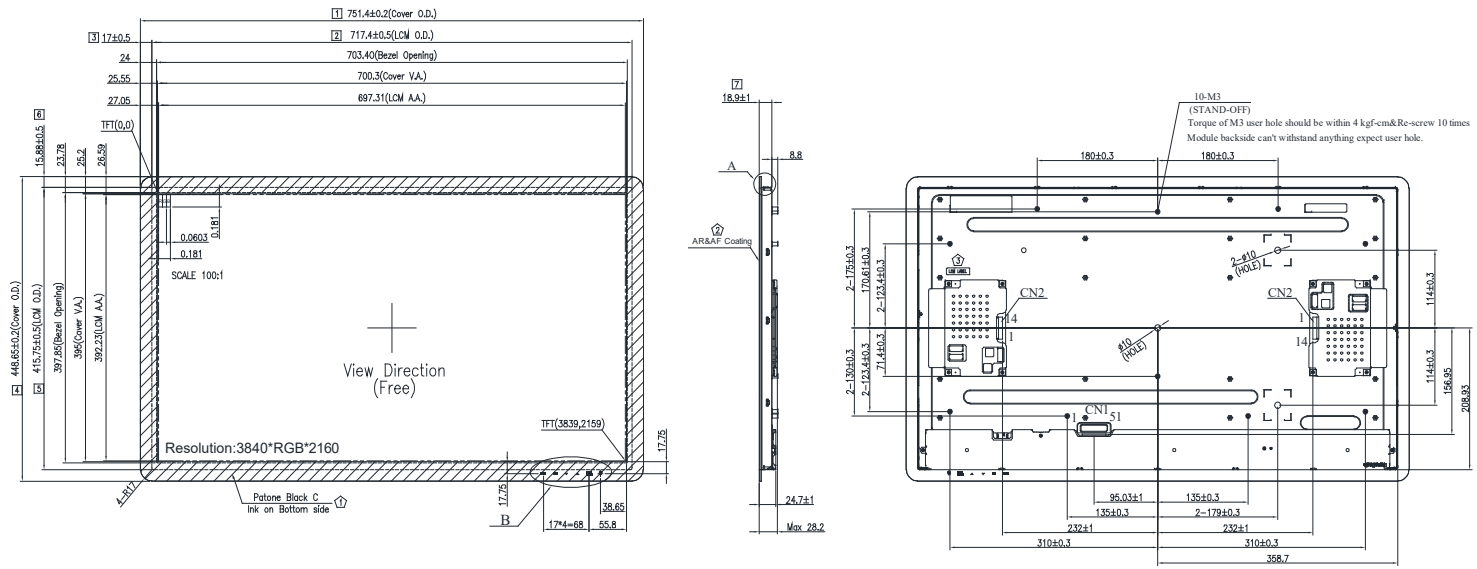
Note 8: Definition of Image sticking (tis):

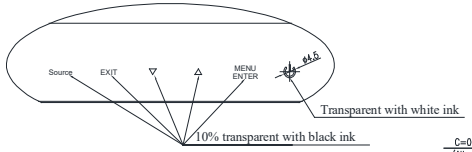
Continuously display the test pattern shown in the figure below for 2 hours. Then display a completely white screen. The previous image shall not persist more than 2 sec at 25 °C

Image sticking pattern

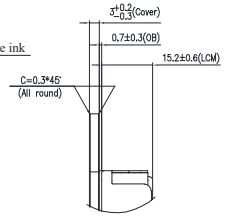


6. MECHANICAL SPECIFICATIONS
6.1 OUTLINE DRAWING





Detail B
Scale 4/1



Detail A
Scale 5/1

CN2 PIN ASSINGMENT					
1	VBL	6	GND	11	DC_Dimming
2	VBL	7	GND	12	BLON
3	VBL	8	GND	13	SEL
4	VBL	9	GND	14	E_PWM
5	VBL	10	GND		

CN1 PIN ASSIGNMENT									
								41	RX4P
1	Vin	11	GND	21	NC	31	RX1N	42	GND
2	Vin	12	GND	22	NC	32	RX1P	43	RX5N
3	Vin	13	GND	23	NC	33	GND	44	RX5P
4	Vin	14	GND	24	NC	34	RX2N	45	GND
5	Vin	15	NC	25	HTPDN	35	RX2P	46	RX6N
6	Vin	16	NC	26	LOCKN	36	GND	47	RX6P
7	Vin	17	NC	27	GND	37	RX3N	48	GND
8	Vin	18	NC	28	RX0N	38	RX3P	49	RX7N
9	NC	19	NC	29	RX0P	39	GND	50	RX7P
10	GND	20	NC	30	GND	40	RX4N	51	GND

General Notes	
Environmental Requirements	RoHS&REACH&Halogen Free.
General Tolerance	±0.5mm
Important Dimension	1 ~ 7
Important Inspection	1 ~ 4
Brightness LCM Only(Typ.)	800 cd/m²
Brightness LCM Only(Min.)	640 cd/m²
Uniformity(Min.)	75%
CN1 Connector	P-TWO 187059-51221 or equivalent.
CN1 Relating Connector	FI-RE51HL or equivalent.
CN2 Connector	FCN JH2-D4-143N or Cvilux CI0114M1HR0-H
CN2 Relating Connector	Cvilux CI01 Housing or equivalent.
Operating Temp.	0 ~ +45°C
Storage Temp.	-20 ~ +60°C

Special Notes	
Strengthening method	Chemically strengtheed glass
INK	Low temp.
AF Coating(Water contact angle)	≧ 110°
AR Coating(Reflective)	< 1%

2AAD617003T(T0203)

設計驗證
工程課
2023.10.27
發行
鈺緯科技開發股份有限公司

AUTH	DESCRIPTION	DATE	APPROVED
	Change drawing from Rev.3 to Rev.A <NPPR-230728002>	2023/10/20	

REVISIONS

DATE:	2021/07/30
DRAWN:	Roger
CHECK:	Owen
APPROVE:	Nomo & Jack

TITLE: 31.5" LCM outline dimension

DWG. NO.	FC310500SG01		
UNITS	M M	REV.	A
SCALE	1 / 1	SHEET 1 OF 1	

DATA IMAGE

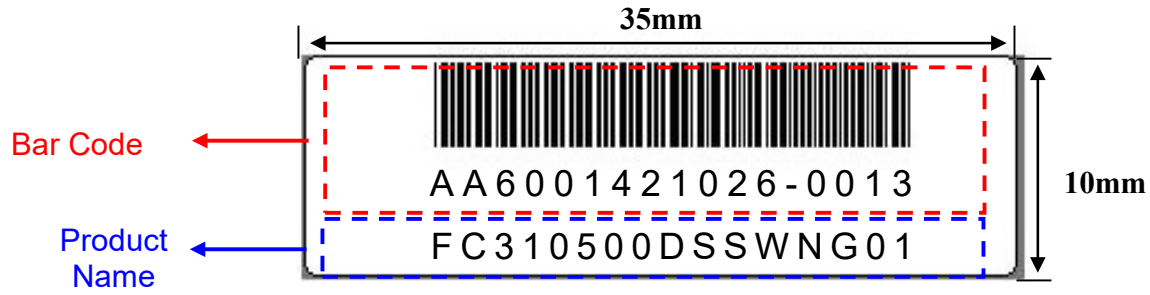
7. RELIABILITY TEST ITEM

No.	Reliability Test Item & Level	Test Level	Remark
1	High Temperature Storage Test	T=60°C,240hrs	IEC60068-2-2
2	Low Temperature Storage Test	T=-20°C,240hrs	IEC60068-2-1
3	High Temperature Operation Test	T=45°C,240hrs	IEC60068-2-2
4	Low Temperature Operation Test	T=0°C,240hrs	IEC60068-2-1
5	High Temperature and High Humidity (No operation)	Ta= 50℃ , 80%RH, 240hours	IEC60068-2-3
6	Thermal Cycling Test (No operation)	-20℃/30min , 60℃ / 30min , 100 cycles	IEC60068-2-14
7	Vibration test (Package)	Frequency:10~55HZ Amplitude:1.5mm Sweep time:11min Test period:6Cycles for each direction of X,Y,Z	IEC60068-2-6
8	Drop test (Package)	Height :60cm 1 conner,3edges,6surfaces	IEC60068-2-32
9	Electrostatic Discharge Test	State: operating Location: LCM/TP surface Condition:150pf 330Ω Contact +/- 8kV Air +/-15kV Criteria: Class C	IEC61000-4-2

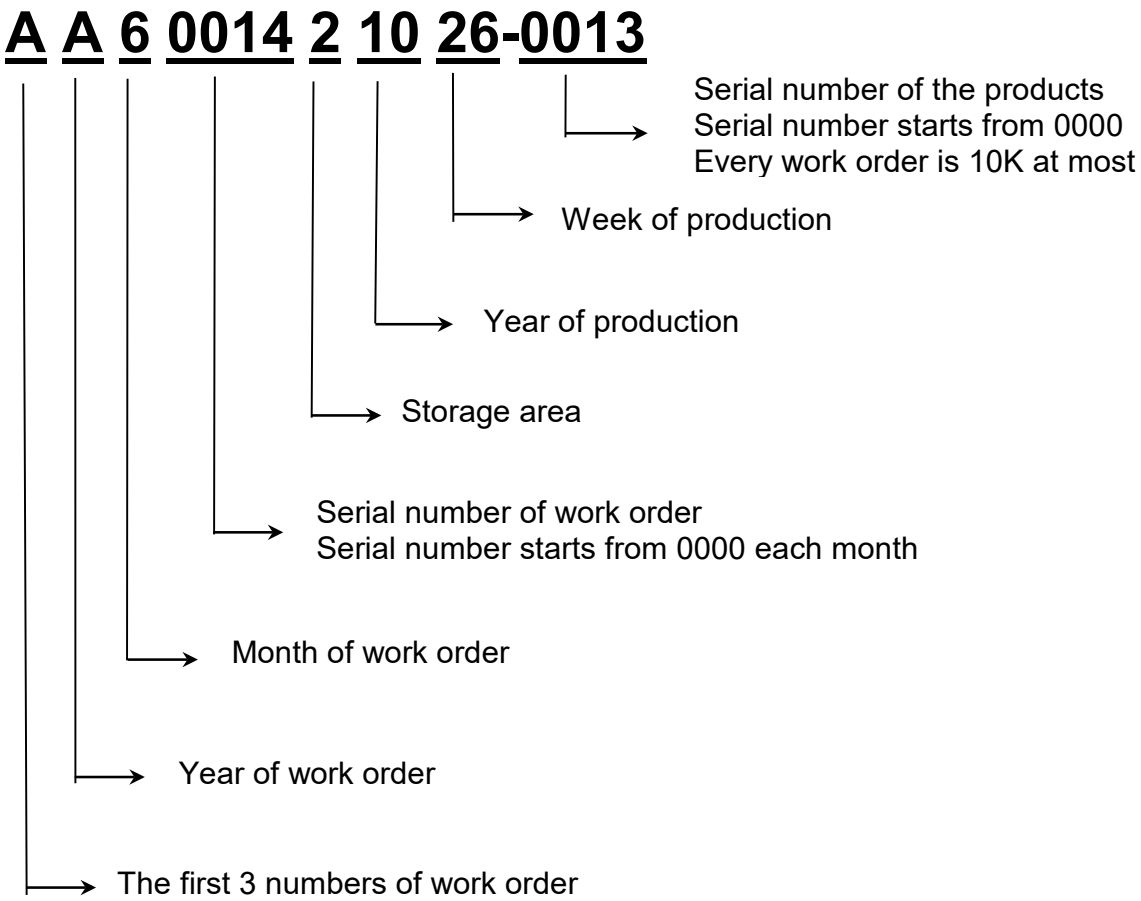
8. LCM PRODUCT LABEL DEFINE

8.1 SHIPPING LABLE

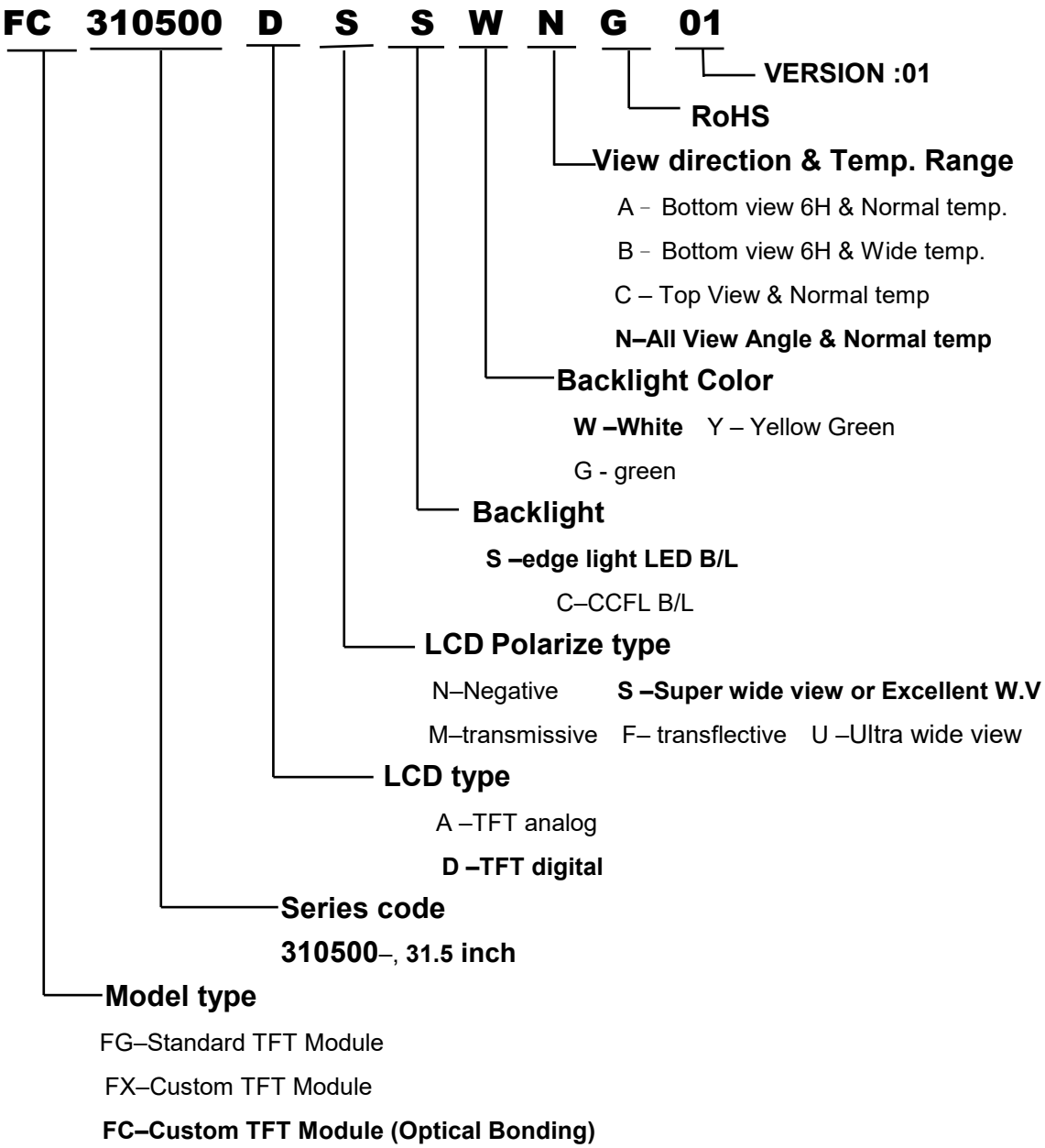
Product Label style:



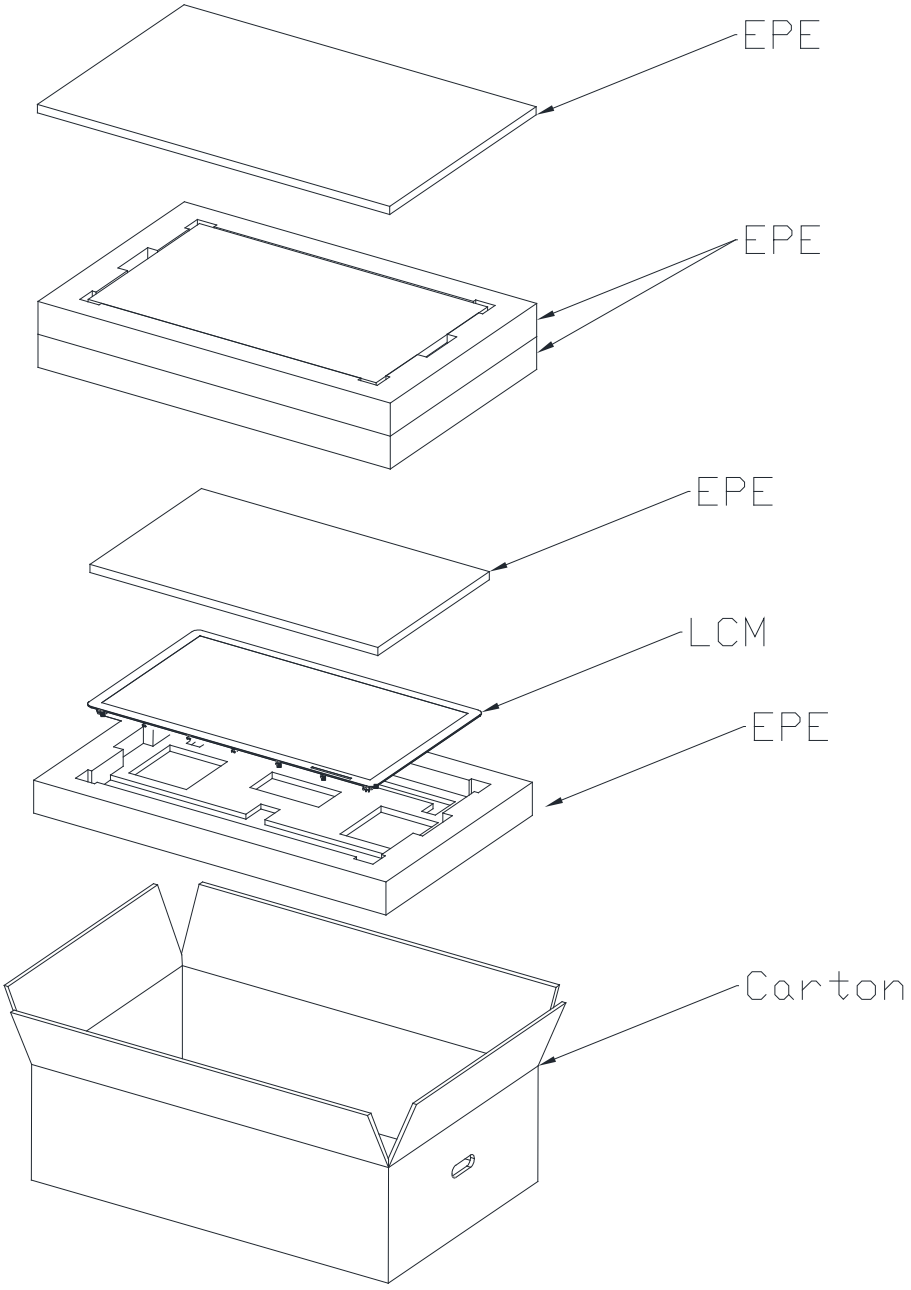
BarCode Define:



Product Name Define:



8.2 CARTON PACKAGE



Item	Size	Quantity	Note
Carton	932*602*280	1	
Quantity per carton		3	
N.W.(kg)	24.82	G.W.(kg)	29.8

9.Precaution

9.1 HANDLING PRECAUTIONS

(1). The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2). While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3). Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4). Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5). If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6). Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7). If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8). Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9). Do not disassemble the module.

(10). Do not pull or fold the LED wire.

(11). Pins of I/F connector should not be touched directly with bare hands.

9.2 STORAGE PRECAUTIONS

(1). High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2). It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3). It may reduce the display quality if the ambient temperature is lower than 10 ºC. For example, the response time will become slowly, and the starting voltage of LED will be higher than the room temperature.

9.3 OPERATION PRECAUTIONS

(1). Do not pull the I/F connector in or out while the module is operating.

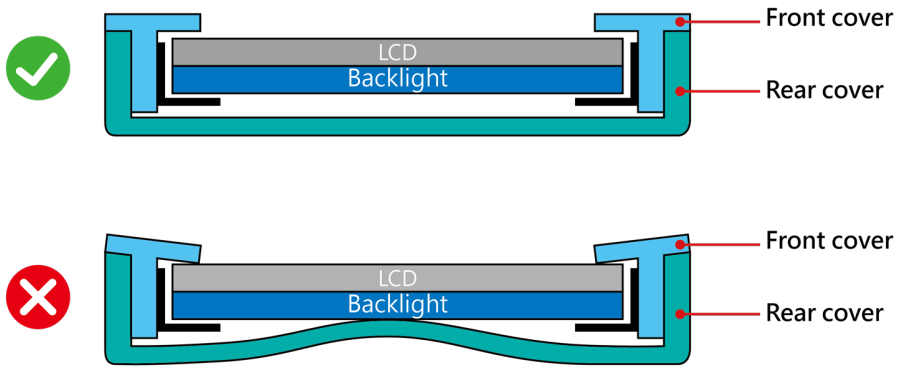
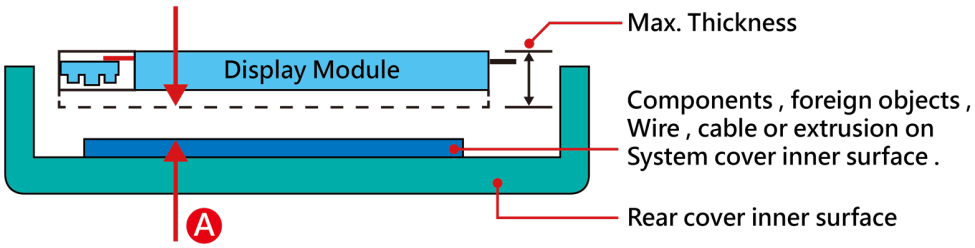
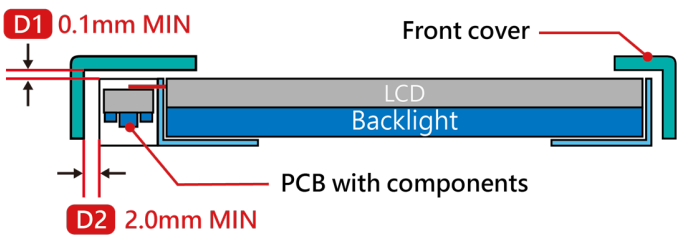
(2). Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

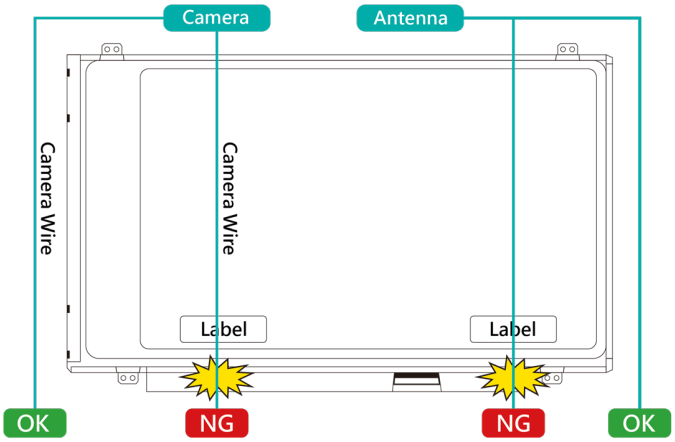
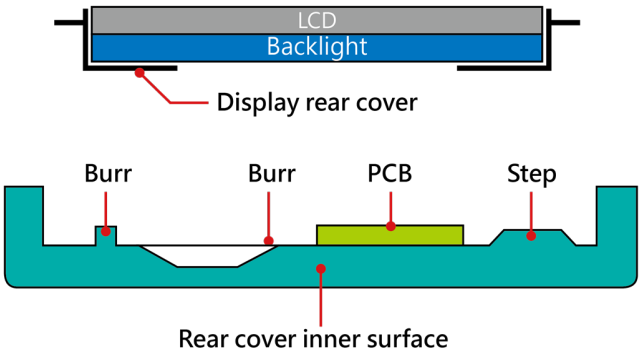
(3). The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the module or insert anything into the Backlight unit.

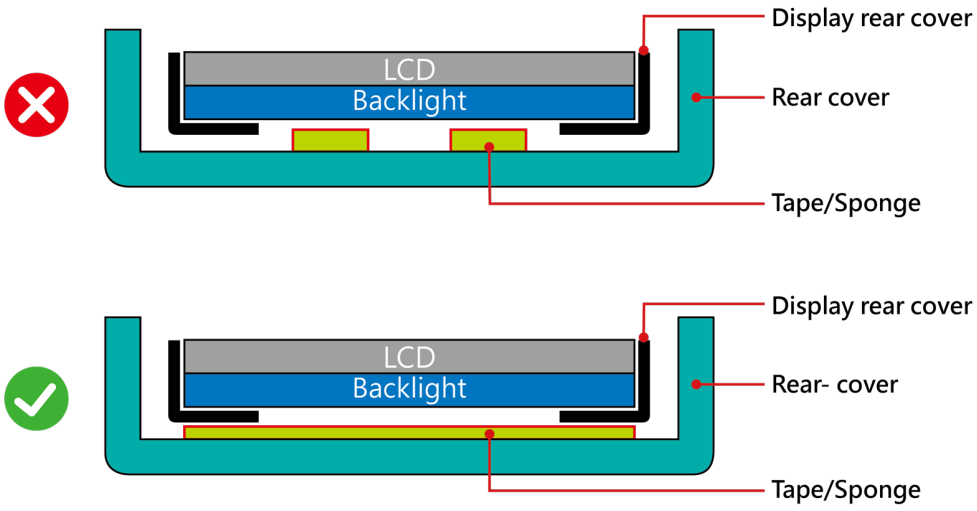
(4). LIMITED WARRANTY

Unless otherwise agreed between DATA IMAGE and customer, DATA IMAGE will replace or repair any of its LCD and LCM which is found to be defective electrically and visually when inspected in accordance with DATA IMAGE acceptance standards, for a period on one year from date of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of DATA IMAGE is limited to repair and/or replacement on the terms set forth above. DATA IMAGE will not responsible for any subsequent or consequential events

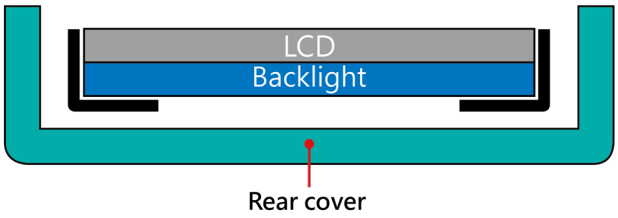
Appendix. Covers Design Guideline

A.	**Permanent deformation of front/rear covers after reliability test**
	
Definition	Front/rear covers may deform during reliability test. Permanent deformation of front/rear covers after reliability test should not interfere with display. Because it may cause issues such as pooling, abnormal display, white spot, and also cell crack.
B.	**Design gap A between display and any components on rear cover**
	
Definition	Gap A between display's maximum thickness boundary and rear cover inner surface components such as wire, cable, extrusion is needed for preventing from backpack or pogo test fail. Because zero gap or interference may cause stress concentration. Issues such as pooling, abnormal display, white spot, white spot and cell crack may occur. Flatness of display and rear cover should be taken into account for gap design.
C.	**Design gap D1 & D2 between front cover and PCB assembly**
	

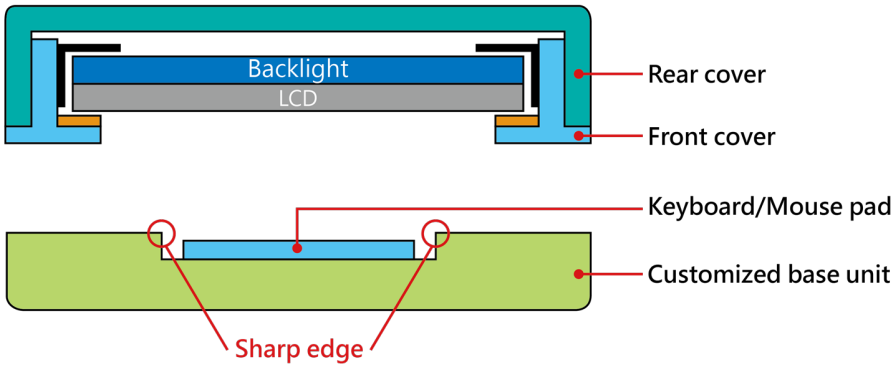
Definition	Gap D1 & D2 between front cover and LCD & front cover and PCBA are needed to prevent pooling or glass broken. Zero gap or interference such as burr and warpage from mold frame may cause pooling issue near front cover opening edge. This phenomenon is obvious during swing test, hinge test, knock test or during pooling inspection procedure. To remain sufficient gap, design with system rib higher than maximum display thickness is recommended.
D.	**Interference examination of camera's and antenna's cable**
	
Definition	Camera's and antenna's cable should not overlap with panel outline. Because issue such as abnormal display and white spot after backpack test, hinge test, twist test or pogo test may occur.
E.	**Rear cover inner surface examination**
	
Definition	Burr at logo edge, steps, protrusions or PCB may cause stress concentration. Whiter spot or glass broken issue may occur during reliability test.
F.	**Tape/sponge design on rear cover inner surface**



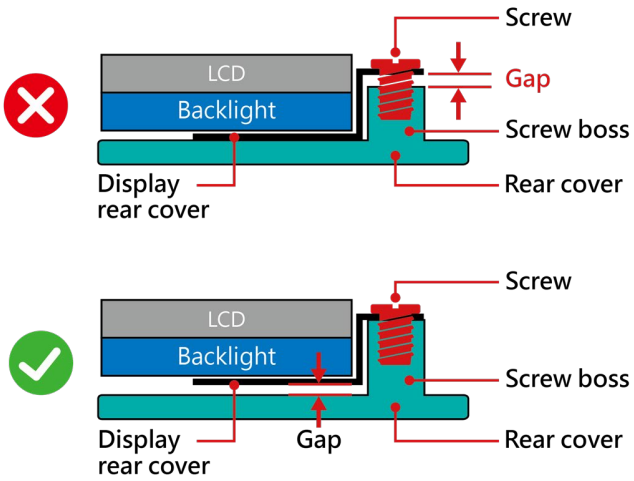
Definition	To prevent abnormal display and white spot after scuffing test, hinge test, pogo test, backpack test, tape/sponge should be well covered under rear cover. Because tape/sponge in separate location may act as pressure concentration location.
G.	**Material used for rear cover**



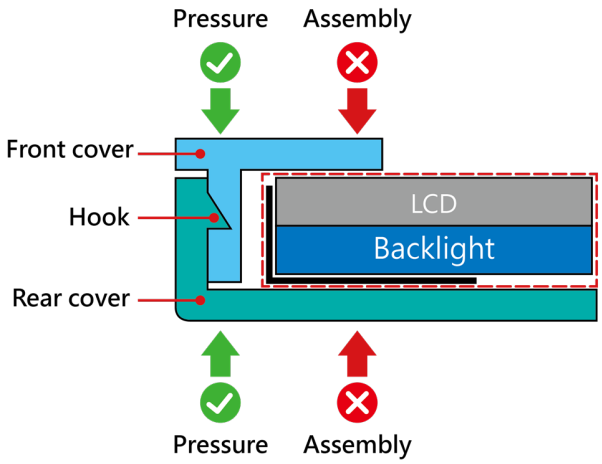
Definition	Rear cover material with high rigidity is needed to resist deformation during scuffing test, hinge test, pogo test or backpack test. Abnormal display, white spot, pooling issue may occur if low rigidity material is used. Pooling issue may occur because screw's boss positioning for module's bracket are deformed during open-close test. Solid structure design of system rear cover may also influence the rigidity of rear cover. The deformation of rear cover should not caused interference.
H.	**Customized base unit design near keyboard and mouse pad**



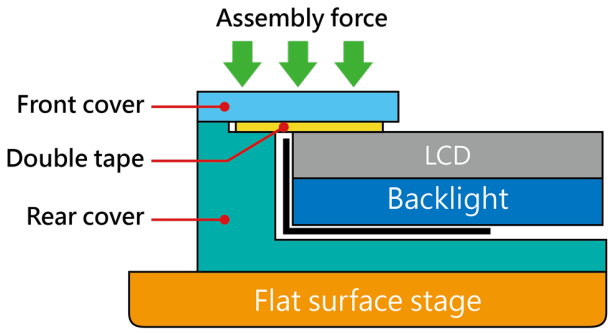
Definition	To prevent abnormal display and white spot after scffing test, hinge test, pogo test, backpack test, sharp edge design in keyboard surface may damage display during the test. We suggest to use slope edge design or to reduce the thickness difference of keyboard/mouse pad from the nearby surface.
I.	**Screw boss height design**



Definition	Screw boss height should be designed with respect to the height of bracket bottom surface to display bottom surface with flatness change of display itset. Because gap will exist between screw boss and bracket, if the screw boss height is smaller. As result while fastening screw, bracket will deformed and pooling issue may occur.
J.	**Assembly SOP examination for front cover with Hook design**



Definition	To prevent display crack during front cvoer assembly process with hook design, it is not recommended to press display or any location that related directly to the display.
L.	**Assembly SOP examination for front cover with Double tape design**



Definition	To prevent display crack during system front cover assembly process with double tape design, it is only allowed to give slight pressure (MAX 3 Kgf/50mm2) with large contact area. This can help to distribute the stress and prevent stress concentration. We also suggest putting the system on a flat surface stage to prevent unequal stress distribution during the assembly.