QUICKSWITCH® PRODUCTS 2.5V/3.3V QUAD 2:1 MUX/DEMUX HIGH BANDWIDTH BUS SWITCH

IDTQS3VH257

FEATURES:

- **N channel FET switches with no parasitic diode to Vcc**
  - *Isolation under power-off conditions*
  - *No DC path to Vcc or GND*
  - *5V tolerant in OFF and ON state*
- **5V tolerant I/Os**
- **Low Ron - 4Ω typical**
- **Flat Ron characteristics over operating range**
- **Rail-to-rail switching 0 - 5V**
- **Bidirectional dataflow with near-zero delay: no added ground bounce**
- **Excellent Ron matching between channels**
- **Vcc operation: 2.3V to 3.6V**
- **High bandwidth - up to 500MHz**
- **LVTTL-compatible control Inputs**
- **Undershoot Clamp Diodes on all switch and control Inputs**
- **Low I/O capacitance, 4pF typical**
- **Available in QSOP, SOIC, and TSSOP packages**

APPLICATIONS:

- **Hot-swapping**
- **Multiplexing/demultiplexing**
- **Low distortion analog switch**
- **Replaces mechanical relay**
- **ATM 25/155 switching**

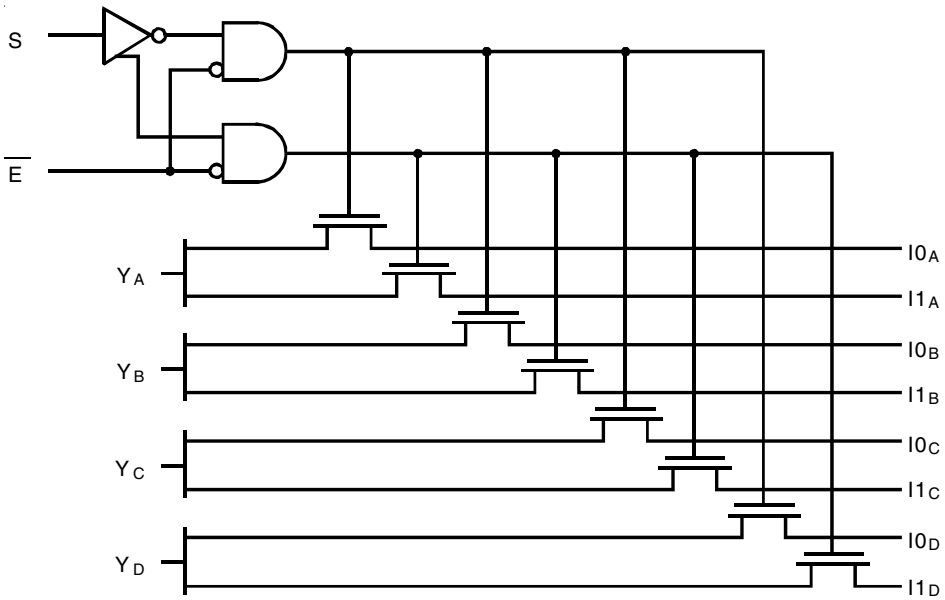
DESCRIPTION:

The QS3VH257 HotSwitch Quad 2:1 multiplexer/demultiplexer is a high bandwidth bus switch. The QS3VH257 has very low ON resistance, resulting in under 250ps propagation delay through the switch. The Select (S) input controls the data flow. The multiplexers/demultiplexers are enabled when the Enable ($\overline{E}$) input is low. In the ON state, the switches can pass signals up to 5V. In the OFF state, the switches offer very high impedence at the terminals.

The combination of near-zero propagation delay, high OFF impedance, and over-voltage tolerance makes the QS3VH257 ideal for high performance communication applications.

The QS3VH257 is characterized for operation from -40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM



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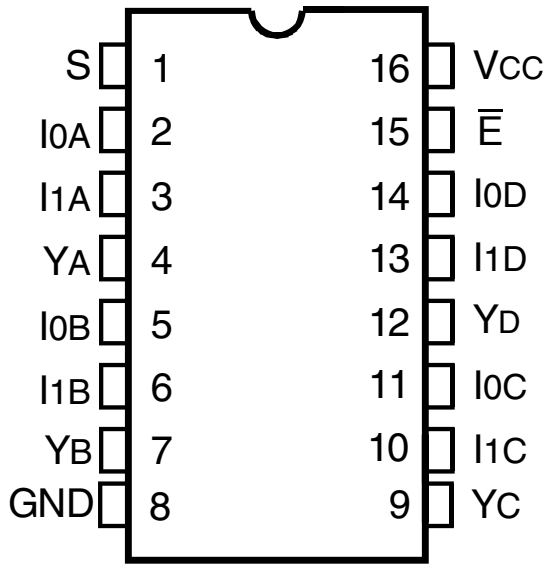
PIN CONFIGURATION



QSOP/ SOIC/ TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{TERM}(2)	SupplyVoltage to Ground	–0.5 to +4.6	V
V_{TERM}(3)	DC Switch Voltage V_S	–0.5 to +5.5	V
V_{TERM}(3)	DC Input Voltage V_{IN}	–0.5 to +5.5	V
V_{AC}	AC Input Voltage (pulse width ≤20ns)	–3	V
I_{OUT}	DC Output Current (max. sink current/pin)	120	mA
T_{STG}	Storage Temperature	–65 to +150	°C

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminals.
3. All terminals except V_{CC} .

CAPACITANCE (T_A = +25°C, F = 1MHz, V_{IN} = 0V, V_{OUT} = 0V)

Symbol	Parameter(1)		Typ.	Max.	Unit
C_{IN}	Control Inputs		3	5	pF
$C_{I/O}$	Quickswitch Channels (Switch OFF)	Demux	4	6	pF
		Mux	7	9	
$C_{I/O}$	Quickswitch Channels (Switch ON)	Demux	10	15	pF
		Mux	10	15	

NOTE:
1. This parameter is guaranteed but not production tested.

PIN DESCRIPTION

Pin Names	I/O	Description
Ixx	I	Data Inputs
S	I	Select Input
$\overline{E}$	I	Enable Input
Y_A - Y_D	O	Data Outputs

FUNCTION TABLE(1)

Inputs		Outputs				
$\overline{E}$	S	Y_A	Y_B	Y_C	Y_D	Function
H	X	Z	Z	Z	Z	Disable
L	L	$I0_A$	$I0_B$	$I0_C$	$I0_D$	Select 0
L	H	$I1_A$	$I1_B$	$I1_C$	$I1_D$	Select 1

NOTE:
1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-Impedence

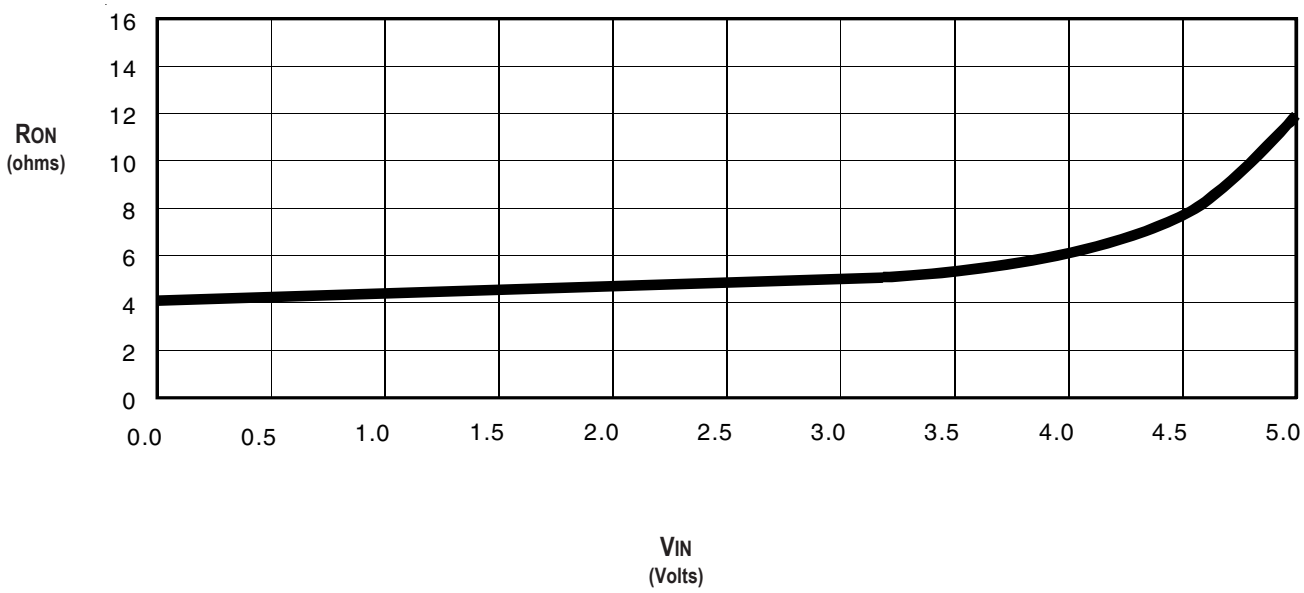
DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = –40°C to +85°C, V_{CC} = 3.3V ±0.3V

Symbol	Parameter	Test Conditions			Min.	Typ.(1)	Max.	Unit
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH	V_{CC} = 2.3V to 2.7V		1.7	—	—	V
		for Control Inputs	V_{CC} = 2.7V to 3.6V		2	—	—	
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW	V_{CC} = 2.3V to 2.7V		—	—	0.7	V
		for Control Inputs	V_{CC} = 2.7V to 3.6V		—	—	0.8	
I_{IN}	Input Leakage Current (Control Inputs)	0V ≤ V_{IN} ≤ V_{CC}			—	—	±1	µA
I_{OZ}	Off-State Current (Hi-Z)	0V ≤ V_{OUT} ≤ 5V, Switches OFF			—	—	±1	µA
I_{OFF}	Data Input/Output Power Off Leakage	V_{IN} or V_{OUT} 0V to 5V, V_{CC} = 0V			—	—	±1	µA
R_{ON}	Switch ON Resistance	V_{CC} = 2.3V	V_{IN} = 0V	I_{ON} = 30mA	—	6	8	Ω
		Typical at V_{CC} = 2.5V	V_{IN} = 1.7V	I_{ON} = 15mA	—	7	9	
		V_{CC} = 3V	V_{IN} = 0V	I_{ON} = 30mA	—	4	6	
			V_{IN} = 2.4V	I_{ON} = 15mA	—	5	8	

NOTE:
1. Typical values are at V_{CC} = 3.3V and T_A = 25°C.

TYPICAL ON RESISTANCE vs V_{IN} AT V_{CC} = 3.3V

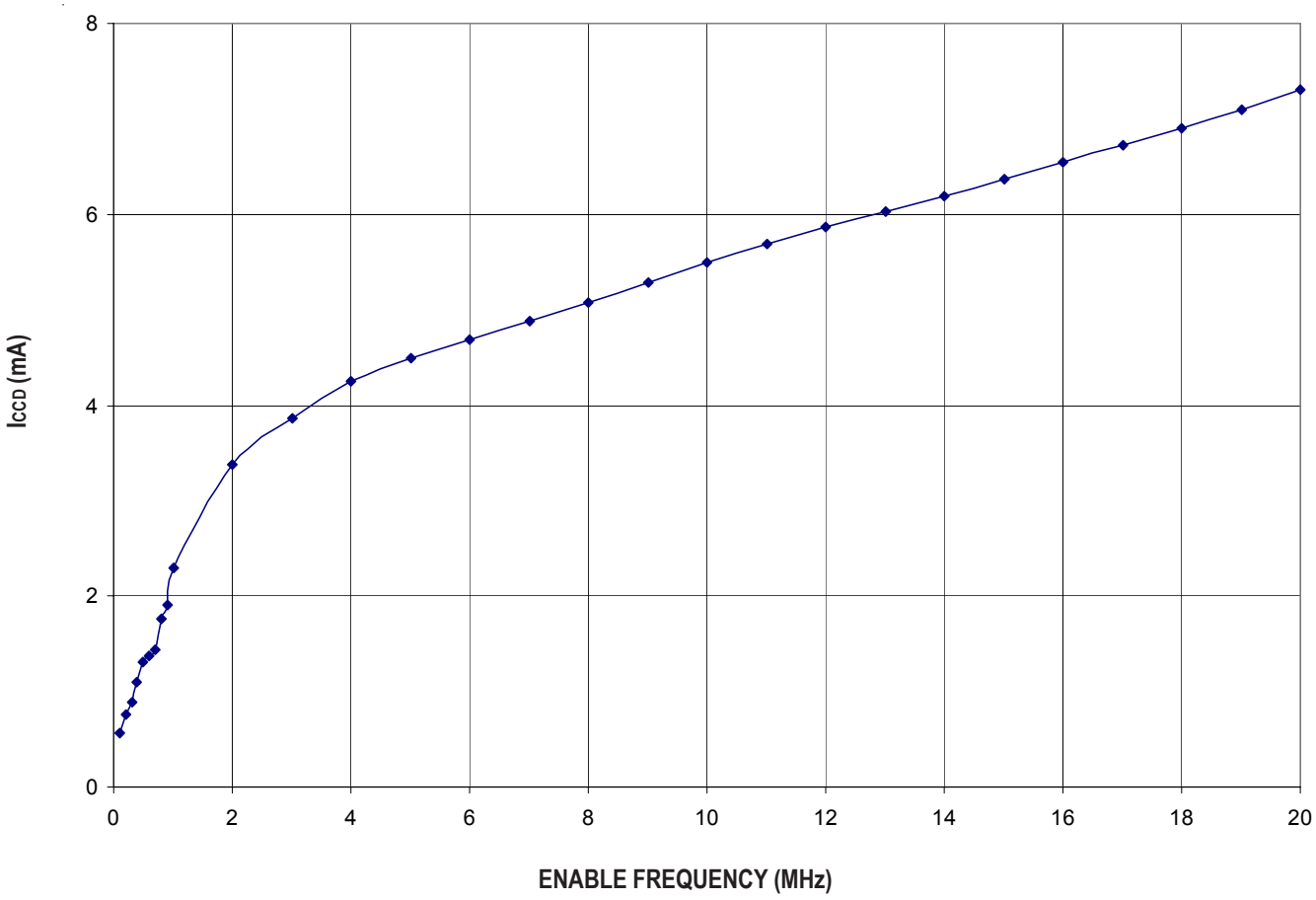


POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]	Min.	Typ.	Max.	Unit
I_{CCQ}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}, f = 0	—	2	4	mA
ΔI_{CC}	Power Supply Current [2,3] per Input HIGH	V_{CC} = Max., V_{IN} = 3V, f = 0 per Control Input	—	—	30	µA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = 3.3V, A and B Pins Open, Control Inputs Toggling @ 50% Duty Cycle	See Typical I_{CCD} vs Enable Frequency graph below			

NOTES:
1. For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.
2. Per input driven at the specified level. Mux/demux pins do not contribute to ΔIcc.
3. This parameter is guaranteed but not tested.
4. This parameter represents the current required to switch internal capacitance at the specified frequency. The mux/demux inputs do not contribute to the Dynamic Power Supply Current. This parameter is guaranteed but not production tested.

TYPICAL I_{CCD} vs ENABLE FREQUENCY CURVE AT V_{CC} = 3.3V



SWITCHING CHARACTERISTICS OVER OPERATING RANGE

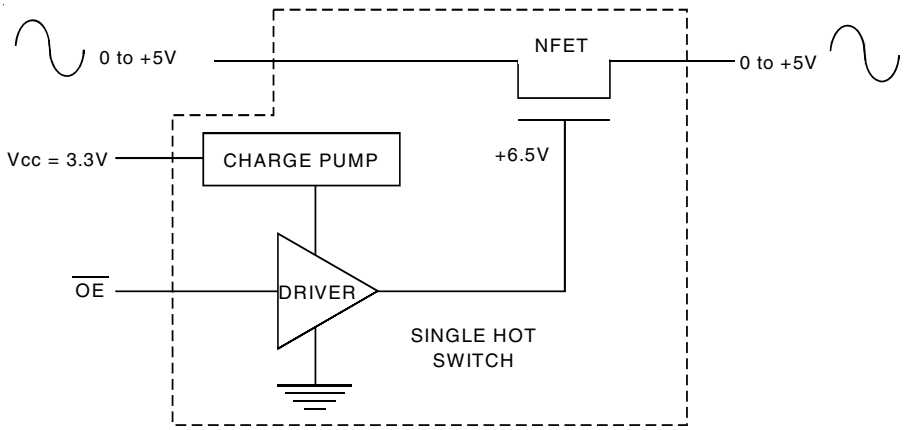
T_A = -40°C to +85°C

Symbol	Parameter	V_{CC} = 2.5 ± 0.2V (1)		V_{CC} = 3.3 ± 0.3V (1)		Unit
		Min. (4)	Max.	Min. (4)	Max.	
t_{PLH} t_{PHL}	Data Propagation Delay(2,3) Yx to Ixx or Ixx to Yx	—	0.2	—	0.2	ns
t_{SEL}	Select Time S to Yx	1.5	9	1.5	8	ns
t_{PZH} t_{PZL}	Enable Time S to Ixx	1.5	9	1.5	9	ns
t_{PHZ} t_{PLZ}	Disable Time S to Ixx	1.5	8	1.5	8	ns
t_{PZH} t_{PZL}	Enable Time $\overline{E}$ to Yx or Ixx	1.5	9	1.5	8	ns
t_{PHZ} t_{PLZ}	Disable Time $\overline{E}$ to Yx or Ixx	1.5	8	1.5	8	ns
$f_{\overline{E}orS}$	Operating Frequency - Enable(2,5)	—	10	—	20	MHz

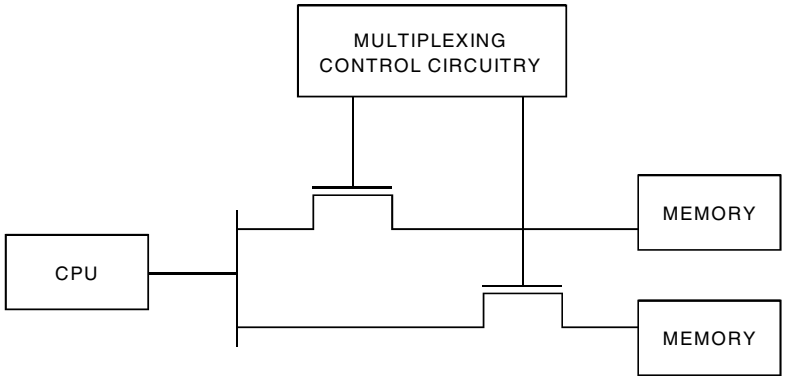
NOTES:

1. See Test Conditions under TEST CIRCUITS AND WAVEFORMS.
2. This parameter is guaranteed but not production tested.
3. The bus switch contributes no propagation delay other than the RC delay of the ON resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.2ns at C_L = 50pF. Since this time constant is much smaller than the rise and fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch, when used in a system, is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.
4. Minimums are guaranteed but not production tested.
5. Maximum toggle frequency for S or $\overline{E}$ control input (pass voltage > V_{CC}, V_{IN} = 5V, $R_{LOAD} \geq 1M\Omega$, no C_{LOAD}).

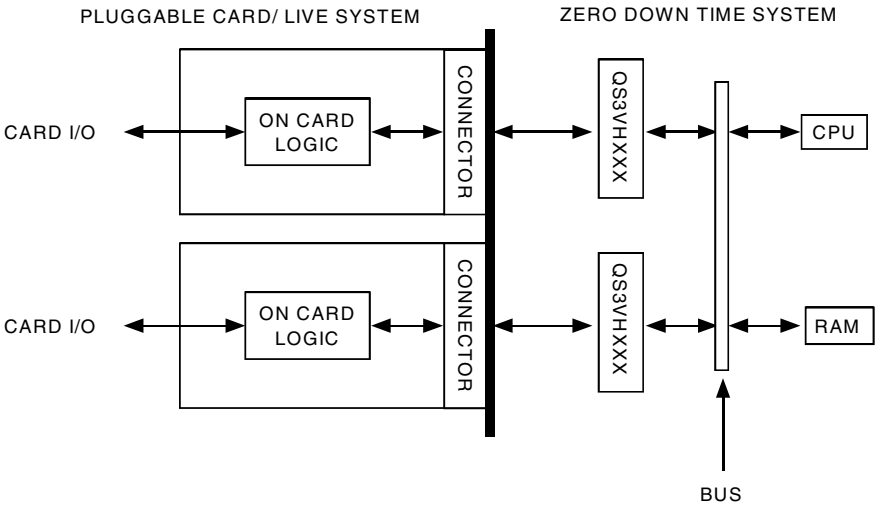
SOME APPLICATIONS FOR HOTSWITCH PRODUCTS



Rail-to-Rail Switching



Multiplexing / Demultiplexing

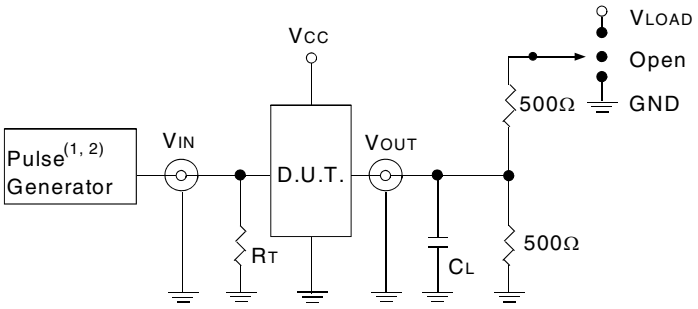


Hot-Swapping

TEST CIRCUITS AND WAVEFORMS

TEST CONDITIONS

Symbol	$V_{CC}^{(1)}$= 3.3V ± 0.3V	$V_{CC}^{(2)}$= 2.5V ± 0.2V	Unit
V_{LOAD}	6	2 x Vcc	V
V_{IH}	3	Vcc	V
V_T	1.5	Vcc/2	V
V_{LZ}	300	150	mV
V_{HZ}	300	150	mV
C_L	50	30	pF



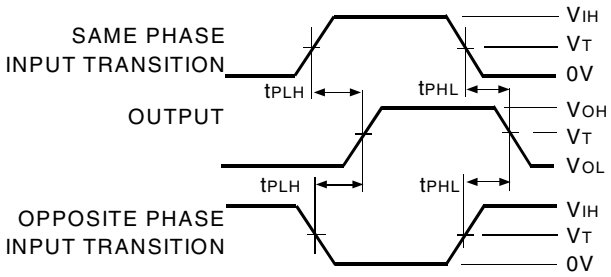
Test Circuits for All Outputs

DEFINITIONS:
C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.

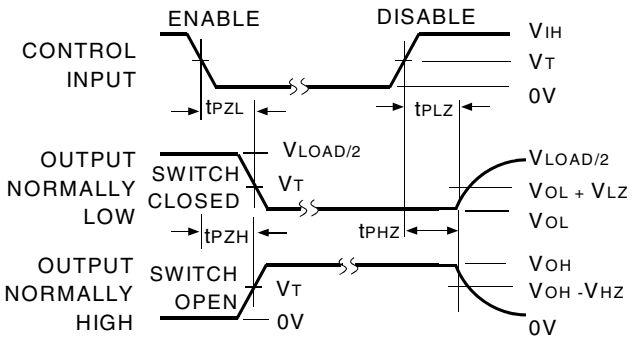
NOTES:
1. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.
2. Pulse Generator for All Pulses: Rate ≤ 10MHz; t_F ≤ 2ns; t_R ≤ 2ns.

SWITCH POSITION

Test	Switch
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND
t_{PD}	Open



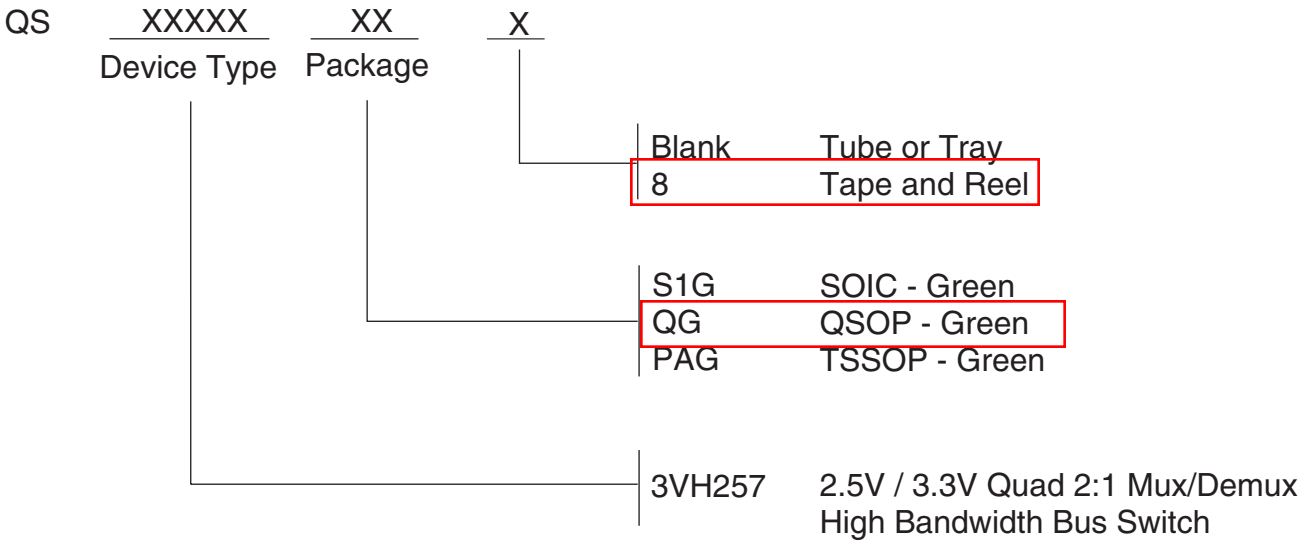
Propagation Delay



NOTE:
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

Enable and Disable Times

ORDERING INFORMATION



Datasheet Document History

09/01/08	Pg. 4, 8	Revise I_{CCQ} Typ. and Max. Remove non green package version and updated the ordering information by removing the "IDT" notation.
02/24/14	Pg. 8	Updated the Ordering Information by Adding Tape and Reel information.

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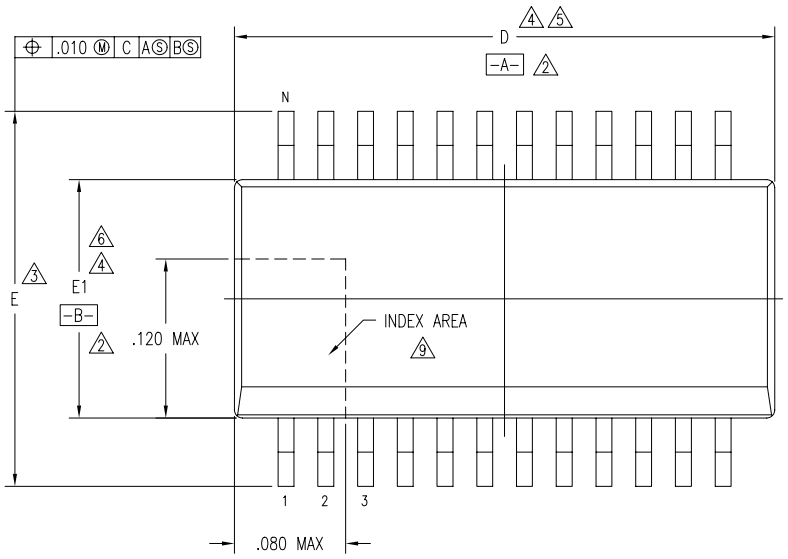
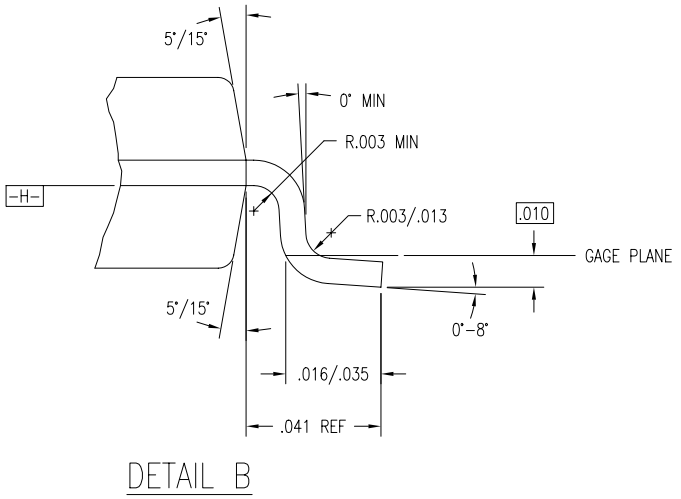
fax: 408-284-2775
www.idt.com

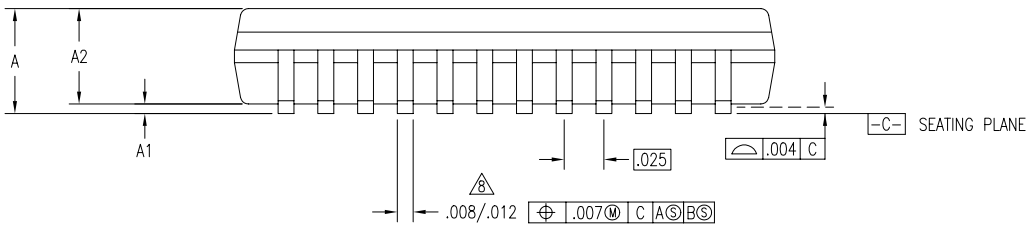
for Tech Support:
logichelp@idt.com

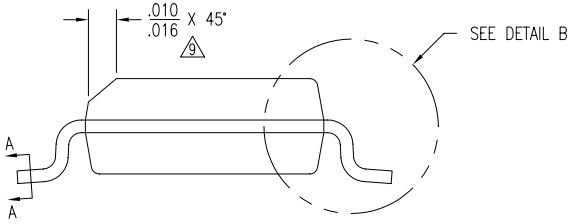
REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27495	01	REDRAW TO JEDEC FORMAT	03/10/95	T. VU
28047	02	ADD 28 LD	08/15/95	T. VU
	03	CHANGE TO QSOP	12/15/99	S.SUE
	04	ADD "GREEN" PCG NOMENCLATURE	10/08/04	TU VU
	05	CHANGE RADIUS DIM	11/15/11	CK LEE

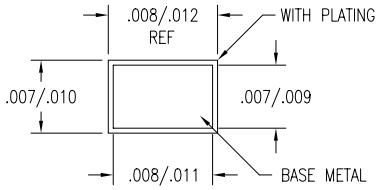




DETAIL B







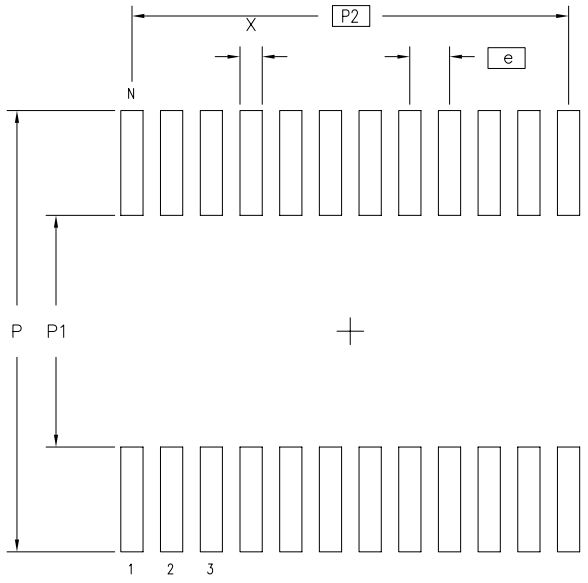
SECTION A-A
7

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± XXXX±	IDT™ www.IDT.com 2975 Stender Way Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674
APPROVALS DATE DRAWN CHECKED	TITLE PC/PCG PACKAGE OUTLINE .150" BODY WIDTH QSOP .025" PITCH
	SIZE C · DRAWING No. PSC-4040 · REV 05
	DO NOT SCALE DRAWING · SHEET 1 OF 2

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
28047	02	ADD 28 LD	08/15/95	T. VU
	03	CHANGE TO QSOP	12/15/99	S.SUE
	04	ADD "GREEN" PCG NOMENCLATURE	10/08/04	TU VU
	05	CHANGE RADIUS DIM	11/15/11	CK LEE

SYMBOL	JEDEC VARIATION AB			NOTE	JEDEC VARIATION AD			NOTE	JEDEC VARIATION AE			NOTE	JEDEC VARIATION AF			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
A	.061	.064	.068		.061	.064	.068		.061	.064	.068		.061	.064	.068	
A1	.004	.006	.010		.004	.006	.010		.004	.006	.010		.004	.006	.010	
A2	.055	.058	.061	11	.055	.058	.061	11	.055	.058	.061	11	.055	.058	.061	11
D	.189	.194	.196	4,5	.337	.342	.344	4,5	.337	.342	.344	4,5	.386	.390	.394	4,5
E	.230	.236	.244	3	.230	.236	.244	3	.230	.236	.244	3	.230	.236	.244	3
E1	.150	.155	.157	4,6	.150	.155	.157	4,6	.150	.155	.157	4,6	.150	.155	.157	4,6
N	16				20				24				28			

LAND PATTERN DIMENSIONS



	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
P	.274	.282	.274	.282	.274	.282	.274	.282
P1	.142	.150	.142	.150	.142	.150	.142	.150
P2	.175 BSC		.225 BSC		.275 BSC		.325 BSC	
X	.010	.018	.010	.018	.010	.018	.010	.018
e	.025 BSC		.025 BSC		.025 BSC		.025 BSC	
N	16		20		24		28	

NOTES:

1 ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982

2 DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-

3 DIMENSION E TO BE DETERMINED AT SEATING PLANE -C-

4 DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE -H-

5 DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .006 PER SIDE

6 DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 PER SIDE

7 THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND .010 FROM LEAD TIP

8 LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .004 IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT

9 THE CHAMFER ON THE PACKAGE BODY IS OPTIONAL. IF IT IS NOT PRESENT, A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE ZONE INDICATED

10 ALL DIMENSIONS ARE IN INCHES

11 THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO–137, VARIATION AB, AD, AE & AF. EXCEPTIONS: JEDEC DIMENSION A2 MAX IS .059

TOLERANCES UNLESS SPECIFIED
DECIMAL ANGULAR
XX± ±
XXX±
XXXX±

APPROVALS	DATE
DRAWN	
CHECKED	

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Santa Clara, CA 95054
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FAX: (408) 492–8674

TITLE PC/PCG PACKAGE OUTLINE .150" BODY WIDTH QSOP .025" PITCH

SIZE	DRAWING No.	REV
C	PSC–4040	05

DO NOT SCALE DRAWING