

設計驗證
工程課
2024 -05- 23
發行
鈺泰科技開發股份有限公司

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APPROVAL SHEET

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APPROVED BY:	
BRAND NAME:	**ITE Tech Inc.**
PART NO.:	**IT6801FN/BX**
DESCRIPTION:	**IC MHL/HDMI RX IT6801FN/BX** **IC (IT6801FN,QFN76,ITE)**
COMPANY PART NO.:	**TY.7AD10.006** **3AIT680101Y** (A0547)
COMPANY MODEL NO.:	
SENDING DATE:	**2024/5/22**
SENT BY:	安 馳 科 技 股 份 有 限 公 司

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安馳科技股份有限公司
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IT6801FN

Single-port MHL2.1/HDMI1.4 Receiver with 3D Support

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ITE TECH. INC.

General Description

The IT6801FN is a single-port HDMI receiver which can operate in both HDMI1.4 and MHL2.1 dual mode, it is fully compatible with MHL2.1, HDMI 1.4b, HDMI 1.4b 3D and HDCP 1.4 and also backward compatible to DVI 1.0 specifications. The IT6801FN with its Deep Color capability (up to 36-bit) ensures robust reception of high-quality uncompressed video content. The IT6801FN also supports all the primary 3D formats which are compliant with the HDMI 1.4b 3D specification.

Aside from the various video output formats supported, the IT6801FN also receives and provides up to 4 channels of I^2S digital audio outputs, with sampling rate up to 192kHz and sample size up to 24 bits, facilitating direct connection to industry-standard low-cost audio DACs. Also, an S/PDIF output is provided to support up to compressed audio of 192kHz frame rate.

Each IT6801FN comes preprogrammed with an unique HDCP key, in compliance with the HDCP 1.4 standard so as to provide secure transmission of high-definition content. Users of the IT6801FN need not purchase any HDCP keys or ROMs.

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Features

- Single-port MHL2.1/HDMI 1.4b receiver.
- Support MHL2.1, HDMI1.4b dual mode input.
- MHL/HDMI mode auto detection.
- MHL RCP command to HDMI CEC interactive translation.
- Compliant with MHL2.1, HDMI 1.4b, HDMI 1.4b 3D, HDCP 1.4 and DVI 1.0 specifications
- Supporting link speeds of up to 3.0Gbps (link clock rate of 300MHz) for 4K2K or 1080p@120hz solution. And up to 1080p@30hz on MHL packed pixel mode.
- Supporting all the primary 3D formats which are compliant with the HDMI 1.4b 3D specification.
  - Supporting 3D video up to 1080P@50/59.95/60/120Hz, 1080P@23.98/24/29.97/30Hz, 1080i@50/59.94/60Hz, 720P@23.98/24/29.97/30Hz, 720P@50/59.94/60Hz
  - Supporting formats: Framing Packing, Side-by-Side (half), Top-and-Bottom.

- Video output interface supporting digital video standards such as:
  - 24-bit RGB/YCbCr 4:4:4
  - 16-bit YCbCr 4:2:2
  - 8-bit YCbCr 4:2:2 (ITU BT-656)
  - 24-bit double data rate interface (full bus width, pixel clock rate halved, clocked with both rising and falling edges)
  - Input channel swap

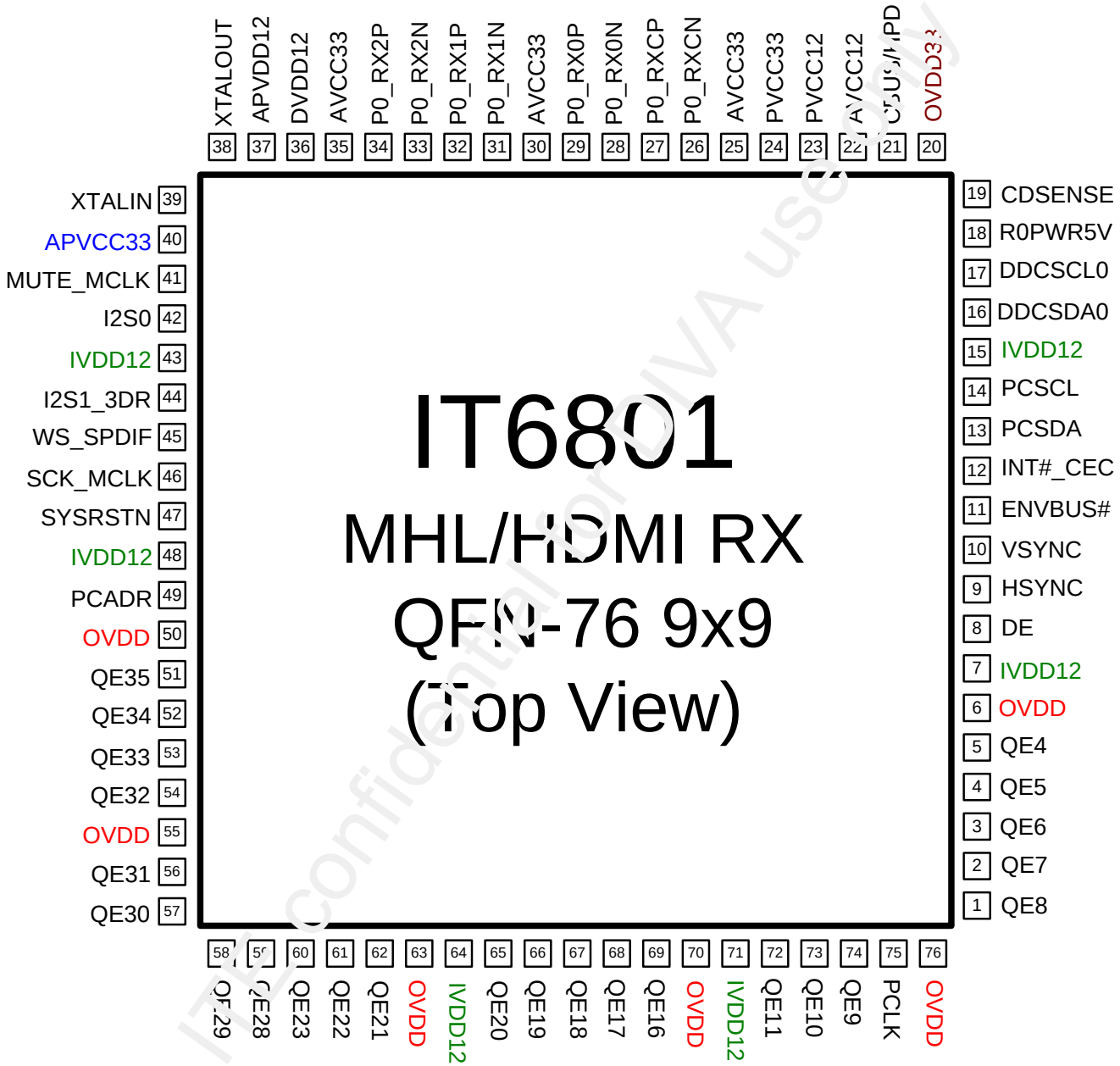
- Bi-direction Color Space Conversion (CSC) between RGB and YCbCr color spaces with programmable coefficients.
- Up/down sampling between YCbCr 4:4:4 and YCbCr 4:2:2
- Dithering for conversion from 12-bit component to 8-bit
- Digital audio output interface supporting
  - up to two I^2S interface supporting 4-channel audio, with sample rates of 32~192 kHz and sample sizes of 16~24 bits
  - S/PDIF interface supporting PCM, Dolby Digital, DTS digital audio at up to 192kHz frame rate
  - automatic audio error detection for programmable soft mute, preventing annoying harsh output sound due to audio error or hot-unplug
- Auto-calibrated input termination impedance provides process-, voltage- and temperature-invariant matching to the input transmission lines.
- Integrated pre-programmed HDCP keys
- Integrated programmable EDID RAM
- Intelligent, programmable power management
- 76-pin QFN (9mm x 9mm) package
- RoHS Compliant (100% Green available)

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Ordering Information

Model	Temperature Range	Package Type	Green/Pb free Option
IT6801FN	-20~70	76-pin QFN	Green

Pin Diagram



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Figure 1. IT6801FN pin diagram

Note:

1. Pins marked with NC should be left unconnected.

Pin Description

Digital Video Output Pins

Pin Name	Direction	Description	Type	Pin No.
QE[35:28] QE[23:16] QE[11:4]	Output	Digital Video Output Pins. Channel swap are supported through register setting.	LVTTL	1-5, 51-54, 56-62, 65-69, 72-74
PCLK	Output	Output data clock. The backend controller should use the rising edge of PCLK to strobe QE Data.	LVTTL	75
DE	Output	Data enable	LVTTL	8
HSYNC	Output	Horizontal sync. signal	LVTTL	9
VSYNC	Output	Vertical sync. signal	LVTTL	10

Digital Audio Output Pins

Pin Name	Direction	Description	Type	Pin No.
XTALIN	Input	Crystal clock input (for Audio PLL)	LVTTL	39
XTALOUT	Output	Crystal clock output (for Audio PLL)	LVTTL	38
MCLK_MUTE	Output	Audio master clock, doubles as Mute output	LVTTL	41
SCK_MCLK	Output	I2S serial clock output, doubles as audio master clock output	LVTTL	46
WS_SPDIF	Output	I2S word select output, doubles as S/PDIF audio output	LVTTL	45
I2S0	Output	I2S serial data output	LVTTL	42
I2S1_3DR	Output	I2S serial data output, doubles as doubles as 3D R/L signal	LVTTL	44

Programming Pins

Pin Name	Direction	Description	Type	Pin No.
INT#_CEC	Output	Interrupt output. Default active-low (5V-tolerant), doubles as CEC function I/O (5V-tolerant)	LVTTL	12
SYSRSTN	Input	Hardware reset pin. Active LOW	Schmitt	47
DDCSCL0	I/O	DDC I2C Clock for HDMI Port 0 (5V-tolerant)	Schmitt	17
DDCSDA0	I/O	DDC I2C Data for HDMI Port 0 (5V-tolerant)	Schmitt	16
R0PWR5V	Input	TMDS transmitter detection for Port 0(5V-tolerant)	LVTTL	18
PCSCL	Input	Serial Programming Clock for chip programming (5V-tolerant)	Schmitt	14
PCSDA	I/O	Serial Programming Data for chip programming (5V-tolerant)	Schmitt	13
PCADR	Input	Serial Programming device address select. Device address is 0x90 when PCADR is pulled low, 0x92 otherwise	LVTTL	49
CDSENSE	Input	This pin is used to detect MHL connection (5V-tolerant)	LVTTL	19
CBUS/HPD	I/O	In MHL mode this pin is the Control Bus signal. The CBUS	LVTTL	21

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		signal is 1.8V. In HDMI mode this pin serves as the HPD out signal		
ENVBUS#	Output	Power supply control output in MHL mode (5V-tolerant)	LVTTL	11

HDMI analog front-end interface pins

Pin Name	Direction	Description	Type	Pin No.
P0_RX2P	Analog	HDMI Channel 2 positive input for HDMI Port 0	TMDS	34
P0_RX2N	Analog	HDMI Channel 2 negative input for HDMI Port 0	TMDS	33
P0_RX1P	Analog	HDMI Channel 1 positive input for HDMI Port 0	TMDS	32
P0_RX1N	Analog	HDMI Channel 1 negative input for HDMI Port 0	TMDS	31
P0_RX0P	Analog	HDMI Channel 0 positive input for MHL/HDMI Port 0	TMDS	29
P0_RX0N	Analog	HDMI Channel 0 negative input for MHL/HDMI Port 0	TMDS	28
P0_RXCP	Analog	HDMI Clock Channel positive input for HDMI Port 0	TMDS	27
P0_RXCN	Analog	HDMI Clock Channel negative input for HDMI Port 0	TMDS	26

Power/Ground Pins

Pin Name	Description	Type	Pin No.
IVDD12	Digital logic power (1.2V)	Power	7, 15, 43, 48, 64, 71
IVSS	Digital logic ground	Ground	77
OVDD	I/O Pin power (3.3V or 1.8V)	Power	6, 50, 55, 63, 70, 76
OVDD33	3/5V I/O Pin power (3.3V)	Power	20
OVSS	I/O Pin ground	Ground	77
AVCC33	MHL/HDMI analog frontend power (3.3V)	Power	25, 30, 35
APVCC33	MHL/HDMI PLL and analog frontend power (3.3V)	Power	40
PVCC33	MHL/HDMI PLL power (3.3V)	Power	24
AVCC12	MHL/HDMI analog frontend power (1.2V)	Power	22,
PVCC12	MHL/HDMI receiver PLL power (1.2V)	Power	23
DVDD12	MHL/HDMI AFE digital power (1.2V)	Power	36
APVDD12	MHL/HDMI audio PLL power (1.2V)	Power	37
Exposed Pad	Analog, Digital, I/O Ground Plane	Ground Plane	77

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Functional Description

The IT6801FN is the 4th generation MHL/HDMI receiver and provides complete solutions for HDMI v1.4b Sink systems, supporting reception and processing of Deep Color video and state-of-the-art digital audio. The IT6801FN with its HDMI input port supports color depths of 10 bits and 12 bits up to 1080p. And with its MHL/HDMI dual mode port support MHL2.1 signal input up to 1080p60hz. Advanced processing algorithms are employed to optimize the performance of video processing such as color space conversion and up/down sampling. The following picture is the functional block diagram of the IT6801FN, which describes clearly the data flow.

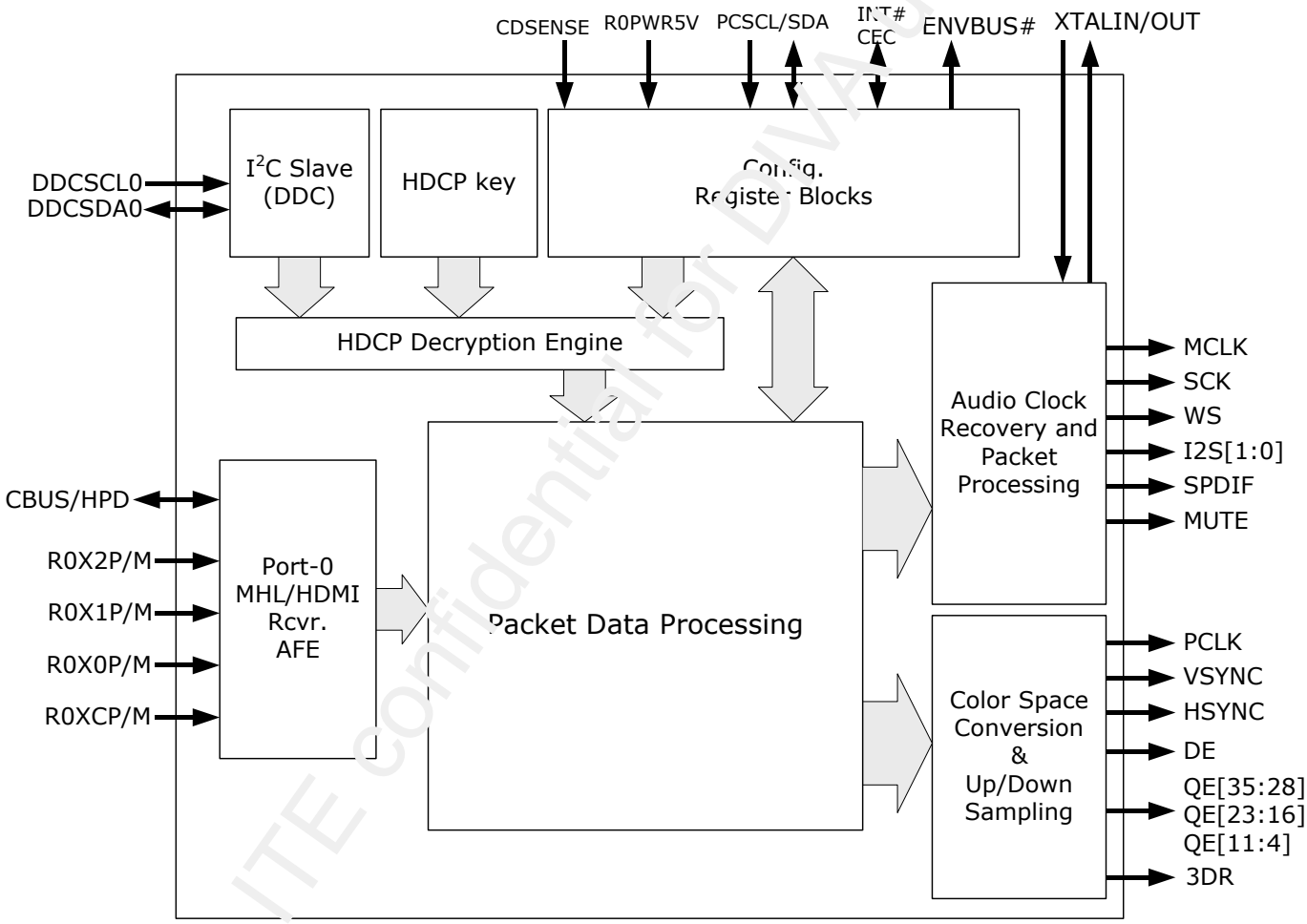


Figure 2. Functional block diagram of the IT6801FN

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Receiver Analog Frontend (Rcvr. AFE)

The integrated TMDS receiver analog frontend macros are capable of receiving and decoding MHL/HDMI data at up to 3.0Gbps (with a TMDS clock of 300MHz). Adaptive equalization is employed to support long cables.

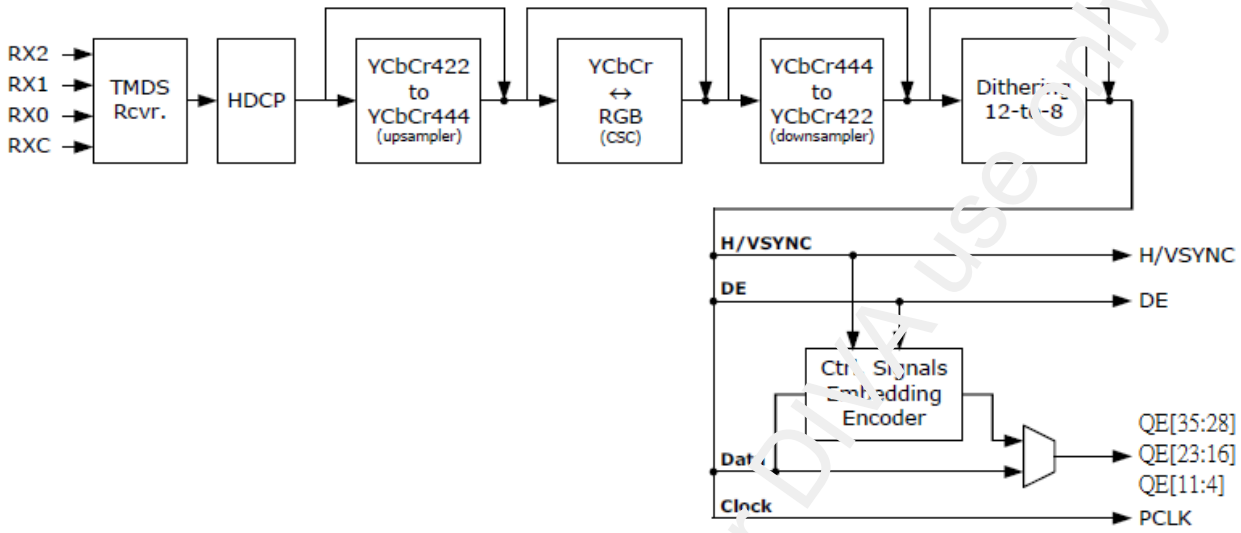


Figure 3. Video Data Processing flow of the IT6801FN

Video Data Processing Flow

Figure 3 depicts the video data processing flow. For the purpose of retaining maximum flexibility, most of the block enablings and path bypassings are controlled through register programming. Please refer to IT6801FN Programming Guide for detailed and precise descriptions.

As can be seen from Figure 3, the received and recovered HDMI raw data is first HDCP-decrypted. The extracted video data then go through various processing blocks, as described in the following paragraphs, before outputting the proper video format to the backend video controller.

The video processing including YCbCr up/down-sampling, color-space conversion and dithering. Depending on the selected input and output video formats, different processing blocks are either enabled or bypassed via register control. For the sake of flexibility, this is all done in software register programming. Therefore, extra care should be taken in keeping the selected output format and the corresponding video processing block selection. Please refer to the IT6801FN Programming Guide for suggested register setting.

The output interface could be configured through register setting to provide various data formats as listed in Table 1 in order to cater to different preferences of different backend controllers.
Major video processing in the IT6801FN are carried out in 14 bits per channel in order to minimize

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rounding errors and other computational residuals that occur during processing. General description of video processing blocks is as follows:

HDCP engine (HDCP)

The HDCP engine decrypts in incoming data. Preprogrammed HDCP keys are embedded in the IT6801FN. Users need not worry about the purchasing and management of the HDCP keys as ITE Tech. will take care of them.

Up-sampling (YCbCr422 to YCbCr444)

In cases where input HDMI video data are in YCbCr 4:2:2 format and output is selected as 4:4:4, this block is enabled to do the upsampling. Well-designed signal filtering is employed to avoid visible artifacts generated during upsampling.

Bi-directional Color Space Conversion (YCbCr <-> RGB)

Many video decoders only offer YCbCr outputs, while DVI 1.0 supports only RGB color space. In order to offer full compatibility between various Source and Sink combination, this block offers bi-directional RGB <-> YCbCr color space conversion (CSC). To provide maximum flexibility, the matrix coefficients of the CSC engine in the IT6801FN are fully programmable. Users could elect to employ their preferred conversion formula.

Down-sampling (YCbCr444 to YCbCr422)

In cases where input HDMI video data are in YCbCr 4:4:4 format and output is selected as YCbCr 4:2:2, this block is enabled to do the downsampling. Well-designed signal filtering is employed to avoid visible artifacts generated during downsampling.

Dithering (Dithering 10-to-8 or 12-to-8)

For outputing to the 8-bits-per-channel formats, decimation might be required depending on the exact input formats. This block performs the necessary dithering for decimation to prevent visible artifacts from appearing.

Supported output Video Formats

Table 1 lists the output video formats supported by the IT6801FN. The listed Output Pixel Clock Frequency in MHz is the actual clock frequency at the output pin PCLK, regardless of the color depth. According to the HDMI Specification v1.4b, the input TMDS clock frequency could be 1.25 times or 1.5 times that of the output PCLK frequency, depending on the color depth:

For 24-bit inputs, TMDS Clock frequency = 1 x PCLK frequency

For 30-bit inputs, TMDS Clock frequency = 1.25 x PCLK frequency

For 36-bit inputs, TMDS Clock frequency = 1.5 x PCLK frequency

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The IT6801FN also provides automatic video mode detection. The system controller can elect to check out respective status registers to get the information.

					Output Pixel Clock Frequency (MHz)			
Color Space	Video Format	Bus Width	H/Vsync	Clocking	480P	720P	1080P	4Kx2K
RGB	4:4:4	24	Seperate	1X	27	74.25	148.5	
		24	Seperate	0.5X, Dual-edged	13.5	37.125	74.25	148.5
YCbCr	4:4:4	24	Seperate	1X	27	74.25	148.5	
		24	Seperate	0.5X, Dual-edged	13.5	37.125	74.25	148.5
	4:2:2	16	Seperate	1X	27	74.25	148.5	
			Seperate	0.5X, Dual-edged	13.5	37.125	74.25	148.5
			Embedded	1X	27	74.25	148.5	
			Embedded	0.5X Dual-edged	13.5	37.125	74.25	148.5
		8	Seperate	2X	54	148.5		
			Seperate	1X, Dual-edged	27	74.25	148.5	
			Embedded	2X	54	148.5		
			Embedded	1X, Dual-edged	27	74.25	148.5	
	BTA1004	16	Embedded	1X	27	74.25	148.5	
			Embedded	0.5X, Dual-edged	13.5	37.125	74.25	148.5

Table 1 Output video formats supported by the T6801FN

Notes:

1. Table cells that are left blanks are those format combinations that are not supported by the IT6801FN.

2. Output channel number is defined by the way the three color components (either R, G & B or Y, Cb & Cr) are arranged. Refer to Video Data Bus Mappings for better understanding.

3. Embedded sync signals are defined by CCIR-656 standard, using SAV/EAV sequences of FF, 00, 00, XY.

4. The lowest TMDS clock frequency specified by the HDMI standard is 25MHz for 640X480@60Hz.

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Supported 3D Formats

The IT6801FN supports all the HDMI 1.4b 3D mandatory formats including

1920x1080P@50Hz --Top-and-Bottom

1920x1080P@59.94/60Hz --Top-and-Bottom

1920x1080P@29.97/30Hz --Framing Packing, Top-and-Bottom

1920x1080P@23.98/24Hz --Framing Packing, Side-by-Side (Half), Top-and-Bottom

1920x1080i@50Hz –Frame Packing, Side-by-Side (Half)

1920x1080i@59.94/60Hz –Frame Packing, Side-by-Side (Half)

1280x 720P@50Hz --Framing Packing, Side-by-Side (Half), Top-and-Bottom

1280x 720P@59.94/60Hz --Framing Packing, Side-by-Side (Half), Top-and-Bottom

Audio Clock Recovery and Data Processing

The audio processing block in the HDMI Sink is crucial to the system performance since human hearing is susceptive to audio imperfection. The IT6801FN prides itself in outstanding audio recovery performances. In addition, the audio clock recovery PLL uses an external crystal reference so as to provide stable and reliable audio clocks for all audio output formats.

The IT6801FN supports up to 4 channels and all audio formats specified by the HDMI Specification v1.4b through I^2S, S/PDIF.

I^2S

Two I^2S outputs are provided to support 4-channel uncompressed audio data at up to 192kHz sample rate. A coherent multiple (master) clock MCLK is generated at pin 41 to facilitate proper functions of mainstream backend audio DAC ICs. The supported multiplied factor and sample frequency as well as the resultant MCLK frequencies are summarized in Table 2.

Multiple of audio sample frequency	Audio sample frequency						
	32kHz	44.1kHz	48kHz	88.2kHz	96kHz	176.4kHz	192kHz
128	4.096	5.645	6.144	11.290	12.288	22.579	24.576
256	8.192	11.290	12.288	22.579	24.576	45.158	49.152
384	12.288	16.934	18.432	33.869	36.864	67.738	73.728
512	16.384	22.579	24.576	45.158	49.152	90.317	98.304
640	20.480	28.224	30.720	56.448	61.440	(112.896)	(122.880)
768	24.576	33.868	36.864	67.738	73.728	(135.475)	(147.456)
896	28.672	39.514	43.008	79.027	86.016	(158.054)	(172.032)
1024	32.768	45.158	49.152	90.316	98.304	(180.634)	(196.608)

Table 2. Output MCLK frequencies (MHz) supported by the T6801FN

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Notes:

1. *The MCLK frequencies in parenthesis are MCLK frequencies over 100MHz. These frequencies are implemented in the IT6801FN and could be output through register setting as well. However, the I/O circuit of the MCLK pin does not guarantee to be operating at such a high frequency under normal operation conditions. In addition, few audio backend ICs such as DACs support such high MCLK frequencies. Therefore, using the MCLKs in parenthesis is strongly discouraged.*

S/PDIF

The S/PDIF output provides 2-channel uncompressed PCM data (IEC 60958) or compressed multi-channel data (IEC 61937) at up to 192kHz. By default the clock of S/PDIF is carried within the data stream itself via coding. The IT6801FN also supplies coherent MCLK in cases of S/PDIF output to help ease the implementation with certain audio processing ICs.

Smart Audio Error Detection

Some previous HDMI Sink products were reported to generate unbearably harsh sounds during hot-plug/unplug as well as unspecified audio error. IT6801FN prides itself for detecting all kinds of audio error and soft-mutes the audio accordingly, therefore preventing unpleasant noise from outputting.

Interrupt Generation

To provide automatic format setting, hot plug/unplug handling and error handling, the system micro-controller should monitor the interrupt signal output at Pin 12 (INT#). The IT6801FN generates an interrupt signal whenever events involving the following signals or situations occur:

1. A status change of incoming 5V power signals at pin 18 (corresponding to plug/unplug)
2. A status change of CDSENSE at pin 19
3. Stable video is acquired
4. Events of audio errors and/or audio mute
5. Events of ECC errors
6. Video mode change

Without software intervention the hardware of the IT6801FN should be able to output some sort of displayable video data in HDMI mode. However, this video could be in the wrong format or color space. Also, hardware alone is not sufficient in handling the exception events listed above. The micro-controller must monitor the INT# signal carefully and poll the corresponding registers for optimum operation.

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Configuration and Function Control

The IT6801FN comes with two serial programming ports: one for interfacing with micro-controller, the other allowing access by HDMI Sources through the DDC channels of the HDMI link or received CBUS to DDC transactions of the MHL link.

The serial programming interface for interfacing the micro-controller is a slave interface, comprising PCSCL (Pin 14) and PCSDA (Pin 13). The micro-controller uses this interface to monitor all the statuses and control all the functions. Two device addresses are available, depending on the input logic level of PCADR (Pin 49). If PCADR is pulled high by the user, the device address is **0x92**. If pulled low, **0x90**.

Since the IT6801FN provides single MHL/HDMI input port, one DDC I^2C interface are present at DDCSCL0(Pin 17)& DDCSDA0(Pin 16). With the interfaces, the IT6801FN responds to the access of HDMI Sources via the DDC channels or translate the CBUS protocol to DDC protocol. HDMI Sources use the interfaces to perform HDCP authentication with the IT6801FN.

All serial programming interfaces conform to standard I^2C transactions and operate at up to 100kHz.

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Electrical Specifications

Absolute Maximum Ratings

Symbol	Parameter	Min	Typ	Max	Unit
AVCC33	HDMI analog frontend power	-0.3		4.0	V
OVDD33	I/O pins supply voltage for 3.3/5V I/O	-0.3		4.0	V
OVDD	I/O pins supply voltage for 3.3V/1.8V IO	-0.3		4.0	V
PVCC33	HDMI receiver PLL power	-0.3		4.0	V
IVDD12	Core logic supply voltage	-0.3		1.5	V
DVDD12	HDMI digital frontend power	-0.3		1.5	V
AVCC12	HDMI analog frontend power	-0.3		1.5	V
PVCC12	HDMI receiver PLL power	-0.3		1.5	V
APVDD12	HDMI audio PLL power	-0.3		1.5	V
VI(non 3/5V)	Input voltage for non 3/5V IO	-0.3		OVDD+0.3	V
VI(3/5V)	Input voltage 3/5V IO	-0.3		5.3	V
Vo	Output Voltage	0.3		OVDD+0.3	V
TJ	Junction Temperature			125	℃
TSTG	Storage Temperature	-65		150	℃
ESD_HB	Human body mode ESD sensitivity	2000			V
ESD_MM	Machine mode ESD sensitivity	200			V

Notes:

1. Stresses above those listed under Absolute Maximum Ratings might result in permanent damage to the device.

Functional Operation Conditions

Symbol	Parameter	Min	Typ	Max	Unit
AVCC33	HDMI analog frontend power	3.0	3.3	3.6	V
OVDD33	I/O pins supply voltage for 3.3/5V I/O	3.0	3.3	3.6	V
OVDD	I/O pins supply voltage for 3.3V/1.8V IO	1.62	3.3/1.8	3.6	V
PVCC33	HDMI receiver PLL power	3.0	3.3	3.6	V
IVDD12	Core logic supply voltage	1.14	1.2	1.35	V
DVDD12	HDMI digital frontend power	1.14	1.2	1.35	V
AVCC12	HDMI analog frontend power	1.14	1.2	1.35	V
PVCC12	HDMI receiver PLL power	1.14	1.2	1.35	V
APVDD12	HDMI audio PLL power	1.14	1.2	1.35	V
$V_{CCNOISE}$	Supply noise			100	mV_{PP}
T_A	Ambient temperature	-20		70	℃
Θ_{ja}	Junction to ambient thermal resistance		TBD		℃/W

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Notes: *1. AVCC33, AVCC12, PVCC33, PVCC12and APVDD12 should be regulated.*

2. AVCC33 supplies the termination voltage. Therefore the range is specified by the HDMI Standard.

Operation Supply Current Specification

Symbol	parameter	PCLK	Typ	Max	Unit
I_{AVCC33_OP}	AVCC33 current under normal operation	27MHz	55.2	58.5	mA
		74.25MHz	55.7	59.1	mA
		148.5MHz	55.8	59.2	mA
		222.75MHz	55.8	59.1	mA
		297MHz	54.4	58.7	mA
I_{OVDD33_OP}	OVDD33 current under normal operation	27MHz	2.6	2.8	mA
		74.25MHz	2.6	2.8	mA
		148.5MHz	2.6	2.8	mA
		222.75MHz	2.6	2.8	mA
		297MHz	2.52	2.7	mA
I_{OVDD_OP} (3.3V)	OVDD current under normal operation	27MHz	10.9	13.80	mA
		74.25MHz	16.9	21.39	mA
		148.5MHz	32.6	41.98	mA
		222.75MHz	37	47.73	mA
		297MHz	50.9	64.40	mA
I_{OVDD_OP} (2.5V)	OVDD current under normal operation	27MHz	10.9	13.69	mA
		74.25MHz	16.1	19.67	mA
		148.5MHz	26.6	33.58	mA
		222.75MHz	26.7	33.81	mA
		297MHz	34.4	43.47	mA
I_{OVDD_OP} (1.8V)	OVDD current under normal operation	27MHz	7.3	9.66	mA
		74.25MHz	10.7	14.15	mA
		148.5MHz	17.3	22.77	mA
		222.75MHz	17.1	23.00	mA
		297MHz	16.5	22.89	mA
I_{PVCC33_OP}	PVCC33 current under normal operation	27MHz	1.5	1.56	mA
		74.25MHz	3.0	3.1	mA
		148.5MHz	3.7	3.9	mA
		222.75MHz	6.0	6.2	mA
		297MHz	9.0	9.2	mA
I_{IVDD12_OP}	IVDD12 current under normal operation	27MHz	9.1	9.9	mA
		74.25MHz	20.0	22.1	mA

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		148.5MHz	36.6	40.5	mA
		222.75MHz	46.1	51.2	mA
		297MHz	60	65	mA
I_{DVDD12_OP}	DVDD12 current under normal operation	27MHz	2.3	2.6	mA
		74.25MHz	6.6	7.3	mA
		148.5MHz	13.2	14.6	mA
		222.75MHz	19.5	21.5	mA
		297MHz	25.3	27	mA
I_{AVCC12_OP}	AVCC12 current under normal operation	27MHz	40.6	46	mA
		74.25MHz	44.0	50	mA
		148.5MHz	46.6	53	mA
		222.75MHz	51.5	56.8	mA
		297MHz	57.2	63.6	mA
I_{PVCC12_OP}	PVCC12 current under normal operation	27MHz	1.1	1.5	mA
		74.25MHz	2.0	2.5	mA
		148.5MHz	3.5	4	mA
		222.75MHz	5.1	5.7	mA
		297MHz	6.6	7	mA
$I_{APVDD12_OP}$	APVDD12 current under normal operation	27MHz	0.77	0.86	mA
		74.25MHz	1.19	1.3	mA
		148.5MHz	1.27	1.41	mA
		222.75MHz	1.31	1.45	mA
		297MHz	2.2	2.4	mA
P_{TOTAL_OP} (OVDD=3.3V)	Total power consumption under normal operation when OVDD is 3.3V.	27MHz	296.30	355.09	mW
		74.25MHz	346.61	419.16	mW
		148.5MHz	433.91	535.91	mW
		222.75MHz	482.83	594.62	mW
		297MHz	566.41	700.86	mW
P_{TOTAL_OP} (OVDD=2.5V)	Total power consumption under normal operation when OVDD is 2.5V.	27MHz	287.58	343.05	mW
		74.25MHz	331.09	396.24	mW
		148.5MHz	392.83	477.15	mW
		222.75MHz	427.48	515.78	mW
		297MHz	484.44	588.56	mW
P_{TOTAL_OP} (OVDD=1.8V)	Total power consumption under normal operation when OVDD is 1.8V.	27MHz	273.47	324.54	mW
		74.25MHz	310.10	370.17	mW
		148.5MHz	357.47	429.89	mW
		222.75MHz	391.51	468.35	mW

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		297MHz	428.14	514.33	mW

Notes:

1. *Typ: OVDD33=AVCC33=PVCC33=3.3V, IVDD12=DVDD12=AVCC12=PVCC12=APVDD12=1.2V. Max:OVDD33=AVCC33=PVCC33=3.6V, IVDD12=DVDD12=AVC12=PVCC12=APVDD12=1.3V, $OVDD_{Max}=1.1*OVDD_{Typ}$.*
   *PCLK=27MHz: 480p with 48kHz/8-channel audio, PCLK=74.25MHz: 720p with 192kHz/8-channel audio, PCLK=148.5MHz: 1080p with 192kHz/8-channel audio, PCLK=222.75MHz: 1080p@**36-bit Deep Color** with 192kHz/8-channel audio, PCLK=297MHz: 4K2K with 192kHz/8-channel audio.*
2. *P_{TOTAL_OP} are calculated by multiplying the supply currents with their corresponding supply voltage and summing up all the items.*

DC Electrical Specification

Under functional operation conditions for OVDD=3.3V

Symbol	Parameter	Pin Type	Conditions	Min	Typ	Max	Unit
V_{IH}	Input high voltage	LVTTL		2.0			V
V_{IL}	Input high voltage	LVTTL				0.8	V
V_T	Switching threshold	LVTTL			1.5		V
V_{T-}	Schmitt trigger negative going threshold voltage	Schmitt		0.8	1.1		V
V_{T+}	Schmitt trigger positive going threshold voltage	Schmitt			1.6	2.0	V
V_{OL}	Ouput low voltage	LVTTL	I_{OL} = 4~16mA			0.4	V
V_{OH}	Output high voltage	LVTTL	I_{OH} = -4~-16mA	2.4			V
I_{IN}	Input leakage current	all	V_{IN} = 3.6V or 0		± 2		μA
I_{OZ}	Tri-state output leakage current	all	V_{IN} = 3.6V or 0		± 5		μA
I_{OL}	Serial programming output sink current	Schmitt	V_{OUT} = 0.2V	4		16	mA
V_{diff}	TMDS input differential swing	TMDS		150		1200	mV

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Under functional operation conditions for OVDD=1.8V

Symbol	Parameter	Pin Type	Conditions	Min	Typ	Max	Unit
V_{IH}	Input high voltage	LVTTL		1.4			V
V_{IL}	Input high voltage	LVTTL				0.4	V
V_T	Switching threshold	LVTTL			0.8		V
V_{T-}	Schmitt trigger negative going threshold voltage	Schmitt		0.45	0.6		V
V_{T+}	Schmitt trigger positive going threshold voltage	Schmitt			0.9	1.1	V
V_{OL}	Ouput low voltage	LVTTL	I_{OL} = 1.8~7.2mA			0.4	V
V_{OH}	Output high voltage	LVTTL	I_{OH} = -1.8~-7.2mA	1.3			V
I_{IN}	Input leakage current	all	V_{IN} = 2.0V or 0		± 2		μA
I_{OZ}	Tri-state output leakage current	all	V_{IN} = 2.0V or 0		± 5		μA
I_{OL}	Serial programming output sink current	Schmitt	V_{OUT} = 0.2V	1.8		7.2	mA
V_{diff}	TMDS input differential swing	TMDS		150		1200	mV

Notes:

1. Guaranteed by I/O design.

2. The serial programming output ports are not real open-drain drivers. Sink current is guaranteed by I/O design under the condition of driving the output pin with 0.2V. In a real I^2C environment, multiple devices and pull-up resistors could be present on the same bus, rendering the effective pull-up resistance much lower than that specified by the I^2C Standard. When set at maximum current, the serial programming output ports of the IT6801FN are capable of pulling down an effective pull-up resistance as low as 500Ω connected to 5V termination voltage to the standard I^2C V_{IL}. When experiencing insufficient low level problem, try setting the current level to higher than default. Refer to IT6801FN Programming Guide for proper register setting.

3. Limits defined by HDMI 1.4b standard

Audio AC Timing Specification

Under functional operation conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{S_I2S}	I2S sample rate	Up to 4 channels	32		192	KHz
F_{S_SPDIF}	S/PDIF sample rate	2 channels	32		192	KHz
F_{XTAL}	External audio crystal frequency	± 50ppm accuracy		27		MHz

Notes:

1. The IT6801FN is designed to work in default with a 27MHz crystal for audio functions.

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Video AC Timing Specification

Under functional operation conditions

Symbol	Parameter	Conditions	Min	Tye	Max	Unit
T_{PIXEL}	PCLK pixel clock period	Single-edged clocking	6.17		40	ns
F_{PIXEL}	PCLK pixel clock frequency		25		162	MHz
T_{CDE}	PCLK dual-edged clock period	Dual-edged clocking	6.66		40	ns
F_{CDE}	PCLK dual-edged clock frequency		25		150	MHz
T_{PDUTY}	PCLK clock duty cycle		40%		60%	
T_{PH}	PCLK falling edge to Transition time	single-pixel mode	0.6		1.2	ns

Notes:

1. *F_{PIXEL} is the inverse of T_{PIXEL}. Operating frequency range is given here while the actual video clock frequency should comply with all video timing standards. Refer to Table 1 for supported video timings and corresponding pixel frequencies.*
2. *All setup time and hold time specifications are with respect to the latching edge of PCLK selected by the user through register programming.*
3. *The PCLK falling edge to transition time could be got when Vclk_inv (reg[0x50]bit[4]='1') is enabled. If user intends to delay 0.5Tpixel for TTL data output, please disable Vclk_inv bit (reg[0x50]bit[4]='0'). And then T_{PH} will increase 0.5Tpixel.*

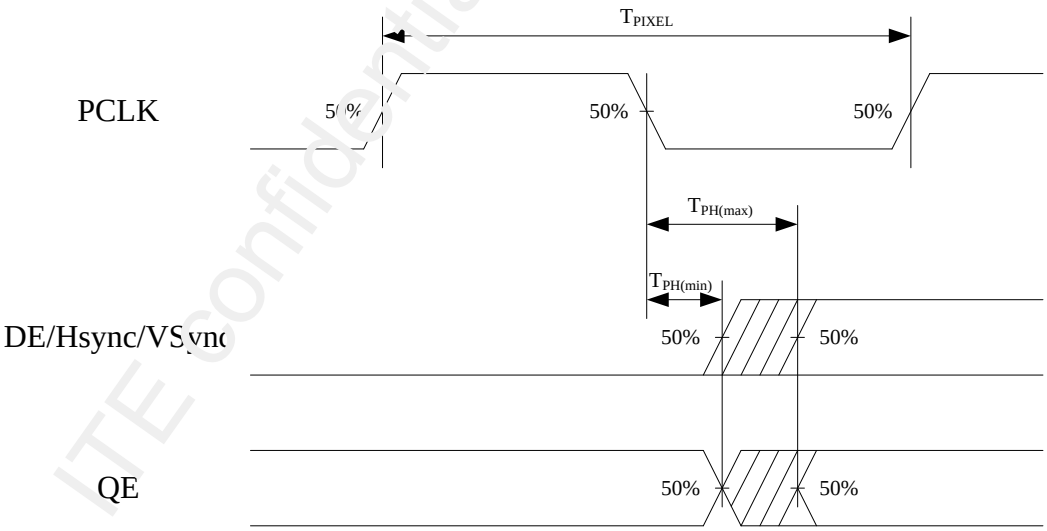
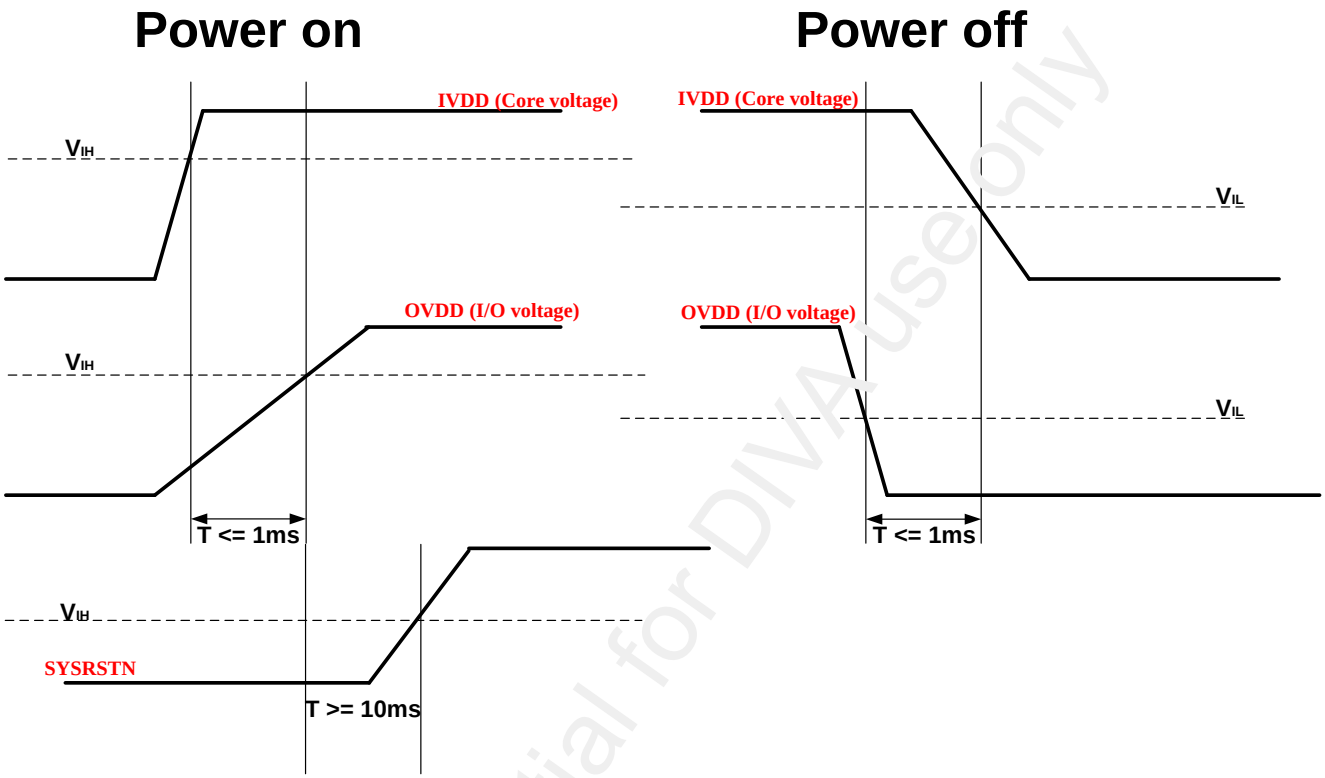


Figure 4. PCLK falling edge to transition time under single-pixel mode

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Power and System Reset Sequence



When power on, please keep IVDD go VIH before OVDD go VIH (IVDD must supply earlier than or equal to OVDD). And please keep the time interval between IVDD and OVDD shorter than 1ms when power on or power off.

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Video Data Bus Mappings

HDMI/MHL Receiver

Color Space	Video Format	Bus Width	H/Vsync	Clocking
RGB	4:4:4	24	Seperate	1X
		24	Seperate	0.5X, Dual-edged
YCbCr	4:4:4	24	Seperate	1X
		24	Seperate	0.5X, Dual-edged
	4:2:2	16	Seperate	1X
			Seperate	0.5X, Dual-edged
			Embedded	1X
			Embedded	0.5X, Dual-edged
		8	Seperate	2X
			Seperate	1X, Dual-edged
			Embedded	2X
			Embedded	1X, Dual-edged
	BTA1004	16	Embedded	1X
			Embedded	0.5X, Dual-edged

Table3. Output video format supported by the HDMI/MHL receiver

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RGB 4:4:4 and YCbCr 4:4:4 with Separate Syncs

	RGB	YCbCr
Pin Name	24-bit	24-bit
QE4	B0	Cb0
QE5	B1	Cb1
QE6	B2	Cb2
QE7	B3	Cb3
QE8	B4	Cb4
QE9	B5	Cb5
QE10	B6	Cb6
QE11	B7	Cb7
QE16	G0	Y0
QE17	G1	Y1
QE18	G2	Y2
QE19	G3	Y3
QE20	G4	Y4
QE21	G5	Y5
QE22	G6	Y6
QE23	G7	Y7
QE28	R0	Cr0
QE29	R1	Cr1
QE30	R2	Cr2
QE31	R3	Cr3
QE32	R4	Cr4
QE33	R5	Cr5
QE34	R6	Cr6
QE35	R7	Cr7
HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC
DE	DE	DE

Table 4. RGB & YCbCr 4:4:4 Mappings

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These are the simpliest formats, with a complete definition of every pixel in each clock period. Timing examples of 24-bit RGB 4:4:4 is depicted in Figure 5.

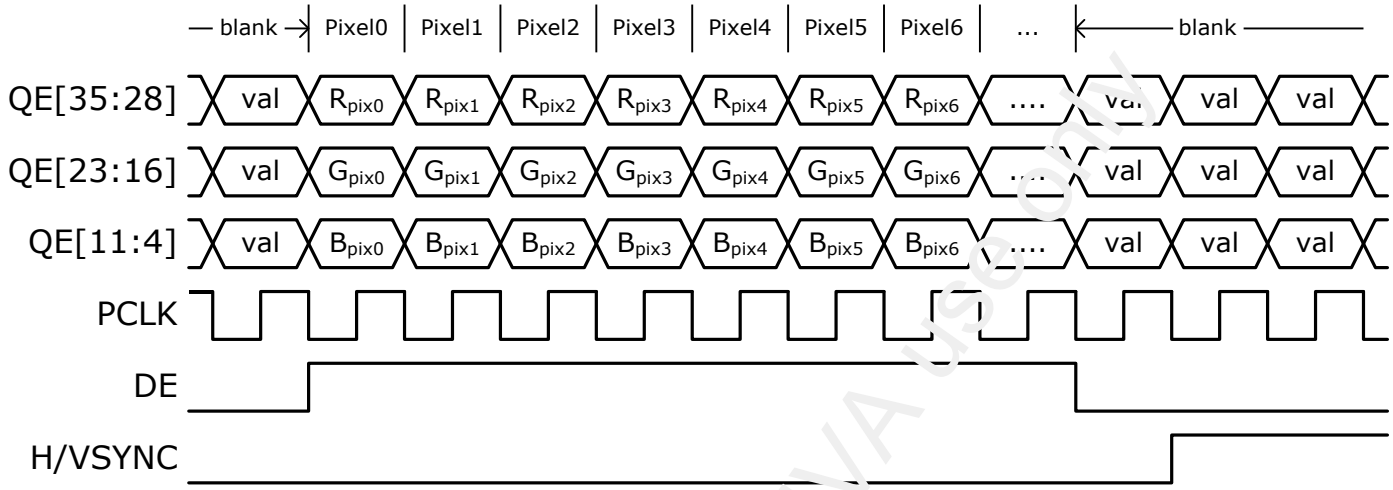


Figure 5. 24-bit RGB 4:4:4 Timing Diagram

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RGB 4:4:4 and YCbCr 4:4:4 Triggered with 0.5X PCLK at Dual Edges

The bus mapping in this format is the same as that of RGB 4:4:4 and YCbCr 4:4:4 with Separate Syncs. The only difference is that the output video clock (PCLK) is now halved in frequency. The data are in turn to be latched in with both the rising and falling edges of the 0.5X PCLK.

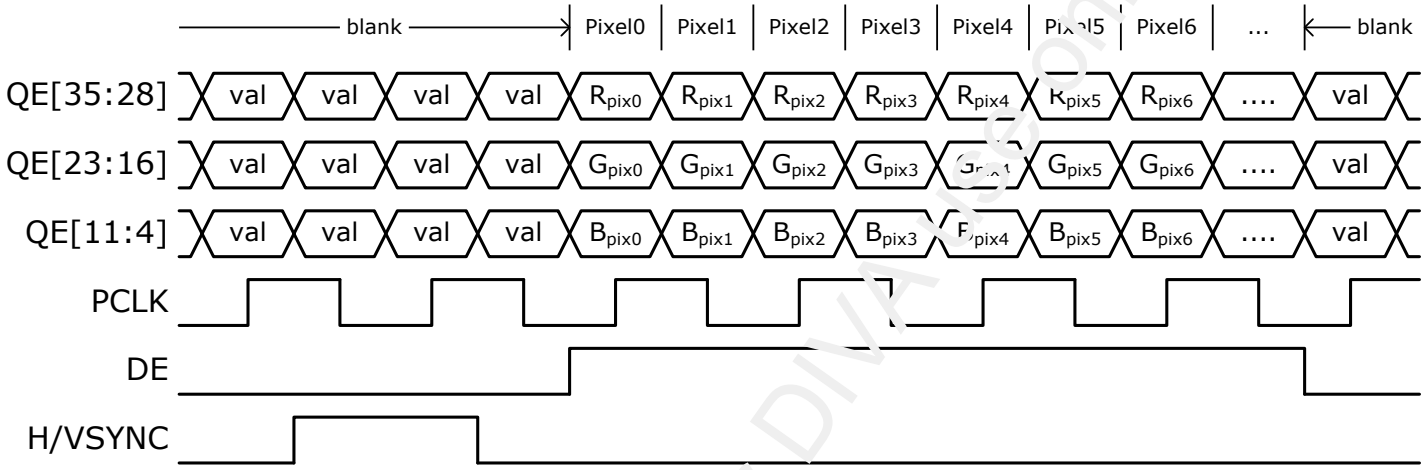


Figure 6. 24-bit RGB 4:4:4 dual-edges triggered with 0.5X PCLK

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YCbCr 4:2:2 with Separate Syncs

	16-bit	
Pin Name	Pixel#2N	Pixel#2N+1
QE4	NC	NC
QE5	NC	NC
QE6	NC	NC
QE7	NC	NC
QE8	NC	NC
QE9	NC	NC
QE10	NC	NC
QE11	NC	NC
QE16	Y0	Y0
QE17	Y1	Y1
QE18	Y2	Y2
QE19	Y3	Y3
QE20	Y4	Y4
QE21	Y5	Y5
QE22	Y6	Y6
QE23	Y7	Y7
QE28	Cb0	Cr0
QE29	Cb1	Cr1
QE30	Cb2	Cr2
QE31	Cb3	Cr3
QE32	Cb4	Cr4
QE33	Cb5	Cr5
QE34	Cb6	Cr6
QE35	Cb7	Cr7
HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC
DE	DE	DE

Table 5. Mappings of YCbCr 4:2:2 with separate syncs

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YCbCr 4:2:2 format does not have one complete pixel for every clock period. Luminace channel (Y) is given for every pixel, while the two chroma channels are given alternatively on every other clock period. The average bit amount of Y is twice that of Cb or Cr. Depending on the bus width, each component could take on different lengths. The DE period should contain an even number of clock periods. Figure 7 gives a timing example of 16-bit YCbCr 4:2:2..

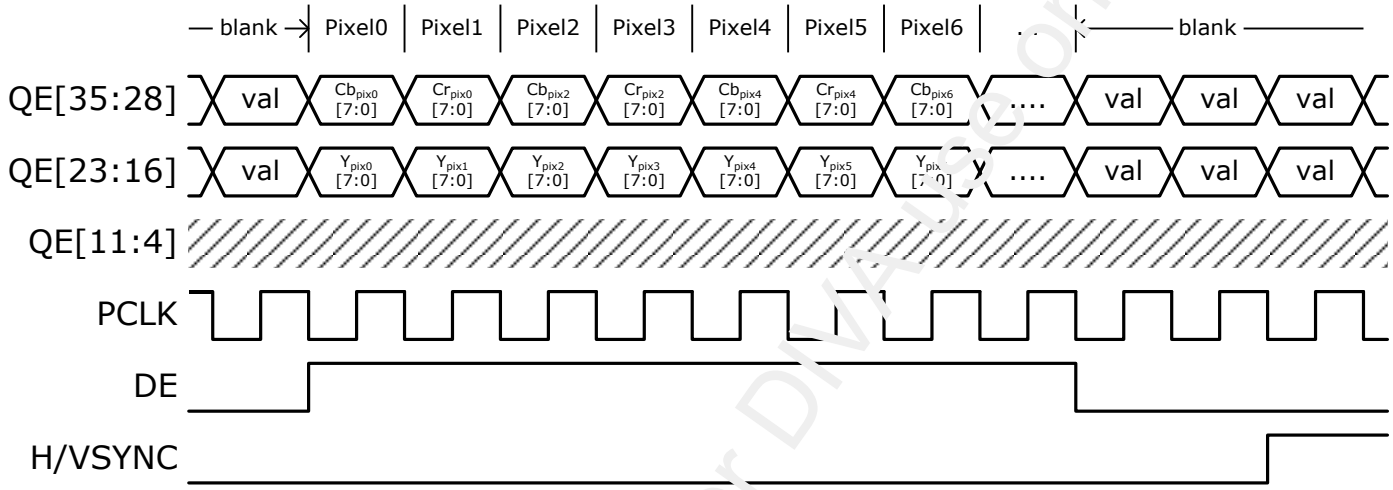


Figure 7. 16-bit YCbCr 4:2:2 with separate syncs

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YCbCr 4:2:2 with Separate Syncs Triggered with 0.5X PCLK at Dual Edges

The bus mapping in this format is the same as that of YCbCr 4:2:2 with Separate Syncs. The only difference is that the output video clock (PCLK) is now halved in frequency. The data are in turn to be latched in with both the rising and falling edges of the 0.5X PCLK.

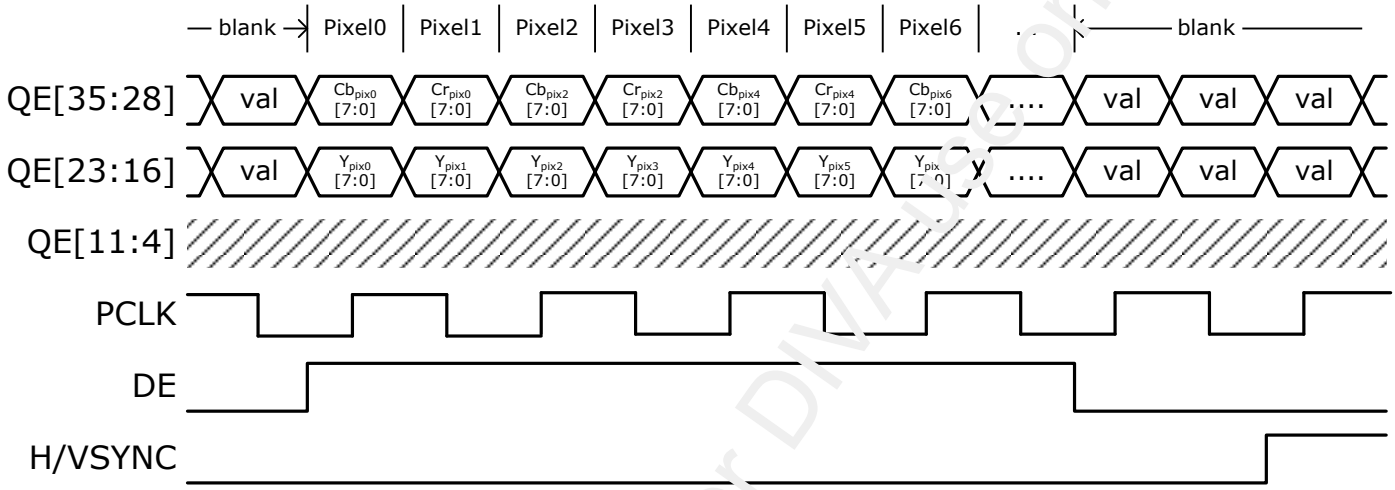


Figure 8. 16-bit YCbCr 4:2:2 with separate syncs dual-edges triggered with 0.5X PCLK

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YCbCr 4:2:2 with Embedded Syncs

	16-bit	
Pin Name	Pixel#2N	Pixel#2N+1
QE4	*NC*	*NC*
QE5	*NC*	*NC*
QE6	*NC*	*NC*
QE7	*NC*	*NC*
QE8	*NC*	*NC*
QE9	*NC*	*NC*
QE10	*NC*	*NC*
QE11	*NC*	*NC*
QE16	Y0	Y0
QE17	Y1	Y1
QE18	Y2	Y2
QE19	Y3	Y3
QE20	Y4	Y4
QE21	Y5	Y5
QE22	Y6	Y6
QE23	Y7	Y7
QE28	Cb0	Cr0
QE29	Cb1	Cr1
QE30	Cb2	Cr2
QE31	Cb3	Cr3
QE32	Cb4	Cr4
QE33	Cb5	Cr5
QE34	Cb6	Cr6
QE35	Cb7	Cr7
HSYNC	*embedded*	*embedded*
VSYNC	*embedded*	*embedded*
DE	*embedded*	*embedded*

Table 6. Mappings of YCbCr 4:2:2 with embedded syncs

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Similar to YCbCr 4:2:2 with Separate Sync. The only difference is that the syncs are now non-explicit, i.e. embedded. Bus width only could be 16-bit. Figure 9 gives a timing example of 16-bit YCbCr 4:2:2. Note that while "embedded syncs" implies that neither DE nor H/VSYNC are required, the IT6801FN optionally output these signals via proper register setting to ease the design for some backend processors.

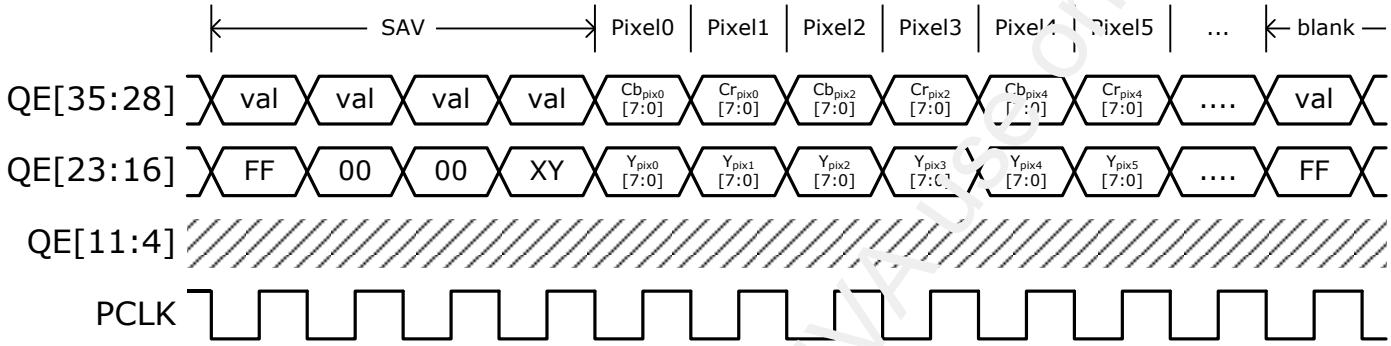


Figure 9. 16-bit YCbCr 4:2:2 with embedded syncs

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YCbCr 4:2:2 with Embedded Syncs Triggered with 0.5X PCLK at Dual Edges

The bus mapping in this format is the same as that of YCbCr 4:2:2 with Embedded Syncs. The only difference is that the output video clock (PCLK) is now halved in frequency. The data are in turn to be latched in with both the rising and falling edges of the 0.5X PCLK.

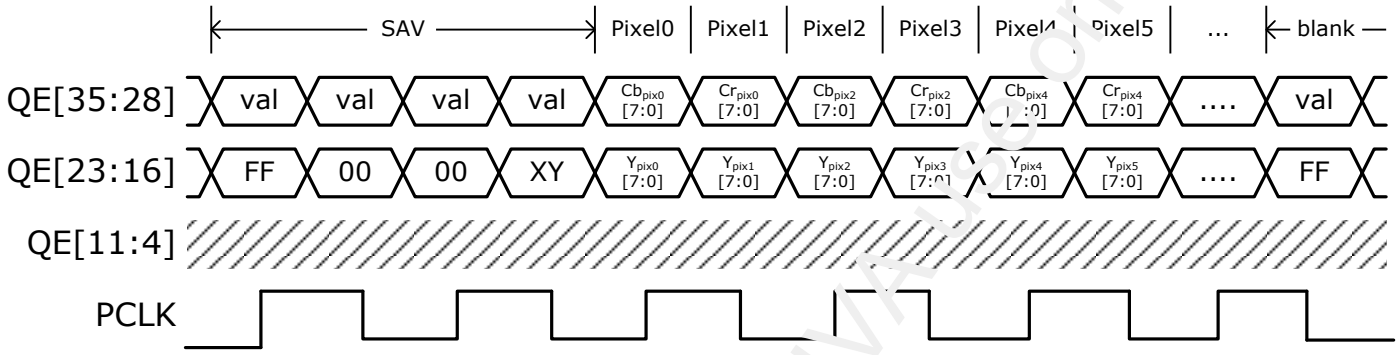


Figure 10. 16-bit YCbCr 4:2:2 with embedded syncs dual-edges triggered with 0.5X PCLK

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CCIR-656 Format

	8-bit	
Pin Name	PCLK#2N	PCLK#2N+1
QE4	NC	NC
QE5	NC	NC
QE6	NC	NC
QE7	NC	NC
QE8	NC	NC
QE9	NC	NC
QE10	NC	NC
QE11	NC	NC
QE16	C0	Y0
QE17	C1	Y1
QE18	C2	Y2
QE19	C3	Y3
QE20	C4	Y4
QE21	C5	Y5
QE22	C6	Y6
QE23	C7	Y7
QE28	NC	NC
QE29	NC	NC
QE30	NC	NC
QE31	NC	NC
QE32	NC	NC
QE33	NC	NC
QE34	NC	NC
QE35	NC	NC
HSYNC	embedded	embedded
VSYNC	embedded	embedded
DE	embedded	embedded

Table 7. Mappings of CCIR-656

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The CCIR-656 format is yet another variation of the YCbCr formats. The bus width is further reduced by half compared from the previous YCbCr 4:2:2 formats to 8-bit. To compensate for the halving of data bus, PCLK frequency is doubled. With the double-rate output clock, luminance channel (Y) and chroma channels (Cb or Cr) are alternated. The syncs signals are embedded in the Y-channel. Normally this format is used only for 480i, 480p, 576i and 576p. The IT6801FN supports CCIR-656 format of up to 720p or 1080i, with the doubled-rate clock running at 148.5MHz. CCIR-656 format supports embedded syncs only. Figure 11 give examples of 8-bit CCIR-656. Note that while "embedded syncs" implies that neither DE nor H/VSYNC are required, the IT6801FN optionally output these signals via proper register setting to ease the design for some backend processors.

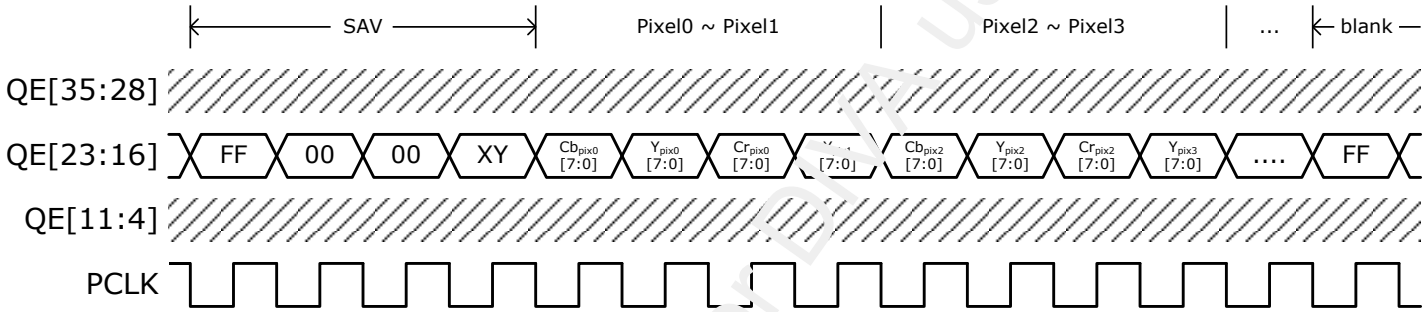


Figure 11. 8-bit CCIR-656

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CCIR-656 Triggered with 0.5X PCLK at Dual Edges

The bus mapping in this format is the same as that of CCIR-656. The only difference is that the output video clock (PCLK) is now halved in frequency. The data are in turn to be latched in with both the rising and falling edges of the 0.5X PCLK.

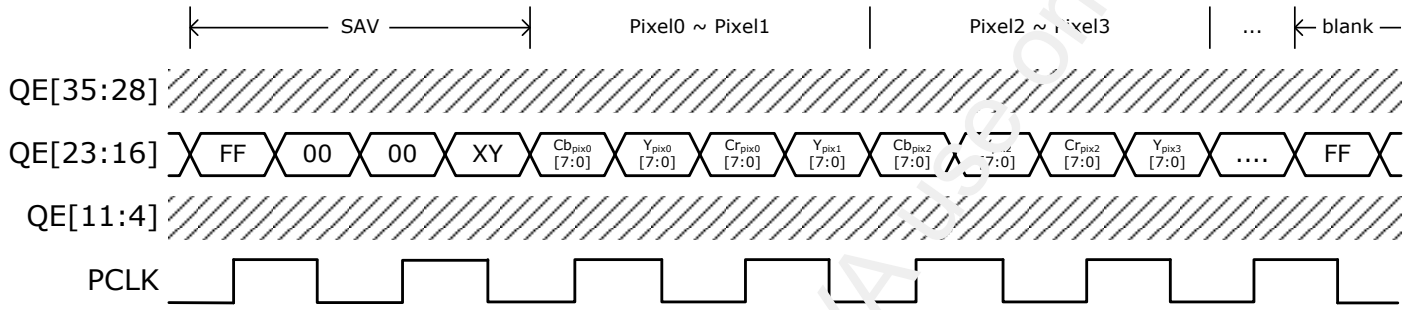


Figure 12. 8-bit CCIR-656 dual-edges triggered with 0.5X PCLK

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CCIR-656 + separate syncs

	8-bit	
Pin Name	PCLK#2N	PCLK#2N+1
QE4	NC	NC
QE5	NC	NC
QE6	NC	NC
QE7	NC	NC
QE8	NC	NC
QE9	NC	NC
QE10	NC	NC
QE11	NC	NC
QE16	C0	Y0
QE17	C1	Y1
QE18	C2	Y2
QE19	C3	Y3
QE20	C4	Y4
QE21	C5	Y5
QE22	C6	Y6
QE23	C7	Y7
QE28	NC	NC
QE29	NC	NC
QE30	NC	NC
QE31	NC	NC
QE32	NC	NC
QE33	NC	NC
QE34	NC	NC
QE35	NC	NC
HSYNC	HSYNC	HSYNC
VSYNC	VSYNC	VSYNC
DE	DE	DE

Table 8 Mappings of CCIR-656 + separate syncs

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This format is not specified by CCIR-656. It's simply the previously mentioned CCIR-656 format plus separate syncs. Examples of this mode are given in Figure 13.

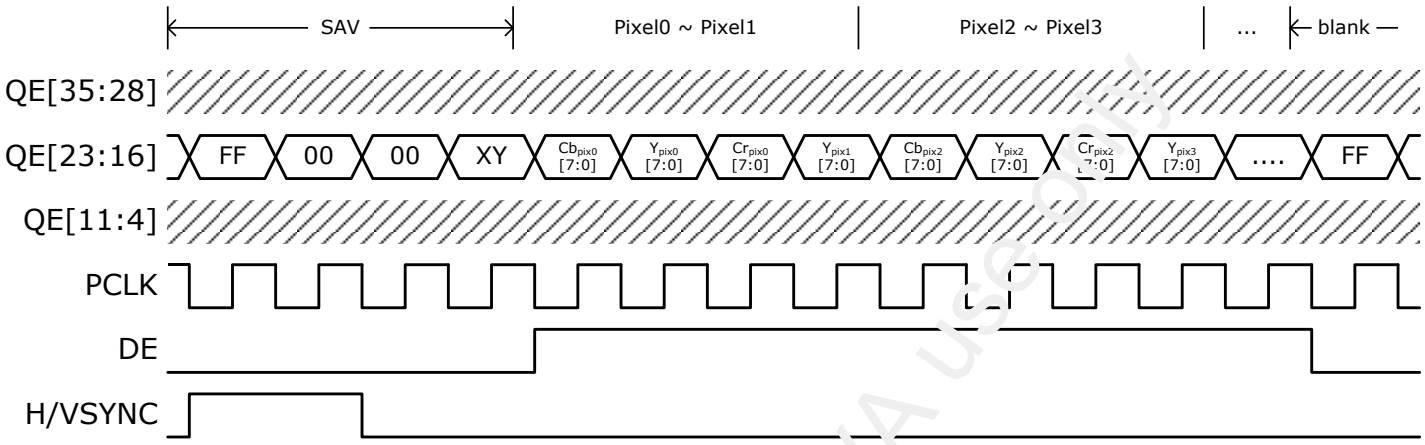


Figure 13. 8-bit CCIR-656 + separate syncs

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CCIR-656 with Separate Syncs Triggered with 0.5X PCLK at Dual Edges

The bus mapping in this format is the same as that of CCIR-656 with separate syncs. The only difference is that the output video clock (PCLK) is now halved in frequency. The data are in turn to be latched in with both the rising and falling edges of the 0.5X PCLK.

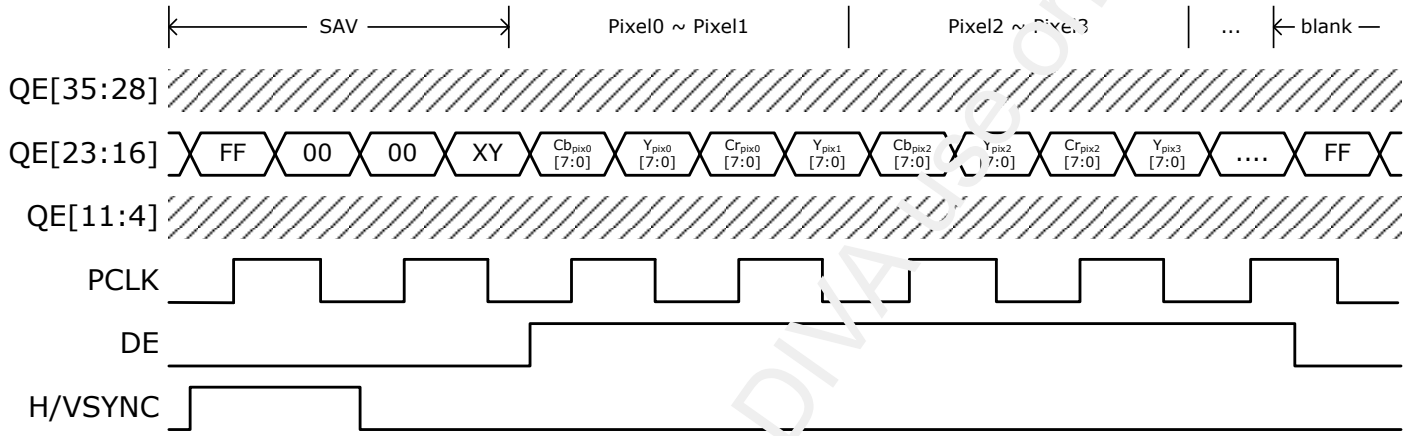


Figure 14. 8-bit CCIR-656 + separate syncs dual-edges triggered with 0.5X PCLK

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BTA1004

	16-bit	
Pin Name	Pixel#2N	Pixel#2N+1
QE4	NC	NC
QE5	NC	NC
QE6	NC	NC
QE7	NC	NC
QE8	NC	NC
QE9	NC	NC
QE10	NC	NC
QE11	NC	NC
QE16	Y0	Y0
QE17	Y1	Y1
QE18	Y2	Y2
QE19	Y3	Y3
QE20	Y4	Y4
QE21	Y5	Y5
QE22	Y6	Y6
QE23	Y7	Y7
QE28	Cb0	Cr0
QE29	Cb1	Cr1
QE30	Cb2	Cr2
QE31	Cb3	Cr3
QE32	Cb4	Cr4
QE33	Cb5	Cr5
QE34	Cb6	Cr6
QE35	Cb7	Cr7
HSYNC	embedded	embedded
VSYNC	embedded	embedded
DE	embedded	embedded

Table 9. Mappings of BTA1004

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BTA1004 data mapping format is the same as YCbCr422 with embedded syncs. The only difference is the mapping of SAV.

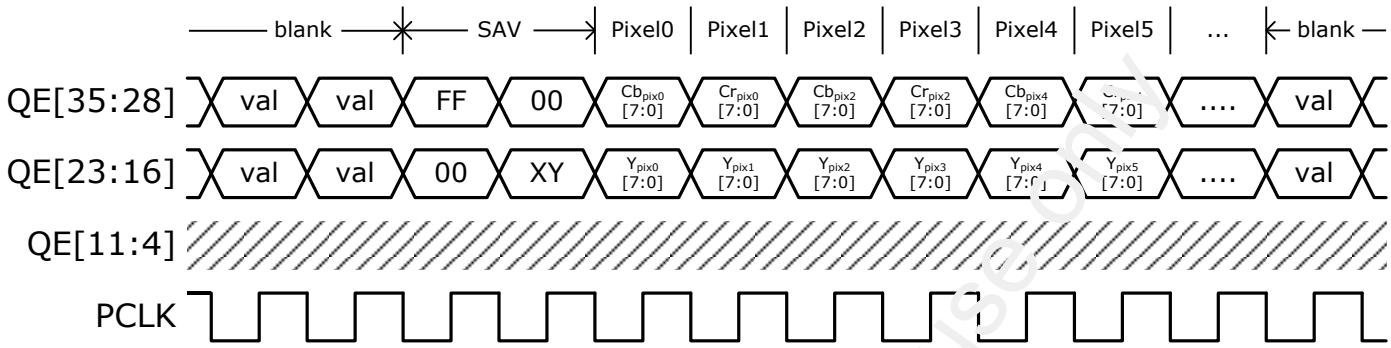


Figure 15. 16-bit BTA1004

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BTA1004 Triggered with 0.5X PCLK at Dual Edges

The bus mapping in this format is the same as that of BTA1004. The only difference is that the output video clock (PCLK) is now halved in frequency. The data are in turn to be latched in with both the rising and falling edges of the 0.5X PCLK.

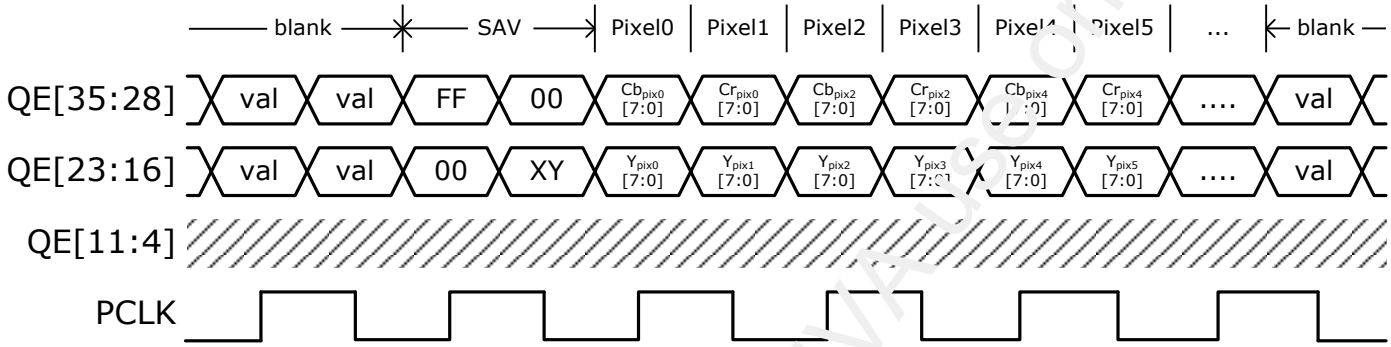


Figure 16. 16-bit BTA1004 dual-edges triggered with 0.5X PCLK

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System Design Consideration

The IT6801FN is a very high-speed interface chip. It receives TMDS differential signals at as high as 3.0 Gbps and output TTL signals at up to 148.5MHz with 24-bit DDR data bus. At such high speeds any PCB design imperfection could lead to compromised signal integrity and hence degraded performance. To get the optimum performance the system designers sould follow the guideline below when designing the application circuits and PCB layout.

1. Pin 22, 35 (APVCC12) should be supplied with clean power: ferrite-decoupled and capacitively -bypassed, since they supply the power for the receiver PLL, which is a crucial block in terms of receiving quality. Excess power noise might degrade the system performance.

2. It is highly recommended that all power pins are decoupled to ground pins via capacitors of 0.01uF and 0.1uF. Low-ESL capacitors are preferred. Generally these capacitors should be placed on the same side of the PCB with the IT6801FN and as close to the pins as possible, preferably within 0.5cm from the pins. It is also recommended that the power and ground traces run relatively short distances and are connected directly to respective power and ground planes through via holes.

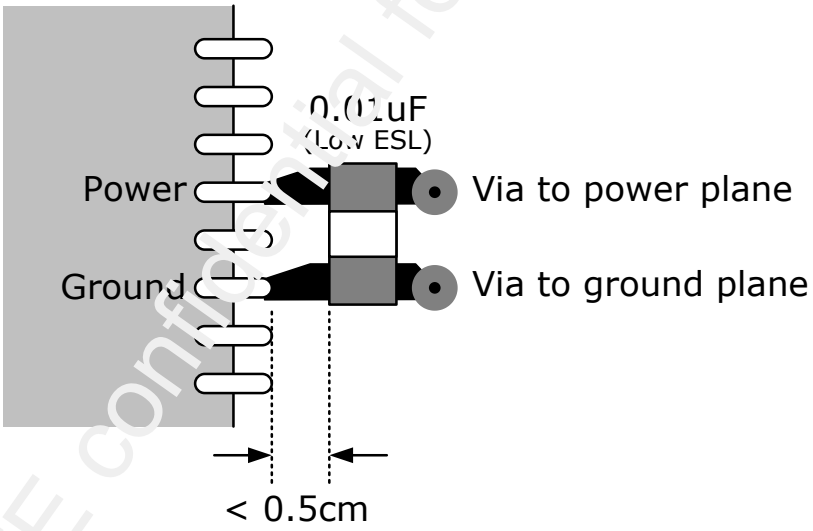


Figure 17. Layout example for decoupling capacitors.

3. The IT6801FN supports 24-bit DDR output bus running at as high as 148.5MHz. To maintain signal integrity and lower EMI, the following guidelines should be followed:

A. Employ **4-layer PCB** design, where a ground or power plane is directly placed under the signal buses at middle layers. The ground and power planes underneath these buses should be continuous in order to provide a solid return path for EM-wave introduced currents.

B. Whenever possible, keep all TTL signal traces on the same layer with the IT6801FN and the

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backend scalars.

C. TTL output traces to the scalar should be kept as short as possible
D. 33Ω resistors could be placed in series to the output pins. This slow down the signal rising edges, reduces current spikes and lower the reflections.
E. The PCLK signal should be kept away from other signal traces to avoid crosstalk interference. A general guideline is 2X the dielectric thickness. For example, if the dielectric layer between the signal layer and the immediate power/ground layer is 7 mil, then the PCLK trace should be kept at least 14 mil away from all other signal traces.

4. The characteristic impedance of all differential PCB traces should be kept at 100Ω all the way from the HDMI connector to the IT6801FN. This is crucial to the system performance at high speeds. When layouting these differential transmission lines, the following guidelines should be followed:

A. The signals traces should be on the outside layers (TOP layer or BOTTOM layer) while beneath it there should be a continuous ground plane in order to maintain the so-called micro-strip transmission line structure, giving stable and well-defined characteristic impedances.
B. Carefully choose the width and spacing of the differential transmission lines as their characteristic impedance depends on various parameters of the PCB: trace width, trace spacing, copper thickness, dielectric constant, dielectric thickness, etc. Careful 3D EM simulation is the best way to derive a correct dimension that enables a nominal 100Ω differential impedance.
C. Cornering, through holes, crossing and any irregular signal routing should be minimized so as to prevent from disrupting the EM field and creating discontinuity in characteristic impedance.
D. The IT6801FN should be placed as close to the HDMI connector as possible. If the distance between the chip and the connector is under 2 cm, the reflections could be kept small even if the PCB traces do not have an 100Ω characteristic impedance. The extra signal attenuation contributed by the PCB traces could be minimized, too.

5. Special care should be taken when adding discrete ESD devices to all differential PCB traces (RX2P/M, RX1P/M, RX0P/M, RXCP/M). The IT6801FN is designed to provide ESD protection for up to 2kV at these pins, which is good enough to prevent damages during assembly. To meet the system EMC specification, external discrete ESD diodes might be added. But note that adding discrete ESD diodes inevitably add capacitive loads, therefore degrade the electrical performance at high speeds. If not chosen carefully, these diodes coupled with less-than-optimal layout would prevent the system from passing the SINK TMDS-Differential Impedance test in the HDMI Compliance Test (Test ID 8-8). One should only use low-capacitance ESD diode to protect these high-speed pins. Commercially available devices such as Semtech's RClamp0524p that take into consideration of all aspects of designing and protecting high-speed transmission lines are recommended. *(http://www.semtech.com/*

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products/product-detail.jsp?navId=H0,C2,C222,P3028).

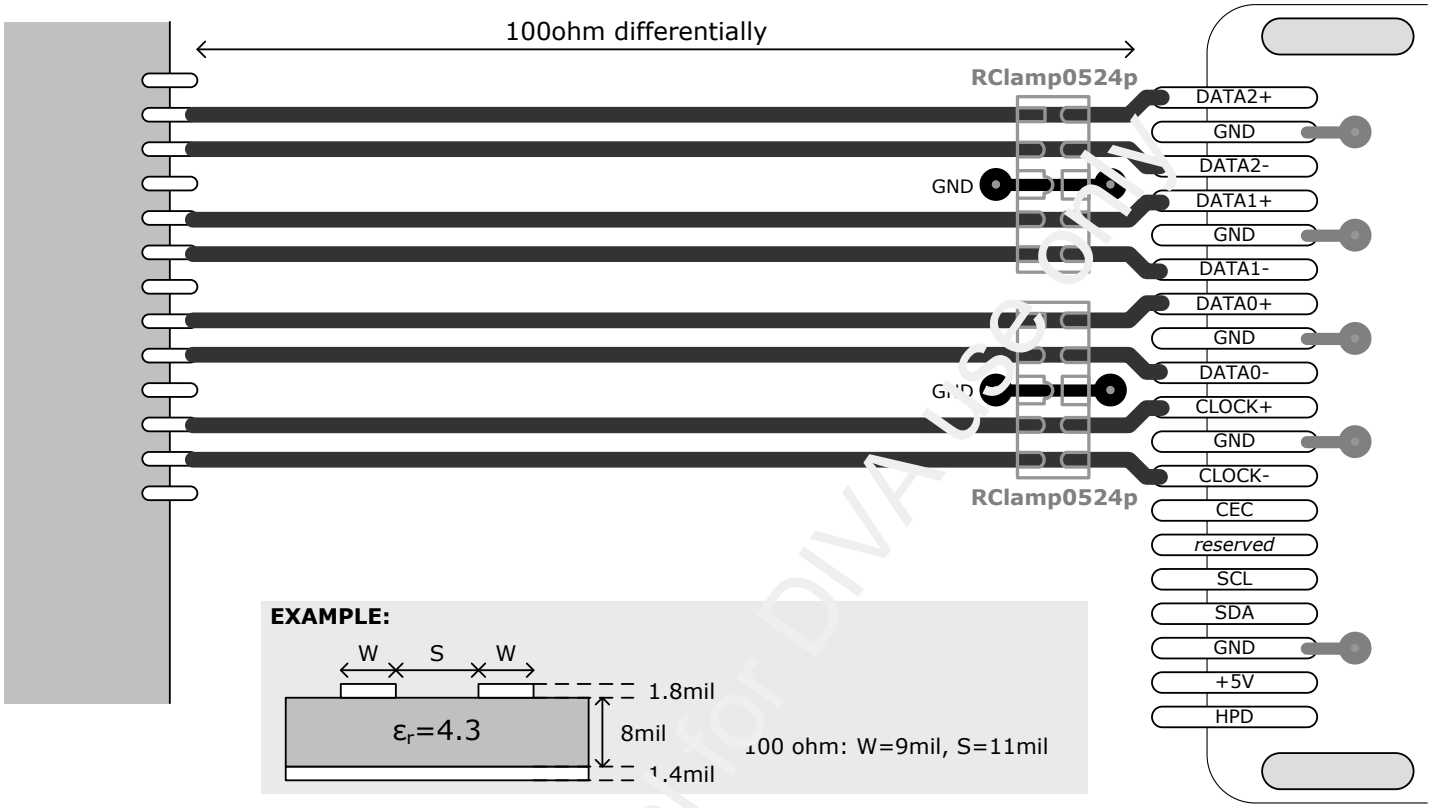
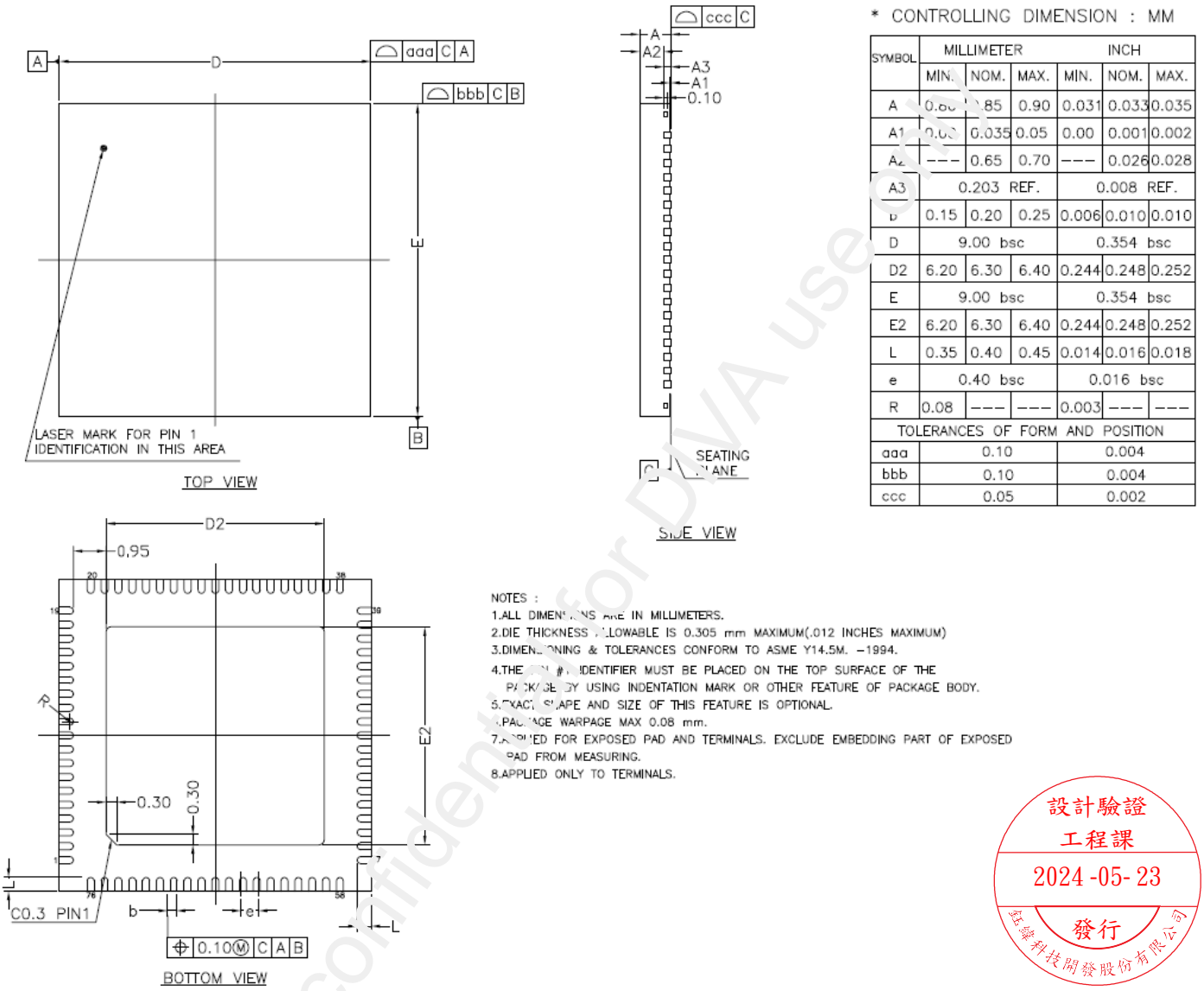


Figure 18. Layout example for High-speed TMDS differential signals

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Package Dimensions



* CONTROLLING DIMENSION : MM

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.035	0.05	0.00	0.001	0.002
A2	---	0.65	0.70	---	0.026	0.028
A3	0.203 REF.			0.008 REF.		
b	0.15	0.20	0.25	0.006	0.010	0.010
D	9.00 bsc			0.354 bsc		
D2	6.20	6.30	6.40	0.244	0.248	0.252
E	9.00 bsc			0.354 bsc		
E2	6.20	6.30	6.40	0.244	0.248	0.252
L	0.35	0.40	0.45	0.014	0.016	0.018
e	0.40 bsc			0.016 bsc		
R	0.08	---	---	0.003	---	---
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		

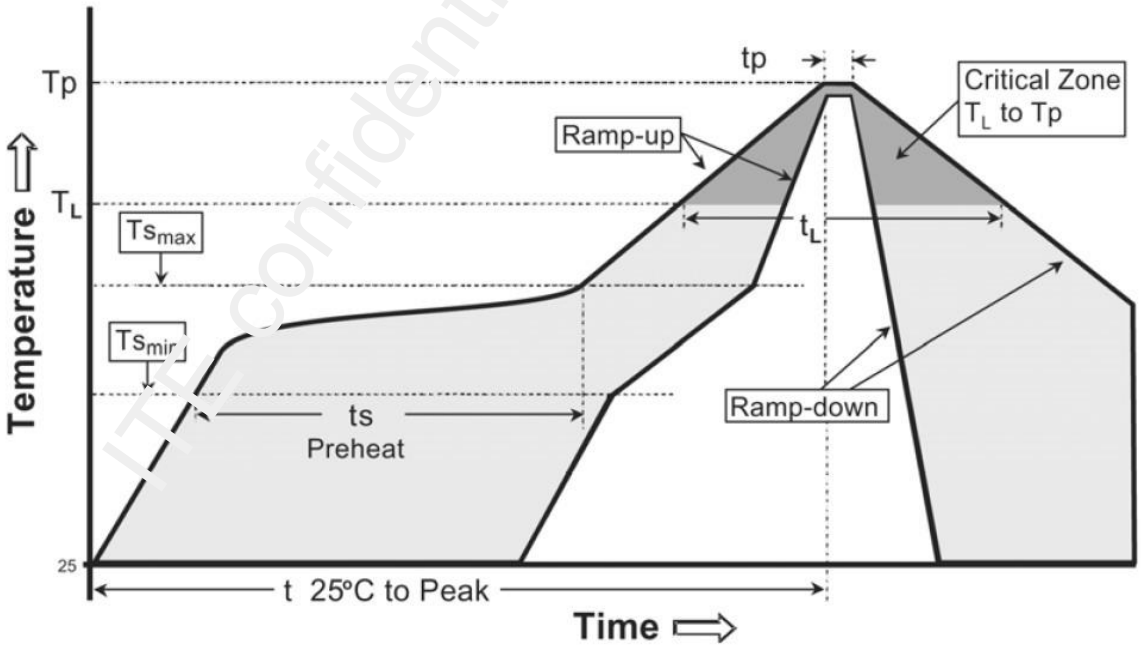
Figure 19. 76-pin QFN Package Dimensions

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Classification Reflow Profiles

Reflow Profile	Pb-Free Assembly
Average Ramp-Up Rate (Ts_{max} to Tp)	3℃/second max.
Preheat -Temperature Min(Ts_{min}) -Temperature Max(Ts_{max}) -Time(ts_{min} to ts ts_{max})	 150℃ 200℃ 60-180 seconds
Time maintained above: -Temperature(T_L) -Time(t_L)	 217℃ 60-150 seconds
Peak Temperature(Tp)	260 +0 /-5℃
Time within 5 ℃ of actual Peak Temperature(tp)	20-40 seconds
Ramp-Down Rate	6℃/second max.
Time 25℃ to Peak Temperature	8 minutes max.

Note: All Temperature refer to topside of the package, measured on the package body surface.



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