2AAD672003T(T0202)

MODEL NO : TM037YVGP01-00

MODEL VERSION: 00

SPEC VERSION : 2.0

ISSUED DATE: 2024-04-10

□**Preliminary Specification**
■**Final Product Specification**

Customer :

Approved by	Notes
設計驗證 工程課 2024-05-03 發行	

TIANMA Confirmed :

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This technical specification is subjected to change without notice

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Record of Revision

Rev	Issued Date	Description	Editor
1.0	2019.12.20	Initial release	Shuqin_Ai
1.1	2022.08.11	Update mechanical drawing	Shuqin_Ai
1.2	2023.02.03	1.Update LCD power consumption information; 2.Update drawing.	Shuqin_Ai
1.3	2023.10.13	Add CTP SPEC	Shuqin_Ai
2.0	2024.4.10	1. Add CNT1 information 2. Update weight information 3. Final SPEC released	Shuqin_Ai

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1 General Specifications

Feature		Spec
Display Spec.	Size	3.7
	Resolution	480(RGB)*800
	Technology Type	SFT
	Pixel Configuration	RGB Vertical Stripe
	Pixel pitch(mm)	0.1005 X 0.1005
	Display Mode	SFT
	Surface Treatment	AG
	Viewing Direction	85/85/85/85
Mechanical Characteristics	LCM (W*H*D) (mm)	LCM:53.14*91.30*1.81(excluding tape)
		CTP+LCM:75.2*109*3.78 (excluding tape)
	Active Area(mm)	TFT LCD:48.24*80.40
		CTP(VA):49.24*81.40
	With /Without TSP	With TSP
	Connection type on FPC	DF40C-30DP-0.4V(51)
	Matching connection type	DF40C-30DS-0.4V(51)
	LED numbers	6
	Weight (g)	55
Electrical Characteristics	Interface	MIPI
	Color Depth	16.7M
Touch Spec	Touch type	Oncell
	Interface	I2C
	Touch method	Finger
	Finger Touch Pitch	5.47mm*5.04mm
	Lamination Type	Optical-bonding
	Number of simultaneous touches	5
	Minimum Touch Area(mm)	φ7mm
	Report rate	≥60HZ
	Slave Address	0x20
	TP power consumption(typ）	30mW

Note 1: Viewing direction for best image quality is different from TFT definition. There is a 180 degree shift.

Note 2: Requirements on Environmental Protection: Q/S0002

Note 3: LCM weight tolerance: ± 5%

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2 Input/ Output Terminals

2.1 CN1 Pin assignment (LCD Interface)

Connector Information	
LCD Module connector	DF40-30DP-0.4V(51)
Matching connector	DF40-30DS-0.4V(51)

Table2.1.1 Connector information

Pin No.	Symbol	I/O	Function	Remark
1	GND	P	Ground	
2	VCC	P	Analog power supply	
3	IOVCC	P	I/O power supply	
4	RESET	I	LCD Reset signal	
5	TE	O	TE signal	
6	GND	P	Ground	
7	D1P	I	MIPI DSI 1 lane(+)	
8	D1N	I	MIPI DSI 1 lane(-)	
9	GND	P	Ground	
10	CLKP	I	MIPI DSI CLK(+)	
11	CLKN	I	MIPI DSI CLK(-)	
12	GND	P	Ground	
13	D0P	I/O	MIPI DSI 0 lane(+)	
14	D0N	I/O	MIPI DSI 0 lane(-)	
15	GND	P	Ground	
16	NC/LEDON	NC	Not Connected	
17	OTP	I	OTP voltage input pin	
18	NC	NC	Not Connected	
19	CABC	O	Driver PWM	
20	NC	NC	Not Connected	
21	LEDA	I	LED ANODE	
22	LEDK	I	LED CATHODE	
23	SWDIO	I/O	TP software input pin	

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24	TP_GND	P	Ground	
25	TP_IOVCC	P	TP IO Power supply	
26	TP_INT	O	TP interruption signal	
27	TP_SCL	I/O	I2C Serial Clock	
28	TP_SDA	I/O	I2C Serial data	
29	TP_RES	I	System reset signal	
30	TP_VDD	P	TP Power supply	

Table 2.1.2 Pin Assignment for LCD Interface

Note1: I/O definition: I---Input, O---Output, P---Power/Ground, NC---No connection

Note2: All of the GND pins should be connected to the system ground.

2.2 CN2 Pin assignment (TP interface)

Pin No	Signals	I/O	Description
1	SWDIO	I/O	TP software input pin
2	TP_RES	I	System reset signal input
3	TP_SDA	I/O	I2C Serial data
4	TP_SCL	I/O	I2C Serial Clock
5	TP_INT	O	TP interruption signal
6	TP_IOVCC	P	TP IO Power supply
7	TP_VDD	P	TP Power supply
8	GND	P	Ground

Table 2.2.2 Pin Assignment for TP Interface

Note1: I/O definition: I---Input, O---Output, P---Power/Ground, N---No connection
Note2: All of the GND pins should be connected to the system ground.

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3 Absolute Maximum Ratings

GND=0V

Item	Symbol	MIN	MAX	Unit	Remark
Power Voltage_LCD	VCC	-0.3	4.6	V	
Supply Voltage_LCD	IOVCC	-0.3	4.6	V	
Supply Voltage_TP	TP_IOVCC	-0.5	6	V	
Power Voltage_TP	TP_VDD	-0.5	6	V	
Operating Temperature	Top	-20	70	℃	
Storage Temperature	Tst	-30	80	℃	
Relative Humidity Note1	RH	--	≤95	%	Ta≤40℃
		--	≤85	%	40℃＜Ta≤50℃
		--	≤55	%	50℃＜Ta≤60℃
		--	≤36	%	60℃＜Ta≤70℃
		--	≤24	%	70℃＜Ta≤80℃
Absolute Humidity	AH	--	≤70	g/m^3	Ta＞70℃

Table 3 Absolute Maximum Ratings

Note1: Ta means the ambient temperature.It is necessary to limit the relative humidity to the specified temperature range.Condensation on the module is not allowed.
Note2: Be sure that you are grounded when handing TP
Note3: If the module exceeds the absolute maximum ratings, it may be damaged permanently. Also, if the module operated with the absolute maximum ratings for a long time, it is reliability may drop

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4 Electrical Characteristics

4.1 LCD Module

GND=0V,Ta=25℃

Item		Symbol	MIN	TYP	MAX	Unit	Remark
Logic Supply Voltage		IOVCC	1.7	1.8	1.9	V	
Analog Supply Voltage		VCC	2.7	2.8	2.9	V	
Input Signal Voltage	High Level	VIH	0.7 IOVCC	-	IOVCC	V	
	Low Level	VIL	-0.3	-	0.3 IOVCC	V	
Output Signal Voltage	High Level	VOH	0.8 IOVCC	-	IOVCC	V	
	Low Level	VOL	0	-	0.2 IOVCC	V	
(Panel+ LSI) Power Consumption		Normal Mode	-	105	-	mW	
		Sleeping Mode	-	25	-	uA	

Table 4.1 LCD module electrical characteristics

4.2 CTP

Item	Symbol	Min	Typ	Max	Unit	Remark
Power Supply	TP_VDD	2.7	2.8	2.9	V	
IO Power Supply	TP_IOVCC	1.7	1.8	1.9	V	
Power supply ripple	Vrip	-	-	±50	mV	Note1
Low input logic level	Vil	-	-	0.3* TP_IOVCC	V	
High input logic level	Vih	0.7* TP_IOVCC	-	-	V	
Low output voltage	Vol	-	-	0.6	V	
High output voltage	Voh	TP_IOVCC-0.5	-	-	V	
Consumption	Operation Mode (1 finger)	-	30	-	mW	

Table 4.2 CTP electrical characteristics

Note1: Vrip is the ripple voltage of TP_VDD and TP_IOVCC

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4.3 Backlight Unit

Ta=25℃

Item	Symbol	MIN	TYP	MAX	Unit	Remark
Forward Current	I_F	-	20	-	mA	LED current
Forward Voltage	V_F	16.2	18.6	19.8	V	LED voltage
Backlight Power Consumption	W_{BL}	-	0.372	-	W	6 LEDs
Lifetime	T	10000	20000	-	Hr	

Table 4.3 backlight unit electrical characteristics

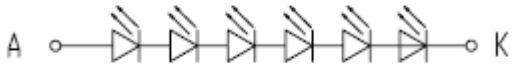


Figure 4.3 LED backlight circuit

Note: The LED lifetime 20000Hrs is defined as the module brightness decay 50% of original brightness at If=20mA,Ta=25 degree.
Environmental conditions such as sustained high operating temperatures, high humidity, operating conditions and other factors will effect on LED Lifetime.

4.4 Touch panel Characteristics

Item	Description	Note
Touch accuracy	Center:±2.0mm/Border:±4.5mm(φ7mm)	
Touch linearity	Center:±2.0mm/Border:±4.5mm(φ7mm)	
Touch Sensitivity	Center:±2.0mm/Border:±4.5mm(φ7mm)	
Touch Precision	Center:±1.5mm/Border:±2.5mm(φ7mm)	

Note1: If the module exceeds the absolute maximum ratings, it may be damaged permanently. Also, if the module operated with the absolute maximum ratings for a long time, it is reliability may drop.

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4.5 LCM module Block Diagram

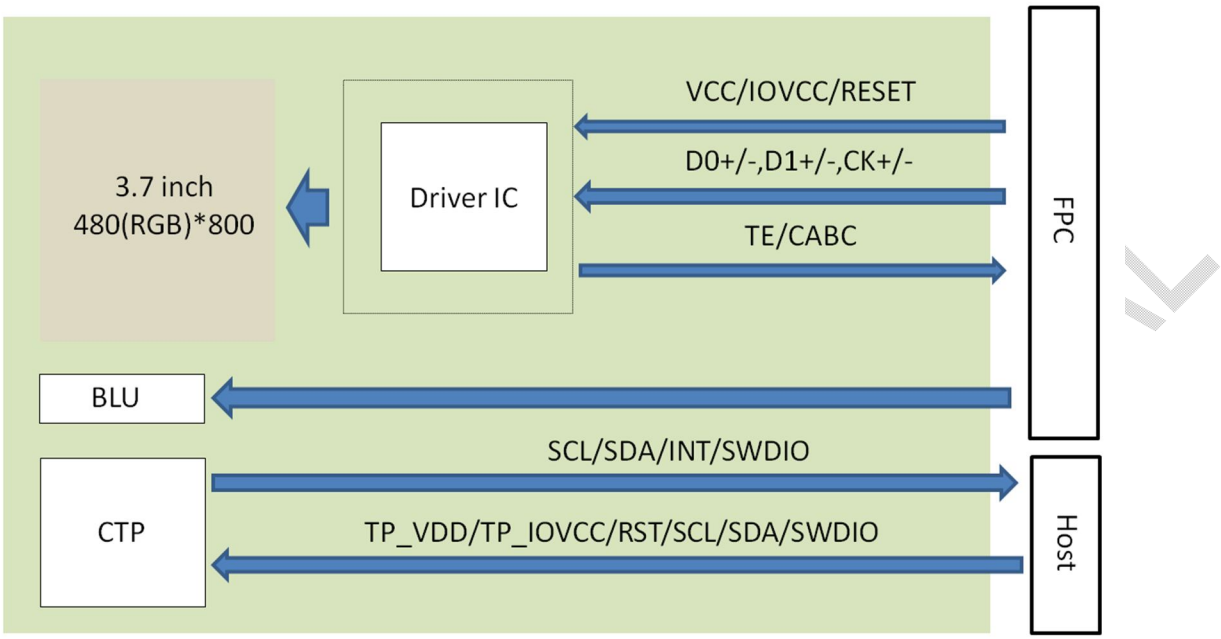


Figure 4.5 LCM module block diagram

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5 Timing Chart

5.1 High speed mode-clock channel timing

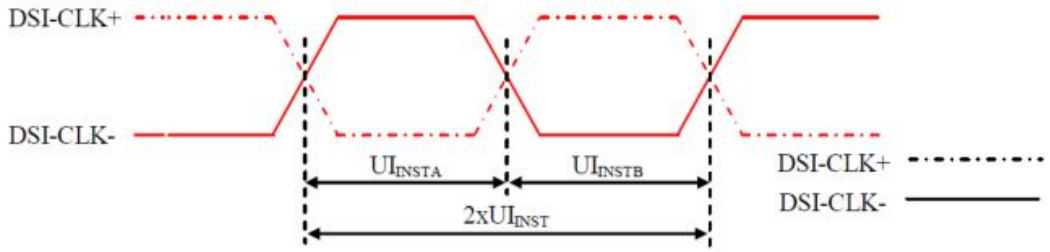


Figure DSI Clock Channel Timming

Signal	Symbol	Parameter	Min	Max	Unit
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	4	25	ns
DSI-CLK+/-	UI_{INSTA},UI_{INSTB}	UI instantaneous Half	2	12.5	ns

Note: $UI = UI_{INSTA} = UI_{INSTB}$

Table DSI Clock Channel Timming

5.2 High speed mode-Data clock channel timing

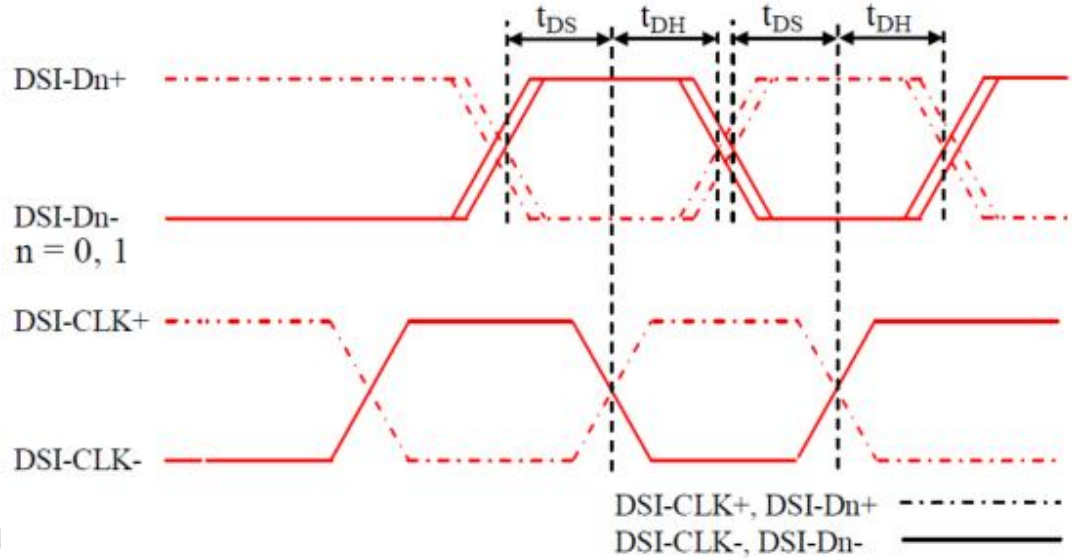


Figure DSI Data to Clock Channel Timings

Signal	Symbol	Parameter	Min	Max
DSI-Dn+/- , n=0 and 1	t_{DS}	Data to Clock Setup time	0.15xUI	-
	t_{DH}	Clock to Data Hold Time	0.15xUI	-

Table DSI Data to Clock Channel Timings

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5.3 High speed mode-Rise and Fall timing

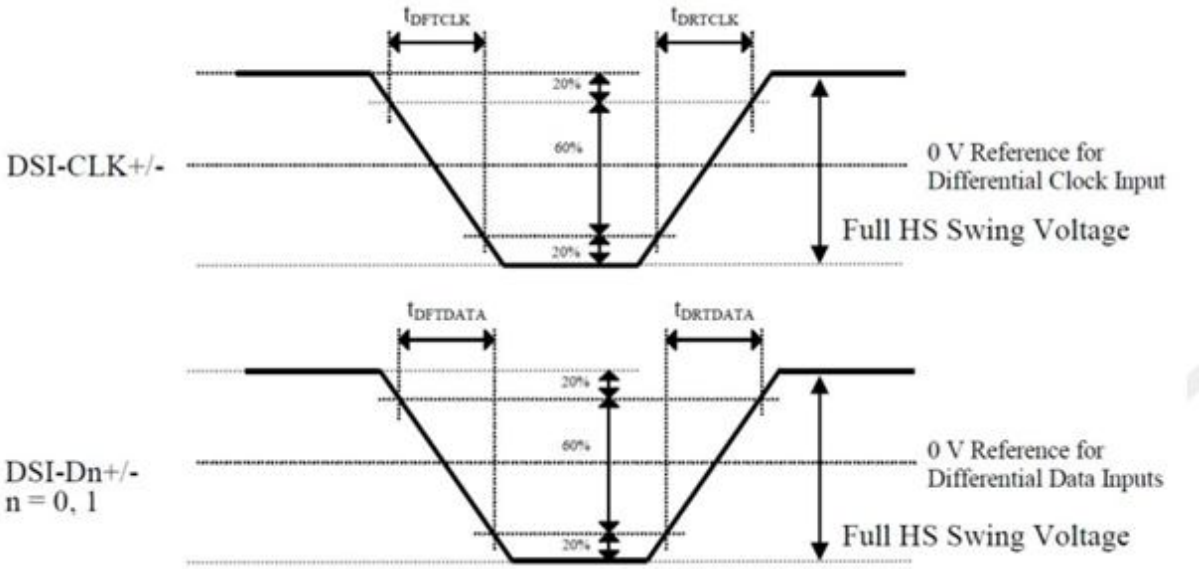


Figure Rise and Fall Timings on Clock and Data Channels

Table 47 Rise and Fall Timings on Clock and Data Channels

Parameter	Symbol	Condition	Specification			
			Min	Typ	Max	Unit
Differential Rise Time for Clock	t_{DRTCLK}	DSI-CLK+/-	150	-	0.3UI (Note)	ps
Differential Rise Time for Data	$t_{DRTDATA}$	DSI-Dn+/- n=0 and 1	150	-	0.3UI (Note)	ps
Differential Fall Time for Clock	t_{DFTCLK}	DSI-CLK+/-	150	-	0.3UI (Note)	ps
Differential Fall Time for Data	$t_{DFTDATA}$	DSI-Dn+/- n=0 and 1	150	-	0.3UI (Note)	ps

Note:The display module has to meet timing requirements, which are defined for the transmitter (MCU) on MIPI D-Phy standard

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5.4 Low speed mode-bus turn around

Lower power mode and its state periods are illustrated for reference purposes on the BusTurnaround(BTA) from the MPU to the Display Modulesequence below.

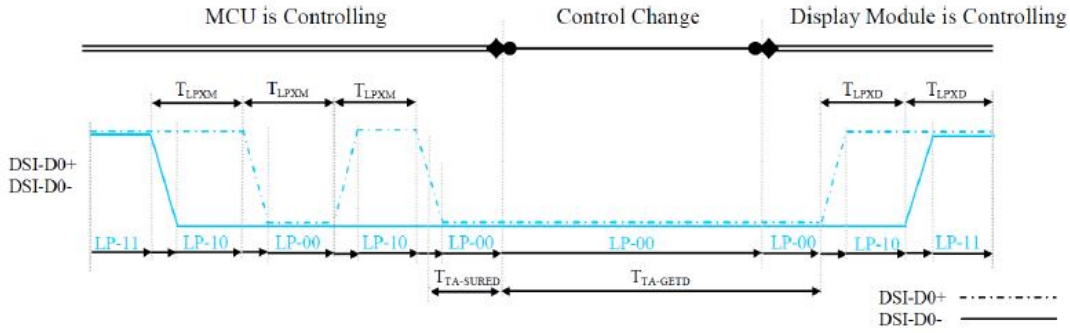


Figure BTA from the MPU to the Display Module

Lower power mode and its state periods are illustrated for reference purposes on the Bus Turnaround(BTA)from the display moduleto the MPU sequence below.

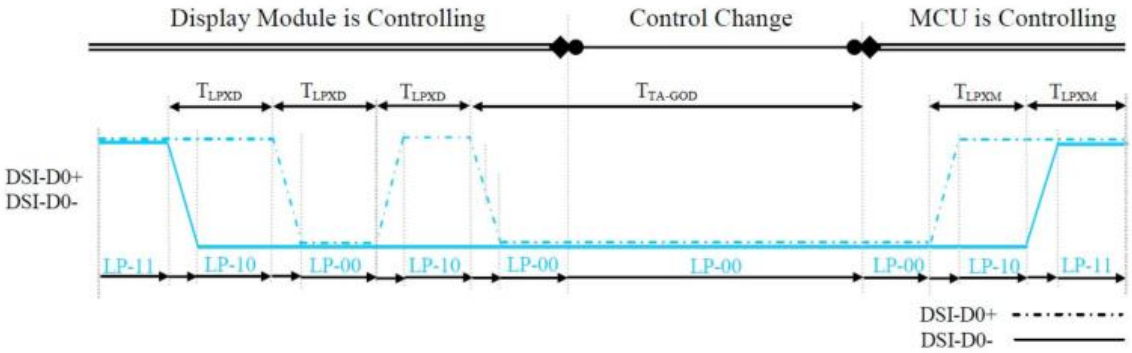


Figure BTA from the Display Module to the MPU

Signal	Symbol	Description	Min	Max	Unit
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU → Display Module	50	75	ns
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module → MPU	50	75	ns
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the Display Module starts driving	T_{LPXD}	$2\times T_{LPXD}$	ns

Table Low Power State Period Timings – A

Table 49 Low Power State Period Timings – B

Signal	Symbol	Description	Time	Unit
DSI-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by Display Module	$5\times T_{LPXD}$	ns
DSI-D0+/-	T_{TA-GOD}	Time to drive LP-00 after turnaround request – MPU	$4\times T_{LPXD}$	ns

Table Low Power State Period Timings – B

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5.5 Data Lanes from Low Power Mode to High Speed Mode

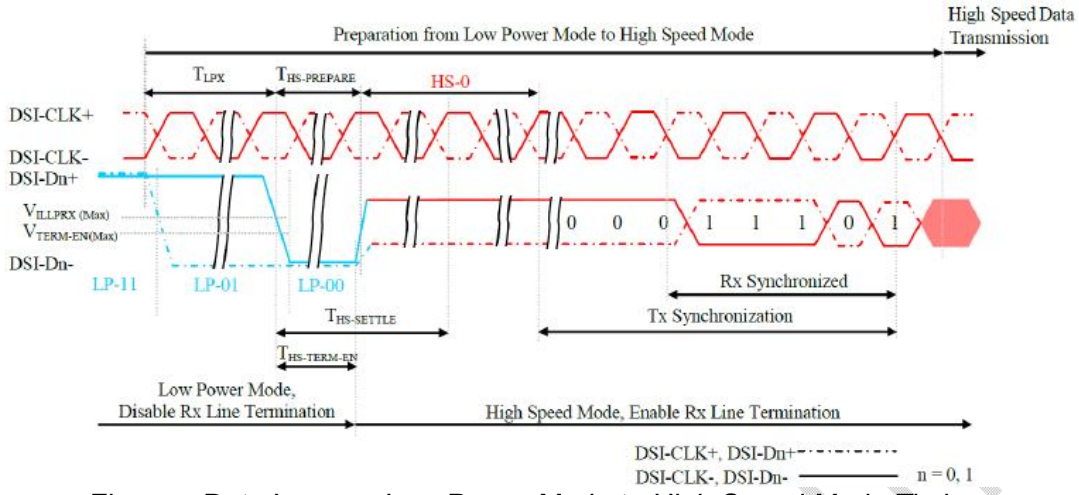


Figure Data Lanes – Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-Dn+/-, n=0 and 1	T_{LPX}	Length of any Low Power State Period	50	-	ns
DSI-Dn+/-, n=0 and 1	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4xUI	85+6xUI	ns
DSI-Dn+/-, n=0 and 1	$T_{HS-TERM-EN}$	Time to enable Data Lane Receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

Table Data Lanes – Low Power Mode to High Speed Mode Timings

5.6 Data Lanes from High Speed Mode to Low power Mode

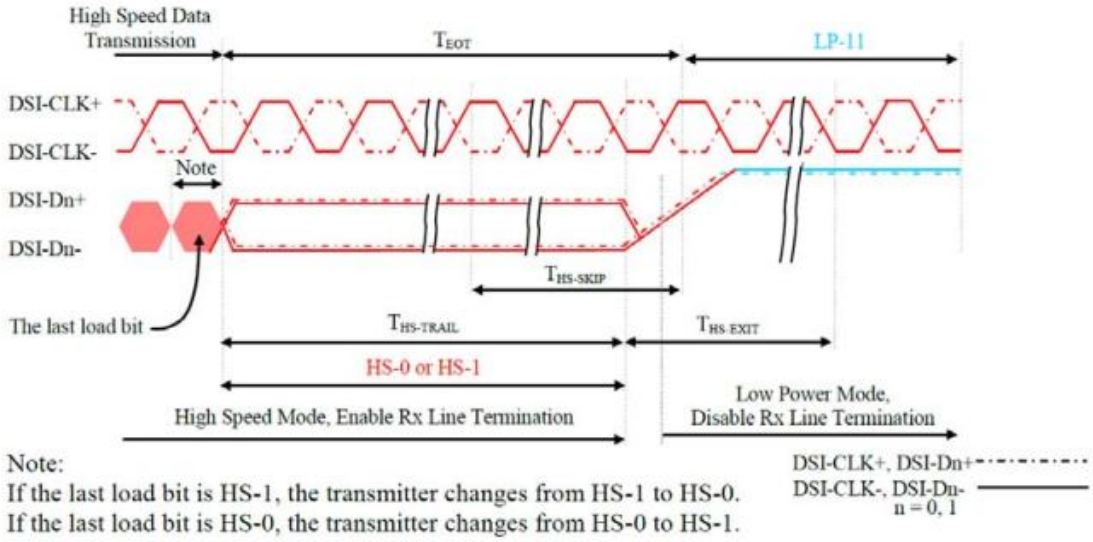


Figure Data Lanes – High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-Dn+/-, n=0 and 1	$T_{HS-SKIP}$	Time-Out at Display Module (ILI9806E) to ignore transition period of EoT	40	55+4xUI	ns
DSI-Dn+/-, n=0 and 1	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	ns

Table Data Lanes – High Speed Mode to Low Power Mode Timings

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5.7 DSI Clock Burst – High speed mode to/from Low power mode

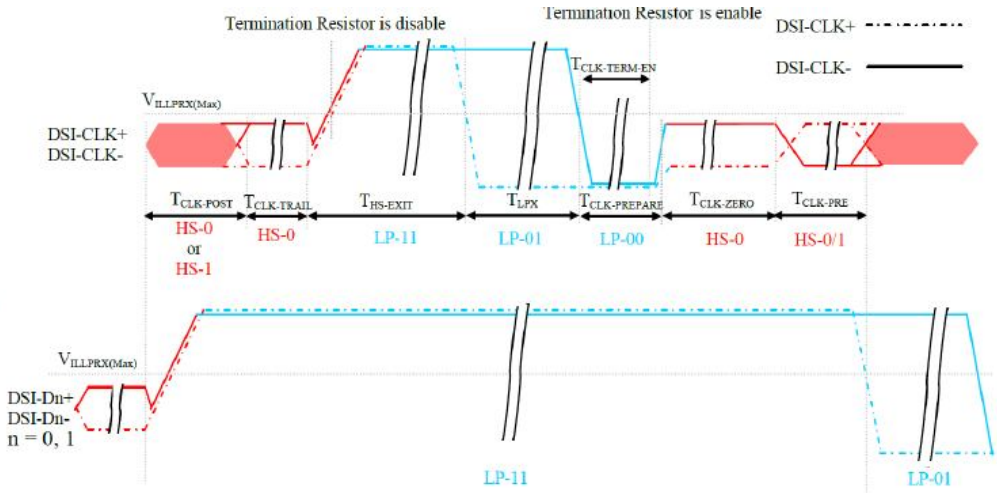


Figure Clock Lanes – High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-CLK+/-	$T_{CLK-POST}$	Time that the MPU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52xUI	-	ns
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	ns
DSI-CLK+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	95	ns
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination	-	38	ns
DSI-CLK+/-	$T_{CLK-PREPARE}$	Minimum lead HS-0 drive period before starting Clock	300	-	ns
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8xUI	-	ns

Table Clock Lanes – High Speed Mode to/from Low Power Mode Timings

5.8 Data Input Timing Parameter Setting

Parameter	Symbol	MIN	TYP	MAX	Units
CLK frequency	DCLK	32	33	34	MHz
Horizontal Back Porch	HBP	70	80	100	DOTCLK
Horizontal Front Porch	HFP	70	80	100	DOTCLK
Horizontal display area	HD		480		DOTCLK
Horizontal period	H	628	648	688	DOTCLK
Horizontal pulse width	HPW	8	8	8	DOTCLK
Vertical Back Porch	VBP	11	16	17	Line
Vertical Front Porch	VFP	11	16	17	Line
Vertical display area	VD		800		Line
Vertical period	V	824	834	836	Line
Vertical pulse width	VPW	2	2	2	Line
Frame rate	FR	-	60	-	Hz

Note:HPW+HBP+HFP≥4.5us

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5.8 Power on/Off Sequence

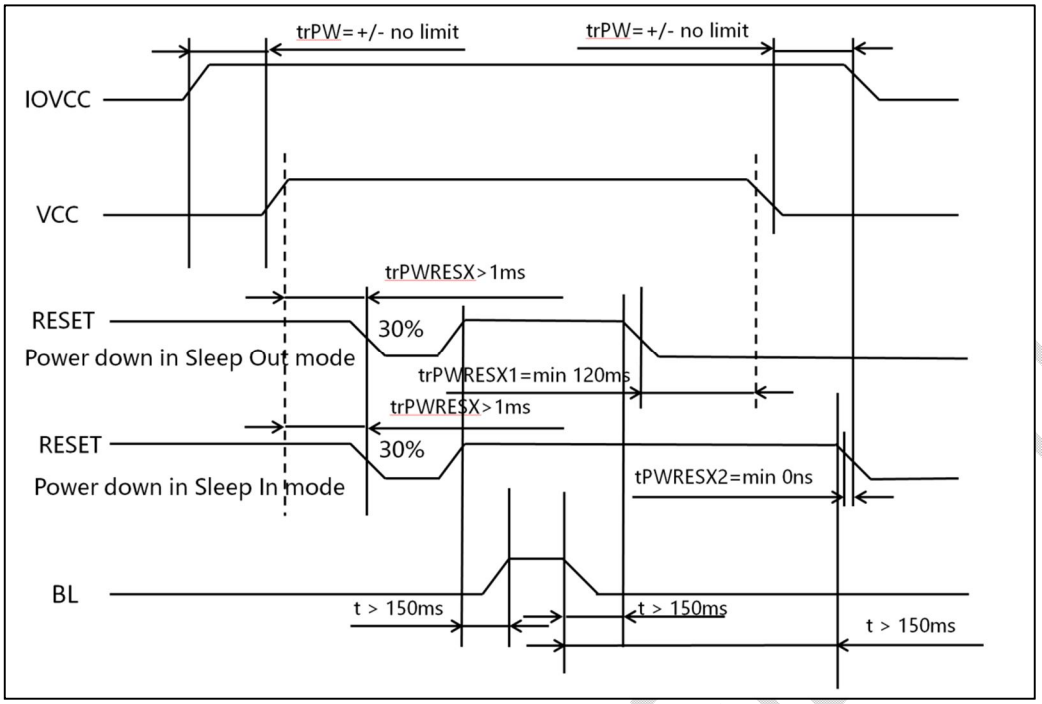


Figure Case 1-RESX line is held High or Unstable by Host at Power on

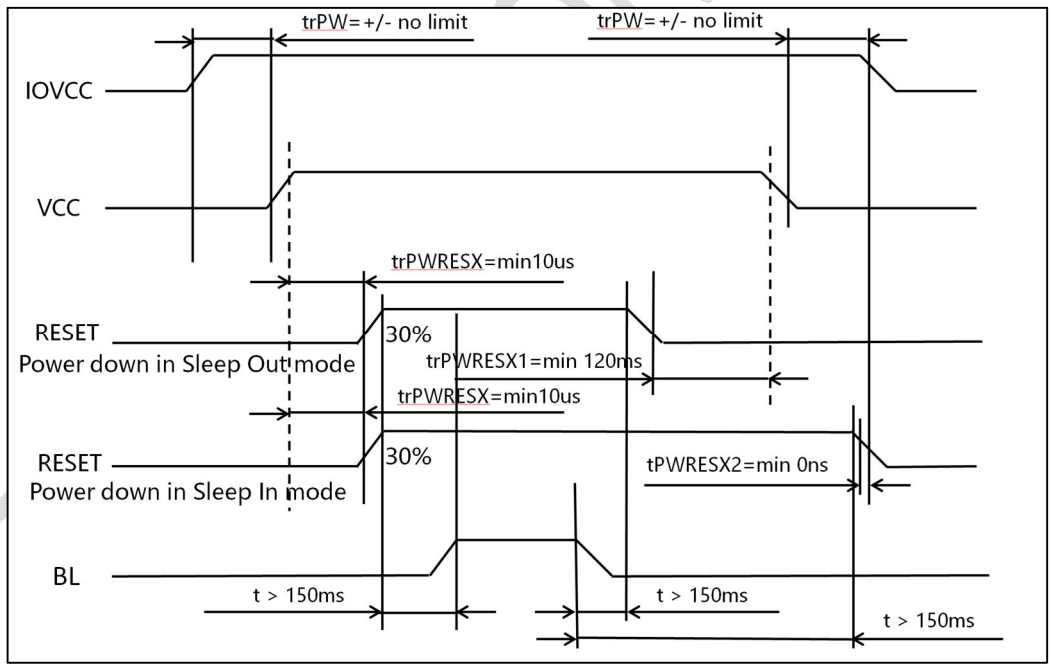


Figure Case 2-RESX line is held Low by Host at Power on

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5.9 RESET timing

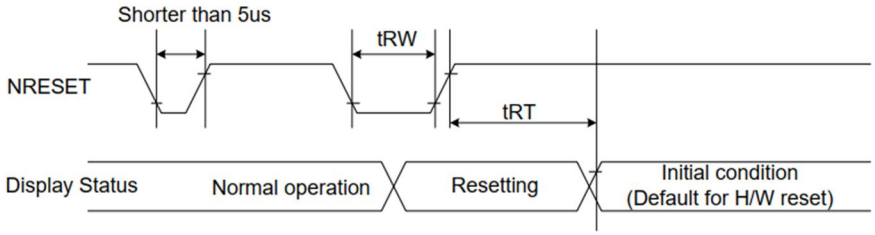


Figure 100 Reset Timing

Table 41 Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		us
	tRT	Reset cancel		5(note 1,5)	ms
				120 (note 1,6,7)	ms

Note:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from OTP to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 42.

Table 42 Reset Descript

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out mode. The display remains the blank state in Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:

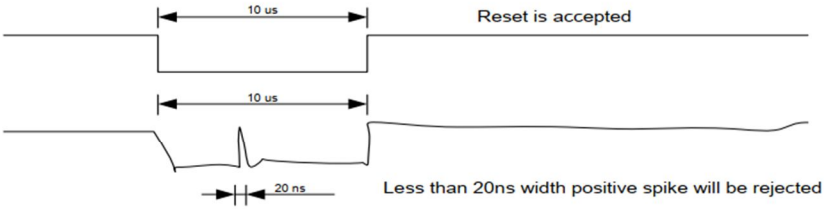


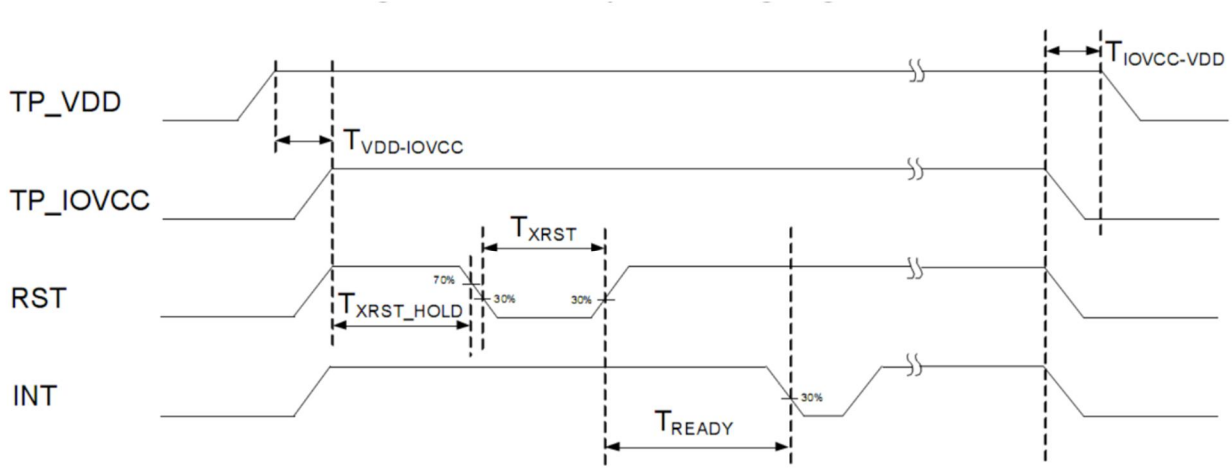
Figure 101 Positive Noise Pulse during Reset Low

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

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6 CTP Timing

6.1 Power On/Off Sequence

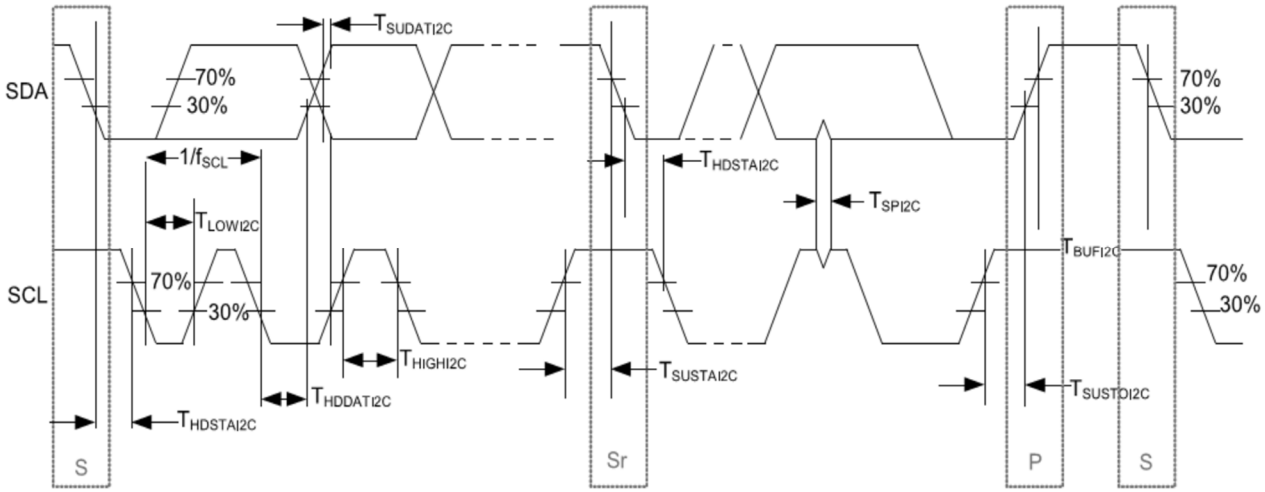


Symbol	Description	Conditions	Min	Typ	Max	Units
PSA_{RAMP}	TP_VDD Ramp Up	–	–	–	100	mV/μs
PSD_{RAMP}	TP_IOVCC Ramp Rate from Ground to Minimum Voltage	–	1	–	40	V/ms
$T_{VDD-IOVCC}$	Time of TP_VDD Ready Time before TP_IOVCC Ready Time	–	0	–	–	ms
T_{XRST_HOLD}	Hold Time before External Reset (RST) Asserted	–	2	–	–	ms
T_{XRST}	External Reset (RST) Pulse width	After TP_IOVCC is valid.	10	–	–	μs
$T_{IOVCC-VDD}$	Time of TP_IOVCC Discharge before TP_VDD Discharge Time	–	0	–	–	ms
T_{READY}	Time from RST Deassertion to INT		–	–	10	ms
T_{CAL}	Calibration Routine Execution Time		–	–	1100	ms

Note:RST=TP_RES,INT=TP_INT

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6.2 CTP I2C Interface Timing



I2C Bus Timing for Fast/Standard Mode

Note: S:I2C Start Condition,SDA=TP_SDA,SCL=TP_SCL, P:I2C Stop Condition;

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
f_{SCLI2C}	SCL Clock Frequency	0	100	0	400	kHz
$T_{HDSTAI2C}$	Hold Time (Repeated) Start Condition First Clock Pulse Is Generated after this Period	4	–	0.6	–	μs
T_{LOWI2C}	LOW Period of SCL Clock	4.7	–	1.3	–	μs
$T_{HIGHI2C}$	HIGH Period of SCL Clock	4	–	0.6	–	μs
$T_{SUSTAI2C}$	Setup Time for Repeated Start Condition	4.7	–	0.6	–	μs
$T_{HDDATI2C}$	Data Hold Time	0	–	0	–	μs
$T_{SUDATI2C}$	Data Setup Time	250	–	100	–	ns
$T_{VDDATI2C}$	Data Valid Time	–	3.45	–	0.9	μs
$T_{VDACKI2C}$	Data Acknowledge Time	–	3.45	–	0.9	μs
$T_{SUSTOI2C}$	Input Hysteresis High Voltage, 1.71V≤TP_IOVCC≤1.95V or 2.0V ≤ TP_IOVCC ≤ 5.5V	4	–	0.6	–	μs
V_{HH}	Bus Free Time between a Stop and Start Condition	0.1*TP_IOVCC	–	0.1*TP_IOVCC	–	V
T_{BUFI2C}	Pulse Width of Spikes that are Suppressed by Input Filter	4.7	–	1.3	–	μs
T_{SPI2C}	Capacitance Load for SDA or SCL	–	–	50	–	ns
C_{BUS}	Input Low Voltage	–	400	–	400	pF
V_{IL_I2C}	Input High Voltage	–0.5	0.3*TP_IOVCC	–0.5	0.3*TP_IOVCC	V
V_{IH_I2C}	Output Low Voltage (TP_IOVCC≤ 2-V, 3-mA sink)	0.7*TP_IOVCC	–	0.7*TP_IOVCC	–	V
$V_{OL_I2C_L}$	Output Low Voltage (TP_IOVCC > 2-V, 3-mA sink)	–	0.2*TP_IOVCC	–	0.2*TP_IOVCC	V
$V_{OL_I2C_H}$	Output Low Current V_{OL} = 0.4V	–	0.4	–	0.4	V
I_{OL_I2C}	Output Low Current V_{OL} = 0.6V	–	3	–	3	mA
	Input Hysteresis	–	–	–	6	mA
V_{H_I2C}	Input hysteresis	0.1*TP_IOVCC	–		–	mV

AC **Characteristics of the SDA and SCL**

Note:SDA=TP_SDA,SCL=TP_SCL

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7 Optical Characteristics

Item		Symbol	Condition	Min	Typ	Max	Unit	Remark
View Angles		θT	CR≧10	75	80		Degree	Note2,3
		θB		75	80			
		θL		75	80			
		θR		75	80			
Contrast Ratio		CR	θ=0°	500	700			Note 3
Response Time		T_r	25℃		25	35	ms	Note 4
		T_f						
Chromaticity	**White**	x	Backlight is on	0.263	0.313	0.363		Note 1,5
		y		0.275	0.325	0.375		
	Red	x		0.538	0.588	0.638		Note 1,5
		y		0.276	0.326	0.376		
	Green	x		0.311	0.361	0.411		Note 1,5
		y		0.541	0.591	0.641		
	Blue	x		0.107	0.157	0.207		Note 1,5
		y		0.051	0.101	0.151		
Uniformity		U		75%	80%		%	Note 6
NTSC					50		%	Note 5
Luminance (with cover lens)		L		300	350		cd/m^2	Note 7

Test Conditions:

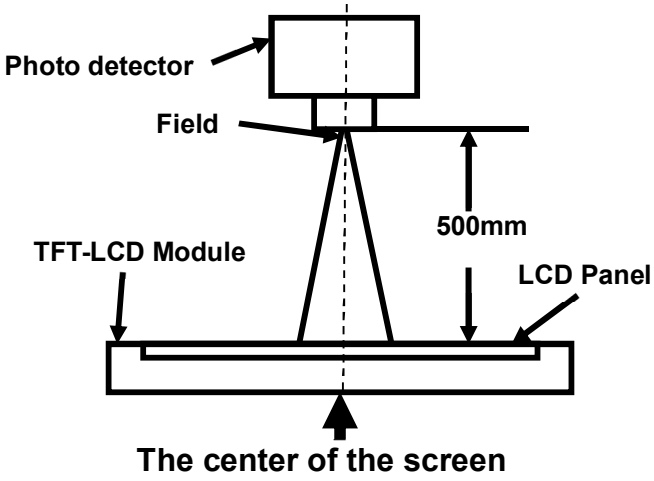
1. I_F= **20** mA, and the ambient temperature is 25℃.
2. The test systems refer to Note 1 and Note 2.

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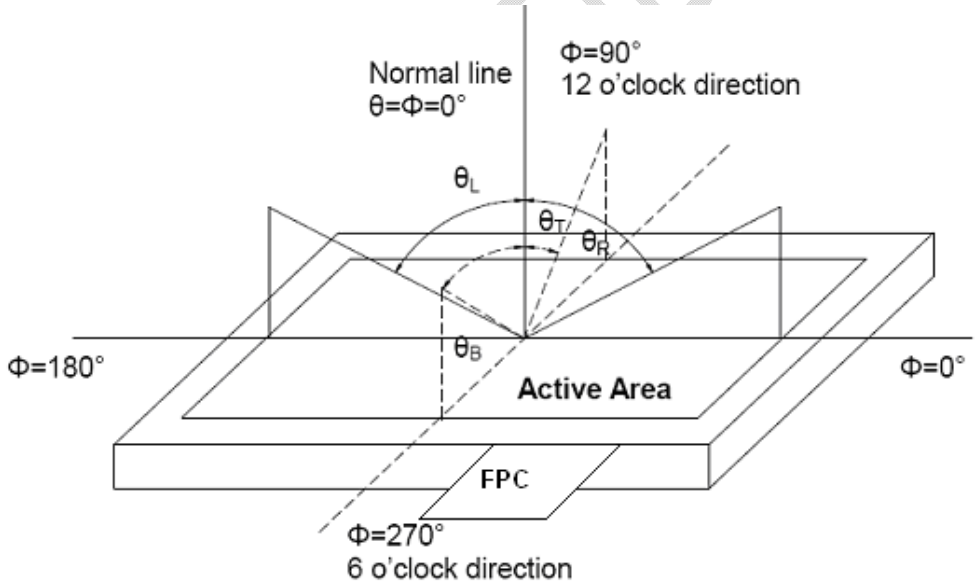
Note 1: Definition of optical measurement system.

The optical characteristics should be measured in dark room. After 5 Minutes operation, the optical properties are measured at the center point of the LCD screen. All input terminals LCD panel must be ground when measuring the center area of the panel.



Note 2: Definition of viewing angle range and measurement system.

viewing angle is measured at the center point of the LCD.



Note 3: Definition of contrast ratio

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance measured when LCD is on the "White" state}}{\text{Luminance measured when LCD is on the "Black" state}}$$

"White state ": The state is that the LCD should drive by Vwhite.

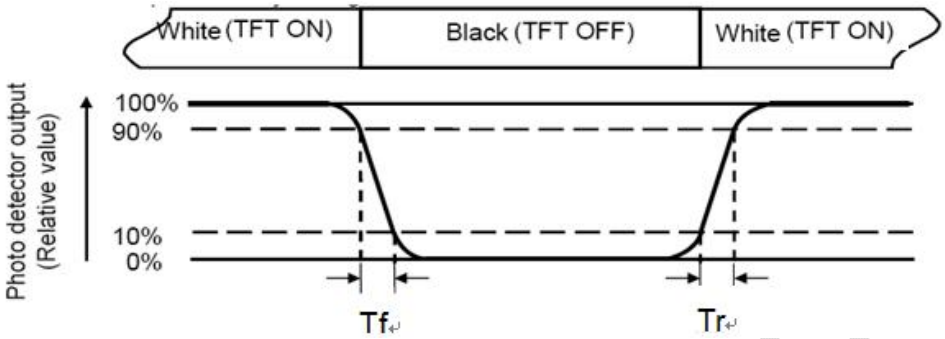
"Black state": The state is that the LCD should drive by Vblack.

Vwhite: To be determined Vblack: To be determined.

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Note 4: Definition of Response time

The response time is defined as the LCD optical switching time interval between “White” state and “Black” state. Rise time (Tr) is the time between photo detector output intensity changed from 10% to 90%. And fall time (Tf) is the time between photo detector output intensity changed from 90% to 10%.



Note 5: Definition of color chromaticity (CIE1931)

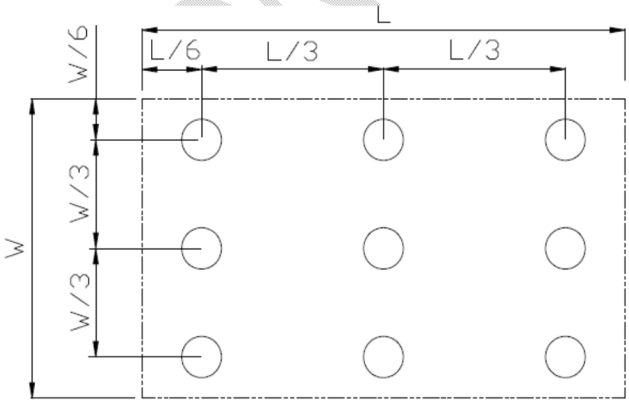
Color coordinates measured at center point of LCD.

Note 6: Definition of Luminance Uniformity

Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area.

Luminance Uniformity (U) = Lmin/ Lmax

L-------Active area length W----- Active area width



Lmax: The measured Maximum luminance of all measurement position.

Lmin: The measured Minimum luminance of all measurement position.

Note 7: Definition of Luminance:

Measure the luminance of white state at center point.

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8 Environmental / Reliability Test

No	Test Item	Condition	Remarks
1	High Temperature Operation	Ta=+70℃, 240hours	IEC60068-2-1:2007 GB2423.2-2008
2	Low Temperature Operation	Ta=-20℃, 240hours	IEC60068-2-1:2007 GB2423.1-2008
3	High Temperature Storage	Ta=+80℃, 240hours	IEC60068-2-1:2007 GB2423.2-2008
4	Low Temperature Storage	Ta=-30℃, 240hours	IEC60068-2-1:2007 GB2423.1-2008
5	Storage at High Temperature and Humidity	Ta=+60℃, RH=90%, 240hours	IEC60068-2-78 :2001 GB/T2423.3—2006
6	Thermal Shock (non-operation)	-30℃(30min)---80℃(30min)change Time:5min,20cycle	Start with cold temperature, End with high temperature, IEC60068-2-14:1984,GB2423.22-2002
7	ESD	C=150pF, R=330Ω Air:±8KV Contact:±4KV 5point/panel，5times (Environment:15℃~35℃, 30%~60%.86Kpa~106Kpa)	IEC61000-4-2:2001 GB/T17626.2-2006
8	Vibration Test	Frequency Range:10~55Hz Stroke:1.5mm Sweep:10Hz~55Hz~10Hz 2 hours for each direction of X.Y.Z. (6 hours for total)	IEC60068-2-6:1982 GB/T2423.10—1995
9	Mechanical Shock (Non OP)	Half Sine Wave 60G,6ms,±X,±Y,±Z 3times for each direction	IEC60068-2-27:1987 GB/T2423.5—1995
10	Package Drop Test	Height: 60cm, 1corner, 3edges,6surfaces	IEC60068-2-32:1990 GB/T2423.8—1995
11	The operating ambient pressure	T=62Kpa, Ta=25℃,1hour	IEC 60068-2-13:1983
12	The non-operating ambient pressure	T=40Kpa, Ta=25℃,1hour	IEC 60068-2-13:1983
13	Image stick	8hours 6X8 checkerboard Ta=25℃ RH=60%, check in gray186 after 30minutes	
14	MTBF	100K Hours(typical) of 25℃ and 60% (RH)	

Note1: Ts is the temperature of panel's surface.

Note2: Ta is the ambient temperature of sample.

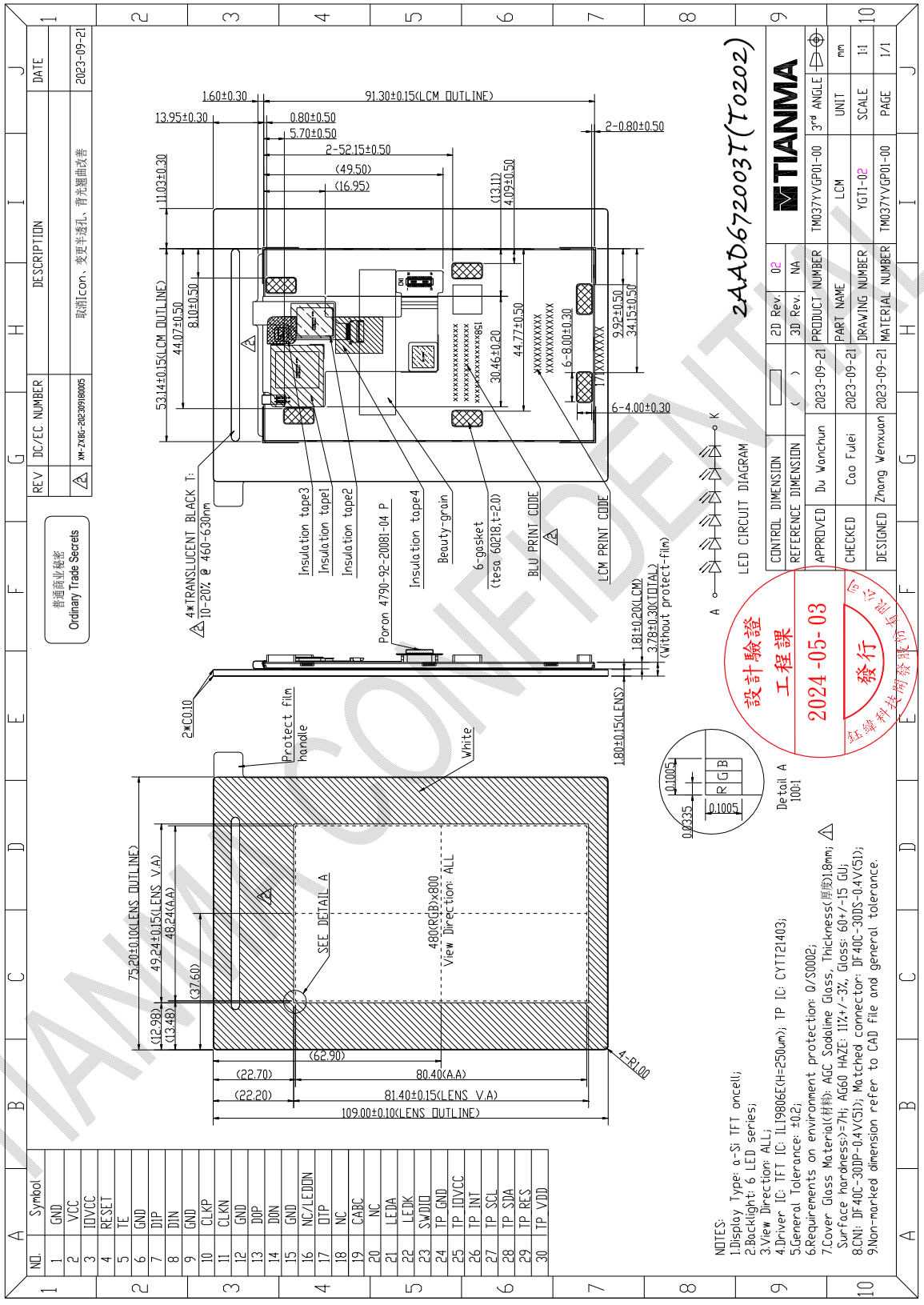
Note3: Before cosmetic and function test, the product must have enough recovery time, at least 2 hours at room temperature.

Note 4: In the standard condition, there shall be no practical problem that may affect the display function. After the reliability test, the product only guarantees operation, but don't guarantee all of the cosmetic specification.

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9 Mechanical Drawing



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Label description:

QR Code

Label Size: 8mm*8mm

Content:
Part of model name + Date code +shift+ production line No. +Serial No.

Example



TM037231201A010001

TM037---Part of model name
231201---Date code(YYMMDD)
A---shift(A/B)
01---production line No
0001---Serial No.(0000~9999)

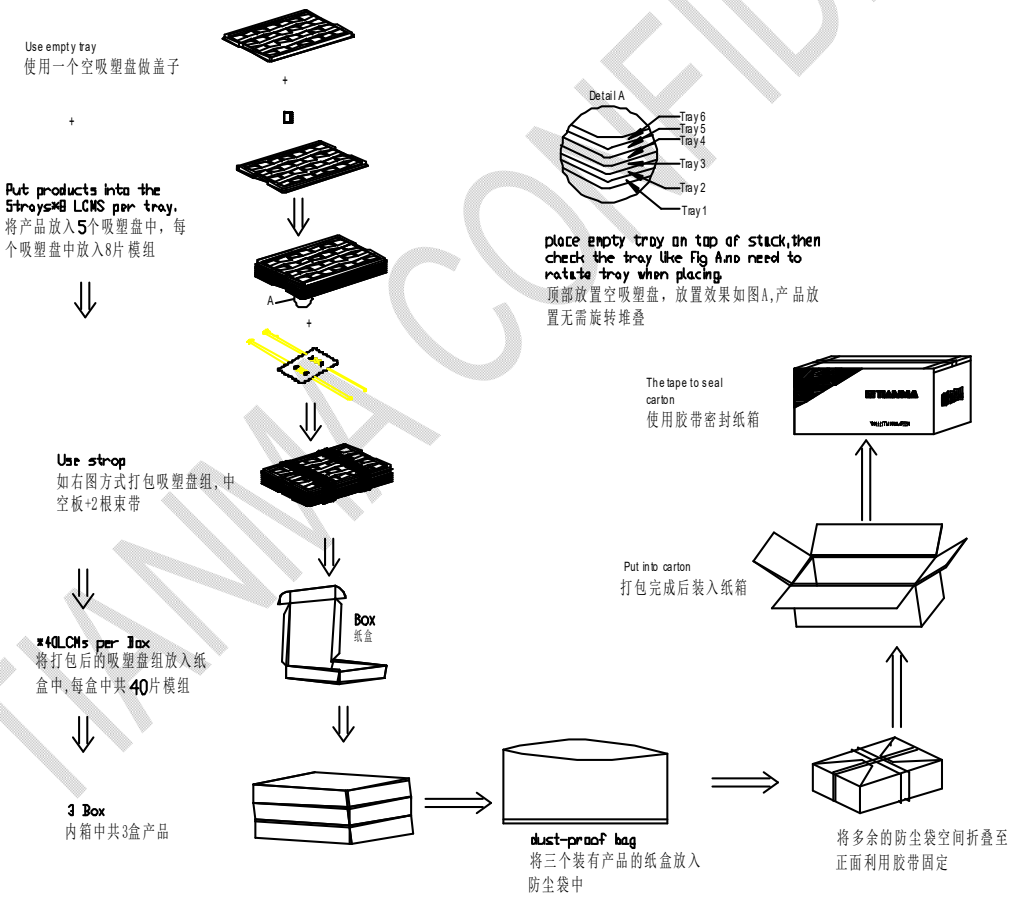
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10 Packing Drawing

Per BOX

No	Item	Model (Material)	Dimensions(mm)	Unit Weight(Kg)	Quantity	Remark
1	CTP+LCM	TM037YVGP01-00	75.2x109x3.78	0.055	120	
2	Tray	PET	485×330×14.2	0.122	18	
3	Dust-Proof Bag	LD-PE	700×545	0.046	1	
4	Plastic Board	PE	485×330×5	0.05	3	
5	Box	CORRUGATED PAPER	520×345×74	0.44	3	
6	Carton	CORRUGATED PAPER	544x365x250	1.01	1	
7	Total weight	11.322 ±5% kg				



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11 Precautions for Use of LCD Modules

11.3 Handling Precautions

11.3.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

11.3.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

11.3.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

11.3.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

11.3.5 If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

- Isopropyl alcohol
- Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

- Water
- Ketone
- Aromatic solvents

11.3.6 Do not attempt to disassemble the LCD Module.

11.3.7 If the logic circuit power is off, do not apply the input signals.

11.3.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

10.1.8.1 Be sure to ground the body when handling the LCD Modules.

10.1.8.2 Tools required for assembly, such as soldering irons, must be properly ground.

10.1.8.3 To reduce the amount of static electricity generated, do not conduct assembly and other work under dry conditions.

10.1.8.4 The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

11.4 Storage precautions

11.4.1 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

11.4.2 The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:

Temperature : 0℃ ～ 40℃ Relatively humidity: ≤80%

11.4.3 The LCD modules should be stored in the room without acid, alkali and harmful gas.

11.5 Transportation Precautions

11.5.1 The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.

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