Application Note: SY8253

High Efficiency, 500kHz, 3A, 23V Input Synchronous Step Down Regulator

General Description

The SY8253 is a high efficiency 500 kHz synchronous step-down DC/DC converter capable of delivering 3A current. The SY8253 operates over a wide input voltage range from 4.5V to 23V and integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

Low output voltage ripple and small external inductor and capacitor sizes are achieved with 500 kHz switching frequency. It adopts the instant PWM architecture to achieve fast transient responses for high step down applications

Features

- low $R_{DS(ON)}$ for internal switches (top/bottom): 105mΩ/50mΩ
- 4.5-23V input voltage range
- 3A output current capability
- 500 kHz switching frequency
- Instant PWM architecture to achieve fast transient responses.
- Cycle-by-cycle peak current limitation
- Internal softstart limits the inrush current
- Hic-cup mode output short circuit protection
- ±1.5% 0.6V reference
- Power good indicator (SY8253AIC only)
- TSOT23-8/ TSOT23-6 package

Ordering Information

SY8253 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SY8253AIC	TSOT23-8	--
SY8253ADC	TSOT23-6	--

Applications

- Set Top Box
- Portable TV
- Access Point Router
- DSL Modem
- LCD TV

Typical Applications

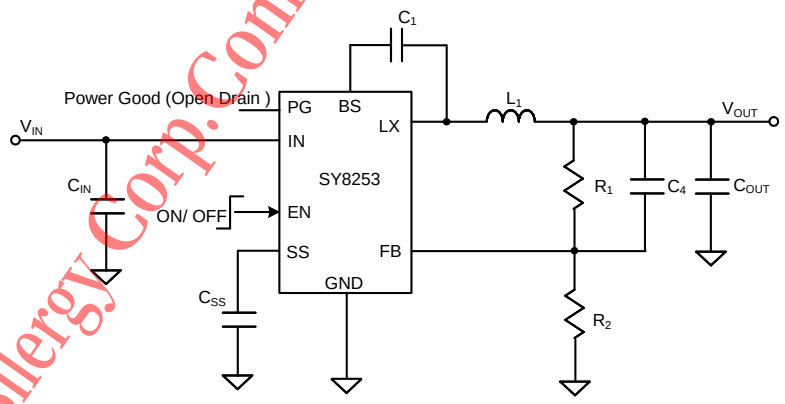

Figure 1. Schematic Diagram (SY8253AIC)

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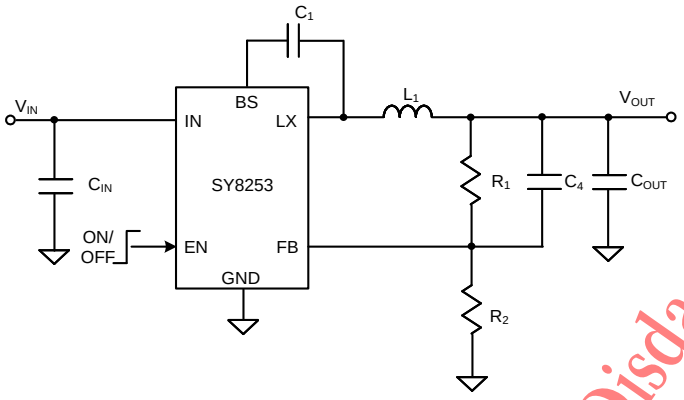

Figure 2. Schematic Diagram (SY8253ADC)

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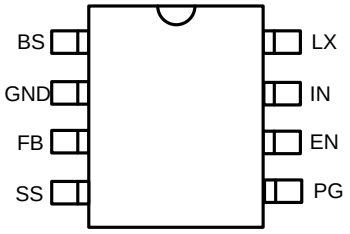
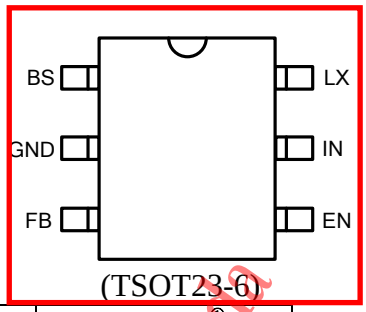
Pinout (top view)



(TSOT23-8)



(TSOT23-6)

Part Number	Package type	Top Mark①
SY8253AIC	TSOT23-8	**XUxyz**
SY8253ADC	TSOT23-6	**XTxyz**

Note①： ***x=year code, y=week code, z= lot number code.***

Pin Name	TSOT23-8	TSOT23-6	Pin Description
BS	1	1	Boot-Strap Pin. Supply high side gate driver. Decouple this pin to LX pin with 0.1uF ceramic cap.
GND	2	2	Ground pin
FB	3	3	Output Feedback Pin. Connect this pin to the center point of the output resistor divider (as shown in Figure 1) to program the output voltage: Vout=0.6*(1+R1/R2)
SS	4	/	Softstart programming pin. Connect a capacitor from this pin to ground to program the softstart time. Tss=Css*0.6V/4uA. Leave this pin open for default 1ms soft-start.
PG	5	/	Power good indicator. Open drain output.
EN	6	4	Enable control. Pull high to turn on. Do not float.
IN	7	5	Input pin. Decouple this pin to GND pin with at least 1uF ceramic cap
LX	8	6	Inductor pin. Connect this pin to the switching node of inductor

Absolute Maximum Ratings (Note 1)

Supply Input Voltage ---------- 25V
BS-LX, SS ---------- 4V
All other pins ---------- VIN + 0.3V
Power Dissipation, PD @ TA = 25℃, TSOT23-8 /TSOT23-6---------- 1.5W
Package Thermal Resistance (Note 2)
θJA ---------- 66℃/W
θJC ---------- 15℃/W
Junction Temperature Range ---------- 150℃
Lead Temperature (Soldering, 10 sec.) ---------- 260℃
Storage Temperature Range ---------- -65℃ to 150℃
Dynamic LX voltage in 10ns duration ---------- IN+3V to GND-5V

Recommended Operating Conditions (Note 3)

Supply Input Voltage ---------- 4.5V to 23V
Junction Temperature Range ---------- -40℃ to 125℃
Ambient Temperature Range ---------- -40℃ to 85℃

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Electrical Characteristics

(V_{IN} = 12V, V_{OUT} =3.3V, L = 4.7uH, C_{OUT} = 47uF, T_A = 25 ℃, I_{OUT} = 1A unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4.5		23	V
Quiescent Current	I_Q	I_{OUT}=0, V_{FB}=V_{REF}*105%		100		μA
Shutdown Current	I_{SHDN}	EN=0		5	10	μA
Feedback Reference Voltage	V_{REF}		0.591	0.6	0.609	V
FB Input Current	I_{FB}	V_{FB}=3.3V	-50		50	nA
Top FET RON	$R_{DS(ON)1}$			105		mΩ
Top FET Peak Current Limit	$I_{LIM,TOP}$		5.1	6	6.9	A
Bottom FET RON	$R_{DS(ON)2}$			50		mΩ
Bottom FET Valley Current Limit	$I_{LIM,BOT}$		3.0	3.7	4.5	A
EN Rising Threshold	V_{ENH}		1.5			V
EN Falling Threshold	V_{ENL}				0.4	V
Power Good Threshold	V_{PG}	V_{FB} falling, PG from high to low		90		%V_{REF}
		V_{FB} rising, PG from low to high		95		%V_{REF}
		V_{FB} rising, PG from high to low		115		%V_{REF}
		V_{FB} falling, PG from low to high		110		%V_{REF}
Power Good Delay Time	T_{PG_F}	PG falling edge		10		μs
	T_{PG_R}	PG rising edge		60		μs
Output OVP Response Time	T_{OVP}			10		μs
Output OVP Off Time	$t_{OFF,OVP}$			1000		μs
Soft-start Charging Current	I_{SS}			4		μA
Short Circuit Protection Wait Time	$t_{WAIT,SCP}$			1.9		ms
Short Circuit Protection Off Time	$t_{OFF,SCP}$			15		ms
Input UVLO Threshold	V_{UVLO}				4.5	V
Input UVLO Hysteresis	V_{HYS}			0.3		V
Min ON Time				80		ns
Min OFF Time				160		ns
Switching Frequency			425	500	575	kHz
Thermal Shutdown Temperature	T_{SD}			150		℃
Thermal Shutdown Hysteresis	T_{HYS}			15		℃

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Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θJA is measured in the natural convection at T_A = 25 ℃ on a two-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

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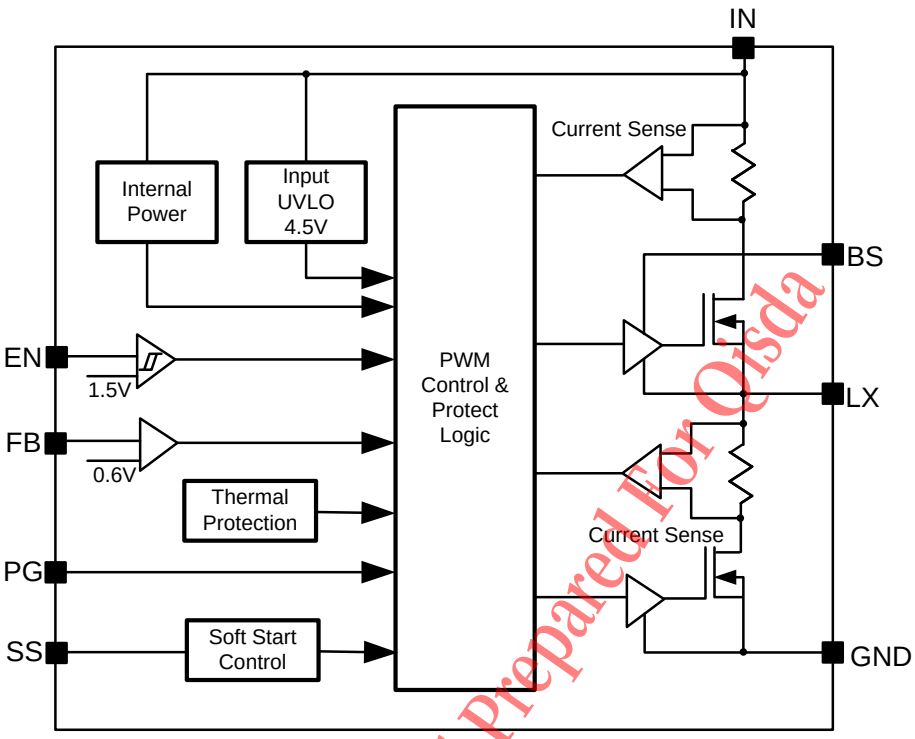
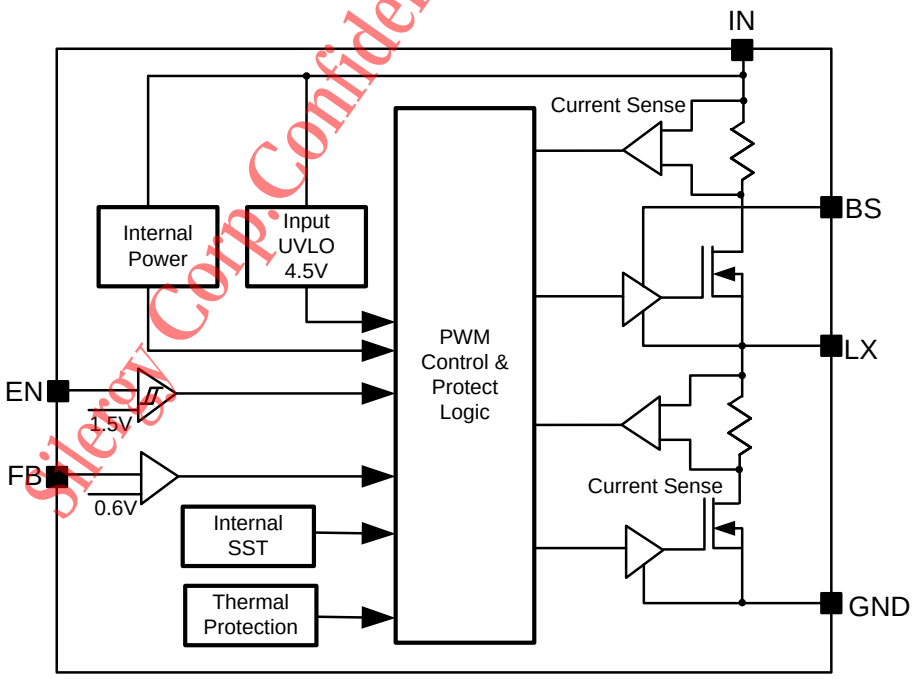
Block Diagram



(SY8253AIC)



(SY8253ADC)

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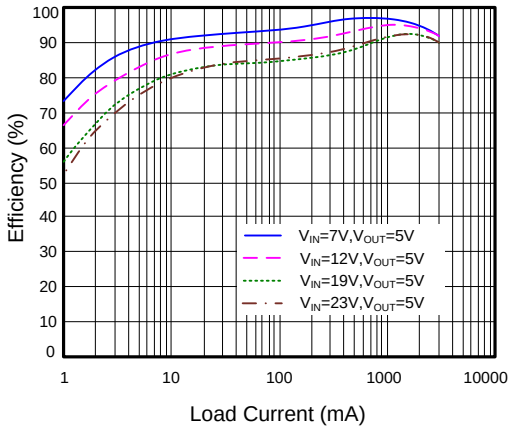
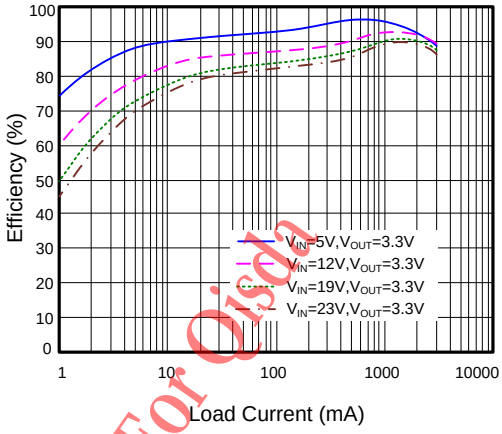
Typical Performance Characteristics

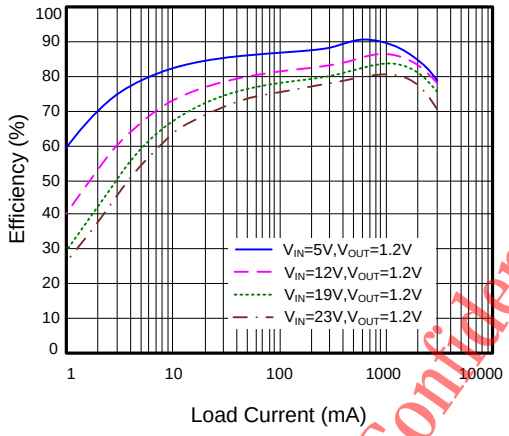
Efficiency vs. Load Current



Efficiency vs. Load Current

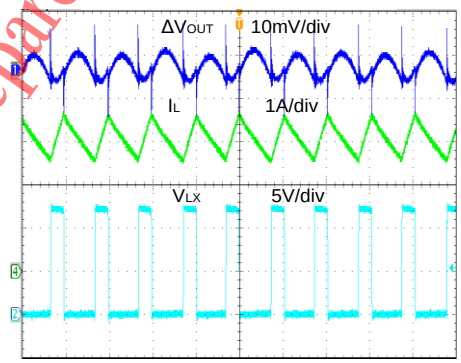


Efficiency vs. Load Current



Output Ripple

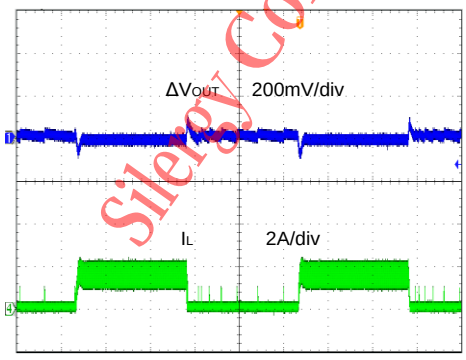
(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=3A)



Time (2μs/div)

Load Transient

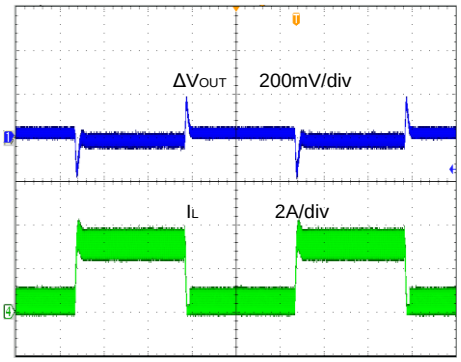
(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=0 -1.5A)



Time (200μs/div)

Load Transient

(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}= 0.3 - 3A)



Time (200μs/div)

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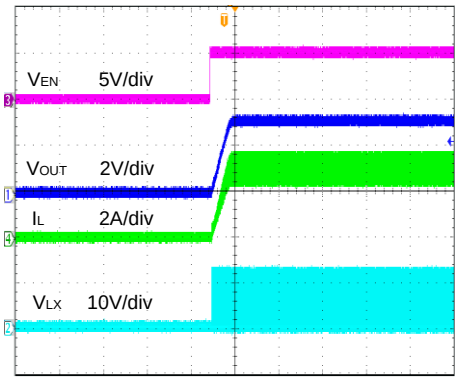
Startup from Enable

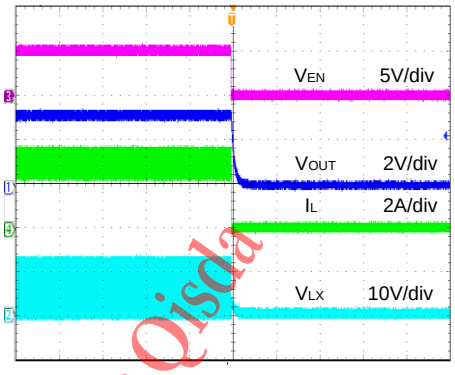
(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=3A)



Time (2ms/div)

Shutdown from Enable

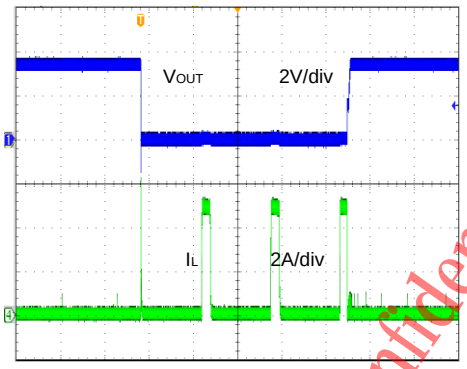
(V_{IN}=12V, V_{OUT}=3.3V, I_{OUT}=3A)



Time (400μs/div)

Short Circuit Protection

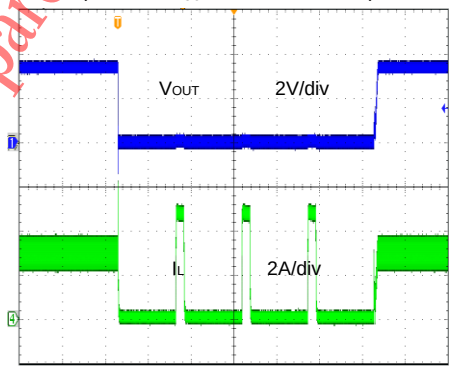
(V_{IN}=12V, V_{OUT}=3.3V, 0A to Short)



Time (10ms/div)

Short Circuit Protection

(V_{IN}=12V, V_{OUT}=3.3V, 3A to Short)



Time (10ms/div)

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Operation

The SY8253 is a high efficiency 500 kHz synchronous step-down DC-DC converter capable of delivering 3A current. The SY8253 operates over a wide input voltage range from 4.5V to 23V and integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss.

Low output voltage ripple and small external inductor and capacitor sizes are achieved with 500 kHz switching frequency. It adopts the instant PWM architecture to achieve fast transient responses for high step down applications

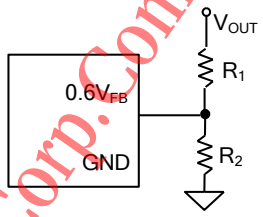
Applications Information

Because of the high integration in the SY8253 IC, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT}, output inductor L and feedback resistors (R_1 and R_2) need to be selected for the targeted applications specifications.

Feedback resistor dividers R_1 and R_2:

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_1 and R_2. A value of between 10kΩ and 1MΩ is highly recommended for both resistors. If V_{OUT} is 3.3V, R_1=100k is chosen, then using following equation, R_2 can be calculated to be 22.1k:

$$R_2 = \frac{0.6V}{V_{OUT} - 0.6V} R_1 .$$



Input capacitor C_{IN}:

The ripple current through input capacitor is calculated as:

$$I_{CIN_RMS} = I_{OUT} \cdot \sqrt{D(1-D)} \cdot$$

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and IN/GND pins. In this case, a 10uF low ESR ceramic capacitor is recommended.

Output capacitor C_{OUT}:

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use X5R or better grade ceramic capacitor greater than 22uF capacitance.

Output inductor L:

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum output current. The inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{F_{SW} \times I_{OUT,MAX} \times 40\%}$$

where Fsw is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The SY8253 regulator IC is quite tolerant of different ripple current amplitude. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

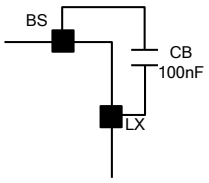
2) The saturation current rating of the inductor must be selected to be greater than the peak inductor current under full load conditions.

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1-V_{OUT}/V_{IN,MAX})}{2 \cdot F_{SW} \cdot L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<50mΩ to achieve a good overall efficiency.

External Bootstrap Cap

This capacitor provides the gate driver voltage for internal high side MOSEFET. A 100nF low ESR ceramic capacitor connected between BS pin and LX pin is recommended.



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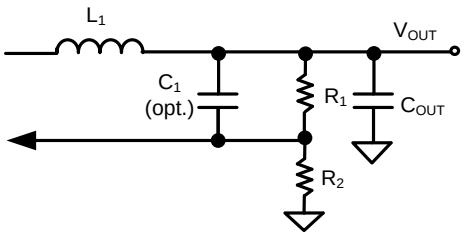
Load Transient Considerations:

The SY8253 regulator IC integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a ceramic capacitor in parallel with R1 may further speed up the load transient responses and it is recommended for applications with large load transient step requirements.



Soft-Start:

The SY8253 provides programmable soft-start time feature. The minimum soft-start time is 1ms typically when SS pin is floating. Connect a capacitor across SS pin and GND to program the soft-start time.

Tss(ms)=Css(nF)*0.6V/4uA

Layout Design:

The layout design of SY8253 regulator is relatively simple. For the best efficiency and minimum noise problem, we should place the following components close to the IC: C_{IN}, L, R1 and R2.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable.

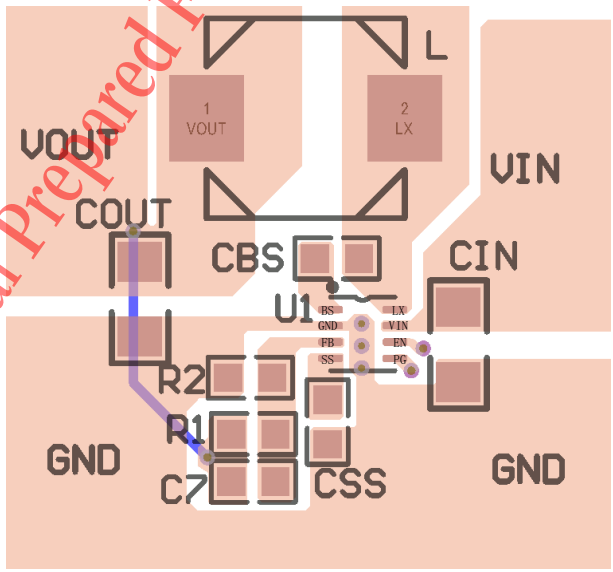
2) C_{IN} must be close to Pins IN and GND. The loop area formed by C_{IN} and GND must be minimized.

3) The PCB copper area associated with LX pin must be minimized to avoid the potential noise problem.

4) The components R_1 and R_2, and the trace connecting to the FB pin must NOT be adjacent to the LX net on the PCB layout to avoid the noise problem.

5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1Mohm resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

PCB Layout Suggestion:



(SY8253AIC)

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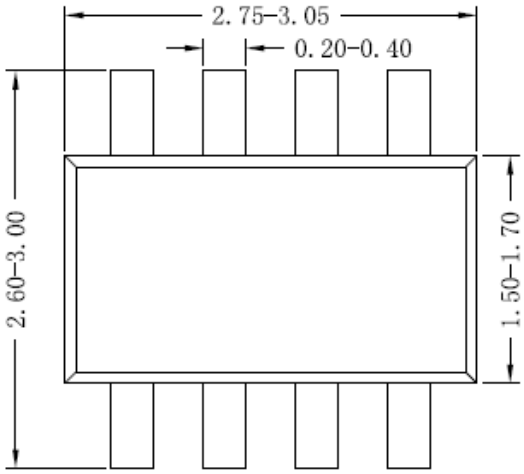
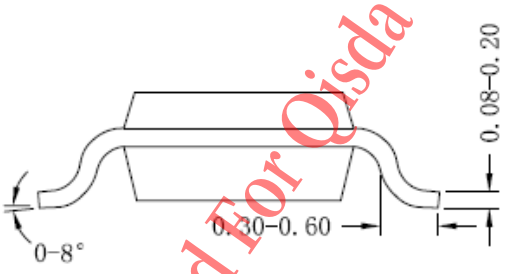
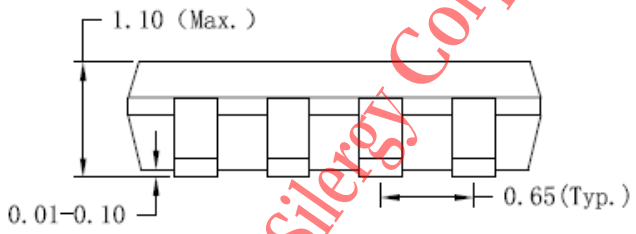
TSOT23-8 Package Outline Drawing



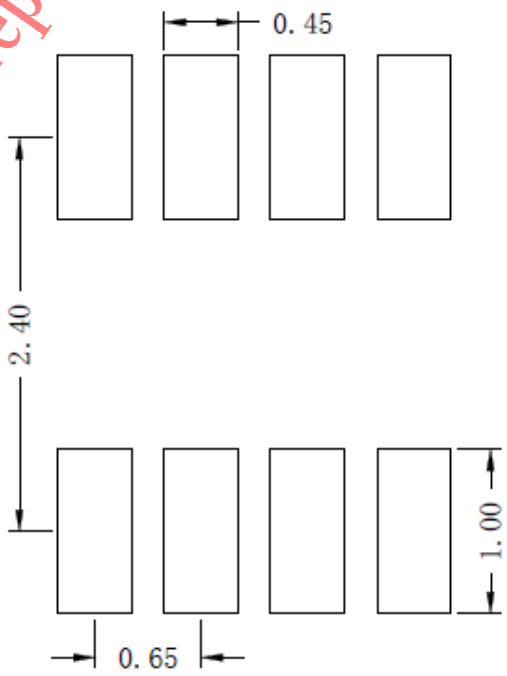
Top view



Side view A



Side view B



Recommended PCB layout

(Reference only)

Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

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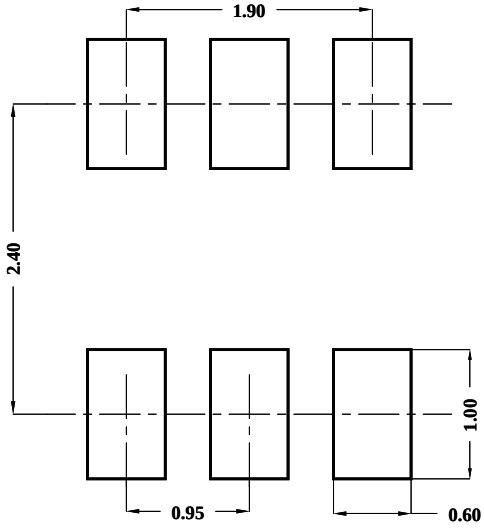
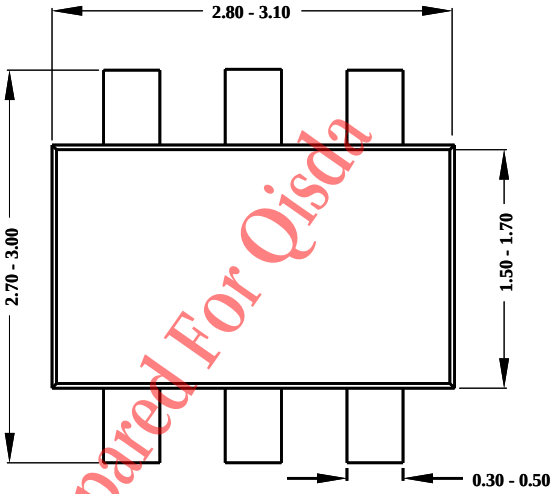
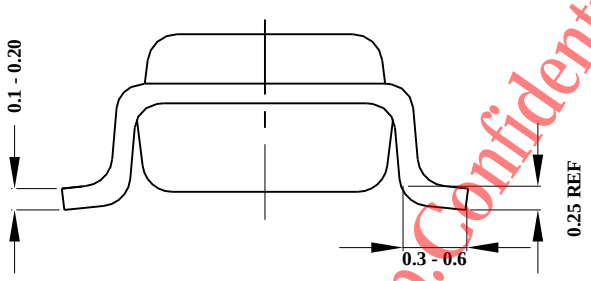
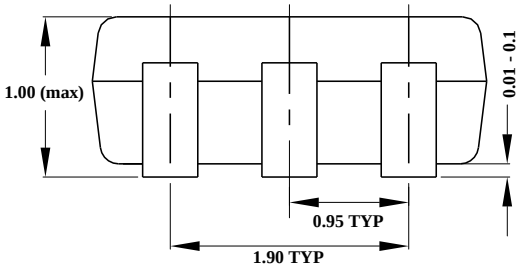
TSOT23-6L Package Outline Drawing





Recommended Pad Layout





Notes: **All dimension in MM**
All dimension don't include mold flash & metal burr

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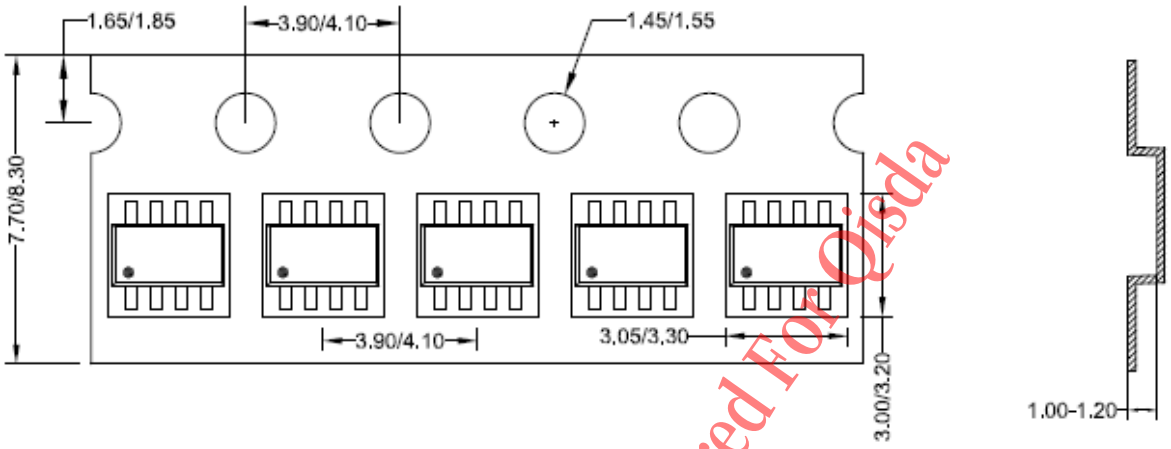
Taping & Reel Specification

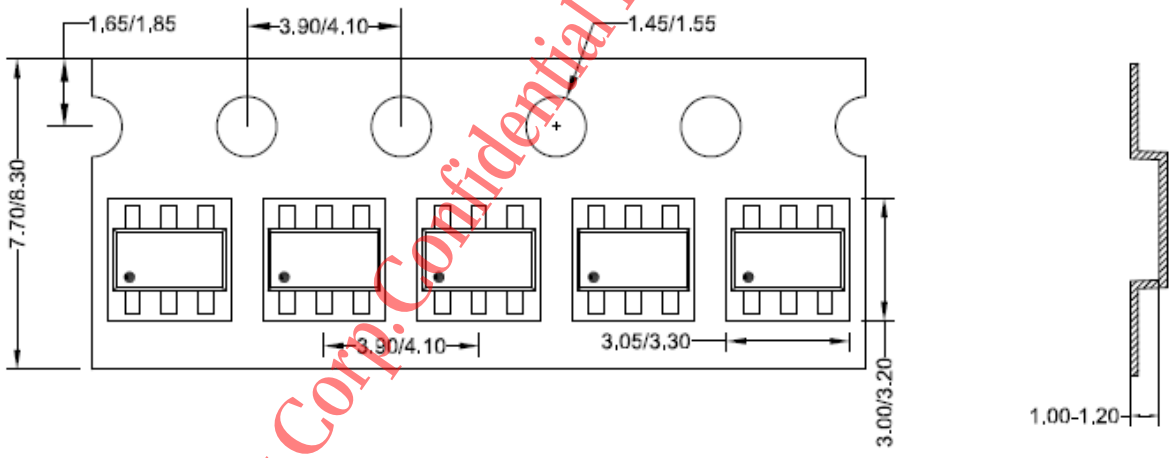
1. Taping orientation

TSOT23-8



Feeding direction →

TSOT23-6



Feeding direction →

2. Carrier Tape & Reel specification for packages

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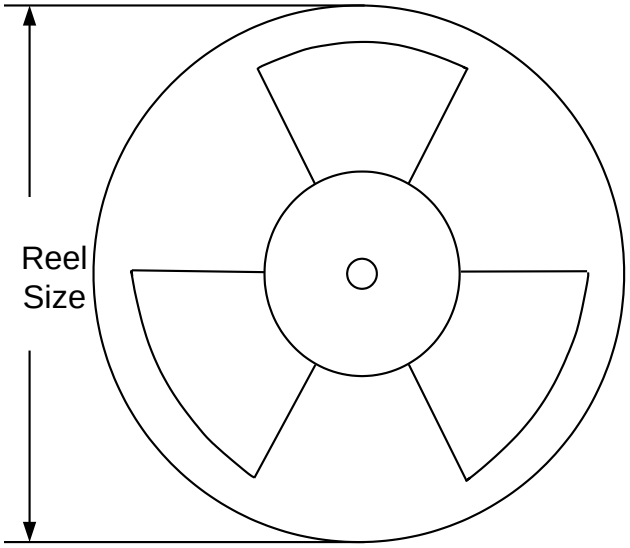

Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
TSOT23-8	8	4	7	400	160	3000
TSOT23-6	8	4	7	400	160	3000

3. Others: NA

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