RTD2738-VW-CG

MULTI-FUNCTION DISPLAY CONTROLLER

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
0.9	2022/02/25	First release.
1.0	2022/04/18	Add Pin information
1.1	2022/05/13	Add NC Pin
1.2	2022/07/29	Add USB D+/D-

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1. General Description

The Realtek RTD2738-VW-CG monitor controller combines the multiple DP1.4 digital input interfaces with HDCP1.4/HDCP2.3 and multiple HDMI2.0 digital input interfaces with HDCP1.4/HDCP2.3.

The RTD2738-VW-CG is suitable for multiple market segments and display applications, such as monitor, All in One PC, and embedded applications.

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2. Features

General

- RTD2738-VW-CG supports input format up to 3440 x 1440 @ 240Hz/1920 x 1080 @ 480Hz via single DP1.4 port with Display Stream Compression
- Support V-by-1 and eDP panel interfaces.
- Zoom scaling up and down
- Embedded 32bit CPU with SPI flash controller.
- It contains 4 ADCs in key pad application
- Require only one crystal to generate all timing.
- Programmable internal low-voltage-reset (LVR)
- High resolution 6 channels PWM output, and wide range selectable PWM frequency

Crystal

- Support 14.318MHz crystal type

DisplayPort Receiver

- RTD2738-VW-CG supports 3 ports of Ultra-High Speed Receiver can support DisplayPort1.4
- In DisplayPort mode, four link layer speed HBR3 (8.1GHz), HBR2 (5.4GHz), HBR (2.7GHz), RBR (1.62GHz) are supported
- 6-bit, 8-bit, 10-bit, and 12-bit color depth transport is supported
- High-Bandwidth Digital Content Protection (HDCP 1.4/HDCP2.3) is supported
- DisplayPort audio is allowed to transmit to I2S/SPDIF output
- VESA Adaptive Sync technology is supported
- Forward Error Correction (FEC) is supported.
- VESA Display Stream Compression (DSC) version 1.2a transport is supported and backward compatible with former version.

HDMI Receiver

- RTD2738-VW-CG supports 2 ports of Ultra-High Speed Receiver can support HDMI2.0
- In HDMI mode, the latest HDMI2.0 (6GHz) is supported
- In HDMI mode, data enable only mode is supported
- In HDMI mode, 6-bit, 8-bit, 10-bit, and 12-bit color depth transport is supported
- In HDMI mode, High-Bandwidth Digital Content Protection (HDCP 1.4/HDCP2.3) is supported
- In HDMI mode, HDMI audio is allowed to transmit to I2S/SPDIF output
- In HDMI mode, AMD HDMI Freesync technology is supported
- AMD HDMI Freesync technology is supported

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Embedded MCU

- 32bit CPU with external serial flash
- Low speed ADC for various application
- I2C Master or Slave hardware supported

Audio

- Output: IIS , SPDIF
- Embedded Audio DAC
- Embedded headphone amp

Scaling

- Fully programmable zoom ratios
- Independent horizontal/vertical scaling
- Advanced zoom algorithm provides high image quality
- Sharpness/Smooth filter enhancement
- Support non-linear scaling from 4:3 to 16:9 or 16:9 to 4:3

Color Processor

- True 12-bit color processing engine
- Programmable 14-bit gamma support
- Programmable 12-bit 3D gamma support
- xvYCC supported
- Adobe/sRGB compliance
- Advanced dithering logic for the fewer panel color depth enhancement
- Dynamic overshoot-smear canceling engine
- Brightness and contrast control
- Peaking/Coring function for video sharpness
- Support UltraVivid III function to enhance image quality with minimal artificial effect on productivity applications
- Panel Uniformity (Brightness and color uniformity)
- Support EOTF(electro-optical transfer function): 10 bits SMPTE 2084
- Support Adaptive Tone-Mapping
- Support segmented backlight control to enhance HDR performance.
- Support BT 2020

VividColorTM

- Independent color management (ICM)
- Dynamic contrast control (DCC)
- 2nd generation of Precise color mapping (PCM)
- Realtek OWL Sight technology
- Realtek Eagle Sight technology
- Image Adaptive Power Saving (IAPS)

Output Interface

- Support 8-bit / 10-bit output through either V-by-1 and eDP
- Supports 16-lane V-by-One, 16-lane eDP (HBR2) for 3440 x 1440 @ 240Hz/1920 x 1080 @ 480Hz

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- Flexible data pair swapping for easier system design.
- Fixed Last Line output for perfect panel capability

Embedded OSD

- Embedded 128K SRAM dynamically stores OSD command and fonts
- Support multi-color RAM font, 1, 2, 4 and 4-bit per pixel
- 64 color palette
- Maximum 26 window with alpha-blending /gradient / gradient target color / gradient reversed color/ dynamic fade-in/fade-out, bordering
- Rotate 90,180,270 degree
- OSD-made internal pattern generator for factory mode
- Support 12x18 proportional font
- Hardware decompression for OSD font
- Support factor scale up
- Support 2 independent font based OSD
- Embedded stream engine for graphics OSD

Frame Buffer Support

- LiveShow™ Function, High-performance RTC (response time compensation).
- Frame Rate Control Function
- Embedded frame buffer
- Support PIP/PBP

Power Supply

- 3.3V / 1.5V / 1.0V power supply

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3. System Applications

- Display System on Motherboard, Monitor
- Display System for All in One PCs and embedded applications

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4. Pin Assignments

HSBGA

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	
A	DGND	DGND	HDMI_CAB_DET3		DPRX_L3N_D2	DPRX_L3P_D2	DPRX_L2N_D2	DPRX_L2P_D2	DPRX_L1N_D2	DPRX_L1P_D2	DPRX_L0N_D2	DPRX_L0P_D2		RX2P_D3				RX3N_D3		RX2P_D4				RX3N_D4							DGND	DGND	A
B	HDMI_HPD_3	PMIC_SW1	PCB_POWE_DOWN	PMIC_DISCHARGE1		DGND		DGND		DGND		DGND	DGND	RX2N_D3	RX1N_D3		RX0P_D3	RX3P_D3		RX2N_D4	RX1N_D4		RX0P_D4	RX3P_D4		VTX_TX0P	VTX_TX1P	VTX_TX2P	VTX_TX3P		VTX_TX4N	VTX_TX4P	B
C	HDMI_HPD_4	EEWD	UART_TX_1	PMIC_INT1	EDID_WP									DGND	RX1P_D3		RX0N_D3	DGND	DGND	DGND	RX1P_D4		RX0N_D4	DGND	DGND	VTX_TX0N	VTX_TX1N	VTX_TX2N	VTX_TX3N		VTX_TX5N	VTX_TX5P	C
D	IICSCL0	UART_TX_2	UART_RX_2	UART_RX_1					DP_CAB_DET1	DP_HPD1					DGND	DGND	DGND				DGND	DGND	DGND			DGND		DGND		DGND	VTX_TX6N	VTX_TX6P	D
E	IICSDA0	EEIICSDA	EEIICSCL	HDMI_CAB_DET4			DP_SINK_ASS_P0_INT1M	DDCSDA_3	DPRX_AUX_P_1	DP_CAB_DET2	BACKLIGHT_ON							EDPTX_HPD_4	USB_SPI_SO_0_1	USB_SPI_CEB0_0_1	USB_SPI_SI_0_1	NC	NC			DGND	DGND	DGND			VTX_TX7N	VTX_TX7P	E
F	DDCSCL_ISP	UART_RX_0	UART_TX_0	IICSCL1			PMIC_ALERT1	VCCK_OFF_EN	DPRX_AUX_N_1	DPRX_AUX_N_2		DGND							V_BY_ONE_SDA_1	V_BY_ONE_SCL_1	USB_SPI_CEB1_0_1		NC					DGND		DGND	DPTX_LANE_N0_1	DPTX_LANE_P0_1	F
G	IICSDA1	PMIC_FRWENUFP1	PMIC_DISCHARGE0	DDCSDA_ISP			DP_SINK_ASS_N0_INT1M	DP_CAB_DET0	DDCSCL_3	DPRX_AUX_P_2	DP_SINK_ASS_N1_INT1M	DGND				DGND	DC2_DDR_1V5_2	DC2_DDR_1V5_2	DGND		USB_SPI_CLK_0_1							DGND			DPTX_LANE_N1_1	DPTX_LANE_P1_1	G
H	PMIC_ALERT0	DPRX_AUX_N_0	DPRX_AUX_P_0	PWM_IN			FLASH_WP		DP_HPD0		DP_SINK_ASS_P1_INT1M					DGND	DC2_DDR_1V5_2	DC2_DDR_1V5_2	NC	NC							DGND	DGND	DGND	DPTX_LANE_N2_1	DPTX_LANE_P2_1	H
J	CEC	DDCSDA_4	DDCSCL_4	DP_HPD2											DGND				NC	NC											DPTX_LANE_N3_1	DPTX_LANE_P3_1	J
K																	B30_SARADC_VSS	B30_SARADC_VSS	VCCK_ON			avdd33ref3_1_VSS	avdd33ref3_1_VSS					DGND	DPTX_LANE_N4_1	DPTX_LANE_P4_1		K
L	LANE 0P_APAD_D1	DGND	DGND					PVCC	PVCC		DPRX_AV1833	DPRX_AV1833		RX_VDD33_HDMI	RX_VDD33_HDMI			BMC_AVDD33		rfsv1_xRFTX_TX_AV33	rfsv1_xRFTX_TX_AV18								DPTX_LANE_N5_1	DPTX_LANE_P5_1	L
M	LANE 0N_APAD_D1							PVCC					DPRXA_V33	RX_VDD18_HDMI	RX_VDD18_HDMI		PVCC	VCCK_OFF	VCCK_OFF		rfsv1_xRFTX_TX_AV18							DGND	DPTX_LANE_N6_1	DPTX_LANE_P6_1		M
N	LANE 1P_APAD_D1 /	DGND	DGND					DPRX_AV1833	DGND		GDI_VDD18	DPRXA_V33	DGND	DGND	RX_VDD18_HDMI	RX_VDD18_HDMI	DGND	DGND		rfsv1_xRFTX_TX_AV33	rfsv1_xRFTX_TX_AV18								DPTX_LANE_N7_1	DPTX_LANE_P7_1		N
P	LANE 1N_APAD_D1							DPRX_AV1833	DGND		GDI_VDD18	VCCK_ON	DGND	DGND	DGND	DGND	DGND	DGND		rfsv1_xRFTX_TX_AV33	rfsv1_xRFTX_TX_AV18						DGND	DPTX_LANE_N0_2	DPTX_LANE_P0_2		P
R	LANE 2P_APAD_D1	DGND		DGND					DGND		GDI_VDD18	VCCK_ON	DGND	DGND	DGND	DGND	DGND	DGND	VCCK_OFF		rfsv1_xRFTX_TX_AV33		avdd33ref3_1_VSS	avdd33ref3_1_VSS					DPTX_LANE_N1_2	DPTX_LANE_P1_2		R
T	LANE 2N_APAD_D1				NC			DPRX_AV33	UX_AV33		GDI_VDD18	VCCK_ON	DGND	DGND	DGND	DGND	DGND	DGND	VCCK_OFF		rfsv1_xRFTX_TX_AV18						DGND	DGND	DPTX_LANE_N2_2	DPTX_LANE_P2_2		T
U	LANE 3P_APAD_D1	DGND		NC	NC			DPRX_AV33	UX_AV33			VCCK_ON	DGND	DGND	DGND	DGND	DGND	DGND											DPTX_LANE_N3_2	DPTX_LANE_P3_2		U
V	LANE 3N_APAD_D1		NC	NC		DPRX_AV1833		DPRX_AV33	DGND				DGND	DGND	DGND	DGND	DGND	DGND	VCCK_OFF		DDR_ZQ	D3_VREF_DQ			D3_VREF_CA	D3_ZQ		DGND	DGND	DPTX_LANE_N4_2	DPTX_LANE_P4_2		V
W	LANE 0P_APAD_D0 /	DGND	NC			DPRX_AV1833			DGND		GDI_VDD18	GDI_VDD18	DGND	DGND	DGND	DGND	DGND	DGND	VCCK_OFF			VCC_15_DDR_CK	DDRPLL_V33	DDRPLL_V33						DPTX_LANE_N5_2	DPTX_LANE_P5_2		W
Y	LANE 0N_APAD_D0			DP_SINK_ASS_N2	DP_SINK_ASS_P2	MCK		PMIC_SW0	DGND		PVCC	PVCC	DGND	DGND	DGND	U_AV33	U_AV33	PVCC	VCCK_OFF		VCC_15_DDR		DDRPLL_V10	DDRPLL_V10					DGND	DPTX_LANE_N6_2	DPTX_LANE_P6_2		Y
AA	LANE 1P_APAD_D0	DGND						IICSDA2					DP_AV33_COMU	DP_AV33_COMU	DGND	U_AV33	U_AV33	PVCC	VCCK_OFF		VCC_15_DDR	VCC_15_DDR		DDR_VREF_23	DDR_VREF_01					DPTX_LANE_N7_2	DPTX_LANE_P7_2		AA
AB	LANE 1N_APAD_D0				HUB_SPWDET	HUB_BPWDET		VCCK_ON	GDI_VDD18	GDI_VDD18	F_AV33	DP_AV33						VCCK_OFF			VCC_15_DDR	VCC_15_DDR		DC2_DDR_1V5_1	D2_VREF_CA		DGND	DGND		DGND	NC	NC	AB
AC	LANE 2P_APAD_D0	DGND			SCK	IICSCL2	DGND	VCCK_ON	DGND		F_AV33	DP_AV33	DP_AV33						AGND33_HP	AGND33_HP		VCC_15_DDR	DGND	DC2_DDR_1V5_1	D2_ZQ		NC	NC	NC	NC	NC	NC	AC
AD	LANE 2N_APAD_D0				GPIO	GPIO					DGND	DP_AV33	DP_AV33		NC	NC			AVDD33_HPD	AVDD33_HPD		VCC_15_DDR	DGND	DC2_DDR_1V5_1	D2_VREF_DQ		NC	NC	NC	NC	NC	NC	AD
AE	LANE 3P_APAD_D0	DGND			WS	SD0	SD1							A_ADC1	NC	NC		AVDD33_DAC	AVDD33_AUDIO	AVDD33_AUDIO		VCC_15_DDR	DGND	DC2_DDR_1V5_1						NC	NC	AE
AF	LANE 3N_APAD_D0	DGND			RESETB		PMIC_IICSCL0						REXT	XTAL_VDD33	A_ADC3		DC2_DDR_1V5_2			AUDIO_REF		VCC_15_DDR		DC2_DDR_1V5_1	DC2_DDR_1V5_1							AF
AG					PWM_OUT	PMIC_INT0	PMIC_IICSDA0					A_ADC0		A_ADC2		DC2_DDR_1V5_2	DC2_DDR_1V5_2	DC2_DDR_1V5_2				AGND33_AUDIO	AGND33_AUDIO	AGND33_AUDIO	NC							AG
AH	PMIC_IICSCL1		SD2					DGND	DGND	DGND		SPI_SI		NC			DGND					LINE_IN_L	AUDIO_LINE_OUTL	AUDIO_HP_OUTL	NC	NC						AH
AJ	PMIC_IICSDA1		SD3					DGND				SPI_CLK		NC	HOST_DM	HOST_DP		EXT_UART_TX_0_6	POL_FLASH_ADDR1	POL_ISP_ADDR2		LINE_IN_R	AUDIO_LINE_OUTR	AUDIO_HP_OUTR	IICSCL_0_7							AJ
AK					NC	NC	DGND	NC				SPI_SO	SPI_CEB				EDPTX_AUX_P_0	EDPTX_AUX_N_0		PANEL_ON	IICSDA_0_7				BACKLIGHT_ADJ	NC	NC	NC	NC				AK
AL	DGND	NC	DGND	DGND	DGND			NC		DGND		DGND		DGND		DGND			XI		DPTX_HPD_0				EDPTX_AUX_N_1	EDPTX_HPD_2	EDPTX_HPD_3	PWM_5	EDPTX_HPD_1	POL_ISP_ADDR1			AL
AM	DGND	NC		NC	NC				NC	NC	NC	NC	NC	NC	NC	NC			XO		PMIC_FRWEN_UFP0				EDPTX_AUX_P_1	EDPTX_AUX_P_2	EDPTX_AUX_N_2	PWM_4	EDPTX_AUX_P_3	EDPTX_AUX_N_3	DGND	DGND	AM
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	

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Figure 1 Pin Diagram of HSBGA

5. Pin Assignments Table

(I/O Legend: A = Analog, I = Input, O = Output, P = Power, G = Ground)

Note Legend:

3(OFF) = 3.3V Tolerance even when power off

5(OFF) = 5V Tolerance even when power off

5(ON) = 5V Tolerance only when power on

IO Type Legend:

▲= GPIO can work only when power normal

Signals Pin Assigment (Total : 273 balls)

Table 1. Signals Pin Assignment of HSBGA

Pin Name	I/O	Pin #	Description	IO Type	Note
HDMI_HPD_3	IO	B1	HDMI_HPD_3(App) / EXT_UART_RX_0_5 / DENA / TCON[10] / GPIO / Test4b		5(off)
HDMI_HPD_4	IO	C1	HDMI_HPD_4(App) / HDMI_RX_HPD_4 / DVS / TCON[11] / GPIO / Test4b		5(off)
IICSCL0	IO	D1	IICSCL0 / SD0 / SPDIF0 / GPIO / Test4b		5(off)
IICSDA0	IO	E1	IICSDA0 / TCON[6] / SD1 / SPDIF1 / GPIO / Test4b		5(off)
DDCSCL_ISP	IO	F1	DDCSCL_ISP / IICSCL_0_0 / USB_SPI_CLK_0_4 / SWDCLK_0_0 / GPIO / Test4b		5(off)
IICSDA1	IO	G1	IICSDA1 / INT0_2 / INT1_2 / TCON[1] / TCON[0] / GPIO / SD3 / SPDIF3 / Test4b		5(off)
PMIC_ALERT0	IO	H1	PMIC_ALERT0(App) / IRDA_IN_0_2 / TCON[0] / TCON[1] / GPIO / Test4b		5(off)
CEC	AIO	J1	CEC / TCON[13] / GPIO / Test4b		3(off)
LANE 0P_APAD_D1	AI	L1	DP Differential Signal input		3(off)
LANE 0N_APAD_D1	AI	M1	DP Differential Signal input		3(off)
LANE 1P_APAD_D1	AIO	N1	DP Differential Signal input		3(off)

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LANE 1N_APAD_D1	AIO	P1	DP Differential Signal input		3(off)
LANE 2P_APAD_D1	AI	R1	DP Differential Signal input		3(off)
LANE 2N_APAD_D1	AI	T1	DP Differential Signal input		3(off)
LANE 3P_APAD_D1	AIO	U1	DP Differential Signal input		3(off)
LANE 3N_APAD_D1	AIO	V1	DP Differential Signal input		3(off)
LANE 0P_APAD_D0	AI	W1	DP Differential Signal input		3(off)
LANE 0N_APAD_D0	AI	Y1	DP Differential Signal input		3(off)
LANE 1P_APAD_D0	AIO	AA1	DP Differential Signal input		3(off)
LANE 1N_APAD_D0	AIO	AB1	DP Differential Signal input		3(off)
LANE 2P_APAD_D0	AI	AC1	DP Differential Signal input		3(off)
LANE 2N_APAD_D0	AI	AD1	DP Differential Signal input		3(off)
LANE 3P_APAD_D0	AIO	AE1	DP Differential Signal input		3(off)
LANE 3N_APAD_D0	AIO	AF1	DP Differential Signal input		3(off)
PMIC_IICSCL1	IO	AH1	PMIC_IICSCL1(App) / TPC_IICSCL_0_0 / GPIO / Test4b		5(off)
PMIC_IICSDA1	IO	AJ1	PMIC_IICSDA1(App) / TPC_IICSDA_0_0 / GPIO / Test4b		5(off)
PMIC_SW1	IO	B2	PMIC_SW1(App) / EXT_UART_RX_0_4 / GPIO / Test4b		5(off)
EEWD	IO	C2	EEWD / USB_SPI_SI_0_0 / GPIO		5(off)

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UART_TX_2	IO	D2	UART_TX_2(App) / EXT_UART_TX_0_2 / SCK / GPIO / Test4b		5(off)
EEIICSDA	IO	E2	EEIICSDA / GPIO		5(off)
UART_RX_0	IO	F2	UART_RX_0(App) / EXT_UART_RX_0_0 / USB_SPI_CEB0_0_0 / CLKO / GPIO / Test4b		5(off)
PMIC_FRWEN_UFP1	IO	G2	PMIC_FRWEN_UFP1(App) / IRDA_IN_0_0 / TCON[3] / GPIO / Test4b		5(off)
DPRX_AUX_N_0	AIO	H2	DPRX_AUX_N_0 / SBU1_0(App) / GPIO		3(off)
DDCSDA_4	IO	J2	DDCSDA_4 / SWDIO_0_2 / GPIO		5(off)
NC	-	AL2	NC		
NC	-	AM2	NC		
HDMI_CAB_DET3	IO	A3	HDMI_CAB_DET3(App) / DCLK / TCON[7] / GPIO / SWDCLK_0_3 / Test4b		5(off)
PCB_POWE_DOWN	IO	B3	PCB_POWE_DOWN(App) / PWM_OUT / PWM_3 / PWM_3_DIMMING / DCLK / TCON[9] / GPIO / Test4b		5(off)
UART_TX_1	IO	C3	UART_TX_1(App) / EXT_UART_TX_0_1 / USB_SPI_CEB1_0_0 / GPIO / Test4b		5(off)
UART_RX_2	IO	D3	UART_RX_2(App) / EXT_UART_RX_0_2 / WS / GPIO / Test4b		5(off)
EEIICSCL	IO	E3	EEIICSCL / GPIO		5(off)
UART_TX_0	IO	F3	UART_TX_0(App) / EXT_UART_TX_0_0 / USB_SPI_SO_0_0 / CLKO / GPIO / Test4b		5(off)
PMIC_DISCHARGE0	IO	G3	PMIC_Discharge0(App) / TCG4_1_PP / TCON[4] / GPIO / Test4b		5(off)
DPRX_AUX_P_0	AIO	H3	DPRX_AUX_P_0 / SBU2_0(App) / GPIO		3(off)
DDCSCL_4	IO	J3	DDCSCL_4 / SWDCLK_0_2 / GPIO		5(off)
NC	-	V3	NC		
NC	-	W3	NC		
SD2	IO	AH3	SD2 / SPDIF2 / TPC_IICSCL_0_2 / IHS / TCG6_1_OD / GPIO / Test4b		5(off)

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SD3	IO	AJ3	SD3 / SPDIF3 / TPC_IICSDA_0_2 / GPIO / Test4b		5(off)
PMIC_DISCHARGE1	IO	B4	PMIC_Discharge1(App) / EXT_UART_TX_0_4 / GPIO / Test4b		5(off)
PMIC_INT1	IO	C4	PMIC_INT1(App) / EXT_UART_TX_0_5 / GPIO / Test4b		5(off)
UART_RX_1	IO	D4	UART_RX_1(App) / EXT_UART_RX_0_1 / Disp_frame_start_in / Disp_frame_start_out / MCK / GPIO / Test4b		5(off)
HDMI_CAB_DET4	IO	E4	HDMI_CAB_DET4(App) / USB_SPI_CLK_0_0 / DHS / TCON[12] / GPIO / Test4b		5(off)
IICSCL1	IO	F4	IICSCL1 / SD2 / SPDIF2 / GPIO / Test4b		5(off)
DDCSDA_ISP	IO	G4	DDCSDA_ISP / IICSDA_0_0 /SWDIO_0_0 / GPIO / Test4b		5(off)
PWM_IN	IO	H4	PWM_IN / PWM_2 / PWM_2_DIMMING / IENA / TCON[5] / GPIO / Test4b		5(off)
DP_HPD2	IO	J4	DP_HPD2(App) / PWM_IN / PWM_1 / PWM_1_DIMMING / GPIO / Test4b		5(off)
NC	-	U4	NC		
NC	-	V4	NC		
DP_SINK_ASS_N2	IO	Y4	DP_SINK_ASS_N2(App) / USB_SPI_CLK_0_6 / IHS/ GPIO / Test4b		5(off)
NC	-	AM4	NC		
DPRX_L3N_D2	AI	A5	DP Differential Signal input		3(off)
EDID_WP	IO	C5	Edid_WP(App) / DENA / TCON[8] / SWDIO_0_3 / GPIO / Test4b		5(off)
NC	-	T5	NC		
NC	-	U5	NC		
DP_SINK_ASS_P2	IO	Y5	DP_SINK_ASS_P2(App) / USB_SPI_CLK_0_5 /DVS / INT0_0 / INT1_0 / GPIO / Test4b		5(off)
HUB_SPWDET	IO	AB5	HUB_SPWDET(App) / IICSCL_0_6 / PWM_5 / PWM_5_DIMMING / DHS / GPIO / Test4b		5(off)
SCK	IO	AC5	SCK / USB_SPI_SI_0_2 / TCON[7] / GPIO / Test4b		5(off)
GPIO	AIO	AD5	GPIO		3(off)

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WS	IO	AE5	WS / USB_SPI_SO_0_2 / TCON[6] / GPIO / Test4b		5(off)
RESETB	I	AF5	Chip reset bar		3(off)
PWM_OUT	IO	AG5	PWM_OUT / PWM_1 / PWM_1_DIMMING / TCON[13] / GPIO / Test4b		5(off)
NC	-	AK5	NC		
NC	-	AM5	NC		
DPRX_L3P_D2	AI	A6	DP Differential Signal input		3(off)
MCK	IO	Y6	MCK / USB_SPI_CLK_0_2 / TCON[8] / GPIO / Test4b		5(off)
HUB_BPWDET	IO	AB6	HUB_BPWDET(App) / IICSDA_0_6 / INT1_1 / IVS / GPIO / Test4b		5(off)
IICSCL2	IO	AC6	IICSCL2 / PWM_0 / PWM_0_DIMMING / IICSCL_0_3 /TCON[2] / GPIO / Test4b		5(off)
GPIO	AIO	AD6	GPIO		3(off)
SD0	IO	AE6	SD0 / SPDIF0 / USB_SPI_CEB0_0_2 / TCON[5] / GPIO / Test4b		5(off)
PMIC_INT0	IO	AG6	PMIC_INT0(App) / INT0_5 / TCG2_0_PP / GPIO / Test4b		5(off)
NC	-	AK6	NC		
DPRX_L2N_D2	AI	A7	DP Differential Signal input		3(off)
DP_SINK_ASS_P0_INT1M	IO	E7	DP_SINK_ASS_P0_int1M(App) / GPIO / Test4b		3(off)
PMIC_ALERT1	IO	F7	PMIC_ALERT1(App) / PWM_UPD_SYNC_0_0 / GPIO / Test4b		5(off)
DP_SINK_ASS_N0_INT1M	IO	G7	DP_SINK_ASS_N0_int1M(App) / GPIO / Test4b		3(off)
FLASH_WP	IO	H7	FLASH_WP (App) / IRQB / TCON[2] / GPIO / Test4b		5(off)
SD1	IO	AE7	SD1 / SPDIF1 / USB_SPI_CEB1_0_2 / PWM_3 / PWM_3_DIMMING / TCON[4] / GPIO / Test4b		5(off)
PMIC_IICSCL0	IO	AF7	PMIC_IICSCL0(App) / TPC_IICSCL_0_1 / GPIO / Test4b		5(off)
PMIC_IICSDA0	IO	AG7	PMIC_IICSDA0(App) / TPC_IICSDA_0_1 / GPIO / Test4b		5(off)
DPRX_L2P_D2	AI	A8	DP Differential Signal input		3(off)
DDCSDA_3	IO	E8	DDCSDA_3 / SWDIO_0_1 / GPIO		5(off)
VCCK_OFF_EN	IO	F8	VCCK_OFF_EN(App) / EXT_UART_RX_0_3 / GPIO / Test4b		5(off)

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DP_CAB_DET0	IO	G8	DP_CAB_DET0(App) / USB_SPI_CEB0_0_3 / GPIO / Test4b		5(off)
PMIC_SW0	IO	Y8	PMIC_SW0(App) / TCG0_0_PP / IHS / GPIO / Test4b		5(off)
IICSDA2	IO	AA8	IICSDA2 / PWM_UPD_SYNC_0_1 / IICSDA_0_3 / INT0_3 / TCON[3] / GPIO / Test4b		5(off)
NC	-	AK8	NC		
NC	-	AL8	NC		
DPRX_L1N_D2	AI	A9	DP Differential Signal input		3(off)
DP_CAB_DET1	IO	D9	DP_CAB_DET1(App) / USB_SPI_SI_0_3 /GPIO / Test4b		5(off)
DPRX_AUX_P_1	AIO	E9	DPRX_AUX_P_1 / SBU2_1(App) / GPIO		3(off)
DPRX_AUX_N_1	AIO	F9	DPRX_AUX_N_1 / SBU1_1(App) / GPIO		3(off)
DDCSCL_3	IO	G9	DDCSCL_3 / SWDCLK_0_1 / GPIO		5(off)
DP_HPD0	IO	H9	DP_HPD0(App) / USB_SPI_CEB1_0_3 / GPIO / Test4b		5(off)
NC	-	AM9	NC		
DPRX_L1P_D2	AI	A10	DP Differential Signal input		3(off)
DP_HPD1	IO	D10	DP_HPD1(App) / USB_SPI_SO_0_3 / GPIO / Test4b		5(off)
DP_CAB_DET2	IO	E10	DP_CAB_DET2(App) / USB_SPI_CLK_0_3 / GPIO / Test4b		5(off)
DPRX_AUX_N_2	AIO	F10	DPRX_AUX_N_2 / SBU1_2(App) / GPIO		3(off)
DPRX_AUX_P_2	AIO	G10	DPRX_AUX_P_2 / SBU2_2(App) / GPIO		3(off)
NC	-	AM10	NC		
DPRX_L0N_D2	AI	A11	DP Differential Signal input		3(off)
BACKLIGHT_ON	IO	E11	Backlight_On(App) / PWM_2 / PWM_2_DIMMING / EXT_UART_TX_0_3 / GPIO / Test4b		5(off)
DP_SINK_ASS_N1_INT1M	IO	G11	DP_SINK_ASS_N1_int1M(App) / GPIO / Test4b		3(off)
DP_SINK_ASS_P1_INT1M	IO	H11	DP_SINK_ASS_P1_int1M(App) / GPIO / Test4b		3(off)
NC	-	AM11	NC		3(off)
DPRX_L0P_D2	AI	A12	DP Differential Signal input		3(off)

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A_ADC0	AIO	AG12	A_ADC0(App) / SARADC_0 /GPIO / Test4b		3(off)
SPI_SI	IO	AH12	Flash SPI_SI		3(off)
SPI_CLK	IO	AJ12	Flash SPI_CLK		3(off)
NC	-	AM12	NC		
REXT	AI	AF13	Impedance Match Reference Resistor. It should be pulled down 12kohm.		3(off)
SPI_SO	IO	AK13	Flash SPI_SO		3(off)
NC	-	AM13	NC		
RX2P_D3	AI	A14	TMDS Differential Signal Input		3(off)
RX2N_D3	AI	B14	TMDS Differential Signal Input		3(off)
A_ADC1	AIO	AE14	A_ADC1(App) / SARADC_1 / GPIO / Test4b		3(off)
A_ADC2	AIO	AG14	A_ADC2(App) / SARADC_2 / INT0_6 / GPIO / Test4b		3(off)
NC	-	AH14	NC		
NC	-	AJ14	NC		
SPI_CEB	IO	AK14	Flash SPI_CEB		3(off)
NC	-	AM14	NC		
RX1N_D3	AI	B15	TMDS Differential Signal Input		3(off)
RX1P_D3	AI	C15	TMDS Differential Signal Input		3(off)
NC	-	AD15	NC		
NC	-	AE15	NC		
A_ADC3	AIO	AF15	A_ADC3(App) / SARADC_3 / GPIO / Test4b		3(off)
HOST_DM	AIO	AJ15	USB Host D-		3(off)
NC	-	AM15	NC		
NC	-	AE16	NC		
HOST_DP	AIO	AJ16	USB Host D+		3(off)
NC	-	AM16	NC		
RX0P_D3	AI	B17	TMDS Differential Signal Input		3(off)
RX0N_D3	AI	C17	TMDS Differential Signal Input		3(off)
EDPTX_AUX_P_0	AIO	AK17	EDPTX_AUX_P_0 / GPIO	▲	3(off)
RX3N_D3	AI	A18	TMDS Differential Signal Input		3(off)
RX3P_D3	AI	B18	TMDS Differential Signal Input		3(off)

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EDPTX_HPD_3	IO	E18	EDPTX_HPD_3 / VB1_PLL_LOCK_1_0 / GPIO	▲	5(off)
EXT_UART_TX_0_6	IO	AJ18	EXT_UART_TX_0_6 / INT0_4 / TCG2_1_PP / GPIO / Test4b	▲	5(off)
EDPTX_AUX_N_0	AIO	AK18	EDPTX_AUX_N_0 / GPIO	▲	3(off)
USB_SPI_SO_0_1	IO	E19	USB_SPI_SO_0_1 / TCON[11] / GPIO / Test4b	▲	5(off)
V_BY_ONE_SDA_1	IO	F19	V_by_One_SDA_1(App) / IICSDA_0_4 / GPIO / Test4b	▲	5(off)
NC	-	H19	NC		
POL_FLASH_ADDR1	IO	AJ19	Flash address select: Pull High: 4 bytes mode Pull Low: 3 bytes mode		5(off)
XI	AI	AL19	Crystal Input		3(off)
XO	AO	AM19	Crystal Output		3(off)
RX2P_D4	AI	A20	TMDS Differential Signal Input		3(off)
RX2N_D4	AI	B20	TMDS Differential Signal Input		3(off)
USB_SPI_CEB0_0_1	IO	E20	USB_SPI_CEB0_0_1 / PWM_4 / PWM_4_DIMMING / TCON[12] / GPIO / Test4b	▲	5(off)
V_BY_ONE_SCL_1	IO	F20	V_by_One_SCL_1(App) / IICSCL_0_4 / GPIO / Test4b	▲	5(off)
NC	-	H20	NC		
NC	-	J20	NC		
AUDIO_REF	AIO	AF20	AUDIO_REF / WS / GPIO	▲	3(off)
POL_ISP_ADDR2	IO	AJ20	ISP slave address [ADDR2:ADDR1] = 00: 0x90 [ADDR2:ADDR1] = 01: 0x94 [ADDR2:ADDR1] = 10: 0x98 [ADDR2:ADDR1] = 11: 0x9C		5(off)
PANEL_ON	IO	AK20	Panel_On(App) / EXT_UART_RX_0_6 / IRDA_IN_0_1 / TCG0_1 / GPIO / Test4b	▲	5(off)
RX1N_D4	AI	B21	TMDS Differential Signal Input		3(off)
RX1P_D4	AI	C21	TMDS Differential Signal Input		3(off)
USB_SPI_SI_0_1	IO	E21	USB_SPI_SI_0_1 / IICSDA_0_5 / TCON[10] / GPIO / Test4b	▲	5(off)
USB_SPI_CEB1_0_1	IO	F21	USB_SPI_CEB1_0_1 / GPIO / Test4b	▲	5(off)
USB_SPI_CLK_0_1	IO	G21	USB_SPI_CLK_0_1 / IICSCL_0_5 / TCON[9] / GPIO / Test4b	▲	5(off)

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DDR_ZQ	I	V21	External reference ball for output drive calibration: This ball is tied to an external 240Ω resistor (1%), which is tied to VSSQ.		-
IICSDA_0_7	IO	AK21	IICSDA_0_7 / TCG4_0_PP / GPIO / Test4b / TTS_SI	▲	5(off)
DPTX_HPD_0	IO	AL21	DPTX_HPD_0 / GPIO / Test4b	▲	5(off)
PMIC_FRWEN_UFP0	IO	AM21	PMIC_FRWEN_UFP0(App) / GPIO / TTS_CEB	▲	5(off)
NC	-	E22	NC		
D3_VREF_DQ	I	V22	DDR Reference Voltage		-
LINE_INL	AIO	AH22	LINE_INL / MCK / GPIO	▲	3(off)
LINE_INR	AIO	AJ22	LINE_INR / SCK / GPIO	▲	3(off)
RX0P_D4	AI	B23	TMDS Differential Signal Input		3(off)
RX0N_D4	AI	C23	TMDS Differential Signal Input		3(off)
NC	-	E23	NC		
NC	-	F23	NC		3(off)
AUDIO_LINE_OUTL	AIO	AH23	AUDIO_SOUTL / SD0 / SPDIF0 / GPIO	▲	3(off)
AUDIO_LINE_OUTR	AIO	AJ23	AUDIO_SOUTR / SD1 / SPDIF1 / GPIO	▲	3(off)
RX3N_D4	AI	A24	TMDS Differential Signal Input		3(off)
RX3P_D4	AI	B24	TMDS Differential Signal Input		3(off)
DDR_VREF_23	I	AA24	DDR Reference Voltage		-
AUDIO_HP_OUTL	AIO	AH24	AUDIO_HOUTL / SD2 / SPDIF2 / GPIO	▲	3(off)
AUDIO_HP_OUTR	AIO	AJ24	AUDIO_HOUTR / SD3 / SPDIF3 / GPIO	▲	3(off)
DDR_VREF_01	I	AA25	DDR Reference Voltage		-
D2_VREF_CA	I	AB25	DDR Reference Voltage		-
D2_ZQ	I	AC25	External reference ball for output drive calibration: This ball is tied to an external 240Ω resistor (1%), which is tied to VSSQ.		-
D2_VREF_DQ	I	AD25	DDR Reference Voltage		-
NC	-	AG25	No Connect		
NC	-	AH25	No Connect		
IICSCL_0_7	IO	AJ25	IICSCL_0_7 / TCG6_0_PP / GPIO / Test4b / TTS_SCLK	▲	5(off)

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BACKLIGHT_ADJ	IO	AK25	Backlight_Adj(App) / PWM_OUT / PWM_0 / PWM_0_DIMMING / GPIO / Test4b	▲	5(off)
EDPTX_AUX_N_1	AIO	AL25	EDPTX_AUX_N_1 / GPIO	▲	3(off)
EDPTX_AUX_P_1	AIO	AM25	EDPTX_AUX_P_1 / GPIO	▲	3(off)
VTX_TX0P	AO	B26	Vby1 output		3(off)
VTX_TX0N	AO	C26	Vby1 output		3(off)
D3_VREF_CA	I	V26	DDR Reference Voltage		-
NC	-	AH26	No Connect		
NC	-	AK26	No Connect		
EDPTX_HPD_1	IO	AL26	EDPTX_HPD_1 / VB1_PLL_LOCK_0_0 / GPIO	▲	5(off)
EDPTX_AUX_P_2	AIO	AM26	EDPTX_AUX_P_2 / GPIO	▲	3(off)
VTX_TX1P	AO	B27	Vby1 output		3(off)
VTX_TX1N	AO	C27	Vby1 output		3(off)
D3_ZQ	I	V27	External reference ball for output drive calibration: This ball is tied to an external 240Ω resistor (1%), which is tied to VSSQ.		-
NC	-	AC27	NC		
NC	-	AD27	NC		
NC	-	AK27	No Connect		
EDPTX_HPD_2	IO	AL27	EDPTX_HPD_2 / VB1_PLL_HPD_1_0 / GPIO	▲	5(off)
EDPTX_AUX_N_2	AIO	AM27	EDPTX_AUX_N_2 / GPIO	▲	3(off)
VTX_TX2P	AO	B28	Vby1 output		3(off)
VTX_TX2N	AO	C28	Vby1 output		3(off)
NC	-	AC28	NC		
NC	-	AD28	NC		
NC	-	AK28	No Connect		
PWM_5	IO	AL28	PWM_5 / PWM_5_DIMMING / GPIO / Test4b / TTS_SO	▲	5(off)
PWM_4	IO	AM28	PWM_4 / PWM_4_DIMMING / GPIO / Test4b	▲	5(off)
VTX_TX3P	AO	B29	Vby1 output		3(off)
VTX_TX3N	AO	C29	Vby1 output		3(off)
NC	-	AC29	NC		

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NC	-	AD29	NC		
NC	-	AK29	No Connect		
EDPTX_HPD_0	IO	AL29	EDPTX_HPD_0 / VB1_PLL_HPD_0_0 / GPIO	▲	5(off)
EDPTX_AUX_P_3	AIO	AM29	EDPTX_AUX_P_3 / GPIO	▲	3(off)
DPTX_LANE_N4_1	AO	K30	eDP output / Vby1 output		3(off)
DPTX_LANE_N5_1	AO	L30	eDP output / Vby1 output		3(off)
DPTX_LANE_N6_1	AO	M30	eDP output / Vby1 output		3(off)
DPTX_LANE_N7_1	AO	N30	eDP output / Vby1 output		3(off)
DPTX_LANE_P0_2	AO	P30	eDP output		3(off)
DPTX_LANE_P1_2	AO	R30	eDP output		3(off)
DPTX_LANE_P2_2	AO	T30	eDP output		3(off)
DPTX_LANE_P3_2	AO	U30	eDP output		3(off)
NC	-	AC30	NC		
NC	-	AD30	NC		
POL_ISP_ADDR1	IO	AL30	ISP slave address [ADDR2:ADDR1] = 00: 0x90 [ADDR2:ADDR1] = 01: 0x94 [ADDR2:ADDR1] = 10: 0x98 [ADDR2:ADDR1] = 11: 0x9C		5(off)
EDPTX_AUX_N_3	AIO	AM30	EDPTX_AUX_N_3 / GPIO	▲	3(off)
VTX_TX4N	AO	B31	Vby1 output		3(off)
VTX_TX5N	AO	C31	Vby1 output		3(off)
VTX_TX6N	AO	D31	Vby1 output		3(off)
VTX_TX7N	AO	E31	Vby1 output		3(off)
DPTX_LANE_N0_1	AO	F31	eDP output / Vby1 output		3(off)
DPTX_LANE_N1_1	AO	G31	eDP output / Vby1 output		3(off)
DPTX_LANE_N2_1	AO	H31	eDP output / Vby1 output		3(off)
DPTX_LANE_N3_1	AO	J31	eDP output / Vby1 output		3(off)
DPTX_LANE_P4_1	AO	K31	eDP output / Vby1 output		3(off)
DPTX_LANE_P5_1	AO	L31	eDP output / Vby1 output		3(off)
DPTX_LANE_P6_1	AO	M31	eDP output / Vby1 output		3(off)
DPTX_LANE_P7_1	AO	N31	eDP output / Vby1 output		3(off)
DPTX_LANE_N0_2	AO	P31	eDP output		3(off)
DPTX_LANE_N1_2	AO	R31	eDP output		3(off)
DPTX_LANE_N2_2	AO	T31	eDP output		3(off)

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DPTX_LANE_N3_2	AO	U31	eDP output		3(off)
DPTX_LANE_P4_2	AO	V31	eDP output		3(off)
DPTX_LANE_P5_2	AO	W31	eDP output		3(off)
DPTX_LANE_P6_2	AO	Y31	eDP output		3(off)
DPTX_LANE_P7_2	AO	AA31	eDP output		3(off)
NC	-	AB31	NC		
NC	-	AC31	NC		
NC	-	AD31	NC		
NC	-	AE31	NC		
VTX_TX4P	AO	B32	Vby1 output		3(off)
VTX_TX5P	AO	C32	Vby1 output		3(off)
VTX_TX6P	AO	D32	Vby1 output		3(off)
VTX_TX7P	AO	E32	Vby1 output		3(off)
DPTX_LANE_P0_1	AO	F32	eDP output / Vby1 output		3(off)
DPTX_LANE_P1_1	AO	G32	eDP output / Vby1 output		3(off)
DPTX_LANE_P2_1	AO	H32	eDP output / Vby1 output		3(off)
DPTX_LANE_P3_1	AO	J32	eDP output / Vby1 output		3(off)
DPTX_LANE_N4_2	AO	V32	eDP output		3(off)
DPTX_LANE_N5_2	AO	W32	eDP output		3(off)
DPTX_LANE_N6_2	AO	Y32	eDP output		3(off)
DPTX_LANE_N7_2	AO	AA32	eDP output		3(off)
NC	-	AB32	NC		
NC	-	AC32	NC		
NC	-	AD32	NC		
NC	-	AE32	NC		

Power / Ground Pin Assignment (Total : 256 balls)

Table 2. Power / Ground Pin Assignment of HSBGA

P/G Pin Name	I/O	Pin #	Description	Note
PVCC	P	L8, L9, M8, M17, Y11, Y12, Y18, AA18, K22, K23, R23, R24,	Pad Power	
VCCK_ON	P	K19, P12, R12, T12, U12, AB8, AC8,	1.0V Core Power	
VCCK_OFF	P	M18, M19, R19, T19, V19, W19, Y19, AA19, AB18,	1.0V Core Power	
DPRXAV33	AP	M13, N12,	3.3V Analog Power	
DPRX_AV1833	AP	L11, L12, N8, P8, V6, W6,	3.3V Analog Power	
DPRX_AV33	AP	T8, U8, V8,	3.3V Analog Power	
F_AV33	AP	AB11, AC11,	3.3V Analog Power	
GDI_VDD10	AP	N11, P11, R11, T11, W11, W12, AB9, AB10,	1.0V Analog Power	
RX_VDD10_HDMI	AP	M14, M15, N15, N16,	1.0V Analog Power	

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RX_VDD33_HDMI	AP	L14, L15,	3.3V Analog Power	
DP_AV33	AP	AC13, AD13,	3.3V Analog Power	
DP_AV10	AP	AB12, AC12, AD12,	1.0V Analog Power	
DP_AV10_CMU	AP	AA13, AA14	1.0V Analog Power	
Vby1_eDPTX_TX_AV33	AP	N20, P20,	3.3V Analog Power	
Vby1_eDPTX_TX_AV10	AP	L20, L21, M21, N21, P21, R21, T21,	1.0V Analog Power	
DDRPLL_V33	AP	W23, W24,	3.3V DRAM PLL Power	
DDRPLL_V10	AP	Y23, Y24,	1.0V DRAM PLL Power	
VCC_15_DDR	P	Y21, AA21, AA22, AB21, AB22, AC22, AD22, AE22, AF22,	1.5V DDR3 Power	
VCC_15_DDR_CK	P	W22,	1.5V DDR3 Power	
DC2_DDR_1V5_1	P	AB24, AC24, AD24, AE24, AF24, AF25,	1.5V DDR3 Power	
DC2_DDR_1V5_2	P	G17, G18, H17, H18, AF17, AG16, AG17, AG18,	1.5V DDR3 Power	
NC	-	AD16,	5V VCONN Power	
NC	-	J19,	5V VCONN Power	
BMC_AVDD33	AP	L18,	3.3V Analog Power	
U_AV33	AP	Y17, AA17,	3.3V Analog Power	
U_AV10	AP	Y16, AA16,	1.0V Analog Power	
B10_SARADC_V33	AP	K16, K17,	3.3V 10bits SARADC Power	
UX_AV33	AP	T9, U9,	3.3V Analog Power	
XTAL_VDD33	AP	AF14,	XTAL Power	
AVDD33_AUDIO	AP	AE19, AE20,	3.3V Audio Power	
AVDD33_HP	AP	AD19, AD20,	3.3V Audio HP Power	
AVDD33_DAC	AP	AE18,	3.3V Audio DAC Power	
AGND33_AUDIO	AG	AG22, AG23, AG24,	Audio Gound	
AGND33_HP	AG	AC19, AC20,	Audio HP Ground	
DGND	G	A1, A2, A31, A32, B6, B8, B10, B12, B13, C14, C18, C19, C20, C24, C25, D15, D16, D17, D21, D22, D23, D26, D28, D30, E26, E27, E28, F12, F28, F30, G12, G16, G19, G28, H16, H28, H29, H30, J15, K29, L2, L3, M29, N2, N3, N9, N13, N14, N17, N18, P9, P13, P14, P15, P16, P17, P18, P29, R2, R4, R9, R13, R14, R15, R16, R17, R18, T13, T14, T15, T16, T17, T18, T28, T29, U2, U13, U14, U15, U16, U17, U18, V9, V13, V14, V15, V16, V17, V18, V29, V30, W2, W9, W13, W14, W15, W16, W17, W18, Y9, Y13, Y14, Y15, Y30, AA2, AA15, AB27, AB28, AB30, AC2, AC7, AC9, AC23, AD11, AD23, AE2, AE23, AF2, AH8, AH9, AH10, AH17, AJ8, AK7, AL1, AL3, AL4, AL5, AL10, AL12, AL14, AL16, AM1, AM31, AM32,	Digital Ground	

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6. Electrical Specifications

Electrical Specifications

HSBGA DC Characteristics

6.1. Recommended Operating Conditions

Table 3. Recommended Operating Conditions of HSBGA

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Voltage on Input (5V tolerance)	V_{IN}	-0.3		5.5	V
Voltage on Input (3.3V tolerance)	V_{IN}	-0.3		3.63	V
Supply Voltage	V33S	3.14	3.30	3.47	V
DDR Voltage	1.5V_DDR	1.43	1.5	1.57	V
Core Power On Voltage	V11S_ON	0.95	1.0	1.05	V
Core Power Off Voltage	V11S_OFF	0.95	1.0	1.05	V
GDI Core Power Voltage	GDI_1V	0.95	1.0	1.05	V
Analog Core Power Voltage	AV_10	0.95	1.0	1.05	V
Electrostatic Discharge	V_{ESD}			±2.5	kV
Latch-Up	I_{LA}			±100	mA
Ambient Operating Temperature	T_A	0		70	ºC
Storage Temperature (plastic)	T_{STG}	-55		125	ºC
Thermal Resistance (Junction to Air)	θ_{JA}				ºC/W
Thermal Resistance (Junction to Case)	θ_{JC}				ºC/W
Junction Acceptable Temperature	T_j			125	ºC

6.2. Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings of HSBGA

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage	V33S			3.6	V
Supply Voltage	V11S_x			1.21	V
Storage Temperature (plastic)	T_{STG}			150	ºC
Junction Acceptable Temperature	T_j			150	ºC

Note : Operation under the absolute maximum ratings does not imply well-functioning. Long-term stress to the absolute maximum ratings would probably affect the device reliability or further cause permanent damage.

6.3. Reset Period

Table 5. Reset Period of HSBGA

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Reset Pulse Period	Trst-en[1]	1120			ns
Power-on-Reset Period	Tpor-rst[2]	145	146.5	148	ms

1. 16 * Xtal_cycle(1/14.3Mhz)
2. 65536*16*2*Xtal_cycle(1/14.3Mhz)

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7. Mechanical Specifications

PBGA

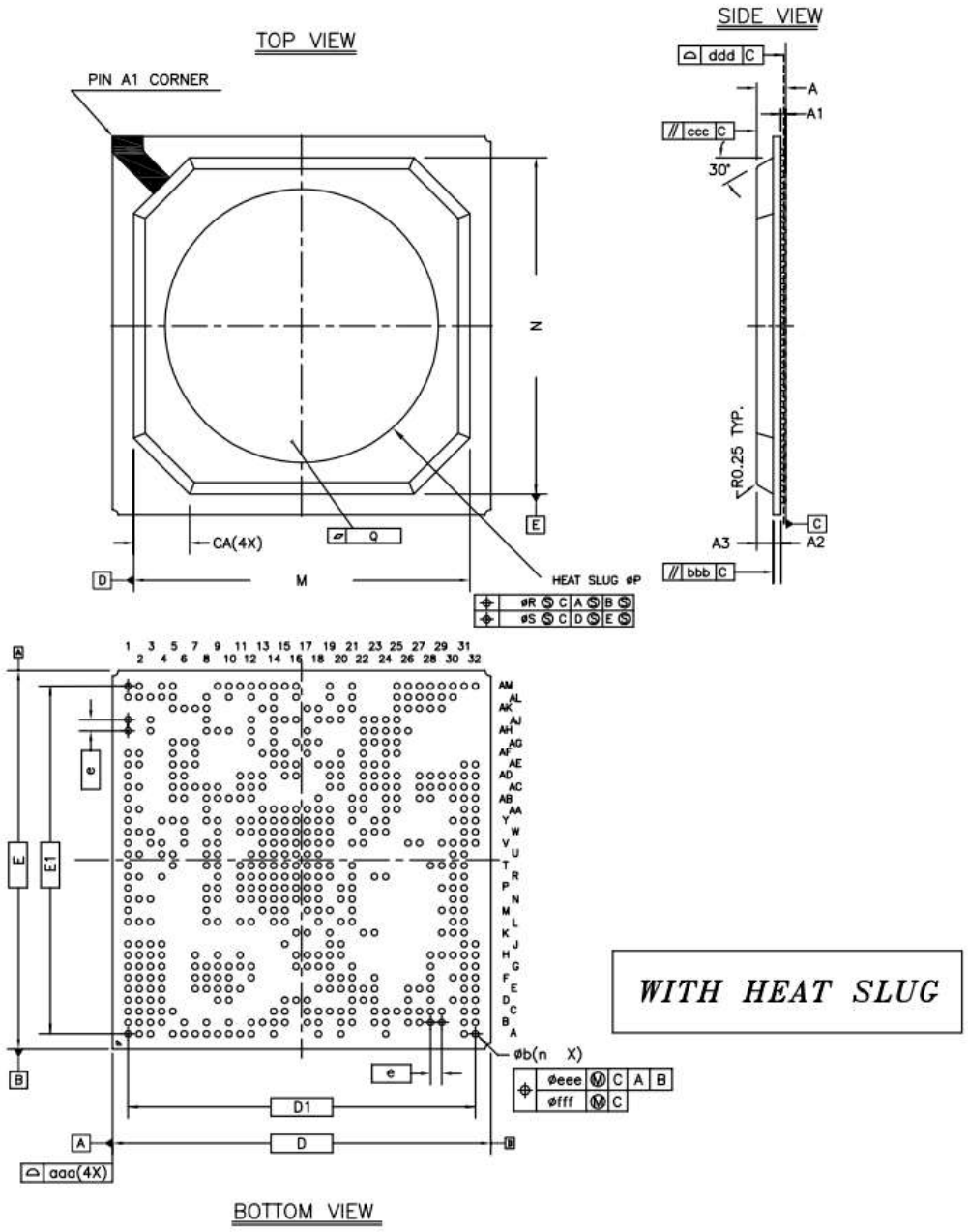


Figure 2 Mechanical Specification of HSBGA (1)

		Symbol	Common Dimensions		
			MIN.	NOM.	MAX.
Package :			HSTK FBGA		
Body Size:	X	D	27.000		
	Y	E	27.000		
Ball Pitch :		e	0.800		
Total Thickness :		A	2.000	2.082	2.164
Mold Thickness :		A3	1.170 Ref.		
Substrate Thickness :		A2	0.542 Ref.		
Ball Diameter :			0.450		
Stand Off :		A1	0.320	–	0.420
Ball Width :		b	0.375	–	0.525
Mold Area :	X	M	24.000		
	Y	N	24.000		
H/S Exposed Size:		P	19 ~ 20		
H/S Flatness		Q	0.100		
H/S Shift With Substrate Edge:		R	0.300		
H/S Shift With Mold Area:		S	0.500		
Chamfer		CA	4.000 Ref.		
Package Edge Tolerance :		aaa	0.150		
Substrate Parallelism :		bbb	0.100		
Mold Parallelism :		ccc	0.200		
Coplanarity:		ddd	0.150		
Ball Offset (Package) :		eee	0.150		
Ball Offset (Ball) :		fff	0.080		
Ball Count :		n	536		
Edge Ball Center to Center :	X	D1	24.800		
	Y	E1	24.800		

Figure 3 Mechanical Specification of HSBGA (2)

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8. Ordering Information

Table 6. Ordering Information

Part No.	Max. Resolution	Input : DP1.4	Input : HDMI2.0	Output : eDP	Output : Vby1	FRC	OD	PKG
RTD2738 -VW-CG	3440 x 1440 @ 240Hz/1920 x 1080 @ 480Hz	3port	2 Ports	•	•	•	•	PBGA

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