

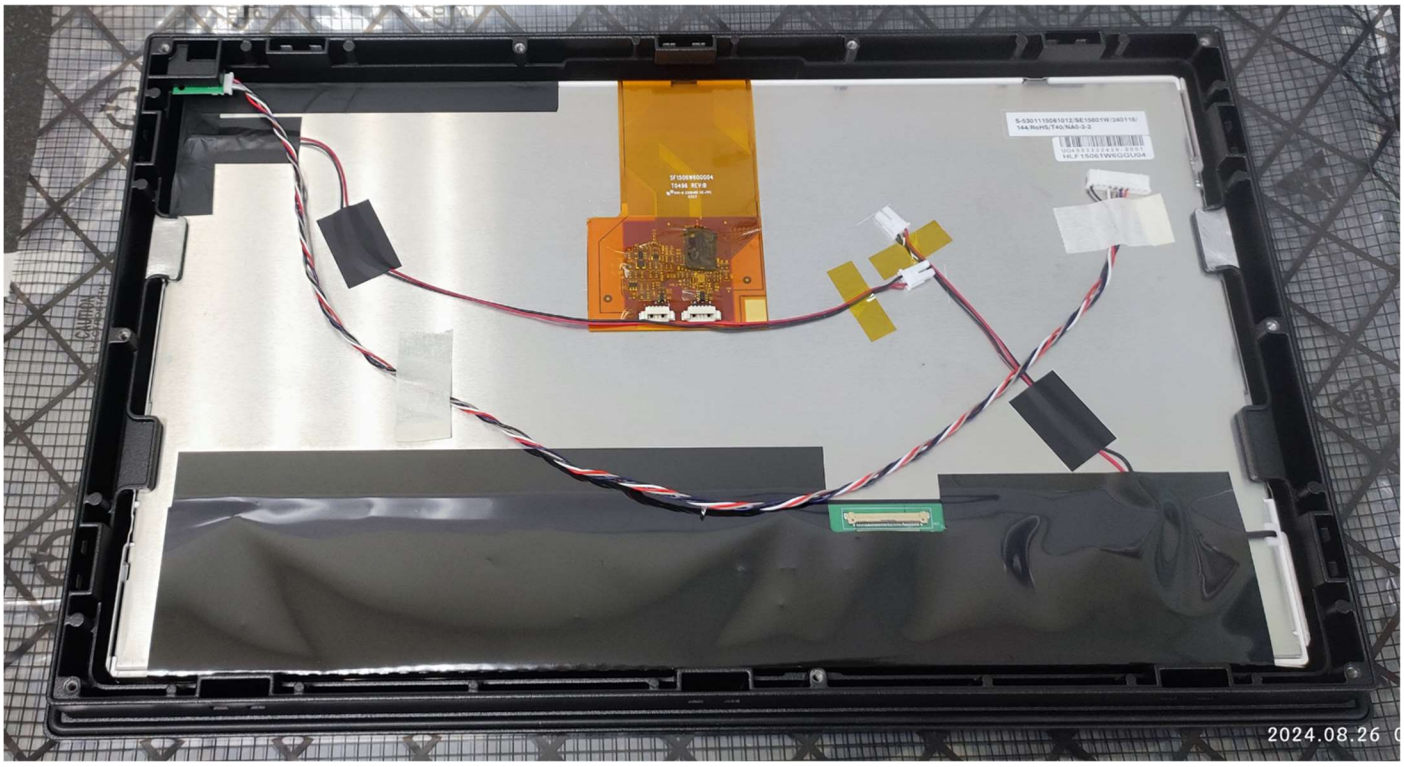

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工程課
2024 -08- 26
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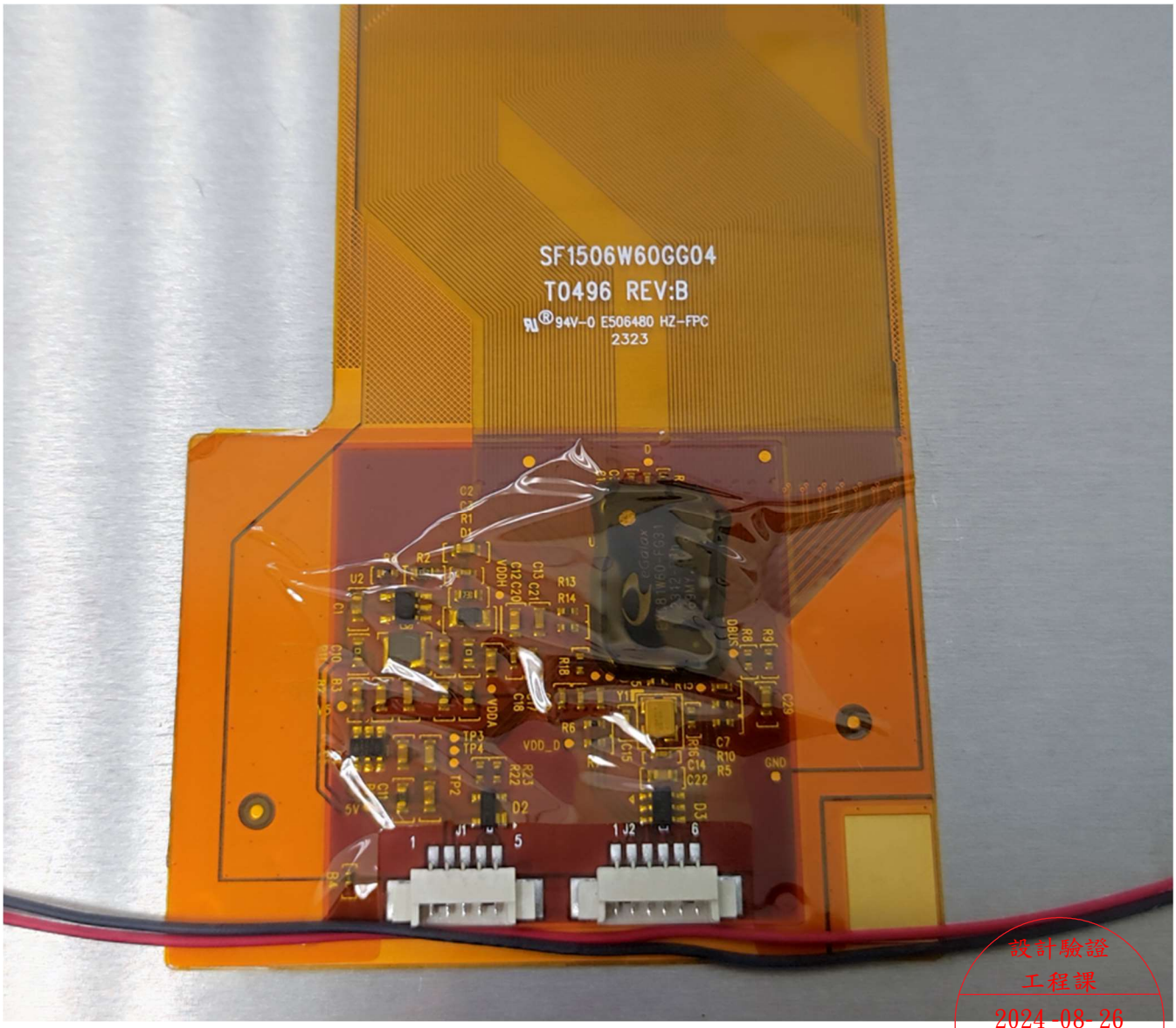

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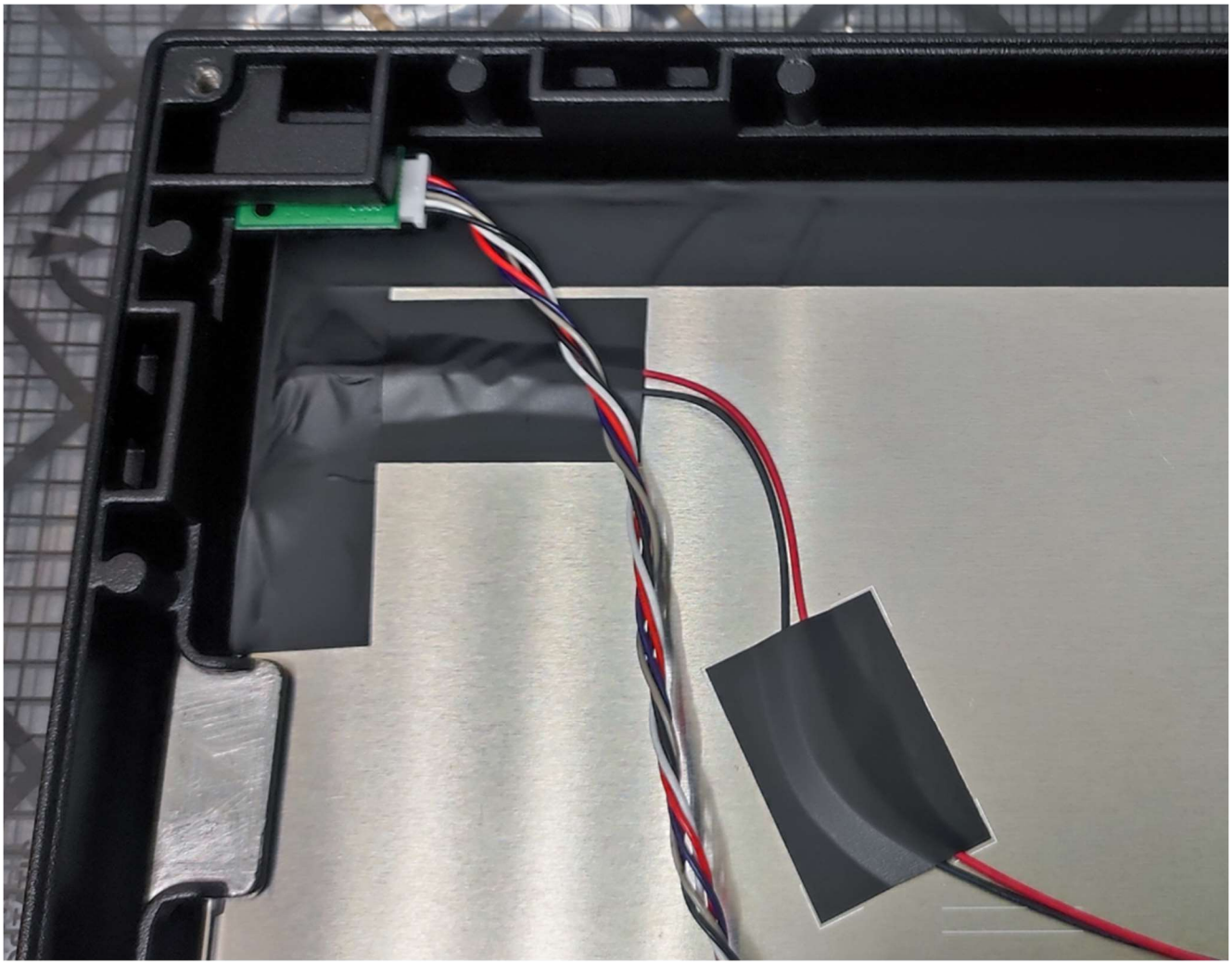

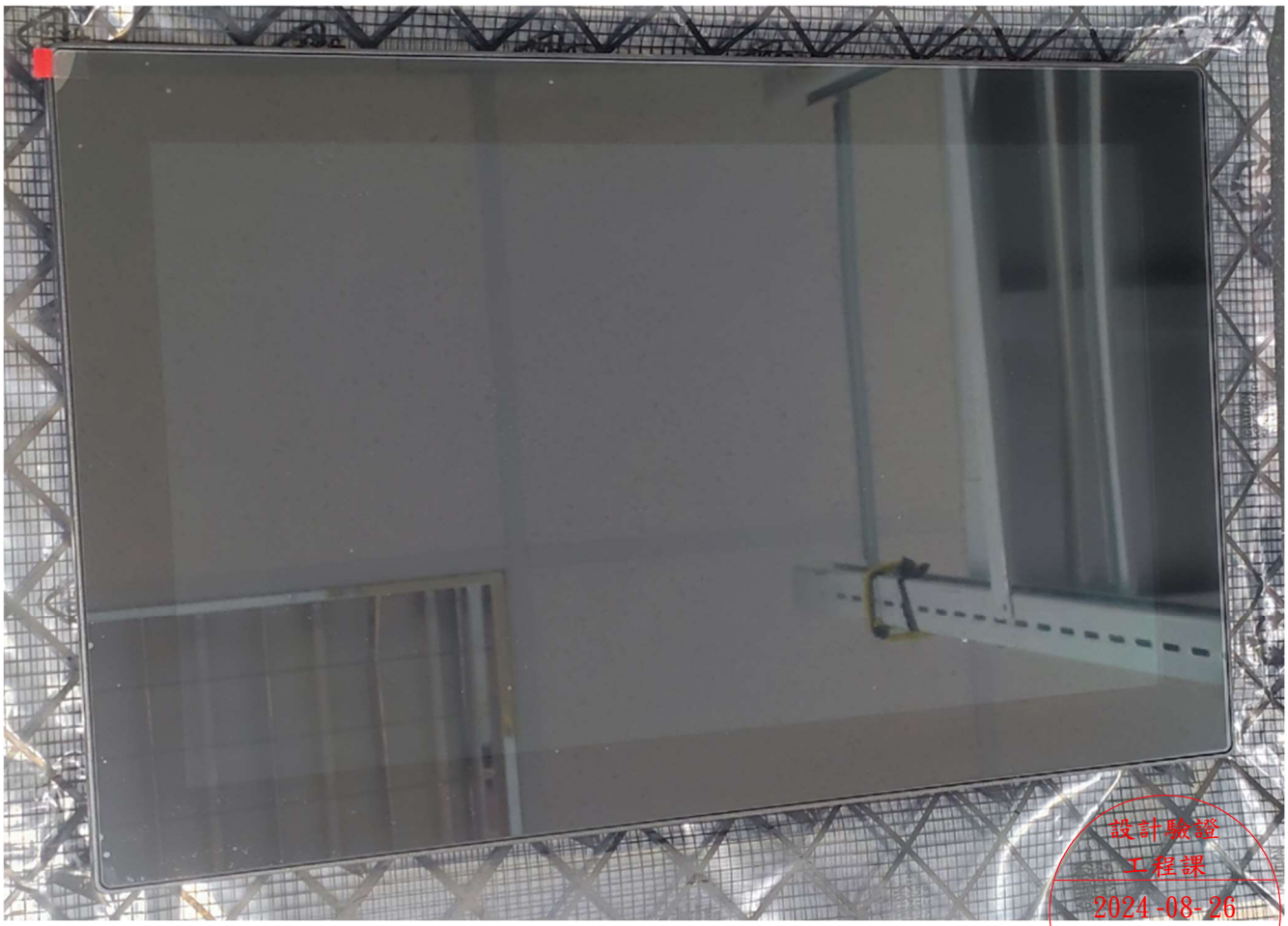

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DATA IMAGE CORPORATION

PRODUCT SPECIFICATION

MODEL NO.: HLF15061W6GGU04

■ Preliminary Specification

☐ Approval Specification

2AAD666013P(T0208)

Customer :

APPROVED BY

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R&D Approved By	Prepared By
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1. GENERAL DESCRIPTION

1.1 OVERVIEW

HLF15061W6GGU04 is a 15.6" (diagonal) a-Si & transmissive type thin film transistor liquid crystal display (TFT-LCD) module with LVDS interface. The module is composed of a TFT-LCD panel, driver circuit, capacitance touch panel and backlight unit.

1.2 TFT LCD MODULE SPECIFICATIONS【Vehicle-1】

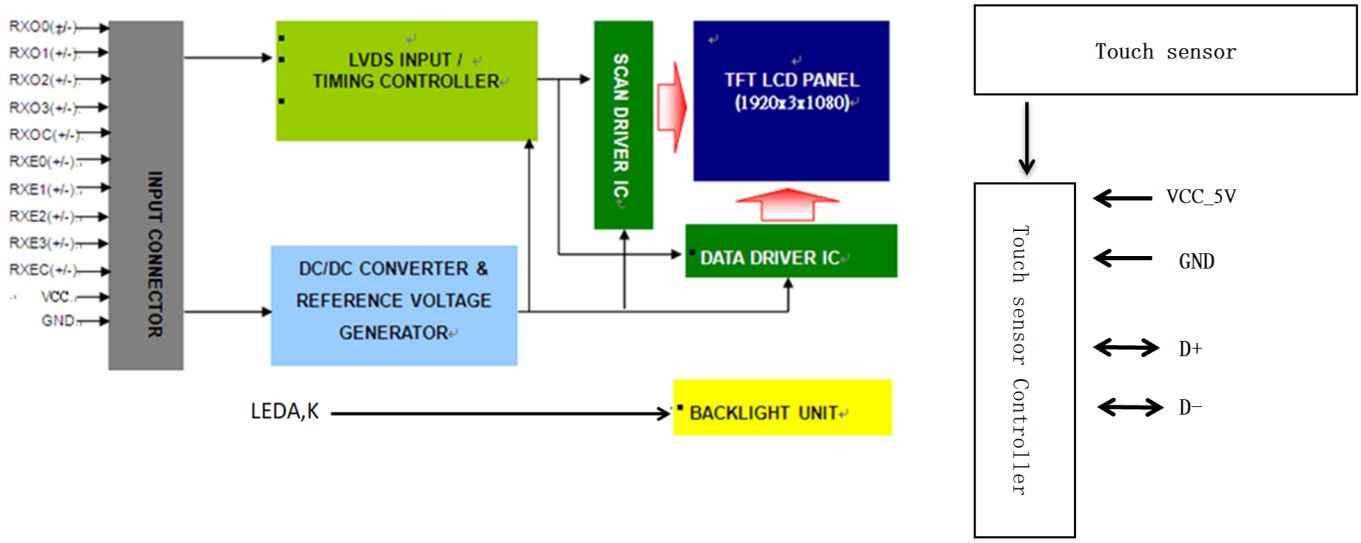
The following items are characteristics summary on the table under 25℃ condition :

Parameter	Specifications	Unit
Screen Size	15.6(diagonal)	inch
LCM With CTP Outline Dimension	401.66H) x 251.09(V) x 26.2(D)	mm
LCD Active Area	344.16 (H) x 193.59(V)	mm
Resolution	1920(H) x (R,G,B) x 1080(V)	Dots
Pixel Pitch	0.17925 (H) x 0.17925 (V)	mm
Pixel Arrangement	RGB vertical stripe	
Display Mode	Normally Black	
Display Colors	16.7M	
View direction	All	
Luminance, White	1000	cd/m^2
LCD Interface	LVDS	
Surface treatment	Clear	
RoHS Compliance	Yes	

1.3 TOUCH MODULE SPECFICATIONS

Parameter	Specifications	Unit
Touch Type	Transparent type projected capacitive touch panel	
Cover Thickness	3	mm
Surface Hardness	≥6H	
Cover Outline Dimension	397.16H) x 246.59(V)	mm
Cover Visual Area	345.16(H) × 194.59(V)	
Sensor Outline Dimension	362.8 × 216.1	mm
Sensor Active Area	347.16 × 196.59	mm
Touch & LCD Bonding	Optical Bonding	
Multi-Touch Point	10	
Touch Interface	USB	
(X,Y)position		

2. FUNCITONAL BLOCK DIAGRAM



3. ABSOLUTE MAXIMUM RATINGS

3.1 ABSOLUTE RATINGS OF ENVIRONMENT

Parameter	Symbol	Min.	Max.	Unit	Remark
Operating Temperature	TOP	-30	85	°C	Note 1,2
Storage Temperature	TST	-30	85	°C	Note 1,2

Note 1: Temperature and relative humidity range is shown in the figure below.
(a) 90 %RH Max. (Ta ≦ 40 ºC).
(b) Wet-bulb temperature should be 39 ºC Max. (Ta > 40 ºC).
(c) No condensation.

Note 2: The absolute maximum rating values of this product are not allowed to be exceeded at any times. The module should not be used over the absolute maximum rating value. It will cause permanently unrecoverable function fail in such a condition.

3.2 ELECTRICAL ABSOLUTE RATINGS

Ta=25°C

Parameter	Symbol	Min.	Max.	Unit	Remark
Power Supply Voltage	V_{CC}	-0.3	3.6	V	Note1
Logic Input Voltage	V_{IN}	-0.3	4.0	V	Note1

Note 1: Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under normal Operating Conditions.

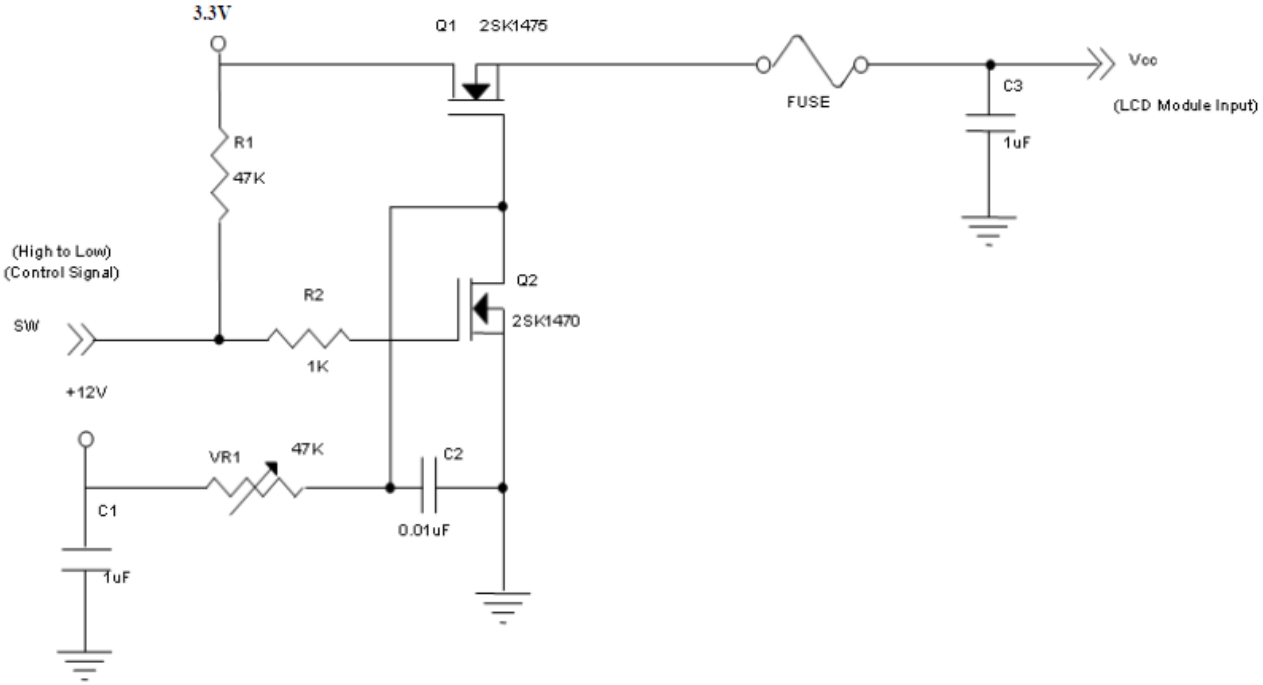
4. ELECTRICAL SPECIFCATIONS
4.1 ELECTRICAL CHARACTERISTICS
4.1.1 TFT LCD MODULE ELETRONICS SPECIFICATION

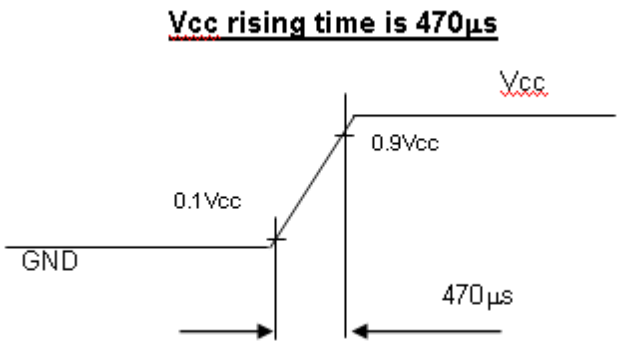
Ta=25°C

Parameter		Symbol	Min.	Typ.	Max.	Unit	Remark
Power Supply Voltage		VCC	3.15	3.3	3.6	V	
Ripple Voltage		V_{RP}	-	-	150	mV	
Rush Current		I_{RUSH}	-	-	3	A	Note2
Power Supply Current	White	-	-	1.22	1.5		Note3
	Black		-	0.51	0.7		Note3
	Vertical Stripe		-	0.82	1		Note3
Power Consumption		PLCD	-	4	5	W	Note4
LVDS differential input voltage		Vid	200	-	600	mV	Note5
LVDS common input voltage		Vic	1.0	1.2	1.4	V	Note5
Differential Input Voltage for LVDS Receiver Threshold		V_{IH}			100	mV	
		V_{IL}	-100			mV	
LVDS terminating resistor		R_T	-	100	-	ohm	

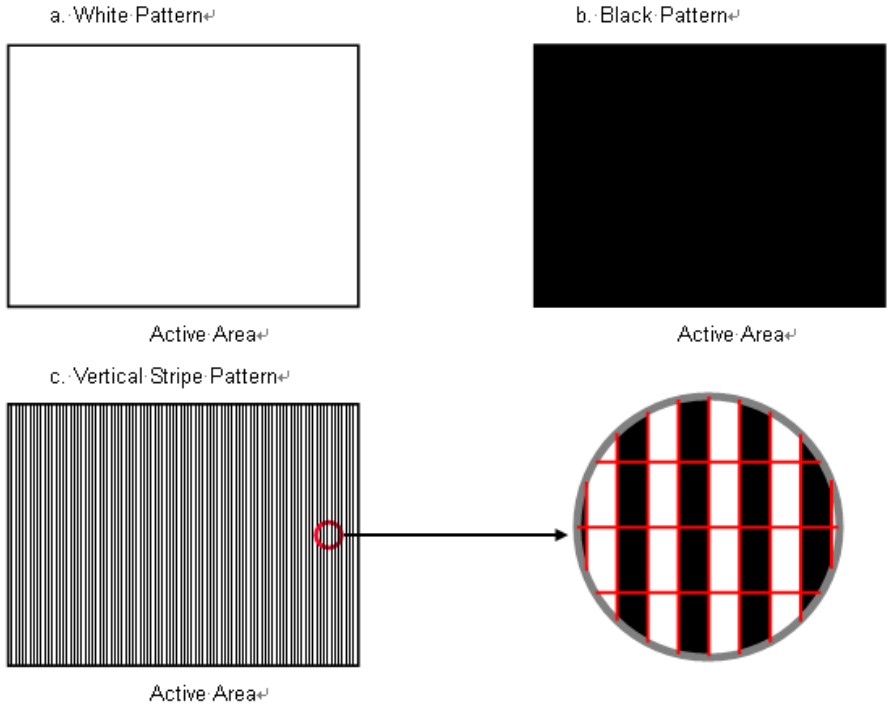
Note1: The ambient temperature is Ta = 25 ± 2℃.

Note2: Measurement Conditions:



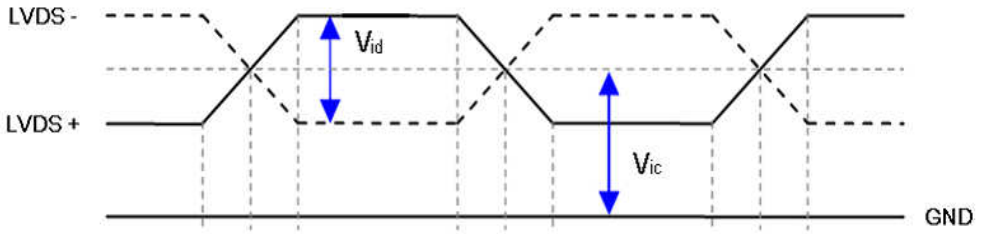


Note 3: The specified power supply current is under the conditions at Vcc = 3.3 V, Ta = 25 ± 2°C, Fr = 60Hz, whereas a power dissipation check pattern below is displayed.



Note 4: The power consumption is specified at the pattern with the maximum current.

Note 5: VID waveform condition

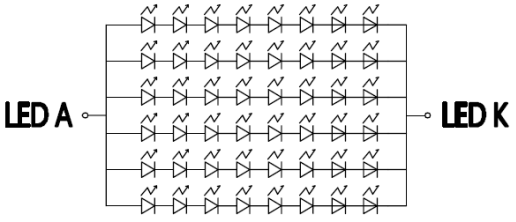


4.1.2 BACKLIGHT UNIT SPECIFICATION

Ta = 25°C

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
LED voltage	V_F	-	25.6	28	V	Note1/one circuit
LED current	I_F	-	420	-	mA	
LED dice Life Time			50,000		Hr	Note2

Note 1: LED Circuit Diagram



Backlight Circuit
One String style
Total 2 String

Note 2: The “LED life time” is defined as the module brightness decrease to 50% original brightness at IF=420mA & Ta=25°C

4.1.3 TOUCH MODULE ELETRONIC SPECIFICATION

Ta=25°C

Symbol	Description	Min	Typ.	Max	Unit	Notes
VCC_5V	Supply voltage	4.8	5	5.2	V	
IVCC_5V	Power Supply current	-	50	80	mA	VCC=5V

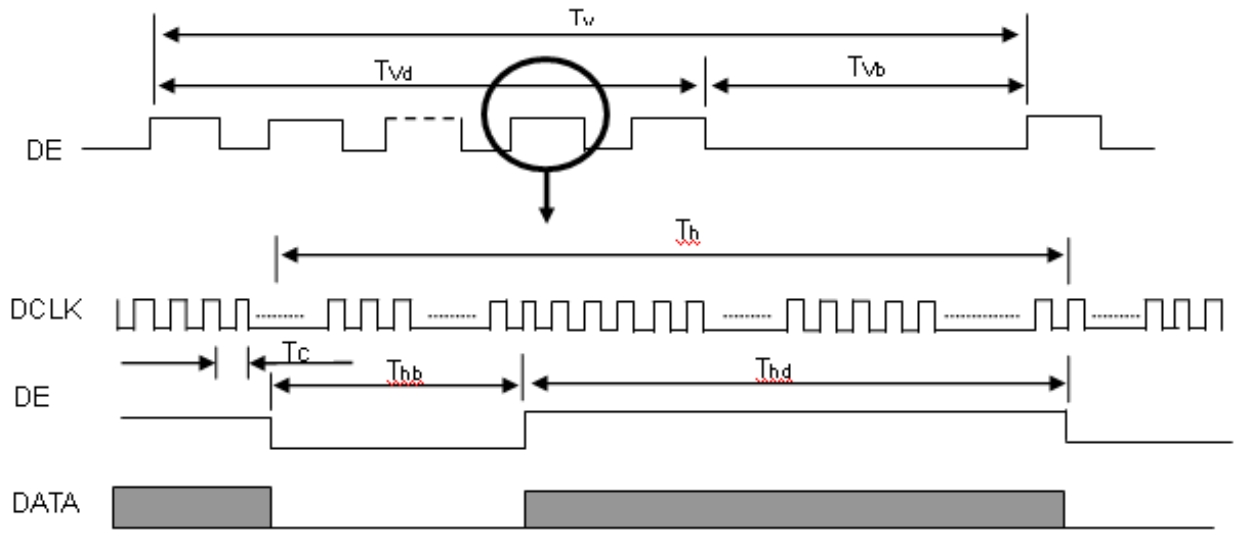
4.2 SIGNAL CHARACTERISTICS

4.2.1 INPUT SIGNAL TIMING

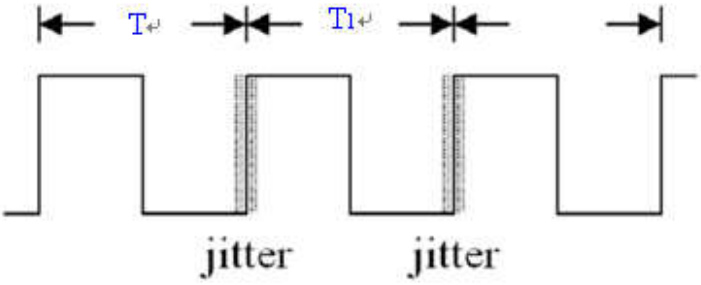
Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Remark
LVDS Clock	Frequency	Fc	60	70.93	73	MHz	-
	Period	Tc	-	14.1	-	ns	-
	Input cycle to cycle jitter	T_{rc}	-0.02* Tc	-	0.02* Tc		Note3
	Input clock to data skew	TLVCCS	-0.02* Tc	-	0.02* Tc		Note4
	Spread spectrum modulation range	Fclkin_mod	Fc*98%	-	Fc*102%	MHz	Note5
	Spread spectrum modulation frequency	F_{SSM}	-	-	200	KHz	
Vertical Display Term	Frame Rate	Fr	50	60	60	Hz	
	Total	Tv	1090	1110	1130	Th	Tv=Tvd+Tvb
	Active Display	Tvd	1080	1080	1080		-
	Blank	Tvb	Tv- Tvd	30	Tv- Tvd		-
Horizontal Display Term	Total	Th	1050	1065	1075	Tc	Th=Thd+Thb
	Active Display	Thd	960	960	960		-
	Blank	Thb	Th - Thd	105	Th - Thd		-

Note 1：Because this module is operated by DE only mode, Hsync and Vsync input signals are ignored.
Note 2：The Tv(Tvd+Tvb) must be integer, otherwise, this module would operate abnormally.

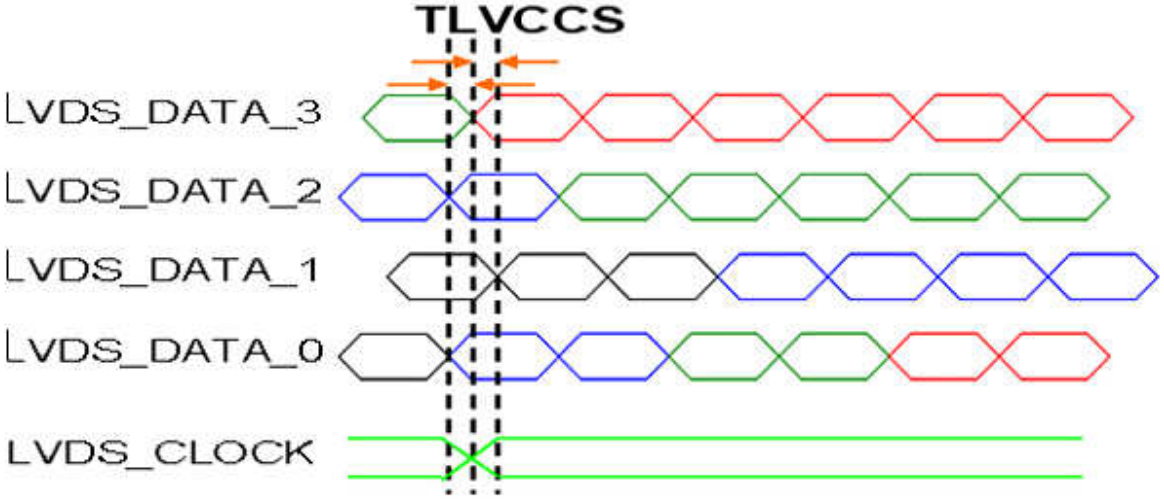
INPUT SIGNAL TIMING DIAGRAM



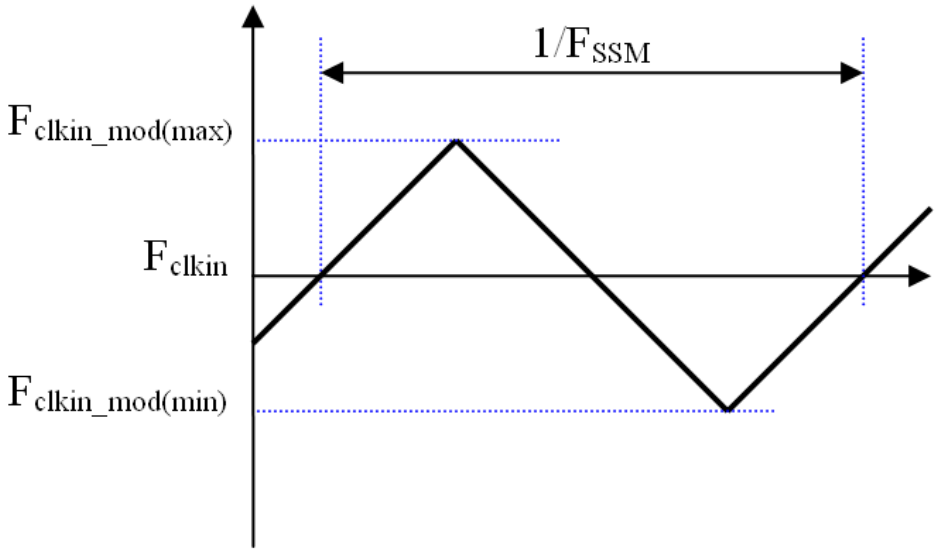
Note 3：The input clock cycle-to-cycle jitter is defined as below figures. Trcl = I T_1 – TI



Note 4：Input Clock to data skew is defined as below figures.



Note 5：The SSCG (Spread spectrum clock generator) is defined as below figures.



4.2.2 LVDS DATA MAPPING TABLE

LVDS Channel O0	LVDS output	D7	D6	D4	D3	D2	D1	D0
	Data order	OG0	OR5	OR4	OR3	OR2	OR1	OR0
LVDS Channel O1	LVDS output	D18	D15	D14	D13	D12	D9	D8
	Data order	OB1	OB0	OG5	OG4	OG3	OG2	OG1
LVDS Channel O2	LVDS output	D26	D25	D24	D22	D21	D20	D19
	Data order	DE	NA	NA	OB5	OB4	OB3	OB2
LVDS Channel O3	LVDS output	D23	D17	D16	D11	D10	D5	D27
	Data order	NA	OB7	OB6	OG7	OG6	OR7	OR6
LVDS Channel E0	LVDS output	D7	D6	D4	D3	D2	D1	D0
	Data order	EG0	ER5	ER4	ER3	ER2	ER1	ER0
LVDS Channel E1	LVDS output	D18	D15	D14	D13	D12	D9	D8
	Data order	EB1	EB0	EG5	EG4	EG3	EG2	EG1
LVDS Channel E2	LVDS output	D26	D25	D24	D22	D21	D20	D19
	Data order	DE	NA	NA	EB5	EB4	EB3	EB2
LVDS Channel E3	LVDS output	D23	D17	D16	D11	D10	D5	D27
	Data order	NA	EB7	EB6	EG7	EG6	ER7	ER6

4.2.3 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 8-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																						
		Red								Green								Blue							
		R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Red(253)	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
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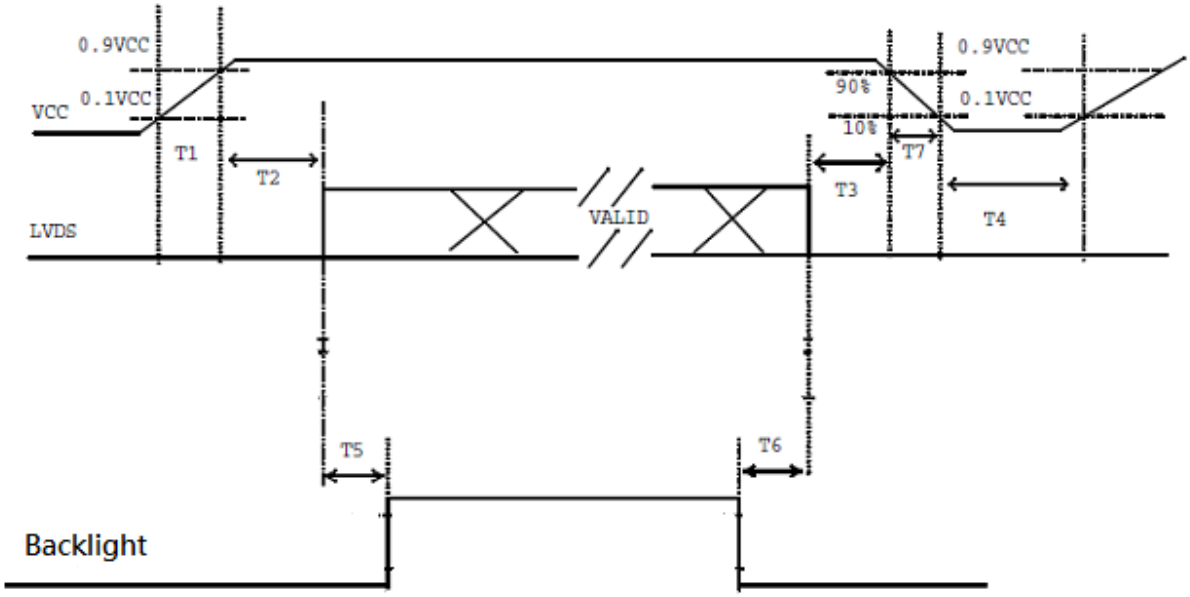
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Green(253)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0
	Green(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	Green(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray Scale Of Blue	Blue(0) / Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	Blue(253)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	1
	Blue(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	Blue(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Note：0: Low Level Voltage, 1: High Level Voltage

4.2.4 POWER ON/OFF SEQUENCE

The power sequence specifications are shown as the following table and diagram.



Parameter	Value			Units
	Min.	Typ.	Max.	
T1	0.5	-	10	ms
T2	0	-	50	ms
T3	0	-	50	ms
T4	500	-	-	ms
T5	500	-	-	ms
T6	250	-	-	ms
T7	10	-	100	ms

Note 1：When the backlight turns on before the LCD turns on, the display may momentarily become abnormal screen.

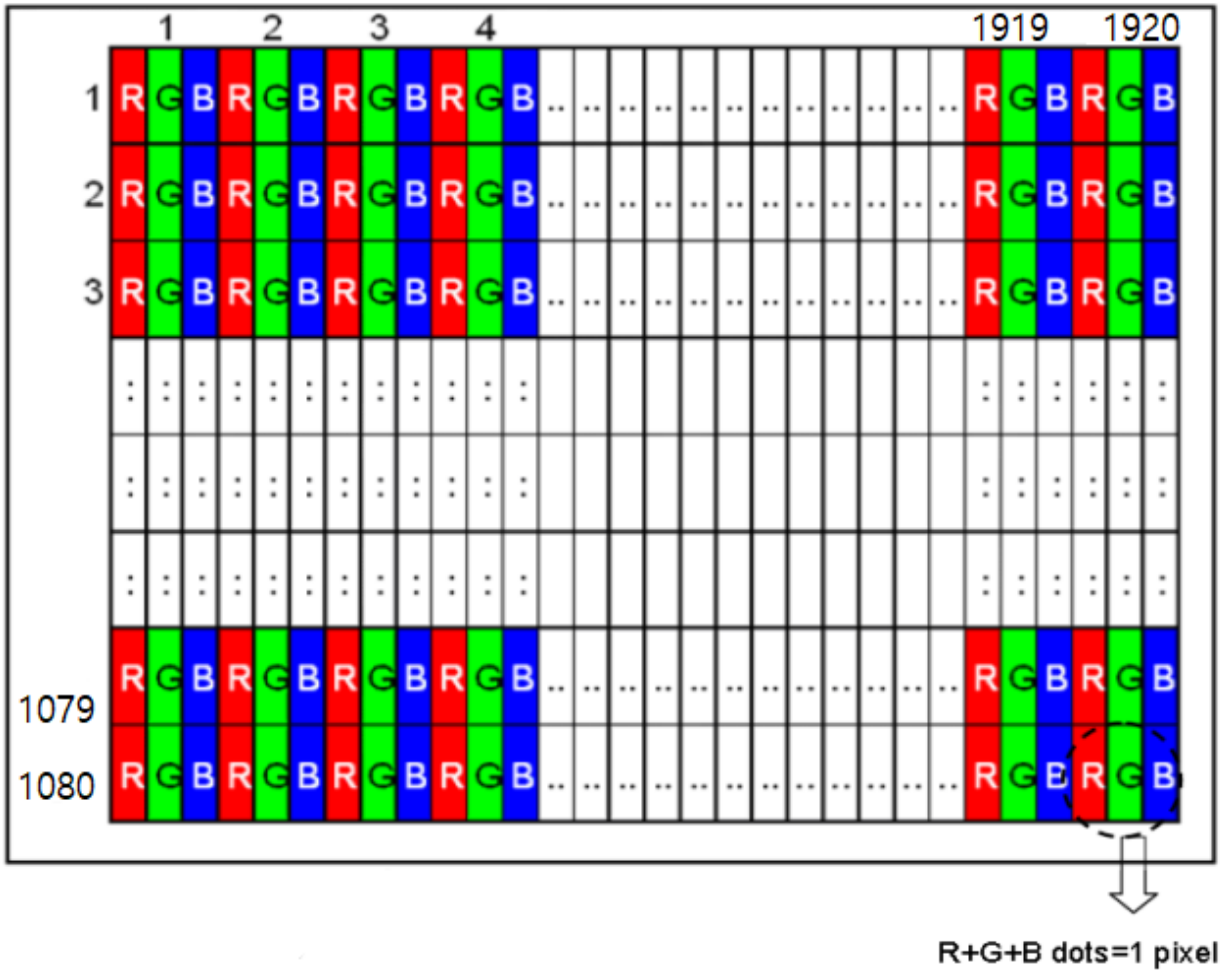
Note 2：In case of VCC = off level, please keep the level of input signals on the low or keep a high impedance

Note 3：T4 should be measured after the module has been fully discharged between power off and on period.

Note 4 : Interface signal shall not be kept at high impedance when the power is on.

Note 5 : There might be slight electronic noise when LCD is turned off (even backlight unit is also off). To avoid this symptom, we suggest "Vcc falling timing" to follow "T7 spec".

4.3 PIXEL FORMAT IMAGE



4.4 INTERFACE CONNECTIONS

4.4.1 LCM PIN FUNCTION

Pin No.	Symbol	Signal	Remarks
1	NC	Not connection, these pins should be open	
2	NC		
3	NC		
4	NC		
5	NC		
6	NC		
7	NC		
8	NC		
9	NC		
10	NC		
11	LCD_VCC	LCD logic and driver power 3.3V	
12	LCD_VCC		
13	LCD_VCC		
14	NC	Not connection, these pins should be open	
15	NC		
16	NC		
17	REV_SCAN	Low or NC: Normal Mode. High: Horizontal & Vertical Reverse Scan	Note1
18	RXO0-	Negative LVDS differential data input. Channel O0 (odd)	
19	RXO0+	Positive LVDS differential data input. Channel O0 (odd)	
20	RXO1-	Negative LVDS differential data input. Channel O1 (odd)	
21	RXO1+	Positive LVDS differential data input. Channel O1 (odd)	
22	RXO2-	Negative LVDS differential data input. Channel O2 (odd)	
23	RXO2+	Positive LVDS differential data input. Channel O2 (odd)	
24	LCD_GND	LCD logic and driver ground	
25	RX0C-	Negative LVDS differential clock input. (odd)	
26	RX0C+	Positive LVDS differential clock input. (odd)	
27	LCD_GND	LCD logic and driver ground	
28	RX03-	Negative LVDS differential data input. Channel O3(odd)	
29	RX03+	Positive LVDS differential data input. Channel O3 (odd)	
30	RXE0-	Negative LVDS differential data input. Channel E0 (even)	
31	RXE0+	Positive LVDS differential data input. Channel E0 (even)	
32	RXE1-	Negative LVDS differential data input. Channel E1 (even)	
33	RXE1+	Positive LVDS differential data input. Channel E1 (even)	
34	LCD_GND	LCD logic and driver ground	
35	RXE2-	Negative LVDS differential data input. Channel E2 (even)	
36	RXE2+	Positive LVDS differential data input. Channel E2 (even)	
37	RXEC-	Negative LVDS differential clock input. (even)	
38	RXEC+	Positive LVDS differential clock input. (even)	

39	RXE3-	Negative LVDS differential data input. Channel E3 (even)	
40	RXE3+	Positive LVDS differential data input. Channel E3 (even)	

Note 1: SCANNING DIRECTION (PCBA on the bottom side)
The following figures show the image see from the front view.

REV_SCAN = Low or NC



REV_SCAN = High



4.4.2 CTP PIN FUNTION

NO.	Name	Description
1	GND	Ground
2	VCC_5V	Power Supply Voltage
3	GND	Ground
4	D+	USB D+
5	D-	USB D-

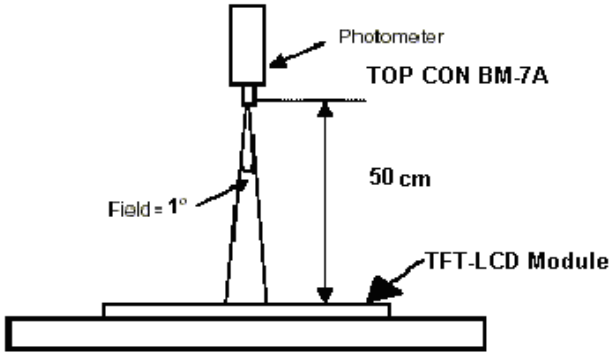
5. OPTICAL SPECIFICATIONS

5.1 OPTICAL CHARACTERISTICS

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remarks
Viewing Angle	Horizontal	θ_x+	Center CR≥10	80	85	--	deg	Note 1,4
		θ_x-		80	85	--		
	Vertical	θ_Y+		80	85	--		
		θ_Y-		80	85	--		
Contrast Ratio		CR	at optimized viewing angle	600	800	--		Note 1,3
Response time	White to black	Ton	Center θx=θy =0°	-	13	18	ms	Note 1,6
	Black to white	Toff		-	12	17		
Uniformity		B-uni	θx=θy =0°	70	--	--	%	Note1,5
Brightness		L	θx=θy =0°	800	1000	--	cd/㎡	Note 1,2
Chromaticity		X_W	Center θx=θy =0°	Typ.-0.05	0.313	Typ.+0.05	--	Note 7
		Y_W			0.329			

The following optical specifications shall be measured in a darkroom or equivalent state (ambient luminance ≤1 lux, and at room temperature). The operation temperature is 25°C±2°C and LED Backlight Current=420mA. The measurement method is shown in Note1.

Note1: The method of optical measurement:

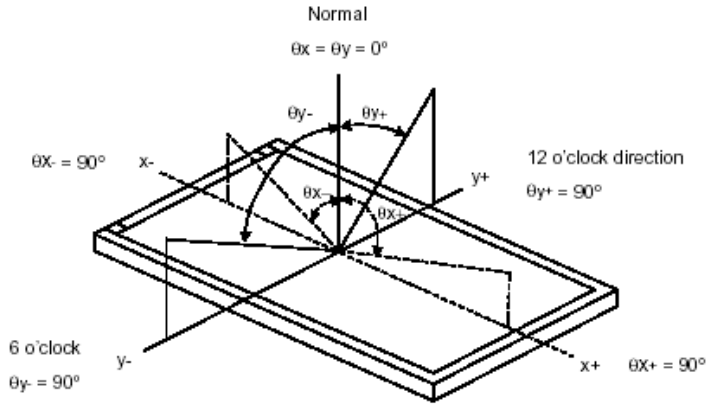


Note2: Measured at the center area of the panel and at the viewing angle of the θx=θy =0°

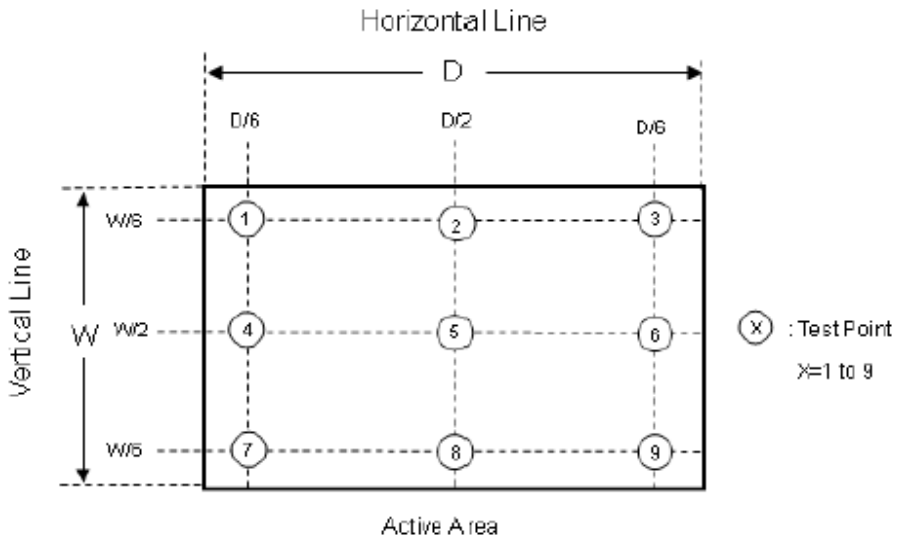
Note3: Definition of Contrast Ratio (CR):

$$CR = \frac{\text{Luminance with all pixels in white state}}{\text{Luminance with all pixels in Black state}}$$

Note4: Definition of Viewing Angle



Note 5: Definition of Brightness Uniformity (B-uni):

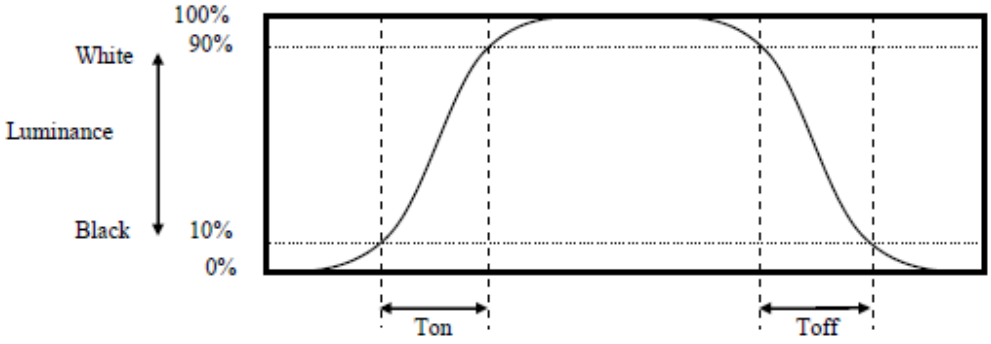


Measure the luminance of gray level 255 at 9 points

δW = (Minimum [L (1) ~ L (9)] / Maximum [L (1) ~ L (9)]) *100%

Note6: Definition of Response Time:

Response time is measured, the luminance changes from " black " to " white ", or " white " to " black " on the same screen point, by photo-detector. Ton is the time it takes the luminance change from 10% up to 90%. Also Toff is the time it takes the luminance change from 90% down to 10% (See the following diagram.).

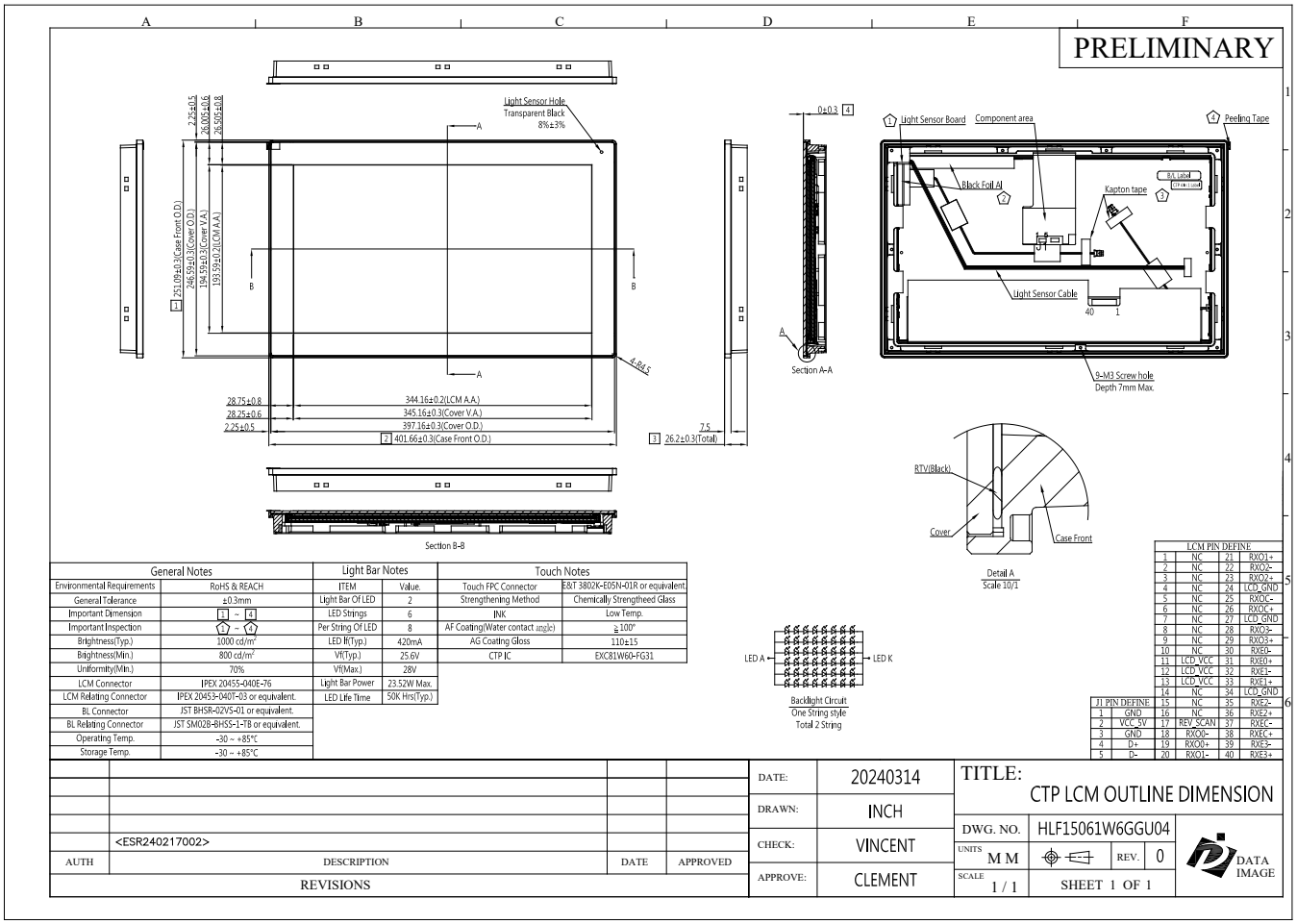


Note 7: Definition of Chromaticity:

The color coordinates (x_W,y_W)is obtained with all pixels in the viewing field at white.

6. MECHANICAL SPECIFICATIONS

6.1 OUTLINE DRAWING



General Notes	
Environmental Requirements	RoHS & REACH
General Tolerance	±0.3mm
Important Dimension	3 ~ 4
Important Inspection	1 ~ 4
Brightness(Typ.)	1000 cd/m²
Brightness(Min.)	800 cd/m²
Uniformity(Min.)	70%
LCM Connector	IPEX 20455-040E-76
LCM Relating Connector	IPEX 20453-040T-03 or equivalent.
BL Connector	JST BHSR-02VS-01 or equivalent.
BL Relating Connector	JST SM02B-BHSS-1-TB or equivalent.
Operating Temp.	-30 ~ +85℃
Storage Temp.	-30 ~ +85℃

Light Bar Notes	
ITEM	Value.
Light Bar Of LED	2
LED Strings	6
Per String Of LED	8
LED If(Typ.)	420mA
Vf(Typ.)	25.6V
Vf(Max.)	28V
Light Bar Power	23.52W Max.
LED Life Time	50K Hrs(Typ.)

Touch Notes	
Touch FPC Connector	E&T 3802K-E05N-01R or equivalent
Strengthening Method	Chemically Strengtheed Glass
INK	Low Temp.
AF Coating(Water contact angle)	≥ 100°
AG Coating Gloss	110±15
CTP IC	EXC81W60-FG31

LCM PIN DEFINE					
1	NC	21	RXO1+		
2	NC	22	RXO2-		
3	NC	23	RXO2+		
4	NC	24	LCD_GND		
5	NC	25	RXOC-		
6	NC	26	RXOC+		
7	NC	27	LCD_GND		
8	NC	28	RXO3-		
9	NC	29	RXO3+		
10	NC	30	RXE0-		
11	LCD_VCC	31	RXE0+		
12	LCD_VCC	32	RXE1-		
13	LCD_VCC	33	RXE1+		
14	NC	34	LCD_GND		
15	NC	35	RXE2-		
16	NC	36	RXE2+		
17	REV_SCAN	37	RXEC-		
18	RXO0-	38	RXEC+		
19	RXO0+	39	RXE3-		
20	RXO1-	40	RXE3+		

J1 PIN DEFINE	
1	GND
2	VCC_5V
3	GND
4	D+
5	D-

AUTH	DESCRIPTION	DATE	APPROVED
	<ESR240217002>		

REVISIONS

DATE:	20240314
DRAWN:	INCH
CHECK:	VINCENT
APPROVE:	CLEMENT

TITLE: CTP LCM OUTLINE DIMENSION

DWG. NO.	HLF15061W6GGU04		
UNITS M M		REV.	0
SCALE 1 / 1	SHEET 1 OF 1		

DATA IMAGE



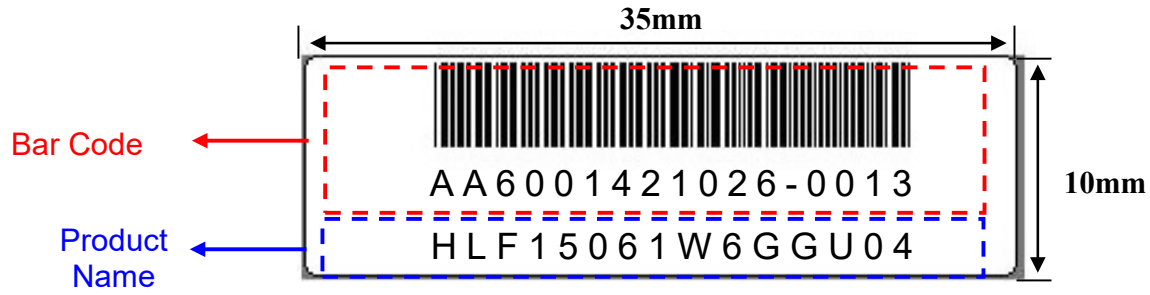
7. RELIABILITY TEST ITEM

Reliability Test Item & Level			Remark
No.	Test Item	Test Level	
1	High Temperature Storage Test	Ta=85°C,240hrs	IEC60068-2-2
2	Low Temperature Storage Test	Ta=-30°C,240hrs	IEC60068-2-1
3	High Temperature Operation Test	Ta=85°C,240hrs	IEC60068-2-2
4	Low Temperature Operation Test	Ta=-30°C,240hrs	IEC60068-2-1
5	High Temperature and High Humidity (No operation)	T=60°C,60%RH,240hrs	IEC60068-2-3
6	Thermal Cycling Test (No operation)	-20°C → +25°C → +60°C ,100 Cycles 30 min 5 min 30 min	IEC60068-2-14
7	Vibration test (Package)	Frequency:10~55HZ Amplitude:1.5mm Sweep time:11min Test period:6Cycles for each direction of X,Y,Z	IEC60068-2-6
8	Drop test (Package)	Height :60cm 1 conner,3edges,6surfaces	IEC60068-2-32
9	Electrostatic Discharge Test	Location: LCM/TP surface Condition:150pf 330Ω Contact +/- 8kV Air +/-15kV Criteria: Class C	IEC61000-4-2

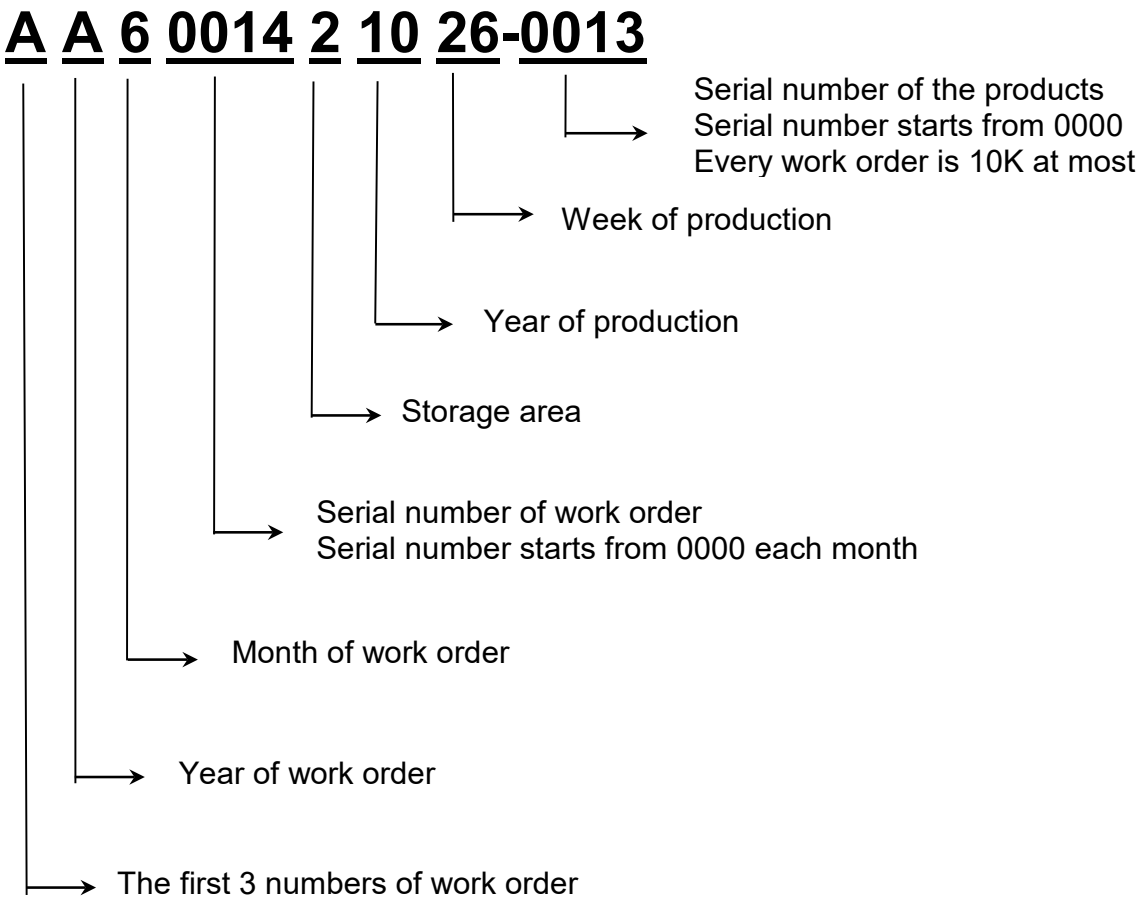
8. LCM PRODUCT LABEL DEFINE

8.1 SHIPPING LABEL

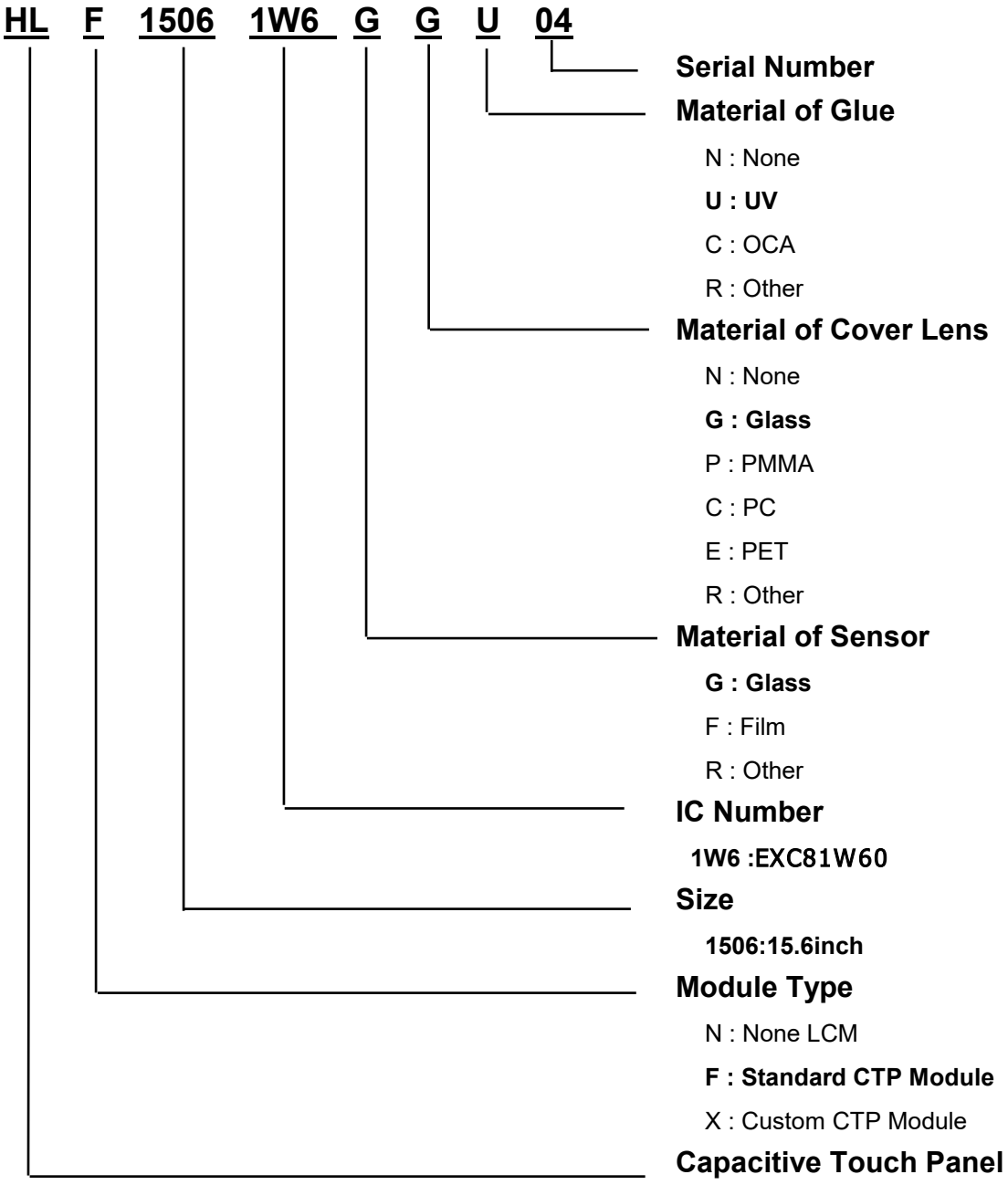
Product Label style:



BarCode Define:



Product Name Define:



8.2 CARTON PACKAGE
TBD

8.3 PACKAGE LABEL STYLE
TBD

8.4 CONTENT
TBD

9.Precaution

9.1 HANDLING PRECAUTIONS

(1). The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.

(2). While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.

(3). Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.

(4). Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.

(5). If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth.

Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or

Methyl chloride. It might permanently damage the polarizer due to chemical reaction.

(6). Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.

(7). If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.

(8). Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.

(9). Do not disassemble the module.

(10). Do not pull or fold the LED wire.

(11). Pins of I/F connector should not be touched directly with bare hands.

9.2 STORAGE PRECAUTIONS

(1). High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.

(2). It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.

(3). It may reduce the display quality if the ambient temperature is lower than 10 ºC. For

example, the response time will become slowly, and the starting voltage of LED will be

higher than the room temperature.

9.3 OPERATION PRECAUTIONS

(1). Do not pull the I/F connector in or out while the module is operating.

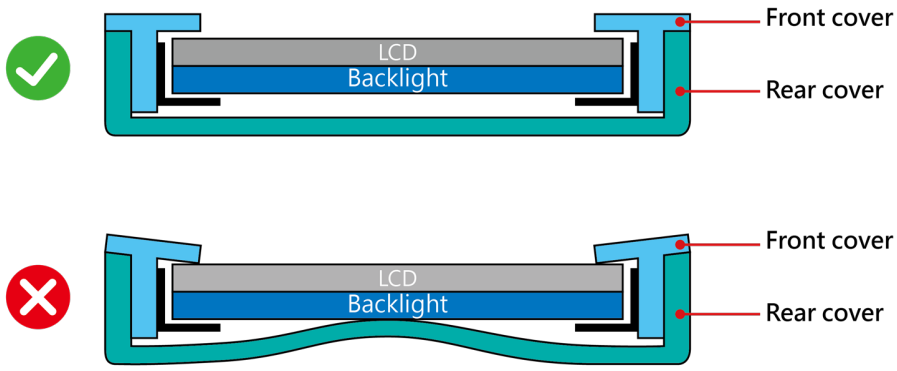
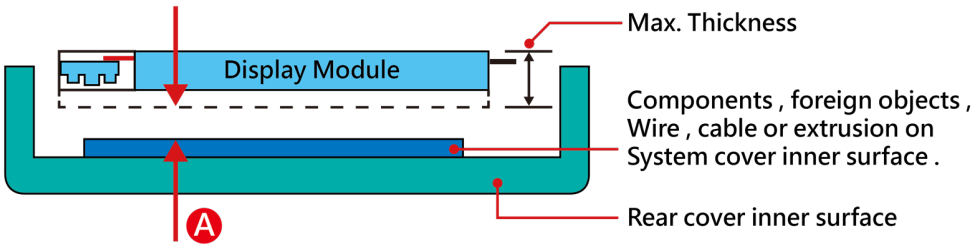
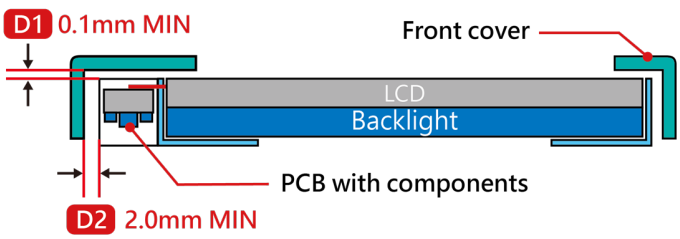
(2). Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.

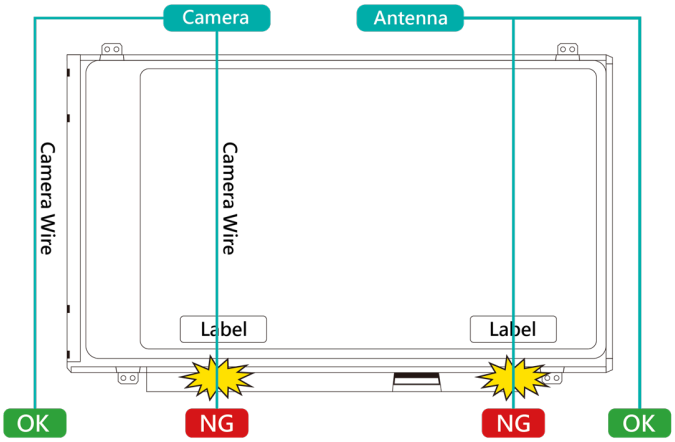
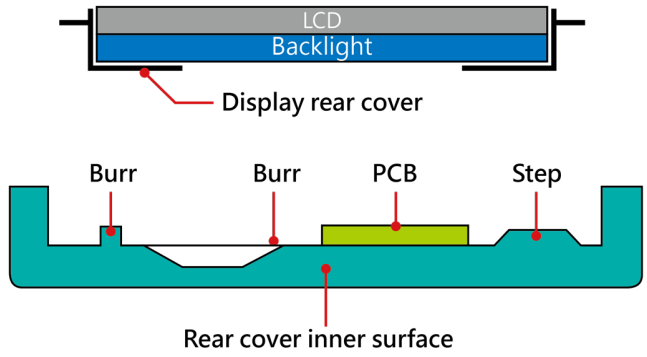
(3). The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with converter. Do not disassemble the module or insert anything into the Backlight unit.

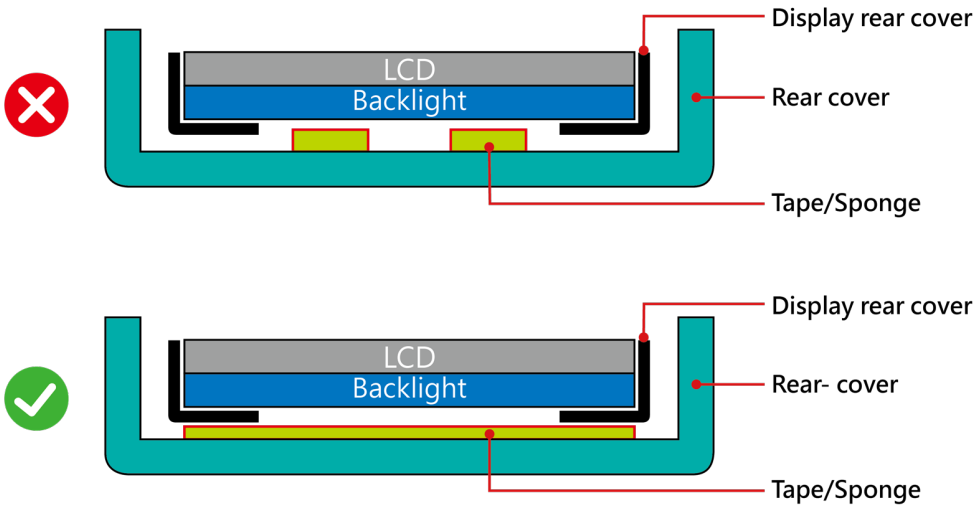
(4). LIMITED WARRANTY

Unless otherwise agreed between DATA IMAGE and customer, DATA IMAGE will replace or repair any of its LCD and LCM which is found to be defective electrically and visually when inspected in accordance with DATA IMAGE acceptance standards, for a period on one year from date of shipment. Confirmation of such date shall be based on freight documents. The warranty liability of DATA IMAGE is limited to repair and/or replacement on the terms set forth above. DATA IMAGE will not responsible for any subsequent or consequential events

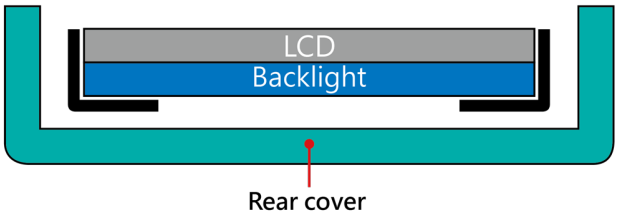
Appendix. Covers Design Guideline

A.	**Permanent deformation of front/rear covers after reliability test**
	
Definition	Front/rear covers may deform during reliability test. Permanent deformation of front/rear covers after reliability test should not interfere with display. Because it may cause issues such as pooling, abnormal display, white spot, and also cell crack.
B.	**Design gap A between display and any components on rear cover**
	
Definition	Gap A between display's maximum thickness boundary and rear cover inner surface components such as wire, cable, extrusion is needed for preventing from backpack or pogo test fail. Because zero gap or interference may cause stress concentration. Issues such as pooling, abnormal display, white spot, white spot and cell crack may occur. Flatness of display and rear cover should be taken into account for gap design.
C.	**Design gap D1 & D2 between front cover and PCB assembly**
	

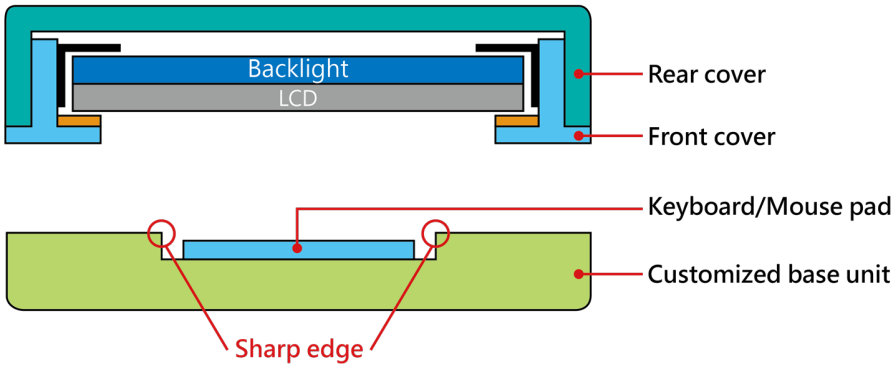
Definition	Gap D1 & D2 between front cover and LCD & front cover and PCBA are needed to prevent pooling or glass broken. Zero gap or interference such as burr and warpage from mold frame may cause pooling issue near front cover opening edge. This phenomenon is obvious during swing test, hinge test, knock test or during pooling inspection procedure. To remain sufficient gap, design with system rib higher than maximum display thickness is recommended.
D.	**Interference examination of camera's and antenna's cable**
	
Definition	Camera's and antenna's cable should not overlap with panel outline. Because issue such as abnormal display and white spot after backpack test, hinge test, twist test or pogo test may occur.
E.	**Rear cover inner surface examination**
	
Definition	Burr at logo edge, steps, protrusions or PCB may cause stress concentration. Whiter spot or glass broken issue may occur during reliability test.
F.	**Tape/sponge design on rear cover inner surface**



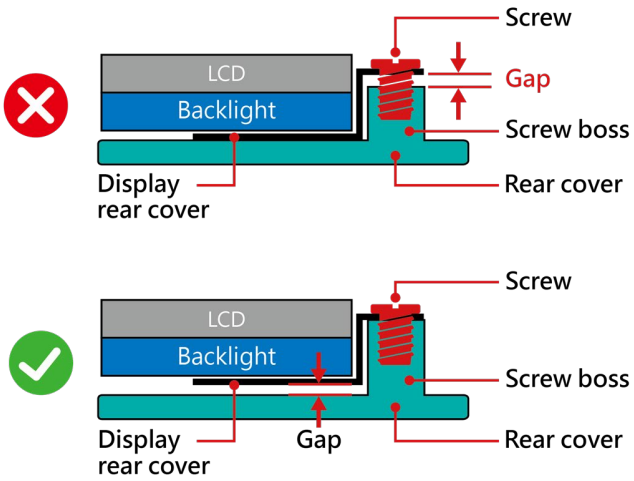
Definition	To prevent abnormal display and white spot after scuffing test, hinge test, pogo test, backpack test, tape/sponge should be well covered under rear cover. Because tape/sponge in separate location may act as pressure concentration location.
G.	**Material used for rear cover**



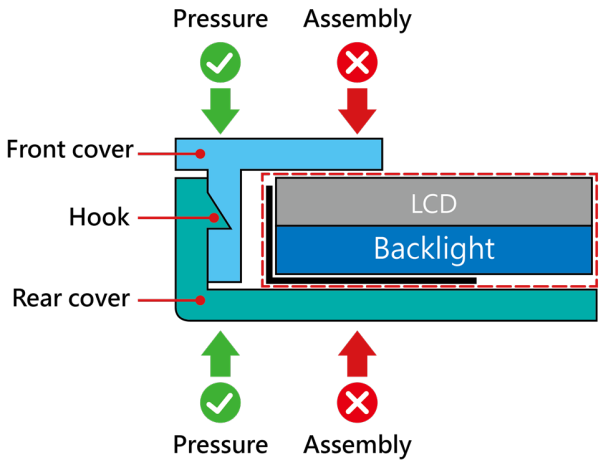
Definition	Rear cover material with high rigidity is needed to resist deformation during scuffing test, hinge test, pogo test or backpack test. Abnormal display, white spot, pooling issue may occur if low rigidity material is used. Pooling issue may occur because screw's boss positioning for module's bracket are deformed during open-close test. Solid structure design of system rear cover may also influence the rigidity of rear cover. The deformation of rear cover should not caused interference.
H.	**Customized base unit design near keyboard and mouse pad**



Definition	To prevent abnormal display and white spot after Scuffing test, hinge test, pogo test, backpack test, sharp edge design in keyboard surface may damage display during the test. We suggest to use slope edge design or to reduce the thickness difference of keyboard/mouse pad from the nearby surface.
I.	**Screw boss height design**

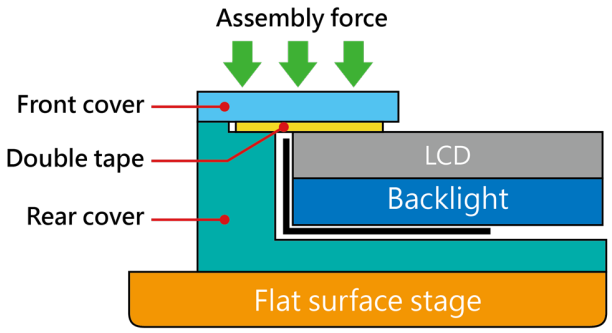


Definition	Screw boss height should be designed with respect to the height of bracket bottom surface to display bottom surface with flatness change of display it set. Because gap will exist between screw boss and bracket, if the screw boss height is smaller. As result while fastening screw, bracket will deformed and pooling issue may occur.
J.	**Assembly SOP examination for front cover with Hook design**



Definition	To prevent display crack during front cover assembly process with hook design, it is not recommended to press display or any location that related directly to the display.

L.	**Assembly SOP examination for front cover with Double tape design**



Definition	To prevent display crack during system front cover assembly process with double tape design, it is only allowed to give slight pressure (MAX 3 Kgf/50mm2) with large contact area. This can help to distribute the stress and prevent stress concentration. We also suggest putting the system on a flat surface stage to prevent unequal stress distribution during the assembly.