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工程課
2024-12-27
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旺玖科技開發股份有限公司

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NuMicro® Family

Arm® Cortex®-M4-based Microcontroller

M480 Series
Datasheet

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1 GENERAL DESCRIPTION

The NuMicro® M480 series microcontroller is embedded with Arm® Cortex®-M4F core with hardware cryptography which supports DSP instruction and integrated floating-point unit. The M480 series consists of six sub-series according to characteristics and applications. The M480 series supports Flash size up to 2560 KB and SRAM size up to 160 KB. The operating frequency is up to 192 MHz with 175/130 µA/ MHz dynamic power consumption and the standby current can be lower to 1 µA.

The M480 series supports secure boot functionality, which provides a constant digital signature of system software for identification during boot up to protect the integrity of Flash content from attack. The embedded hardware cryptography engine provides fast and easy encryption, decryption, ID certification, private key and public key features. Additionally, the M480 series supports 10/100Mbps Ethernet RMII, high-speed USB 2.0 OTG, dual 12-bit 5 MSPS SAR ADC, camera interface and versatile peripherals, eligible for IoT, industrial automation, sensor network, automotive device, RC aircraft, smart home, network gateway and consumer electronics.

The NuMicro® M480 series consists of six sub-series:

- NuMicro® M481 Base series: high performance, low power consumption, versatile high speed UART/SPI/I2C/PWM peripherals, eligible for data collector.
- NuMicro® M482 USB FS OTG series: Integrated USB 2.0 full speed interface with on-chip OTG PHY, eligible for gaming or PC accessories.
- NuMicro® M483 CAN series: Integrated 2 or 3 sets of CAN 2.0B interfaces, 2 sets of USB 2.0 interfaces, dual ADC and up to 9 sets of UART interfaces, eligible for IoV and industrial control
- NuMicro® M484 USB HS OTG series: Integrated 2 sets of USB 2.0 interface with op-chip full speed and high-speed OTG PHY, eligible for data concentrator of USB sensor.
- NuMicro® M485 Crypto series: Integrated hardware cryptography engine and random number generator for randomly fabricating the key for data encryption/decryption and certification, eligible for fingerprint module, smart payment and secure USB device.
- NuMicro® M487 Ethernet series: Integrated 10/100Mbps Ethernet MAC with industrial standard RMII interface for quickly implementing the network connection, eligible for industrial IoT gateway, UART-to-Ethernet converter, industrial automation, smart home, etc.

Series	USB Full Speed	USB High Speed	CAN 2.0B	Cryptography	Ethernet
M481					
M482	√				
M483	√	√	√	√	
M484	√	√			
M485	√	√		√	
M487	√	√	√	√	√

2 FEATURES

Core and System	
Arm® Cortex®-M4F	• Arm® Cortex®-M4F core, running up to 192 MHz • Built-in Memory Protection Unit (MPU) • Built-in Nested Vectored Interrupt Controller (NVIC) • Hardware IEEE 754 compliant Floating-point Unit (FPU) • DSP extension with hardware divider and single-cycle 32-bit hardware multiplier • 24-bit system tick timer • Programmble and maskable interrupt • Low Power Sleep mode by WFI and WFE instructions
Brown-out Detector (BOD)	• Eight-level BOD with brown-out interrupt and reset option. (3.0V/2.8V/2.6V/2.4V/2.2V/2.0V/1.8V/1.6V)
Low Voltage Reset (LVR)	• LVR with 1.5V threshold voltage level.
Security	• 96-bit Unique ID (UID). • 128-bit Unique Customer ID (UCID). • One built-in temperature sensor with 1°C resolution.
Memories	
Boot Loader (M48xGC/M48xE8)	• Factory pre-loaded 8 KB mask ROM for secure boot procedure • Uses ECC to validate data in APROM, LDROM and external SPI Flash
Flash	• Dual bank 512/256 KB on-chip Application ROM (APROM) for Over-The-Air (OTA) upgrade. (M48xID) • Dual bank 512 KB on-chip Application ROM (APROM) for Over-The-Air (OTA) upgrade. (M487KMCAN) • Single bank 256/128 KB on-chip Application ROM (APROM). (M48xGC/M48xE8) • Four eXecute-Only-Memory regions for data protection. (M48xGC/M48xE8) • 192 MHz maximum frequency, with performance at zero wait cycle in continuous address read access • 4 KB on-chip Flash for user-defined loader (LDROM) • 8 KB non-readble Key Protection ROM (KPROM) for firmware programming protection • 4 KB non-readble Security Protection ROM (SPROM) for intelectual property protection • 3 KB One Time Programable (OTP) ROM for data security.

	(M48xID/M487KMCAN) • 2 KB One Time Programable (OTP) ROM for data security. (M48xGC/M48xE8) • All on-chip Flash support 4 KB page erase • Fast Flash programming verification with CRC • On-chip Flash programming with In-Chip Programming (ICP), In-System Programming (ISP) and In-Application Programming (IAP) capabilities • Configurable boot up sources including boot loader, user-defined loader (LDROM) or Application ROM (APROM) • Data Flash with configurable memory size • 2-wired ICP Flash updating through SWD interface • 32-bit/64-bit and multi-word Flash programming function
SRAM	• Up to 160 KB on-chip SRAM includes: (M48xID/ M487KMCAN) – 32 KB SRAM located in bank 0 that supports hardware parity check and retenion mode; Exception (NMI) generated upon a parity check error – 96/32 KB SRAM located in bank 1 – 32 KB SRAM located in bank 2 that can be used as cache for external SPI Flash memory • Up to 128/64 KB on-chip SRAM includes: (M48xGC/M48xE8) – 32 KB SRAM located in bank 0 that supports hardware parity check and retenion mode; Exception (NMI) generated upon a parity check error – 96/32 KB SRAM located in bank 1 • Byte-, half-word- and word-access • PDMA operation
Cyclic Redundancy Calculation (CRC)	• Supports CRC-CCITT, CRC-8, CRC-16 and CRC-32 polynomials • Programmable initial value and seed value • Programmable order reverse setting and one's complement setting for input data and CRC checksum • 8-bit, 16-bit, and 32-bit data width • 8-bit write mode with 1-AHB clock cycle operation • 16-bit write mode with 2-AHB clock cycle operation • 32-bit write mode with 4-AHB clock cycle operation • Uses DMA to write data with performing CRC operation
Peripheral DMA (PDMA)	• 16 independent and configurable channels for automatic data transfer between memories and peripherals • Basic and Scatter-Gather transfer modes • Each channel supports circular buffer management using Scatter-Gather Transfer mode • Stride function for rectangle image data movement

	• Fixed-priority and Round-robin priorities modes • Single and burst transfer types • Byte-, half-word- and word tranfer unit with count up to 65536 • Incremental or fixed source and destination address
Clocks	
External Clock Source	• 4~24 MHz High-speed eXternal crystal oscillator (HXT) for precise timing operation • 32.7688 kHz Low-speed eXternal crystal oscillator (LXT) for RTC function and low-power system operation • Supports clock failure detection for external crystal oscillators and exception generatation (NMI)
Internal Clock Source	• 48 MHz High-speed Internal RC oscillator (HIRC48M) dedicated for crystal-less USB. (M48xGC/M48xE8) • 12 MHz High-speed Internal RC oscillator (HIRC) trimmed to 2% accuracy that can optionally be used as a system clock • 10 kHz Low-speed Internal RC oscillator (LIRC) for watchdog timer and wakeup operation • Up to 480 MHz on-chip PLL, sourced from HIRC or HXT, allows CPU operation up to the maximum CPU frequency without the need for a high-frequency crystal
Real-Time Clock (RTC)	• Real-Time Clock with a separate power domain and independent V_{BAT} pin. (M48xGC/M48xE8) • The RTC clock source includes Low-speed external crystal oscillator (LXT) • The RTC block includes 80 bytes of battery-powered backup registers, which can be cleared by tamper pins. (M48xID/M487KMCAN) • The RTC block includes 20 bytes of battery-powered backup registers, which can be cleared by tamper pins. (M48xGC/M48xE8) • Supports 6 static and dynamic tamper pins • Able to wake up CPU from any reduced power mode • Supports ±5ppm within 5 seconds software clock accuracy compensation • Supports Alarm registers (second, minute, hour, day, month, year) • Supports RTC Time Tick and Alarm Match interrupt • Automatic leap year recognition • Supports 1 Hz clock output for calibration
Timers	
32-bit Timer	**TIMER** • Four sets of 32-bit timers with 24-bit up counter and one 8-bit

	pre-scale counter from independent clock source • One-shot, Periodic, Toggle and Continuous Counting operation modes • Supports event counting function to count the event from external pins • Supports external capture pin for interval measurement and resetting 24-bit up counter • Supports chip wake-up function, if a timer interrupt signal is generated **PWM** • Eight 16-bit PWM counters with 12-bit clock prescale • Supports 12-bit deadband (dead time) • Up, down or up-down PWM counter type • Supports brake function • Supports mask function and tri-state output for each PWM channel
Enhanced PWM (EPWM)	• Twelve 16-bit counters with 12-bit clock prescale for twelve 192 MHz PWM output channels • Up to 12 independent input capture channels with 16-bit resolution counter • Supports dead time with maximum divided 12-bit prescale • Up, down or up-down PWM counter type • Supports complementary mode for 3 complementary paired PWM output channels • Synchronous function for phase control • Counter synchronous start function • Brake function with auto recovery mechanism • Mask function and tri-state output for each PWM channel • Trigger EADC or DAC to start conversion immediately. • Trigger EADC to start conversion after a short delay. (M48xGC/M48xE8) • Hardware short-circuit output check. (M48xGC/M48xE8)
Basic PWM (BPWM)	• Two 16-bit counters with 12-bit clock prescale for twelve 192 MHz PWM output channels. • Up to 6 independent input capture channels with 16-bit resolution counter • Up, down or up-down PWM counter type • Counter synchronous start function • Mask function and tri-state output for each PWM channel • Able to trigger EADC to start conversion.
Watchdog	• 18-bit free running up counter for WDT time-out interval • Supports multiple clock sources from LIRC (default selection),

	HCLK/2048 and LXT with 8 selectable time-out period • Able to wake up system from Power-down or Idle mode • Time-out event to trigger interrupt or reset system • Supports four WDT reset delay periods, including 1026, 130, 18 or 3 WDT_CLK reset delay period • Configured to force WDT enabled on chip power-on or reset.
Window Watchdog	• Clock sourced from HCLK/2048 or LIRC; the window set by 6-bit counter with 11-bit prescale • Suspended in Idle/Power-down mode
Analog Interfaces	
Enhanced Analog-to-Digital Converter (EADC) **(M48xID/M487KMCAN)**	• One 12-bit, 19-ch 5 MSPS SAR EADC with up to 16 single-ended input channels or 8 differential input pairs; 10-bit accuracy is guaranteed. • Three internal channels for V_{BAT}, band-gap VBG input and Temperature sensor input • Supports external V_{REF} pin or internal reference voltage V_{REF}: 1.6V, 2.0V, 2.5V, and 3.0V. • Two power saving modes: Power-down mode and Standby mode • Supports calibration capability. • Analog-to-Digital conversion can be triggered by software enable, external pin, Timer 0~3 overflow pulse trigger or PWM trigger. • Configurable EADC sampling time. • Double data buffers for sample module 0~3. • PDMA operation.
Enhanced Analog-to-Digital Converter (EADC) **(M48xGC/M48xE8)**	• One 12-bit, 19-ch 5 MSPS SAR EADC with up to 16 single-ended input channels or 8 differential input pairs; 10-bit accuracy is guaranteed. • One 12-bit, 16-ch 5 MSPS SAR EADC with up to 16 single-ended input channels or 8 differential input pairs; 10-bit accuracy is guaranteed. • Three internal channels for V_{BAT}, band-gap VBG input and Temperature sensor input • Supports external V_{REF} pin or internal reference voltage V_{REF}: 1.6V, 2.0V, 2.5V, and 3.0V. • Two power saving modes: Power-down mode and Standby mode • Supports calibration capability. • Analog-to-Digital conversion can be triggered by software enable, external pin, Timer 0~3 overflow pulse trigger or PWM trigger. • Configurable EADC sampling time. • Double data buffers for sample module 0~3.

	• Supports simultaneously trigger mode. • PDMA operation.
Digital-to-Analog Converter (DAC)	• 12-bit, 1 MSPS voltage type DAC with 8-bit mode and 8μs rail-to-rail settle time. • Maximum output voltage AV_{DD} -0.2V at buffer mode • Digital-to-Analog conversion triggered by Timer0~3, EPWM0, EPWM1, external trigger pin to start DAC conversion or software. • Supports group mode for synchronized data update of two DACs. (M48xID/M487KMCAN) • PDMA operation
Analog Comparator (ACMP)	• Two rail-to-rail Analog Comparators. • Supports four multiplexed I/O pins at positive input. • Supports I/O pins, band-gap, DAC, and 16-level Voltage divider from AV_{DD} or V_{REF} at negative input • Supports four programmable propagation speeds for power saving • Supports wake up from Power-down by interrput • Supports triggers for brake events and cycle-by-cycle control for PWM • Supports window compare mode and window latch mode. • Supports programmable hysteresis window: 0mV, 10mV, 20mV and 30mV
Operational Amplifier (OPA) **(M48xID/M487KMCAN)**	• Three Operational Amplifiers with 0~AV_{DD} input voltage range. • OPA schmitt trigger buffer output used as the interrupt source of comparator.
Communication Interfaces	
Low-power UART	• Low-power UARTs with up to 17.45 MHz baud rate. • Auto-Baud Rate measurement and baud rate compensation function. • Supports low power UART (LPUART): baud rate clock from LXT(32.768 kHz) with 9600bps in Power-down mode even system clock is stopped. • 16-byte FIFOs with programmable level trigger • Auto flow control (nCTS and nRTS) • Supports IrDA (SIR) function • Supports LIN function on UART0 and UART1 • Supports RS-485 9-bit mode and direction control • Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function in idle mode. • Supports hardware or software enables to program nRTS pin to

	control RS-485 transmission direction • Supports wake-up function • 8-bit receiver FIFO time-out detection function • Supports break error, frame error, parity error and receive/transmit FIFO overflow detection function • PDMA operation.
Smart Card Interface	• ISO-7816-3 which are compliant with ISO-7816-3 T=0, T=1 • Supports full duplex UART function. • 4-byte FIFOs with programmable level trigger • Programmable guard time selection (11 ETU ~ 266 ETU) • One 24-bit and two 8 bit time-out counters for Answer to Request (ATR) and waiting times processing • Auto inverse convention function • Stop clock level and clock stop (clock keep) function • Transmitter and receiver error retry function • Supports hardware activation, deactivation and warm reset sequence process • Supports hardware auto deactivation sequence after card removal.
I^2C	• Three sets of I^2C devices with Master/Slave mode • Supports Standard mode (100 kbps), Fast mode (400 kbps), Fast mode plus (1 Mbps) and High speed mode (3.4Mbps) • Supports 10 bits mode • Programmable clocks allowing for versatile rate control • Supports multiple address recognition (four slave address with mask option) • Supports SMBus and PMBus • Supports multi-address power-down wake-up function • PDMA operation
SPI Master (SPI Flash) (M48xID)	• Maximum 32 MB external SPI Flash memory with standard (1-bit), dual (2-bit) and quad (4-bit) transfer mode. • 32 KB cache memory for enhancing program execution performance. • 64-bit key length for code protection. • DMA mode for code transfer between SPI Flash memory and SRAM. • SPI Master function with 8-, 16-, 24-, and 32-bit length of transaction and burst mode operation, which can transmit/receive data up to four successive transactions in one transfer. • Supports eXcute-In-Place (XIP)

Quad SPI	• SPI Quad controller with Master/Slave mode, up to 96 MHz at 2.7V~3.6V stsyem voltage. • Supports Dual and Quad I/O Transfer mode • Supports one/two data channel half-duplex transfer. (M48xID/M487KMCAN) • Supports one data channel half-duplex transfer. (M48xGC/M48xE8) • Supports double data rate mode. (M48xGC/M48xE8) • Supports receive-only mode • Configurable bit length of a transfer word from 8 to 32-bit • Provides separate 8-level depth transmit and receive FIFO buffers • Supports MSB first or LSB first transfer sequence • Supports the byte reorder function • Supports Byte or Word Suspend mode • Supports 3-wired, no slave select signal, bi-direction interface • PDMA operation.
SPI/I²S	• SPI/I²S controllers with Master/Slave mode. • SPI/I²S provides separate 4-level of 32-bit (or 8-level of 16-bit) transmit and receive FIFO buffers. **SPI** • Up to 96 MHz in both Master/Slave mode @ 2.7V-3.6V • Configurable bit length of a transfer word from 8 to 32-bit. • MSB first or LSB first transfer sequence. • Byte reorder function. • Supports Byte or Word Suspend mode. • Supports one data channel half-duplex transfer. • Supports receive-only mode. **I²S** • Supports mono and stereo audio data with 8-, 16-, 24- and 32-bit audio data sizes. • Supports PCM mode A, PCM mode B, I²S and MSB justified data format. • PDMA operation.
I²S	• One set of I²S interface with Master/Slave mode. • Supports mono and stereo audio data with 8-, 16-, 24- and 32-bit word sizes. • Two 16-level FIFO data buffers, one for transmitting and the other for receiving. • Supports I²S protocols: Philips standard, MSB-justified, and LSB-justified data format. • Supports PCM protocols: PCM standard, MSB-justified, and

	LSB-justified data format. • PCM protocol supports TDM multi-channel transmission in one audio sample; the number of data channel can be set as 2, 4, 6 or 8. • PDMA operation.
Universal Serial Control Interface (USCI) **(M48xID/M487KMCAN)**	• Two sets of USCI,configured as UART, SPI or I²C function. • Supports single byte TX and RX buffer mode **UART** • Supports one transmit buffer and two receive buffers for data payload. • Supports hardware auto flow control function and programmable flow control trigger level. • 9-bit Data Transfer. • Baud rate detection by built-in capture event of baud rate generator. • Supports wake-up function. • PDMA operation. **SPI** • Supports Master or Slave mode operation. • Supports one transmit buffer and two receive buffer for data payload. • Supports additional receive/transmit 16 entries FIFO for data payload. • Configurable bit length of a transfer word from 4 to 16-bit (SPI Quad transmission only supports 8 to 16-bit of word length). • Supports MSB first or LSB first transfer sequence. • Supports Word Suspend function. • Supports 3-wire, no slave select signal, bi-direction interface. • Supports wake-up function: input slave select transition. • PDMA operation. **I²C** • Supports master and slave device capability. • Supports one transmit buffer and two receive buffer for data payload. • Communication in standard mode (100 kbps), fast mode (up to 400 kbps), and Fast mode plus (1 Mbps). • Supports 10-bit mode. • Supports 10-bit bus time out capability. • Supports bus monitor mode. • Supports power-down wake-up by data toggle or address match. • Supports multiple address recognition. • Supports device address flag.

	• Programmable setup/hold time.
Controller Area Network (CAN)	• CAN 2.0B controllers. • Each supports 32 Message Objects; each Message Object has its own identifier mask. • Programmable FIFO mode (concatenation of Message Object). • Disabled Automatic Re-transmission mode for Time Triggered CAN applications. • Supports power-down wake-up function.
Secure Digital Host Controller (SDHC)	• Secure Digital Host Controllers are compliant with SD Memory Card Specification Version 2.0. • Supports 50 MHz to achieve 200 Mbps at 3.3V operation. • Supports dedicated DMA master with Scatter-Gather function to accelerate the data transfer between system memory and SD/SDHC/SDIO card.
External Bus Interface (EBI)	• Supports up to three memory banks with individual adjustment of timing parameter. • Each bank supports dedicated external chip select pin with polarity control and up to 1 MB addressing space. • 8-/16-bit data width. • Supports byte write in 16-bit data width mode. • Configurable idle cycle for different access condition: Idle of Write command finish (W2X) and Idle of Read-to-Read (R2R). • Supports Address/Data multiplexed mode. • Supports address bus and data bus separate mode. • Supports LCD interface i80 mode. • PDMA operation.
GPIO	• Supports four I/O modes: Quasi bi-direction, Push-Pull output, Open-Drain output and Input only with high impendence mode. • Selectable TTL/Schmitt trigger input. • Configured as interrupt source with edge/level trigger setting. • Supports independent pull-up/pull-down control. • Supports high driver and high sink current I/O. • Supports software selectable slew rate control. • Supports 5V-tolerance function except analog I/O.
Control Interfaces	
Quadrature Encoder Interface (QEI)	• Two QEI phase inputs (QEI_A, QEI_B) and one Index input (QEI_INDEX). • Supports 2/4 times free-counting mode and 2/4 compare-counting mode. • Supports encoder pulse width measurement mode with ECAP.

Enhanced Capture (ECAP)	**Input Capture Timer/Counter** • Supports three input channels with independent capture counter hold register. • 24-bit Input Capture up-counting timer/counter supports captured events reset and/or reload capture counter. • Supports rising edge, falling edge and both edge detector options with noise filter in front of input ports. • Supports compare-match function.
Advanced Connectivity	
USB 2.0 Full Speed with on-chip transceiver	**USB 2.0 Full Speed OTG (On-The-Go)** • On-chip USB 2.0 full speed OTG transceiver. • Compliant with USB OTG Supplement 2.0 • Configurable as host-only, device-only or ID-dependent **USB 2.0 Full Speed Host Controller** • Compliant with USB Revision 1.1 Specification. • Compatible with OHCI (Open Host Controller Interface) Revision 1.0. • Supports full-speed (12Mbps) and low-speed (1.5Mbps) USB devices. • Supports Control, Bulk, Interrupt, Isochronous and Split transfers. • Integrated a port routing logic to route full/low speed device to OHCI controller. • Supports an integrated Root Hub. • Supports port power control and port over current detection. • Built-in DMA. **USB 2.0 Full Speed Device Controller** • Compliant with USB Revision 2.0 Specification. • Supports suspend function when no bus activity existing for 3 ms. • 12 configurable endpoints for configurable Isochronous, Bulk, Interrupt and Control transfer types. • 1024 bytes configurable RAM for endpoint buffer. • Remote wake-up capability. • Supports crystall-less features. (M48xGC/M48xE8) • USB 2.0 link power management. (M48xID/M487KMCAN)
USB 2.0 High Speed with on-chip transceiver **(M48xID/M487KMCAN)**	**USB 2.0 High Speed OTG (On-The-Go)** • On-chip USB 2.0 high speed OTG transceiver. • Compliant with USB OTG Supplement 2.0. • Configurable as host-only, device-only or ID-dependent.

	USB 2.0 High Speed Host Controller • Compliant with USB Revision 2.0 Specification. • Compatible with EHCI (Enhanced Host Controller Interface) Revision 1.0. • Compatible with OHCI (Open Host Controller Interface) Revision 1.0. • Supports high-speed (480Mbps), full-speed (12Mbps) and low-speed (1.5Mbps) USB devices. • Integrated a port routing logic to route full/low speed device to OHCI controller. • Supports an integrated Root Hub. • Built-in DMA. **USB 2.0 High Speed Device Controller** • Compliant with USB Revision 2.0 Specification. • Supports one dedicate control endpoint and 12 configurable endpoints; each can be Isochronous, Bulk or Interrupt and either IN or OUT direction. • 4096 bytes configurable RAM for endpoint buffer and up to 1024 bytes maximum packet size. • Three different operation modes of an in-endpoint: Auto Validation mode, Manual Validation mode and Fly mode. • Suspend, resume and remote wake-up capability. • Built-in DMA.
Ethernet MAC **(M48xID/M487KMCAN)**	• IEEE Std. 802.3 CSMA/CD protocol. • Ethernet frame time stamping for IEEE Std. 1588 – 2002 protocol. • Supports both half and full duplex for 10 Mbps or 100 Mbps operation. • RMII (Reduced Media Independent Interface) and serial management interface (MDC/MDIO). • Pause and remote pause function for flow control. • Long frame (more than 1518 bytes) and short frame (less than 64 bytes) reception. • CAM function for Ethernet MAC address recognition. • Supports Magic Packet recognition to wake system up from Power-down mode. • Built-in DMA.
Digital Camera Interface	
Camera Capture Interface (CCAP) **(M48xGC/M48xE8)**	• Supports CCIR601, CCIR656 and 4-bit interfaces for CMOS sensor. • Color format for data input supports YUV4:2:2 and RGB565. • Color format for data output supports YUV4:2:2, RGB565, RGB555 and Y-only.

	• Supports 1-bit Y(luminance) output with 8-bit threshold setting for image thresholding. • Supports image cropping and downscaling.
Cryptography Accelerator	
Elliptic Curve Cryptography (ECC)	• Hardware ECC accelerator. • Supports 192-bit and 256-bit key length. • Supports both prime field GF(p) and binary field GF(2^m). • Supports NIST P-192, P-224, P-256, P-384 and P-521 curve sizes. • Supports NIST B-163, B-233, B-283, B-409 and B-571 curve sizes. • Supports NIST K-163, K-233, K-283, K-409 and K-571 curve sizes. • Supports point multiplication, addition and doubling operations in GF(p) and GF(2^m). • Supports modulus division, multiplication, addition and subtraction operations in GF(p).
Advanced Encryption Standard (AES)	• Hardware AES accelerator. • Supports 128-bit, 192-bit and 256-bit key length and key expander, and is compliant with FIPS 197. • Supports ECB, CBC, CFB, OFB, CTR, CBC-CS1, CBC-CS2 and CBC-CS3 block cipher modes • Compliant with NIST SP800-38A and addendum.
Data Encryption Standard (DES) **(M48xID/M487KMCAN)**	• Hardware DES accelerator. • Supports ECB, CBC, CFB, OFB, and CTR block cipher mode. • Compliant with FIPS 46-3.
Triple Data Encryption Standard (3DES) **(M48xID/M487KMCAN)**	• Hardware Triple DES accelerator. • Supports two or three different keys in each round. • Supports ECB, CBC, CFB, OFB, and CTR block cipher mode. • Implemented based on X9.52 standard and compliant with FIPS SP 800-67.
Secure Hash Algorithm (SHA)	• Hardware SHA accelerator. • Supports SHA-160, SHA-224, SHA-256, SHA-384 and SHA-512. (M48xID/M487KMCAN) • Supports SHA-256. (M48xID/M487KMCAN) • Compliant with FIPS 180/180-2.
keyed-Hash Message	• Hardware HMAC accelerator.

Authentication Code (HMAC)	• Supports HMAC-SHA-160, HMAC-SHA-224, HMAC-SHA-256, HMAC-SHA-384, and HMAC-SHA-512. (M48xID/M487KMCAN) • Supports HMAC-SHA-256. (M48xID/M487KMCAN) • Compliant with FIPS 180/180-2.
True Random Number Generator (TRNG) **(M48xGC/M48xE8)**	• 800 random bits per second.

3 PARTS INFORMATION

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

3.1 Package Type

Part No.	QFN33	QFN48	LQFP48	LQFP64	LQFP128	LQFP144
M481	M481ZGCAE M481ZIDAE M481ZE8AE		M481LGCAE M481LIDAE M481LE8AE	M481SGCAE M481SIDAE M481SE8AE M481SGCAE2A		
M482	M482ZGCAE M482ZIDAE M482ZE8AE		M482LGCAE M482LIDAE M482LE8AE	M482SGCAE M482SIDAE M482SE8AE	M482KGCAE M482KIDAE	
M483				M483SGCAE M483SIDAE M483SE8AE M483SGCAE2A	M483KGCAE M483KIDAE M483KGCAE2A	
M484				M484SIDAE M484SIDAE2U	M484KIDAE	
M485	M485ZIDAE	M485YIDAE	M485LIDAE	M485SIDAE	M485KIDAE	
M487				M487SIDAE	M487KIDAE M487KMCAN	M487JIDAE

3.2 M480 Series Selection Guide

3.2.1 M481 Base Series (M481xIDAE)

PART NUMBER		M481		
		ZIDAE	LIDAE	SIDAE
Flash (KB)		512		
SRAM (KB)		160 (include 32 KB cache for XIP)		
ISP Loader ROM (KB)		4		
I/O		26	41	52
32-bit Timer		4		
Peripheral DMA		16		
Tamper		-	-	1
Connectivity	LPUART	6		
	ISO-7816	3		
	SPI Master	1 (Support XIP)		
	Quad SPI	1		
	SPI/I²S	3	3	4
	I²S	1		
	I²C	3		
	USCI	2		
	CAN	-		
	LIN	2		
	SDHC	1	2	2
16-bit PWM		24		
QEI		1	2	2
ECAP		-	1	1
USB 2.0 FS OTG		-		
USB 2.0 HS OTG		-		
12-bit ADC		10	12	16
12-bit DAC		2		
Analog Comparator		2		
Operational Amplifier		1	2	2
Ethernet		-		
Cryptography		-		
External Bus Interface		-	√	√
Package		QFN 32	LQFP 48	LQFP 64

3.2.2 M481 Base Series (M481xGCAE / M481xE8AE)

PART NUMBER		M481						
		ZE8AE	ZGCAE	LE8AE	LGCAE	SE8AE	SGCAE	SGCAE2A
Flash (KB) (Support XOM)		128	256	128	256	128	256	256
SRAM (KB)		64	128	64	128	64	128	128
ISP Loader ROM (KB)		4						
I/O		26		41		52		52
32-bit Timer		4						
Peripheral DMA		16						
Tamper		-		-		1		1
Connectivity	LPUART	8						
	ISO-7816	1						
	SPI Master	-						
	Quad SPI	2						
	SPI/I²S	2		3		3		3
	I²S	1						
	I²C	3						
	USCI	-						
	CAN	-						
	LIN	2						
	SDHC	1						
16-bit PWM		24						
QEI		1		2		2		2
ECAP		-		1		1		1
USB 2.0 FS OTG		-						
USB 2.0 HS OTG		-						
12-bit ADC		10		12		16		**8+8**
12-bit DAC		1						
Analog Comparator		2						
Operational Amplifier		-						
Ethernet		-						
Cryptography		√						
TRNG		√						
External Bus Interface		-		√		√		√
Camera Interface		-		-		√		√
Package		QFN33		LQFP 48		LQFP 64		LQFP 64

3.2.3 M482 USB FS OTG Series (M482xIDAE)

PART NUMBER		M482			
		ZIDAE	LIDAE	SIDAE	KIDAE
Flash (KB)		512			
SRAM (KB)		160 (include 32 KB cache for XIP)			
ISP Loader ROM (KB)		4			
I/O		26	41	52	100
32-bit Timer		4			
Peripheral DMA		16			
Tamper		-	-	1	6
Connectivity	LPUART	6			
	ISO-7816	3			
	SPI Master	1 (Support XIP)			
	Quad SPI	1			
	SPI/I²S	3	3	4	4
	I²S	1			
	I²C	3			
	USCI	2			
	CAN	-			
	LIN	2			
	SDHC	1	2	2	2
16-bit PWM		24			
QEI		1	2	2	2
ECAP		-	1	1	2
USB 2.0 FS OTG		√			
USB 2.0 HS OTG		-			
12-bit ADC		10	12	16	16
12-bit DAC		2			
Analog Comparator		2			
Operational Amplifier		1	2	2	3
Ethernet		-			
Cryptography		-			
External Bus Interface		-	√	√	√
Package		QFN33	LQFP 48	LQFP 64	LQFP 128

3.2.4 M482 USB FS OTG Series (M482xGCAE / M482xE8AE)

PART NUMBER		M482						
		ZE8AE	ZGCAE	LE8AE	LGCAE	SE8AE	SGCAE	KGCAE
Flash (KB) (Support XOM)		128	256	128	256	128	256	256
SRAM (KB)		64	128	64	128	64	128	128
ISP Loader ROM (KB)		4						
I/O		26		41		52		100
32-bit Timer		4						
Peripheral DMA		16						
Tamper		-		-		1		6
Connectivity	LPUART	8						
	ISO-7816	1						
	SPI Master	-						
	Quad SPI	2						
	SPI/I²S	2		3		3		3
	I²S	1						
	I²C	3						
	USCI	-						
	CAN	-						
	LIN	2						
	SDHC	1						
16-bit PWM		24						
QEI		1		2		2		2
ECAP		-		1		1		2
USB 2.0 FS OTG		√ (Crystal-less)						
USB 2.0 HS OTG		-						
12-bit ADC		10		12		16		16
12-bit DAC		1						
Analog Comparator		2						
Operational Amplifier		-						
Ethernet		-						
Cryptography		√						
TRNG		√						
External Bus Interface		-		√		√		√
Camera Interface		-		-		√		√
Package		QFN33		LQFP 48		LQFP 64		LQFP 128

3.2.5 M483 CAN Series (M483xIDAE)

PART NUMBER		M483	
		SIDAE	KIDAE
Flash (KB)		512	
SRAM (KB)		160 (include 32 KB cache for XIP)	
ISP Loader ROM (KB)		4	
I/O		44	100
32-bit Timer		4	
Peripheral DMA		16	
Tamper		1	6
Connectivity	LPUART	6	
	ISO-7816	3	
	SPI Master	1	
	Quad SPI	1	
	SPI/I²S	4	
	I²S	1	
	I²C	3	
	USCI	2	
	CAN	2	
	LIN	2	
	SDHC	2	
16-bit PWM		24	
QEI		2	
ECAP		1	2
USB 2.0 FS OTG		-	√
USB 2.0 HS OTG		√	
12-bit ADC		16	
12-bit DAC		2	
Analog Comparator		2	
Operational Amplifier		2	3
Ethernet		-	
Cryptography		-	
External Bus Interface		√	
Package		LQFP 64	LQFP 128

3.2.6 M483 CAN Series (M483xGCAE / M483xE8AE)

PART NUMBER		M483				
		SE8AE	SGCAE	SGCAE2A	KGCAE	KGCAE2A
Flash (KB) (Support XOM)		128	256	256	256	
SRAM (KB)		64	128	128	128	
ISP Loader ROM (KB)		4				
I/O		52		52	100	
32-bit Timer		4				
Peripheral DMA		16				
Tamper		1		1	6	
Connectivity	LPUART	8				
	ISO-7816	1				
	SPI Master	-				
	Quad SPI	2				
	SPI/I²S	3				
	I²S	1				
	I²C	3				
	USCI	-				
	CAN	3				
	LIN	2				
	SDHC	1				
16-bit PWM		24				
QEI		2				
ECAP		1		1	2	
USB 2.0 FS OTG		√ (Crystal-less)				
USB 2.0 HS OTG		-				
12-bit ADC		16		**8+8**	16	**16+8**
12-bit DAC		1				
Analog Comparator		2				
Operational Amplifier		-				
Ethernet		-				
Cryptography		√				
TRNG		√				
External Bus Interface		√				
Camera Interface		√				
Package		LQFP 64		LQFP 64	LQFP 128	

3.2.7 M484 USB HS OTG Series

PART NUMBER		M484		
		SIDAE	SIDAE2U	KIDAE
Flash (KB)		512		
SRAM (KB)		160 (include 32 KB cache for XIP)		
ISP Loader ROM (KB)		4		
I/O		44	44	100
32-bit Timer		4		
Peripheral DMA		16		
Tamper		1	1	6
Connectivity	LPUART	6		
	ISO-7816	3		
	SPI Master	1		
	Quad SPI	1		
	SPI/I²S	4		
	I²S	1		
	I²C	3		
	USCI	2		
	CAN	-		
	LIN	2		
	SDHC	2		
16-bit PWM		24		
QEI		2		
ECAP		1	1	2
USB 2.0 FS OTG		-	√	√
USB 2.0 HS OTG		√		
12-bit ADC		16		
12-bit DAC		2		
Analog Comparator		2		
Operational Amplifier		2	2	3
Ethernet		-		
Cryptography		-		
External Bus Interface		√		
Package		LQFP 64	LQFP 64	LQFP 128

3.2.8 M485 Crypto Series

PART NUMBER		M485				
		ZIDAE	YIDAE	LIDAE	SIDAE	KIDAE
Flash (KB)		512				
SRAM (KB)		160 (include 32 KB cache for XIP)				
ISP Loader ROM (KB)		4				
I/O		26	41	41	44	100
32-bit Timer		4				
Peripheral DMA		16				
Tamper		-	-	-	1	6
Connectivity	LPUART	6				
	ISO-7816	3				
	SPI Master	1				
	Quad SPI	1				
	SPI/I²S	3	4	3	4	4
	I²S	1				
	I²C	3				
	USCI	2				
	CAN	-	2	-		
	LIN	2				
	SDHC	1	1	2	2	2
16-bit PWM		24				
QEI		1	2	2	2	2
ECAP		-	-	1	1	2
USB 2.0 FS OTG		√	√	√	-	√
USB 2.0 HS OTG		-	-	-	√	√
12-bit ADC		10	16	12	16	16
12-bit DAC		2				
Analog Comparator		2				
Operational Amplifier		1	1	2	2	3
Ethernet		-				
Cryptography		√				
External Bus Interface		-	-	√	√	√
Package		QFN33	QFN48	LQFP 48	LQFP 64	LQFP 128

3.2.9 M487 Ethernet Series

PART NUMBER		M487			
		SIDAE	KIDAE	JIDAE	KMCAN
Flash (KB)		512			2560
SRAM (KB)		160			
ISP Loader ROM (KB)		4			
I/O		44	100	114	94
32-bit Timer		4			
Peripheral DMA		16			
Tamper		1	6	6	6
Connectivity	LPUART	6			
	ISO-7816	3			
	SPI Master	1			-
	Quad SPI	1			
	SPI/I²S	4			
	I²S	1			
	I²C	3			
	USCI	2			
	CAN	2			
	LIN	2			
	SDHC	2			
16-bit PWM		24			
QEI		2			
ECAP		1	2	2	2
USB 2.0 FS OTG		-	√	√	√
USB 2.0 HS OTG		√			
12-bit ADC		16			
12-bit DAC		2			
Analog Comparator		2			
Operational Amplifier		2	3	3	3
Ethernet		√			
Cryptography		√			
External Bus Interface		√			
Package		LQFP 64	LQFP 128	LQFP 144	LQFP 128

3.3 M480 Selection Code

M4	81	Z	G	D	A	E	2A
Core	Series	Package	Flash Size	SRAM Size	Revision	Temperature	Peripheral
Cortex®-M4F	81: Base 82: USB FS 83: CAN 84: USB HS 85: Crypto 87: Ethernet	Z: QFN33 (5x5 mm) Y: QFN48 (5x5 mm) L: LQFP48 (7x7 mm) C: WLCSP S: LQFP64 (7x7 mm) O: QFN88 (10x10 mm) V: LQFP100 (14x14 mm) K: LQFP128 (14x14 mm) J: LQFP144 (20x20 mm)	A: 8 Kbytes B: 16 Kbytes C: 32 Kbytes D: 64 Kbytes E: 128 Kbytes F: 192 Kbytes G: 256 Kbytes H: 384 Kbytes I: 512 Kbytes M: 2560 Kbytes	1: 4 Kbytes 2: 8 Kbytes 3: 16 Kbytes 4: 20 Kbytes 5: 24 Kbytes 6: 32 Kbytes 7: 48 Kbytes 8: 64 Kbytes 9: 80 Kbytes A: 96 Kbytes B: 112 Kbytes C: 128 Kbytes D: 160 Kbytes		E:-40°C ~ 105°C N:-40°C ~ 85°C	2A: 2 EADCs 2U: 2 USB ports

4 PIN CONFIGURATION

4.1 Pin Configuration

Users can find pin configuration information in chapter 4 or by using NuTool - PinConfig. The NuTool - PinConfigure contains all NuMicro Family chip series with all part number, and helps users configure GPIO multi-function correctly and handily.

4.1.1 QFN-33 Pin Diagram

Corresponding Part Number: M481ZE8AE, M481ZGCAE, M481ZIDAE, M482ZE8AE, M482ZGCAE, M482ZIDAE, M485ZIDAE

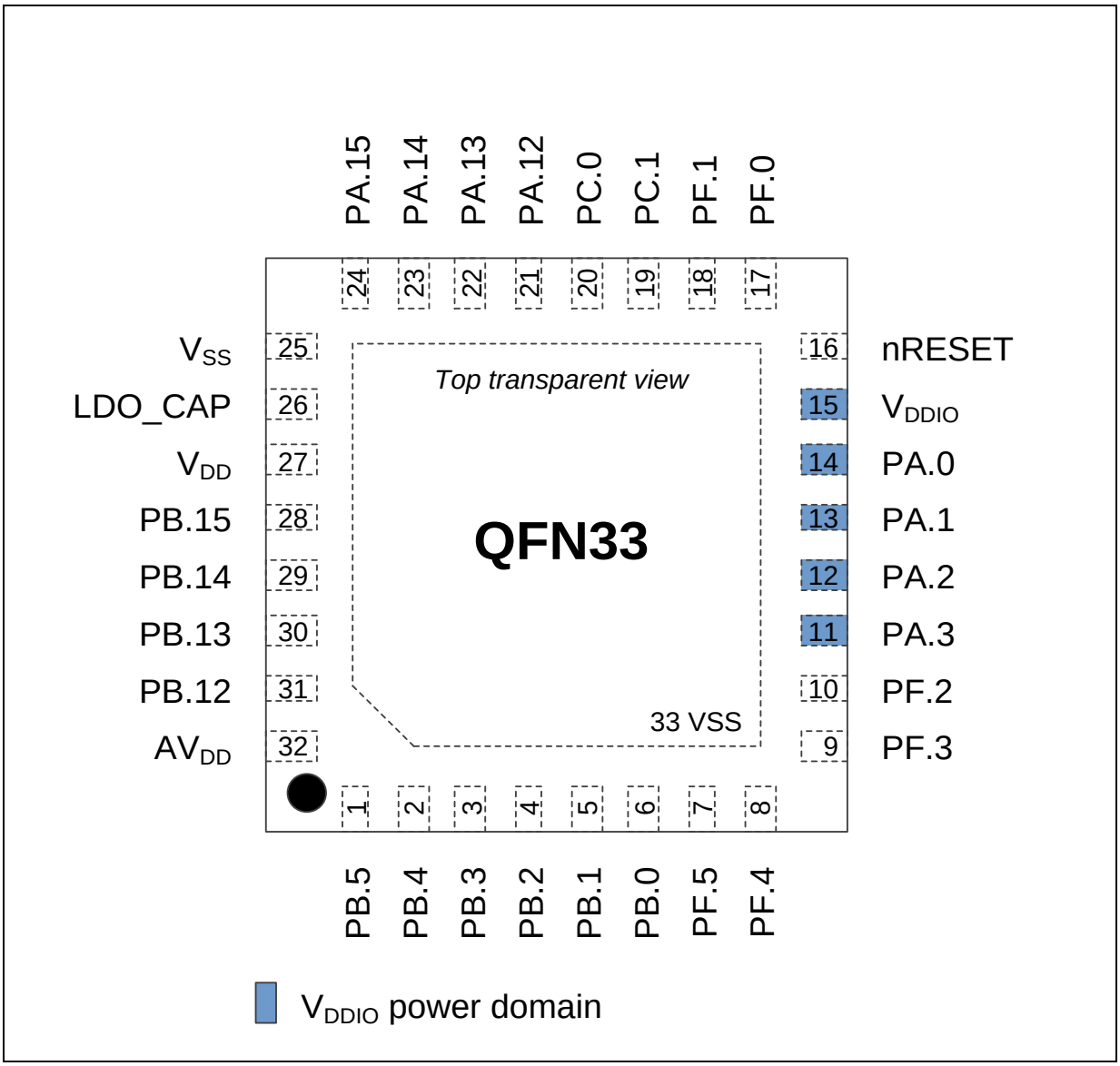

Figure 4.1-1 QFN-33 Pin Diagram (0/1 USB FS)

4.1.2 QFN-48 Pin Diagram

Corresponding Part Number: M485YIDAE

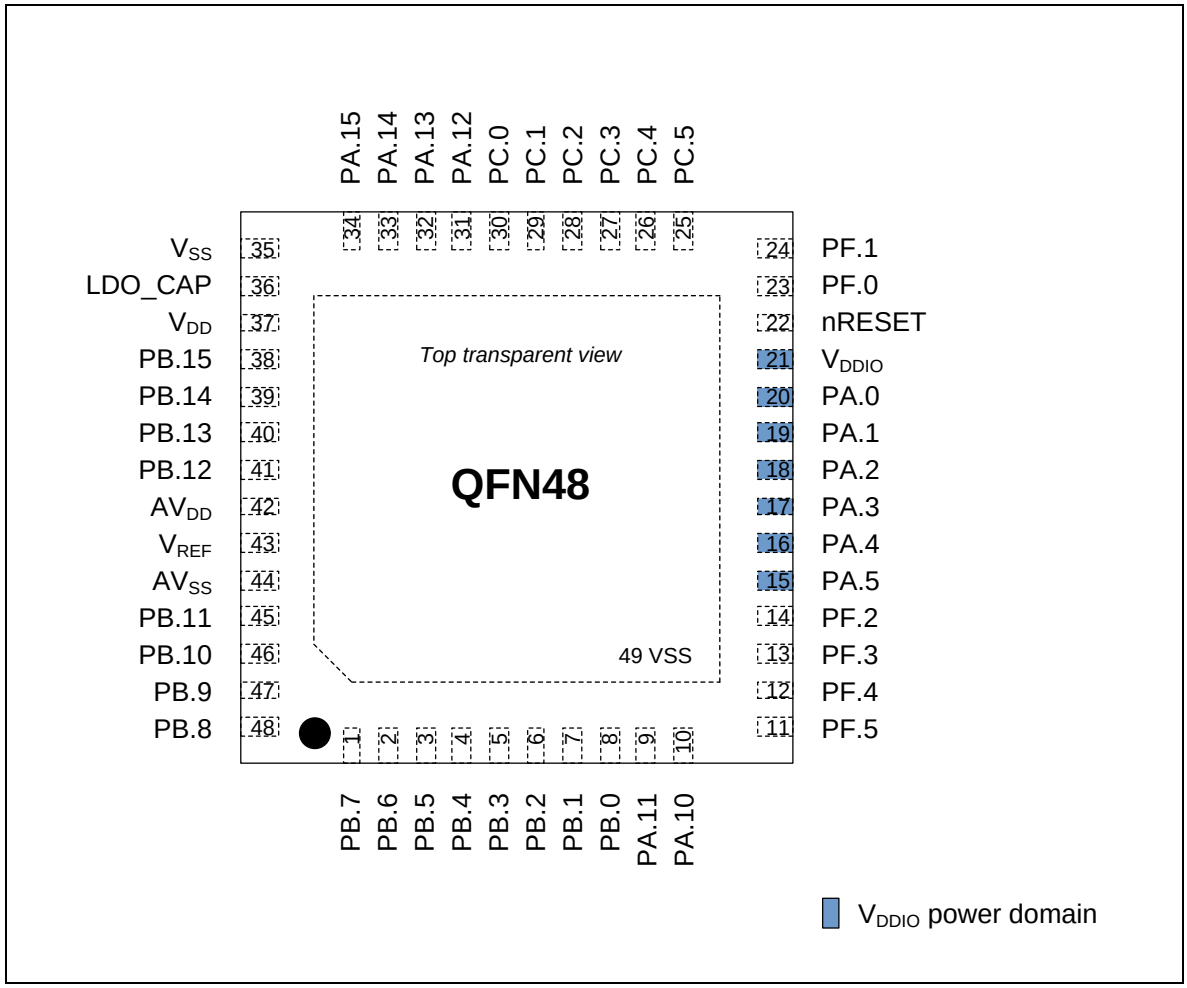

Figure 4.1-2 QFN-48 Pin Diagram

4.1.3 LQFP-48 Pin Diagram (0/1 USB FS)

Corresponding Part Number: M481LE8AE, M481LGCAE, M481LIDAE, M482LE8AE, M482LGCAE, M482LIDAE, M485LIDAE

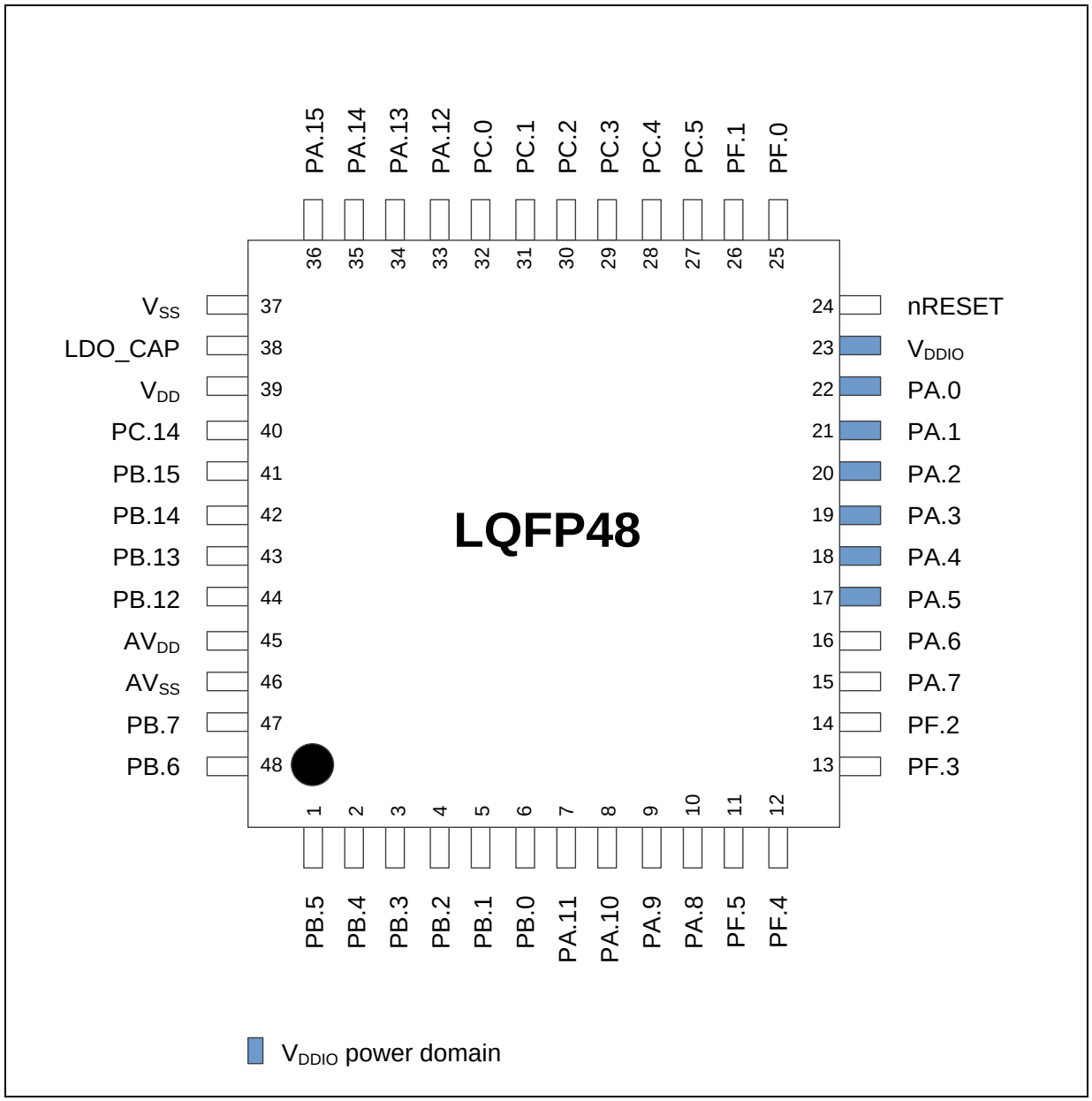

Figure 4.1-3 LQFP-48 Pin Diagram (0/1 USB FS)

4.1.4 LQFP-64 Pin Diagram (0/1 USB FS)

Corresponding Part Number: M481SIDAE, M482SIDAE

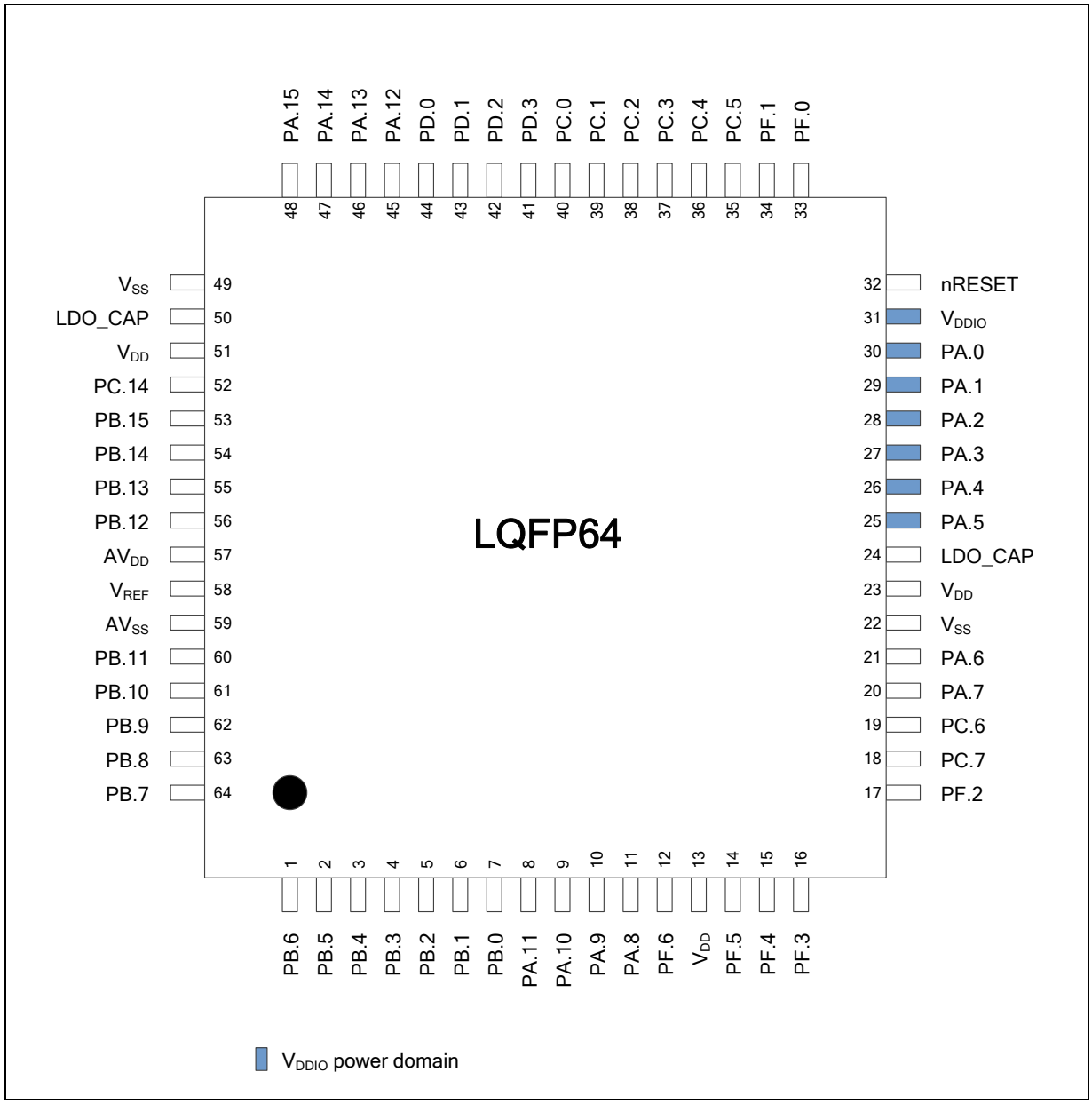

Figure 4.1-4 LQFP-64 Pin Diagram (0/1 USB FS)

4.1.5 LQFP-64 Pin Diagram (0/1 USB FS with V_{BAT})

Corresponding Part Number: M481SE8AE, M481SGCAE, M481SGCAE2A, M482SE8AE, M482SGCAE, M483SE8AE, M483SGCAE, M483SGCAE2A

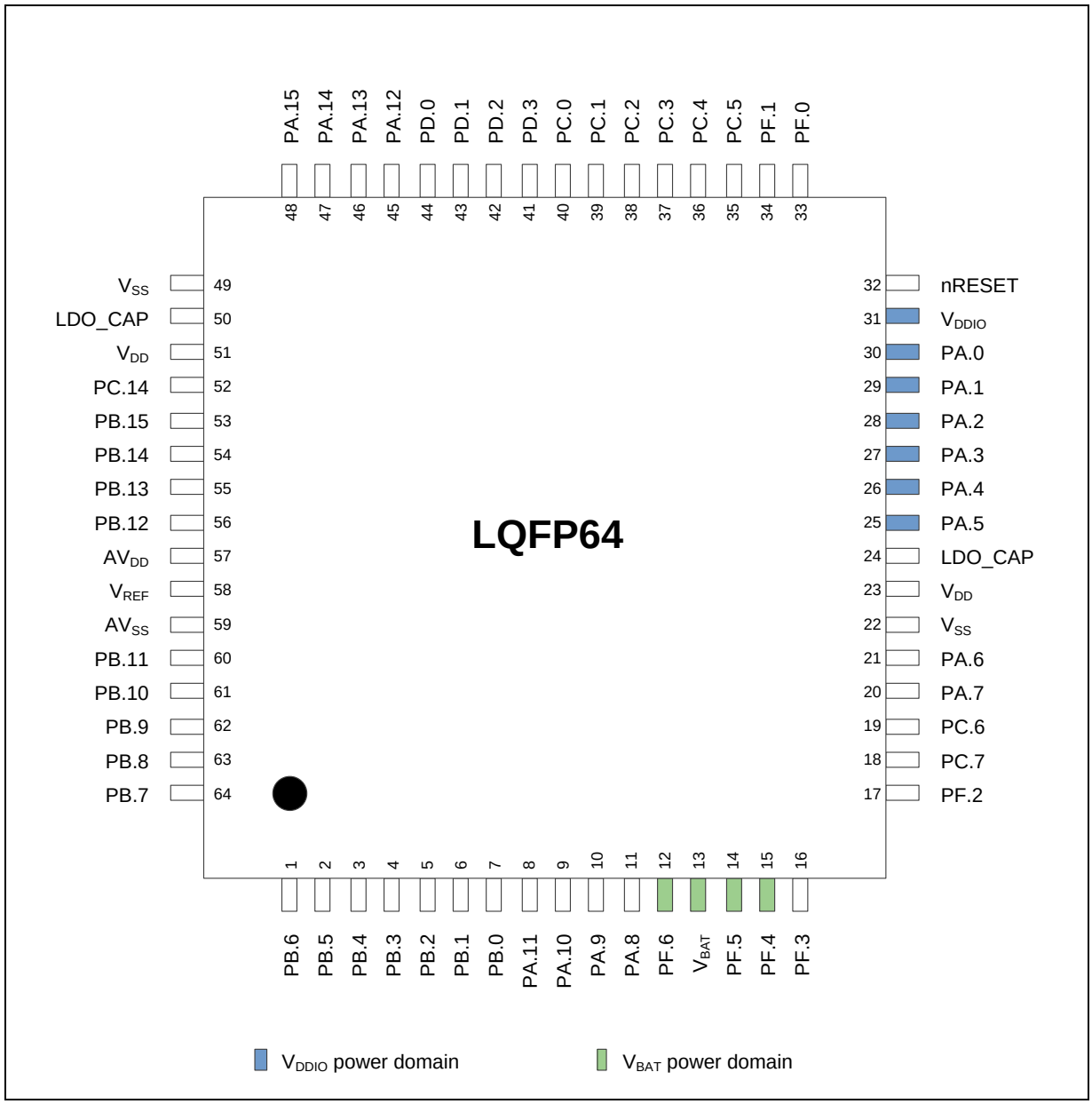

Figure 4.1-5 LQFP-64 Pin Diagram (0/1 USB FS with V_{BAT})

4.1.6 LQFP-64 Pin Diagram (1 USB HS)

Corresponding Part Number: M483SIDAE, M484SIDAE, M485SIDAE, M487SIDAE

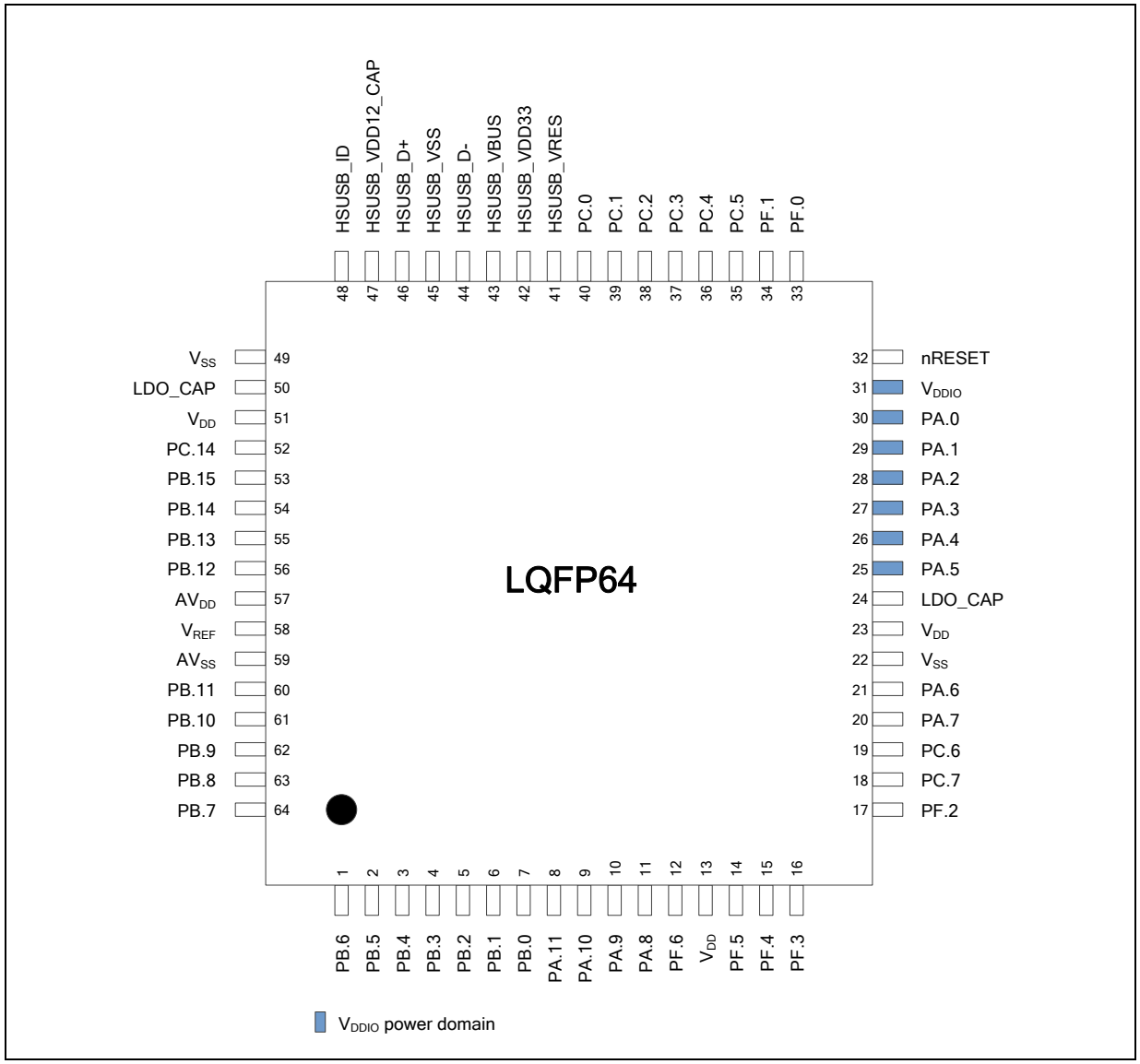

Figure 4.1-6 LQFP-64 Pin Diagram (1 USB HS)

4.1.7 LQFP-64 Pin Diagram (USB FS + USB HS)

Corresponding Part Number: M484SIDAE2U

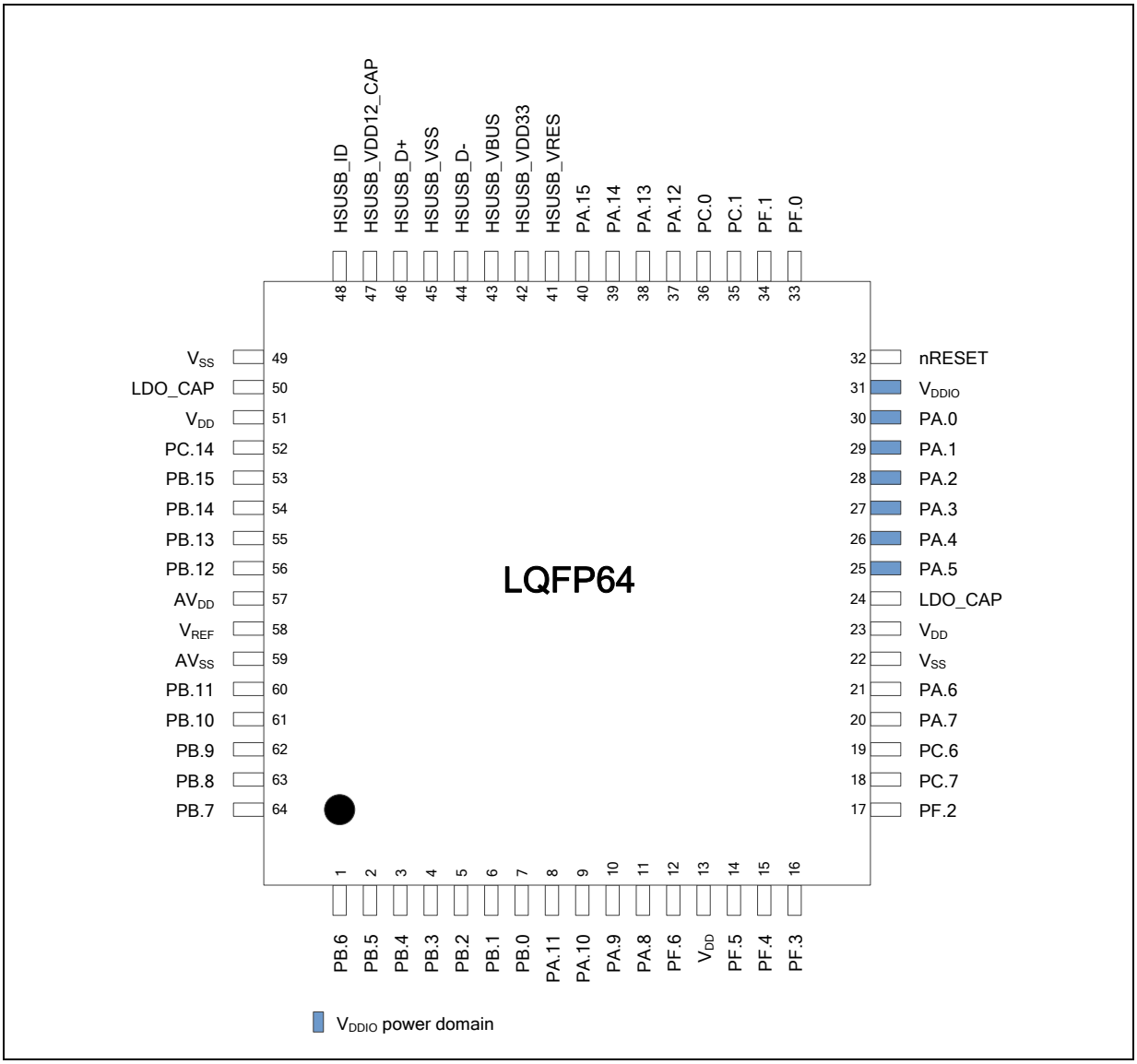

Figure 4.1-7 LQFP-64 Pin Diagram (USB FS + USB HS)

4.1.8 LQFP-128 Pin Diagram (1 USB FS)

Corresponding Part Number: M482KIDAE

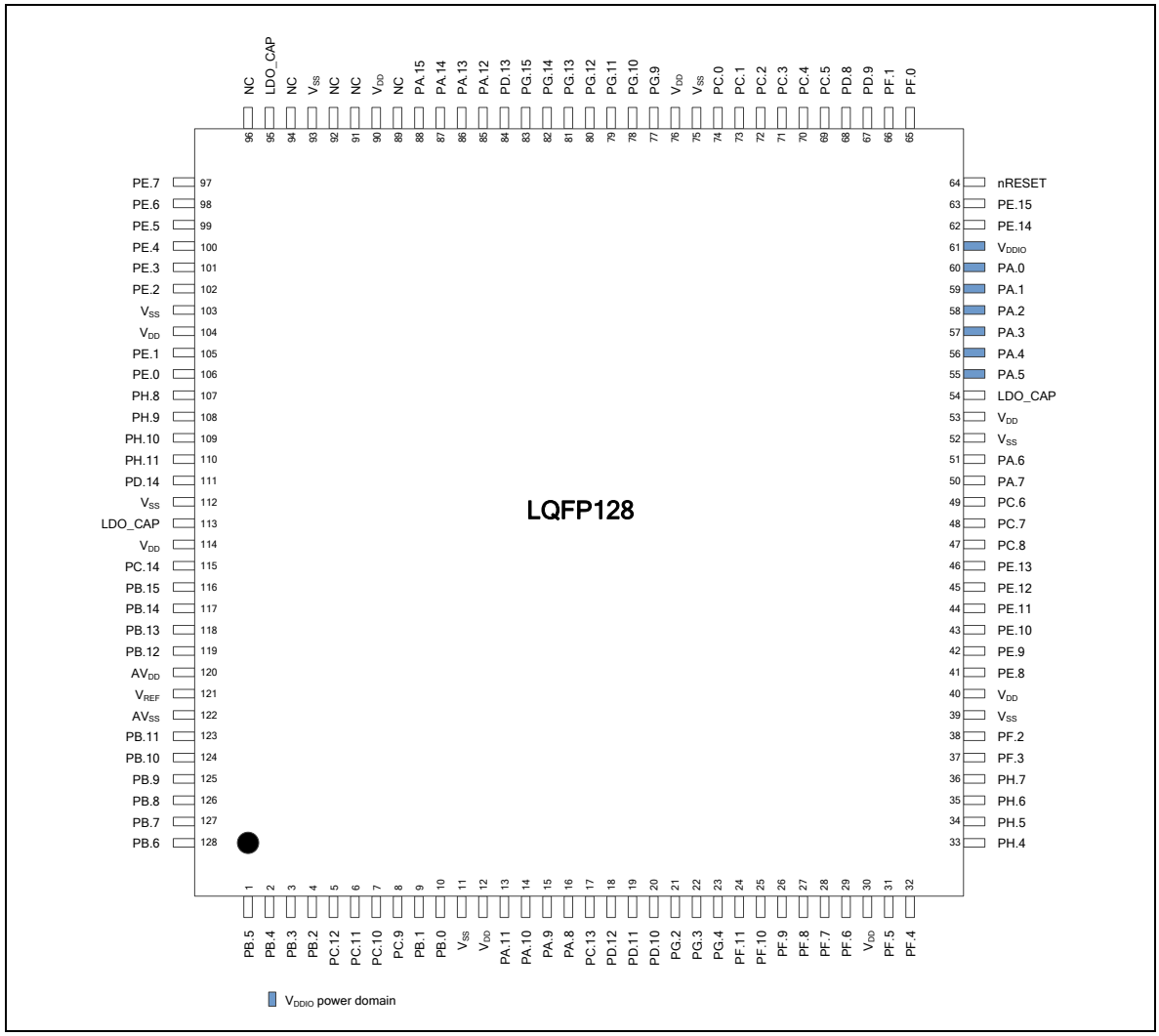

Figure 4.1-8 LQFP-128 Pin Diagram (1 USB FS)

4.1.9 LQFP-128 Pin Diagram (1 USB FS with V_{BAT})

Corresponding Part Number: M482KGCAE, M483KGCAE, M483KGCAE2A

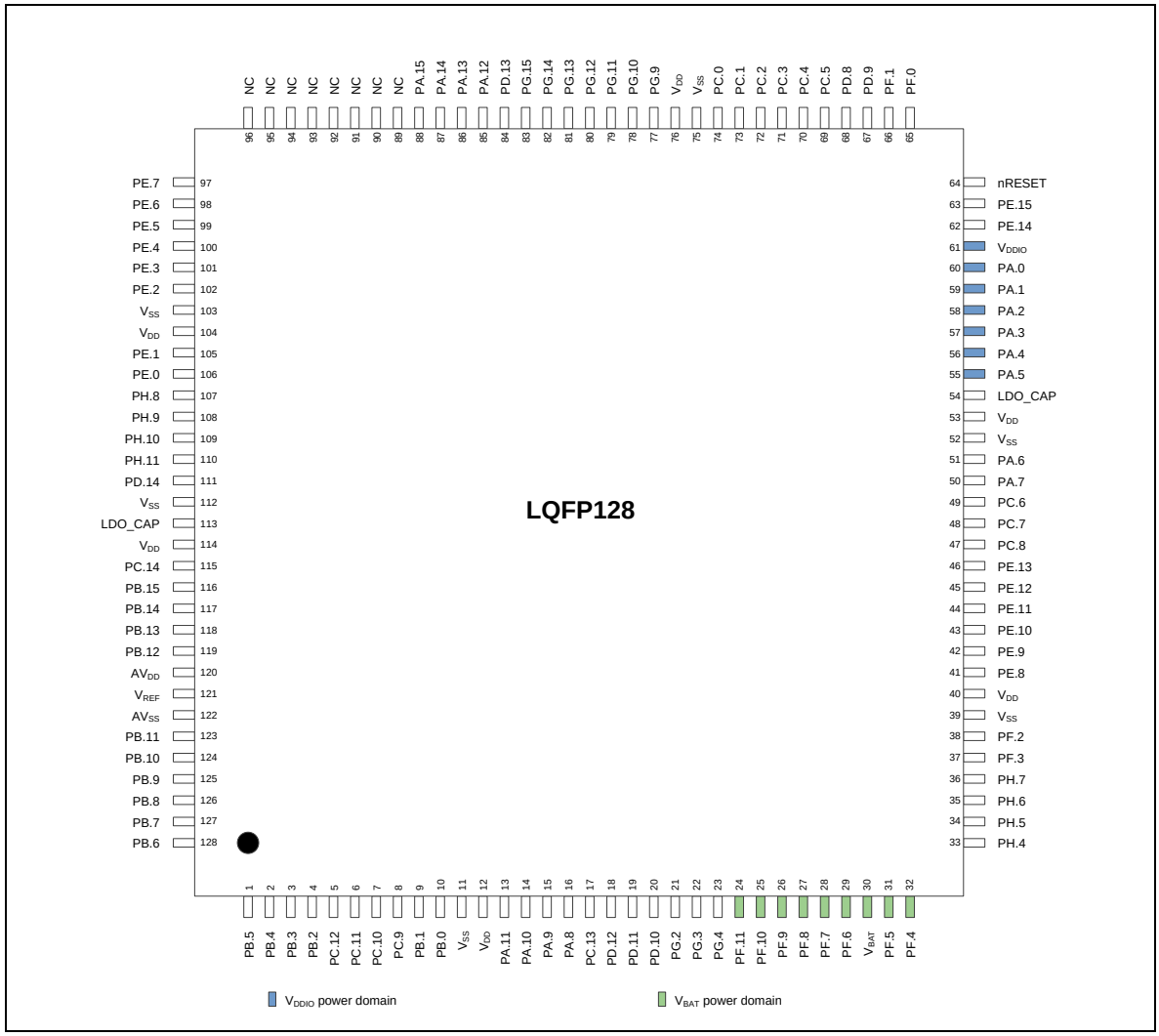

Figure 4.1-9 LQFP-128 Pin Diagram (1 USB FS)

4.1.10 LQFP-128 Pin Diagram (USB FS + USB HS)

Corresponding Part Number: M483KIDAE, M484KIDAE, M485KIDAE, M487KIDAE

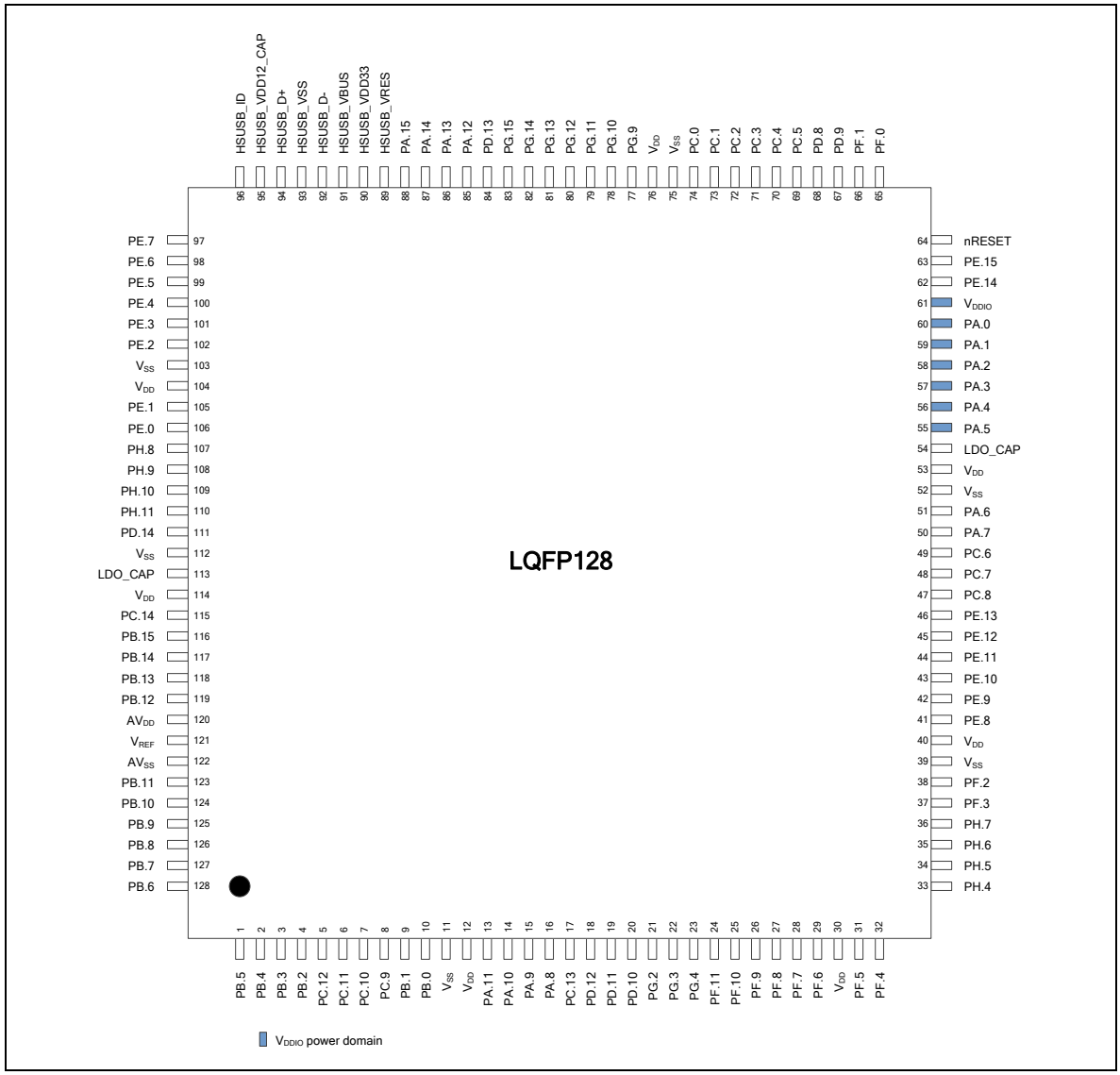

Figure 4.1-10 LQFP-128 Pin Diagram (USB FS + USB HS)

4.1.11 LQFP-128 Pin Diagram (USB FS + USB HS)

Corresponding Part Number: M487KMCAN

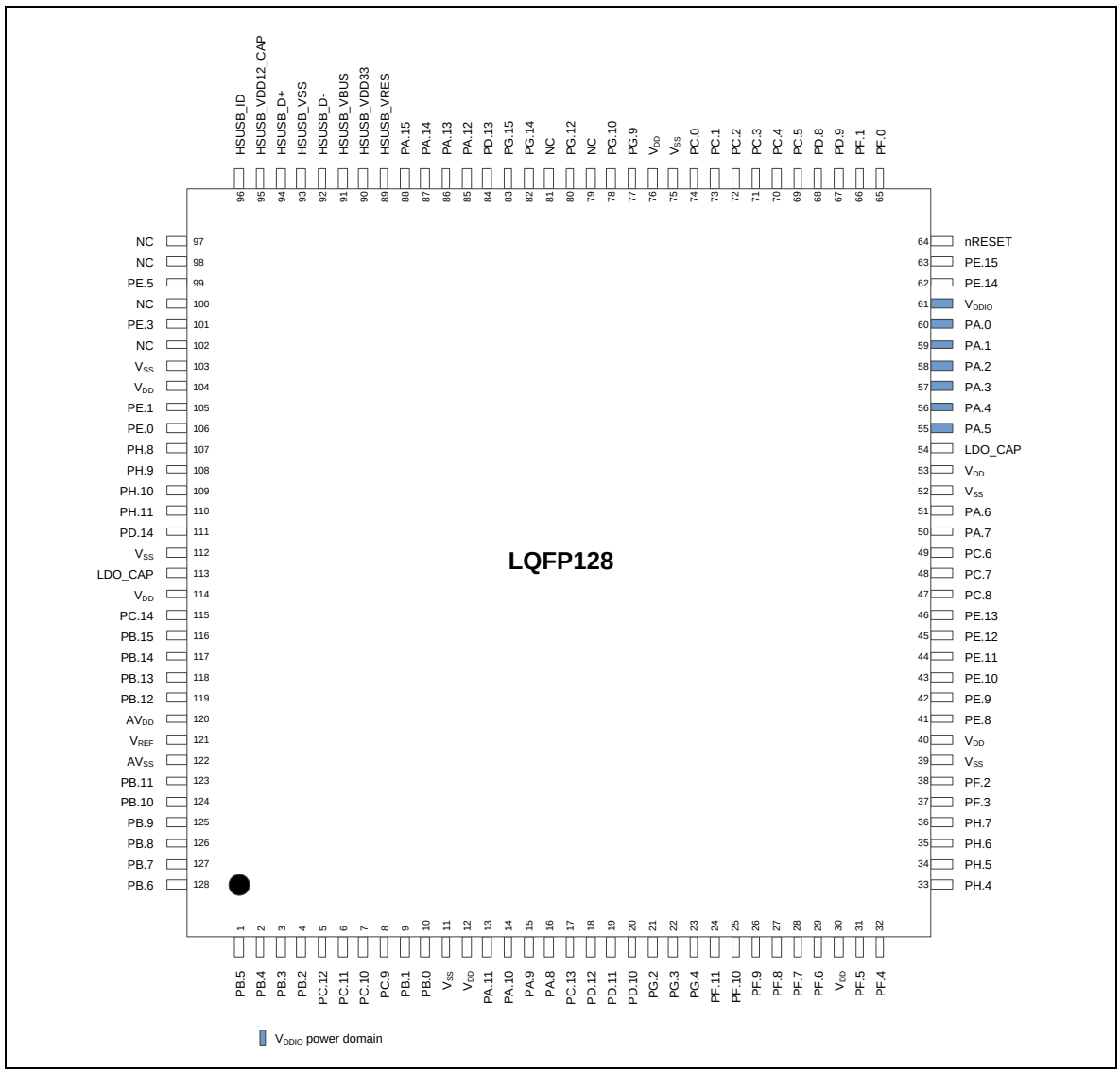

Figure 4.1-11 LQFP-128 Pin Diagram (USB FS + USB HS)

4.1.12 LQFP-144 Pin Diagram

Corresponding Part Number: M487JIDAE

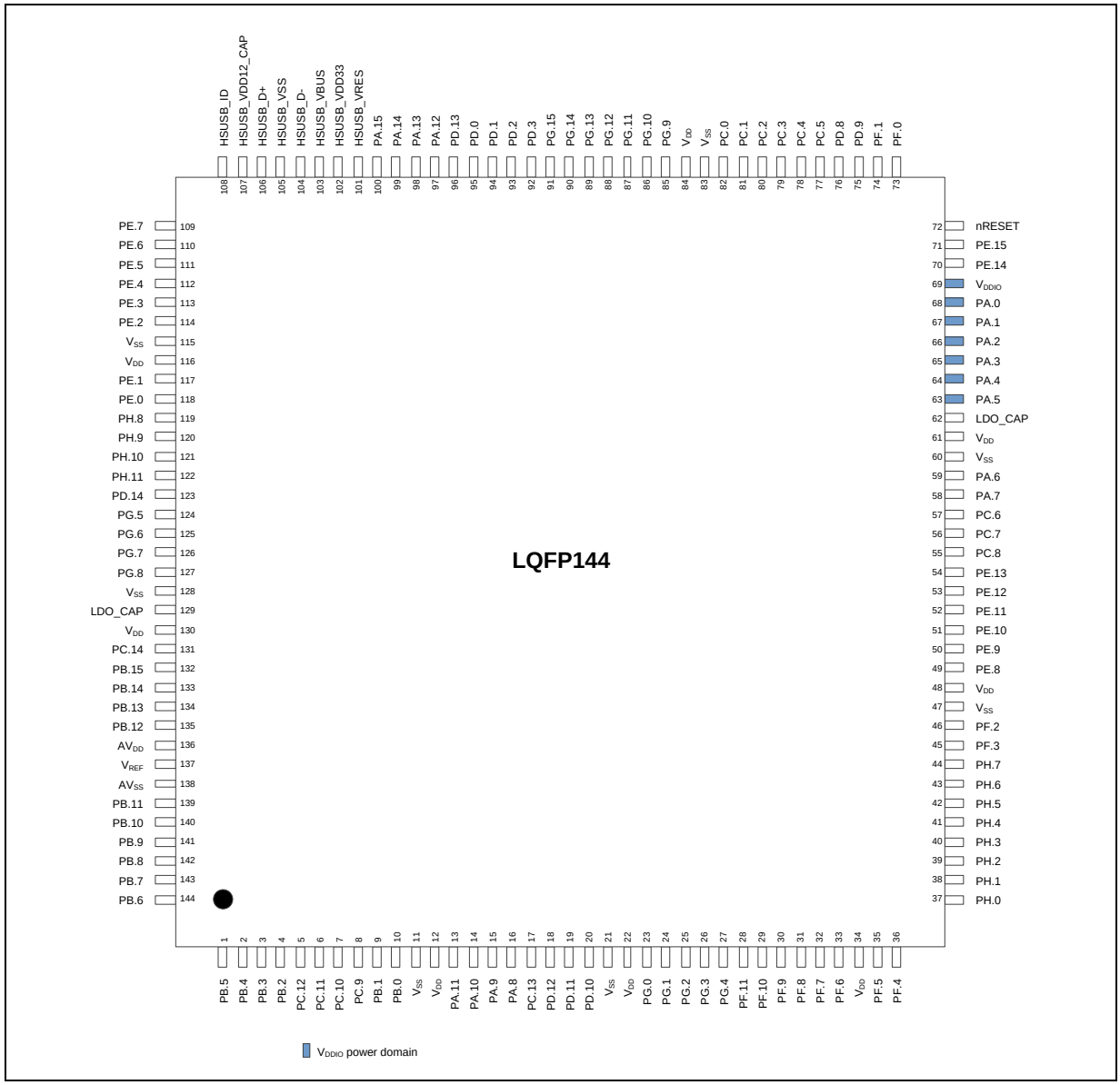

Figure 4.1-12 LQFP-144 Pin Diagram