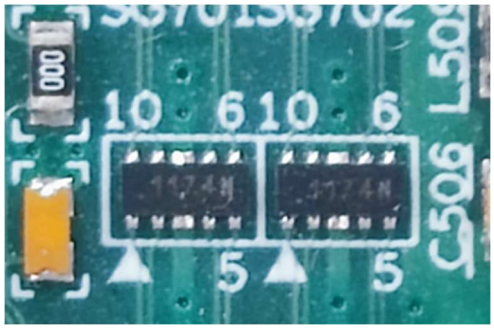


設計驗證
工程課
2025-01-14
發行
虹鋒科技開發股份有限公司

ARROW
ARROW ELECTRONICS TAIWAN LTD.,

艾睿電子股份有限公司
新北市中和區建一路150號17樓
TEL: 7703-8156 FAX: 7723-8168

承　　認　　書
(APPROVAL SHEET)

公司名稱: DIVA Laboratories. Ltd.
鈺緯科技開發股份有限公司

設計驗證
工程課
2025-01-14
發行
鈺緯科技開發股份有限公司

廠　　牌: AMAZING

品名規格: AZ1045-04F.R7G

客戶料號: 3DTAZ10451Y (D0172)

日　　期: 2024/12/30

SALES : 許 廷 宇 Joe *Hsu*　　*艾睿電子股份有限公司　　啟*

艾睿電子股份有限公司 發票專用章

AZ1045-04F

Ultra Low Capacitance ESD Protection Array For High Speed I/O Port

Features

- ESD Protect for Transition Minimized Differential Signaling (TMDS) channels
- Protects four I/O lines
- Provide ESD protection for each line to
  IEC 61000-4-2 (ESD) ±15kV (air), ±10kV (contact)
  IEC 61000-4-5 (Lightning) 3.5A (8/20μs)
- **For operating voltage of 5V and below**
- **Ultra low capacitance : 0.5pF typical**
- Fast turn-on and Low clamping voltage
- Array of ESD rated diodes with internal equivalent TVS (Transient Voltage Suppression) diode
- Simplified layout for HDMI connectors
- Solid-state silicon-avalanche and active circuit triggering technology
- ***Green part***

Applications

- **High Definition Multi-Media Interface (HDMI) 1.3 & 1.4 version**
- **DisplayPort interface**
- **SATA and eSATA interface**
- **USB3.0**
- Digital Visual Interface (DVI)
- USB2.0 up to 480Mb/s
- IEEE 1394 up to 3.2 Gb/s
- Ethernet port: 10/100/1000 Mb/s
- Desktop and Notebooks PCs
- Consumer Electronics
- Set Top Box
- DVDRW Players
- Graphics Cards

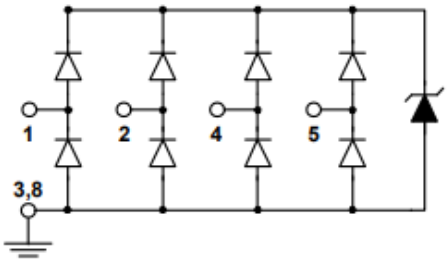
Description

AZ1045-04F is a design which includes ESD rated diode arrays to protect high speed data interfaces. The AZ1045-04F has been specifically designed to protect sensitive components which are connected to data and transmission lines from over-voltage caused by Electrostatic Discharging (ESD).

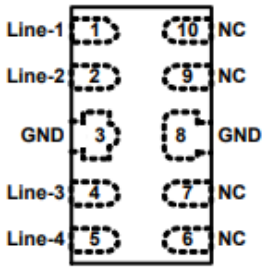
AZ1045-04F is a unique design which includes ESD rated, ultra low capacitance steering diodes and a unique design of clamping cell which is an equivalent TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the internal ESD line or to ground line. The internal unique design of clamping cell prevents over-voltage on the internal ESD line and on the I/O line, which is protecting any downstream components.

AZ1045-04F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 (±15kV air, ±8kV contact discharge).

Circuit Diagram



Pin Configuration



DFN2510P10E (Top View)

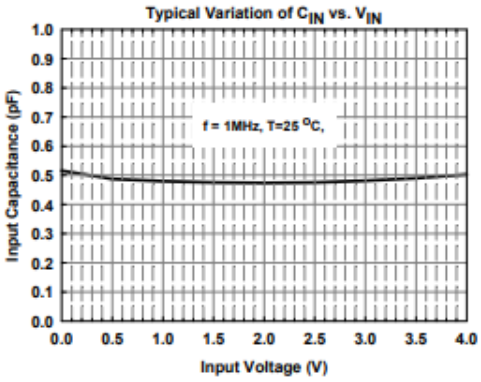
 ©2013 Amazing Micro.

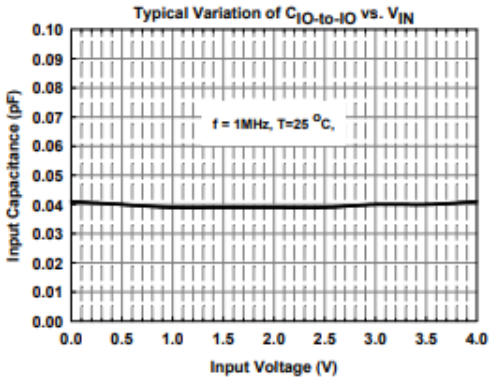
SPECIFICATIONS

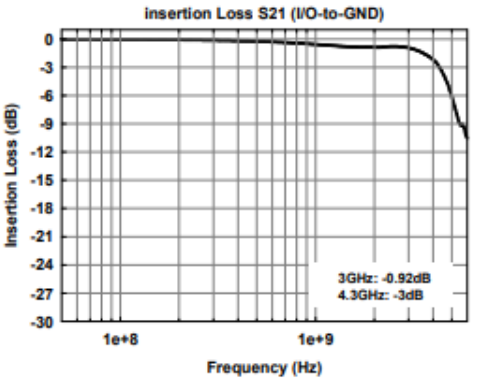
ABSOLUTE MAXIMUM RATINGS			
PARAMETER	**SYMBOL**	**RATING**	**UNITS**
Peak Pulse Current (tp =8/20μs)	I_{PP}	3.5	**A**
Peak Pulse Power (tp =8/20μs)	P_{PP}	30	**W**
Operating Voltage (I/O pin-GND)	V_{DC}	(GND – 0.5) to 6	**V**
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	15 10	**kV**
Lead Soldering Temperature	T_{SOL}	260 (10 sec.)	**°C**
Operating Temperature	T_{OP}	-55 to +85	**°C**
Storage Temperature	T_{STO}	-55 to +150	**°C**

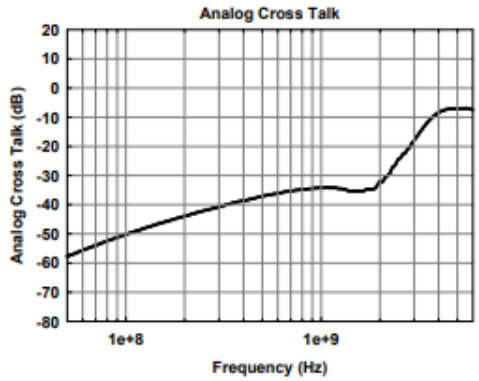
ELECTRICAL CHARACTERISTICS						
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Reverse Stand-Off Voltage	V_{RWM}	Pin-1,-2,-4,-5 to pin-3,-8, T=25 °C			5	**V**
Channel Leakage Current	$I_{CH-Leak}$	$V_{Pin-1,-2,-4,-5}$ = 5V, $V_{Pin-3,-8}$ = 0V, T=25 °C			1.5	**μA**
Reverse Breakdown Voltage	V_{BV}	I_{BV} = 1mA, T=25 °C, Pin-1,-2,-4,-5 to pin-3,-8	6			**V**
Forward Voltage	V_F	I_F = 15mA, T=25 °C, pin-3,-8 to pin-1,-2,-4,-5		0.9	1.1	**V**
ESD Clamping Voltage	V_{clamp}	IEC 61000-4-2 +6kV,T=25 °C, Contact mode, any I/O pin to Ground		12		**V**
ESD Dynamic Turn-on Resistance	$R_{dynamic}$	IEC 61000-4-2, 0~+6kV,T=25 °C, Contact mode, any I/O pin to Ground		0.3		**Ω**
Channel Input Capacitance	C_{IN}	$V_{pin-3,-8}$ = 0V,**V_{IN} = 2.5V**,f = 1MHz,T=25 °C, any I/O pin to Ground		0.5	0.65	**pF**
Channel to Channel Input Capacitance	C_{CROSS}	$V_{pin-3,-8}$ = 0V, **V_{IN} = 2.5V**, f = 1MHz, T=25 °C , between I/O pins		0.04	0.08	**pF**

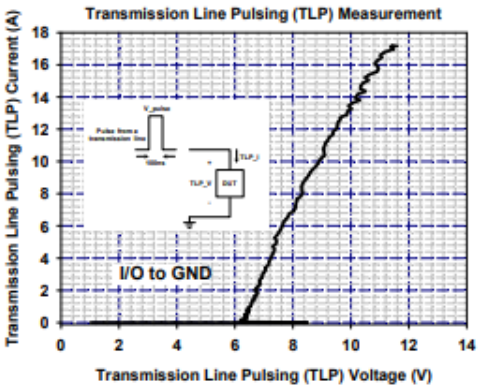
Typical Characteristics











Applications Information

A. Device Connection

The AZ1045-04F is designed to protect four data lines from transient over-voltage (such as ESD stress pulse). The device connection of AZ1045-04F is shown in the Fig. 1. In Fig. 1, the four protected data lines are connected to the ESD protection pins (pin1, pin2, pin4, and pin5) of AZ1045-04F. The ground pins (pin3 and pin8) of AZ1045-04F are the negative reference pins. These pins should be directly connected to the GND rail of PCB (Printed Circuit Board). To get minimum parasitic inductance, the path length should keep as short as possible.

AZ1045-04F can provide ESD protection for 4 I/O signal lines simultaneously. If the number of I/O signal lines is less than 4, the unused I/O pins can be simply left as NC pins.

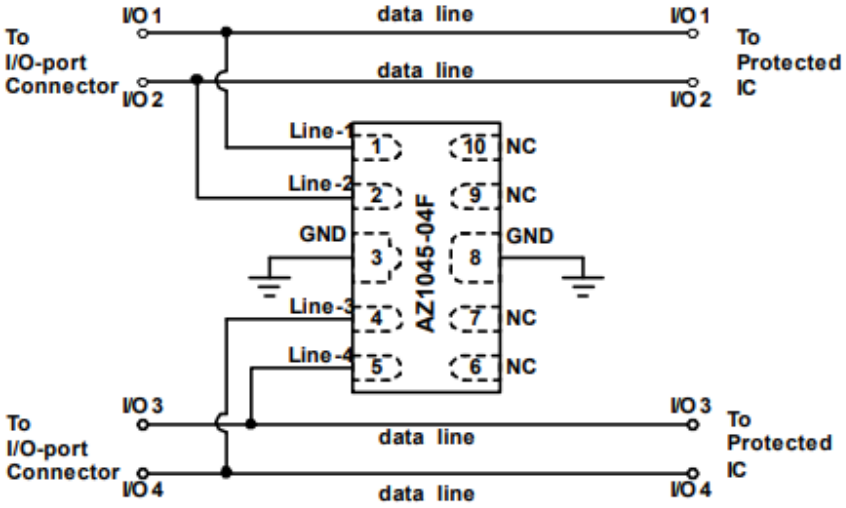


Fig. 1 Data lines connection of AZ1045-04F.

B. Application

AZ1045-04F is designed for protecting high speed I/O ports from over-voltage caused by Electrostatic Discharging (ESD). Thus, a lot of kinds of high speed I/O ports can be the applications of AZ1045-04F, especially, the HDMI port.

HDMI Protection for High and Low speed signals

The HDMI Compliance Test Specification (CTS) requires sink (receiver) ports maintain a differential impedance of 100 Ohms +/- 15%.

ESD protection devices have an inherent junction capacitance. Even a small amount of added capacitance on a HDMI port will cause the impedance of the differential pair to drop. Thus, some form of compensation to the layout will be required to bring the differential pairs back within the required 100 Ohm +/- 15% range. The higher the added capacitance, the more extreme the modifications will need to be. If the added capacitance is too high, compensation may not even be possible. The AZ1045-04F presents **0.5pF** capacitance to each differential signal while being rated to handle >8kV ESD contact

discharges (>15kV air discharge) as outlined in IEC 61000-4-2. Therefore, it is possible to **make none** adjustment to the board layout parameters to compensate for the added capacitance of the AZ1045-04F. Figure 2 shows how to implement the AZ1045-04F in a HDMI application.

The AZ1045-04F is designed for allowing the traces to run straight through the device to simplify the PCB layout. As shown in Figure 2, the best way to design the PCB trace is using the flow through layout. The solid line represents the PCB trace. Note that the PCB traces are used to connect the pin pairs for each line (pin 1 to pin 10, pin 2 to pin 9, pin 4 to pin 7, pin 5 to pin 6). For example, line 1 enters at pin 1 and exits at Pin 10 and the PCB trace connects pin 1 and 10 together. Lines 2, 3, and 4 have the same way of connection. The ground pins (pin3 and pin8) of AZ1045-04F are the negative reference pins. These pins should be directly connected to the GND plane of PCB. To get minimum parasitic inductance, the path length should keep as short as possible. **In Figure 2, the none-TMDS signals, DDC_CLK, DDC_DAT, CE_REMOTE, and HOTPLUG_DET, can be protected with another low cost part, e.g., AZC199-04S.**

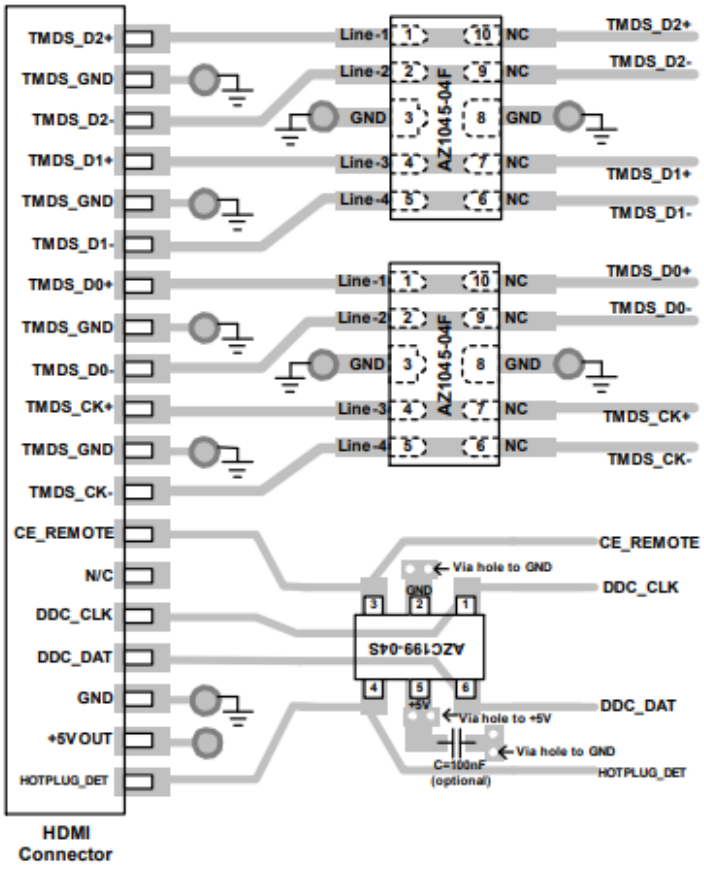


Fig. 2 HDMI Protection for High and Low speed signals.

C. Measurement Results on a HDMI port

Fig. 3a and 3b show the test boards for measuring the differential impedance of a HDMI port without using ESD protection array, and with using AZ1045-04F ESD protection array, respectively.

Fig. 4 shows the differential impedance measurement results. The range of the differential impedance without ESD protection array on it is from 96Ω to 106Ω, which meets the spec of 100 Ohms +/- 15%. And the range of the differential impedance with AZ1045-04F ESD protection array on it is from 88.9Ω to 104Ω, which still meets the spec of 100 Ohms +/- 15%. From the measured results shown in Fig. 4, the degradation of the differential impedance induced by the parasitic effects of AZ1045-04F is at the range of 12.8Ω to 14.2Ω. This demonstrates when the PCB differential impedance is designed at around 105Ω, then **none** adjustment to the board layout parameters is needed to compensate for the added ultra small capacitance of the AZ1045-04F and the test results can pass the spec of 100Ω +/- 15%.

Fig. 5 shows the HDMI Eye Diagram performance when the AZ1045-04F is under used. No apparent affection is shown due to the low capacitance feature of the AZ1045-04F.

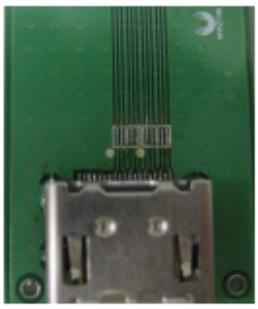


Fig. 3a The test board for measuring the differential impedance of a HDMI port without using ESD protection array.



Fig. 3b The test board for measuring the differential impedance of a HDMI port with using ESD protection array, AZ1045-04F.

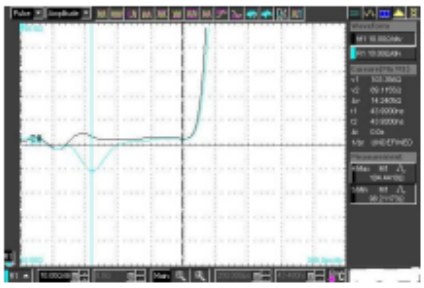


Fig. 4a The measured differential impedance of Data0- and Data0+ (103.3Ω without ESD protection array, and 89.1Ω with AZ1045-04F).

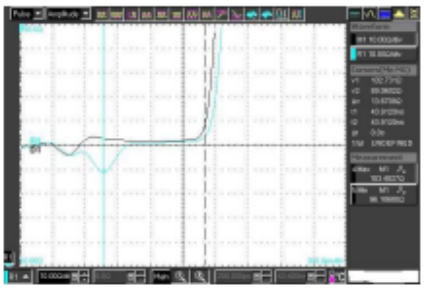


Fig. 4b The measured differential impedance of Data1- and Data1+ (102.7Ω without ESD protection array, and 89.1Ω with AZ1045-04F).

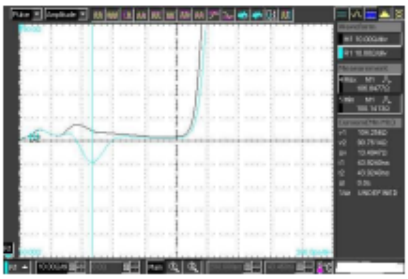


Fig. 4c The measured differential impedance of Data2- and Data2+ (104.2Ω without ESD protection array, and 90.8Ω with AZ1045-04F).

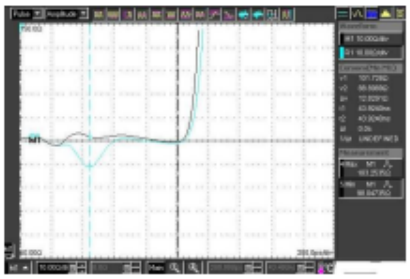


Fig. 4d The measured differential impedance of Clock- and Clock+ (101.7Ω without ESD protection array, and 88.9Ω with AZ1045-04F).

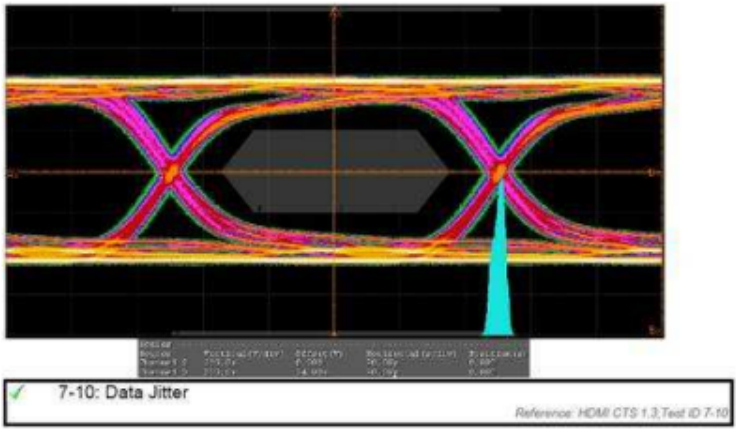
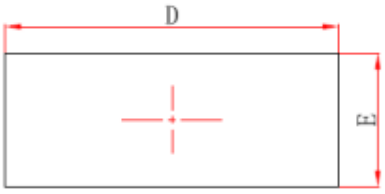
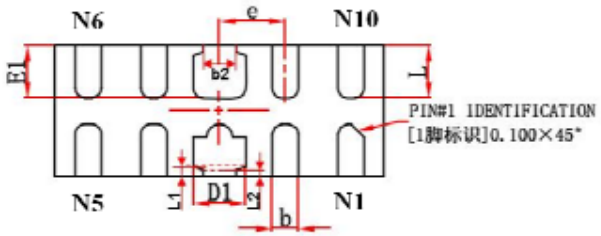


Fig. 5 the HDMI Eye Diagram performance when the AZ1045-04F is under used. No apparent affection is shown due to the low capacitance feature of the AZ1045-04F.

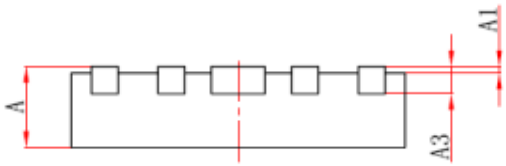
PACKAGE OUTLINE (DFN2510P10E)



TOP VIEW (unit in mm)



BOTTOM VIEW (unit in mm)



SIDE VIEW (unit in mm)

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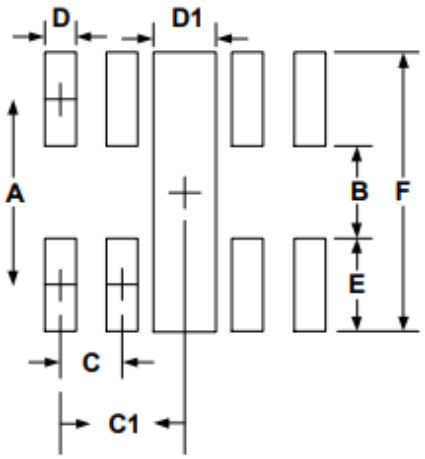
Symbol	Millimeters		Inches	
	min	max	min	max
A	0.40	0.55	0.016	0.022
A1	0.00	0.05	0.000	0.002
A3	0.152REF.		0.006 BSC	
D	2.45	2.55	0.096	0.100
E	0.95	1.05	0.037	0.041
D1	0.35	0.45	0.014	0.018
E1	0.35	0.45	0.014	0.018
b	0.15	0.25	0.006	0.010
e	0.5 BSC		0.019 BSC	
L1	0.075 REF		0.0029 REF	
L2	0.05 REF		0.0019 REF	
b2	0.20	0.30	0.0079	0.012
L	0.35	0.45	0.014	0.018

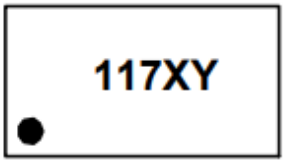
LAND LAYOUT



Dimensions		
Index	**Millimeter**	**Inches**
A	0.875	0.034
B	0.20	0.008
C	0.50	0.02
C1	1.00	0.039
D	0.25	0.01
D1	0.4	0.016
E	0.675	0.027
F	1.55	0.061

Notes:
This LAND LAYOUT is for reference purposes only. Please consult your manufacturing partners to ensure your company's PCB design guidelines are met.

MARKING CODE



117 = Device Code
X = Date Code
Y= Control Code

Part Number	Marking Code
AZ1045-04F (Green part)	**117XY**

Note. Green means Pb-free, RoHS, and Halogen free compliant.

Ordering Information

PN#	Material	Type	Reel size	MOQ/interal box	MOQ/carton
AZ1045-04F.R7G	Green	T/R	7 inch	4 reel= 12,000/box	6 box =72,000/carton

Revision History

Revision	Modification Description
Revision 2008/12/09	Preliminary Release.
Revision 2009/01/16	The Initial Formal Release.
Revision 2009/05/15	Correct the typos at Package Outline.
Revision 2009/06/10	1. Correct the typos at the ABSOLUTE MAXIMUM RATINGS. 2. Update the information of the measurement results on a HDMI port.
Revision 2009/09/08	1. Update the bottom view indication of the Package Outline. 2. Update the "D" value of Land Layout.
Revision 2009/11/25	Increase the Lightning (8/20μs) spec.
Revision 2009/12/26	Update the PACKAGE DIMENSIONS.
Revision 2011/05/05	1. Update the Company Logo. 2. Add the Ordering Information.
Revision 2011/07/16	Add the Applications of USB3.0 and HDMI 1.4 version.
Revision 2012/02/09	Modify the Bottom View of Package Outline to add three parameters, b2, L1, and L2.
Revision 2012/03/23	Add Fig. 5 of HDMI Eye Diagram.
Revision 2012/06/05	Update the diagram of the Pin Configuration on page 1.
Revision 2013/03/08	Update the "A" value of Package Outline.

MATERIAL Composition

Product name：AZ1045-04F.R7G
Part total weight：3.9mg
Release date :2020/2/20

Composition part□ 構成部件	Supplier 供应商	Material Name.□ 部件材質名	Element name composition □ 構成之元素名稱	CAS No.	Substance Mass(mg)		ICP Test Report No.	ICP TEST Date	Test Result										SGS Report	MSDS Report
					mass(mg)	%			Cd	Pb	Hg	Cr^{+6}	PBB	PBDE	Br	Cl	PFOA	PFOS		
Wafer	Wavetek	……	Silicon	7440-21-3	0.106200	100.00%	ETR23C04171 ETR23C04174 ETR23C04172	2024/1/5	N.D.	N.D.	ND	ND	ND	ND	ND	ND	ND	ND		
	Episil	……	Silicon	7440-21-3		100.00%	ETR24805457	2024/9/5	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND		
	Nuvoton	……	Silicon	7440-21-3		100.00%	ETR24303083	2024/3/21	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND		
	PSMC	……	Silicon	7440-21-3		100.00%	ETR24800011	2024/8/8	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND		
Lead Frame	QPL	Al94	Copper	7440-50-8	1.354527	96.49%	CANEC24017899601 CANEC24017931201	2024/9/4 2024/9/3	ND	19	ND	ND	ND	ND	ND	ND	ND	ND	 	
			Iron	7439-89-6	0.032287	2.30%														
			phosphorus	7723-14-0	0.001404	0.10%														
			Zinc	7440-66-6	0.001404	0.10%														
			Lead	7439-92-1	0.000140	0.01%														
			Silver	7440-22-4	0.014038	1.00%														
	寶雞華天機械	C194	Copper	7440-50-8	1.337751	95.30%	CANEC24013270701 CANEC24018784101	2024/7/15 2024/9/4	ND	18	ND	ND	ND	ND	ND	ND	ND	ND	 	
			Iron	7439-89-6	0.035095	2.50%														
			Phosphorus	7723-14-0	0.001404	0.10%														
			Zinc	7440-66-6	0.001404	0.10%														
			Silver	7440-22-4	0.028076	2.00%														
			Lead	7439-92-1	0.000070	0.01%														
Epoxy	Henkel	ATB-F125E	Silicon dioxide	7631-86-9	0.090000	60.00%	ETR24300158 ETR24300155 ETR24300159	2024/3/7	ND	ND	ND	ND	ND	ND	ND	91.3	ND	ND	  	
			Modified Epoxy Resin	Proprietary	0.022500	15.00%														
			], a-hydro-w-hydroxy-, ether with 2-eth	244772-00-7	0.015000	10.00%														
			Phenol-formaldehyde polymer	9003-35-4	0.015000	10.00%														
			epichlorhydrin); epoxy resin (number a	25068-38-6	0.007500	5.00%														
Wire	Ningbo Kangqiang	KCB	Aurum	7440-57-5	0.169983	99.99%	NCBEC24006799501	2024/11/27	ND	ND	ND	ND	ND	ND	ND	ND	ND	ND		
			Others	/	0.000017	0.01%														
Mold Compound	RESCNAC	CEL-9220HF10	Epoxy Resin 1	Trade secret	0.009500	0.50%	SHAEC24024777905 SHAEC24024777910	2024/11/11	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	N.D.	 	
			Epoxy Resin 2	Trade secret	0.009500	0.50%														
			Epoxy Resin 3	Trade secret	0.009500	0.50%														
			Phenolic Resin	Trade secret	0.038000	2.00%														
			Catalyst	Trade secret	0.000950	0.05%														
			Carbon black	1333-86-4	0.003800	0.20%														
			Amorphous silica1	60676-86-0	1.735650	91.35%														
			Amorphous silica2	7631-86-9	0.093100	4.90%														
Plating	ALSEN	Tin	Tin	7440-31-5	0.169983	99.99%	SHAEC24010829503	2024/5/29	ND	14	ND	ND	ND	ND	ND	ND	ND	ND		
			Others	/	0.000009	0.01%														
Total mass (mg)					3.9000															

N.D.=Not detected