Genesys Logic, Inc.

GL854G-65

USB 2.0 MTT 7-Port Hub Controller

Datasheet

Revision 1.10
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Revision	Date	Description
1.00	12/29/2023	First formal release
1.10	03/15/2024	Add pin description and port configuration information

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CHAPTER 1 GENERAL DESCRIPTION

GL854G is Genesys Logic's premium 7-port hub solution which fully complies with Universal Serial Bus Specification Revision 2.0. GL854G implements multiple TT* *(Note1)* architecture that provide dedicated TT* to each downstream (DS) ports, which guarantee Full-Speed(FS) data passing bandwidth when multiple FS device perform heavy loading operations. The controller inherits Genesys Logic's cutting edge technology on cost and power efficient serial interface design. GL854G has proven compatibility, lower power consumption figure and better cost structure above all USB 2.0 hub solutions worldwide.

GL854G implements multiple hub configuration features onto internal mask ROM, which traditionally requires external EEPROM. The microprocessor detects general purpose I/O (GPIO) status during the initial stage to configure hub settings such as (1) declare of compound device (2) gang/individual mode selection…etc. External EEPROM can be removed if no vendor specified PID/VID or product string is required for the application.

GL854G provides 12MHz clock output that can be used as a reference clock source for multi-chip, hub compound applications. The output clock provides enough driving capacity to support up to 2 devices that connected to the downstream port. The chip-to-chip clock trace is relatively sensitive to PCB noise. Please refer to design guide for PCB layout suggestions.

*Note 1: TT (transaction translator) is the main traffic control engine in an USB 2.0 hub to handle the unbalanced traffic speed between the upstream port and the downstream ports.

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CHAPTER 2 FEATURES

- Multiple Chip Package (MCP) architecture
  - Integrates two standard USB 4-port hub silicon dies into single chip
  - Supports 7 USB 2.0 compliant downstream ports
- Multiple Transaction Translator (MTT)
  - Provides dedicated TT control logics for each downstream port
  - Superior performance when multiple FS devices operate concurrently
- Compliant with USB specification Revision 2.0
  - Upstream port supports both high-speed (HS) and full-speed (FS) traffic
  - Downstream ports support HS, FS, and low-speed (LS) traffic
  - Backward compatible to USB specification Revision 1.1
  - Each downstream port supports status indicator, with automatic and manual modes
  - Conform to self power and bus power requirements
- Integrated USB transceiver
  - Compliant with USB electrical requirements
  - Ultralow power consumption
  - Improve output drivers with slew-rate control for EMI reduction
  - Internal power-fail detection for ESD recovery
- On-chip 8-bit micro-processor
  - Support customized PID, VID by reading external EEPROM/ SMBUS
  - Support downstream port configuration by reading external EEPROM/ SMBUS
- Smart power management features
  - Support individual / gang mode over-current detection for all downstream ports
  - Automatic switching between self-powered and bus-powered modes
- Lower BOM cost
  - Single external 12 MHz crystal / Oscillator clock input
  - On-chip 5V to 3.3V power regulator
  - Built-in upstream port 1.5KΩ pull-up and downstream port 15KΩ pull-down resistors
  - Support low-cost 24C02 EEPROM
- Features for hub compound applications
  - Support compound-device (non-removable in downstream ports) by SMBUS / EEPROM / IO Strapping
  - Provide 12MHz clock source for other USB device connected to the downstream ports
- Available package type: 64 pin LQFP package (7x7mm)
- Applications:
  - UMPC/MID, motherboard on-board applications
  - Consumer electronics built-in hub application
  - Monitor built-in hub
  - Embedded systems
  - Hub compound applications

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CHAPTER 3 PIN ASSIGNMENT

3.1 Pin-out

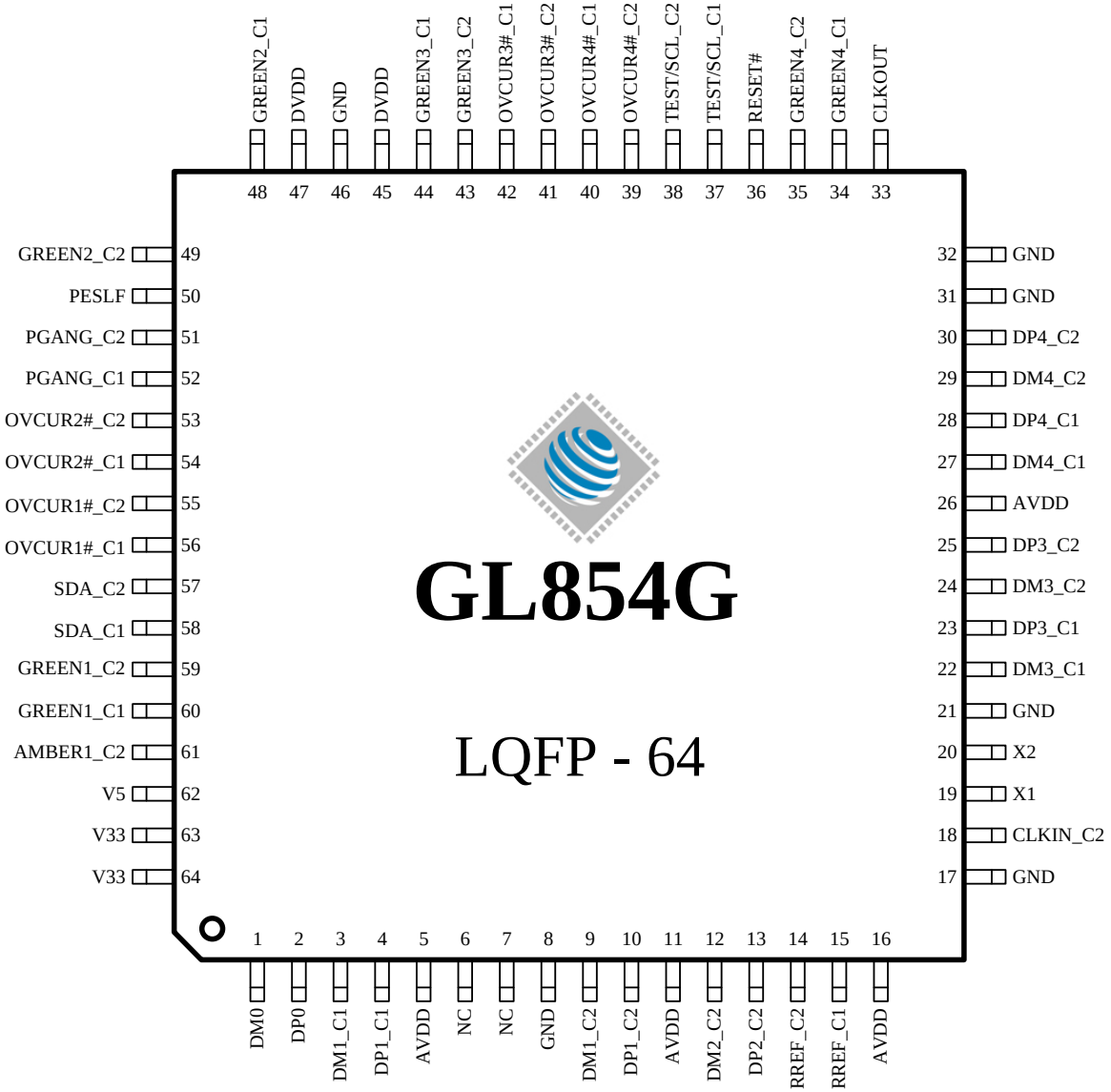

Figure 3.1 - GL854G 64 Pin LQFP Pin-out Diagram

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3.2 Pin List

Table 3.1 - GL854G 64 Pin List

Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type
1	DM0	B	17	GND	P	33	CLKOUT	O	49	GREEN2_C2	B
2	DP0	B	18	CLKIN_C2	I	34	GREEN4_C1	B	50	PSELF	I_5V
3	DM1_C1	B	19	X1	I	35	GREEN4_C2	B	51	PGANG_C2	B
4	DP1_C1	B	20	X2	O	36	RESET#	I_5V	52	PGANG_C1	B
5	AVDD	P	21	GND	P	37	TEST/SCL_C1	B	53	OVCUR2#_C2	I_5V
6	NC	-	22	DM3_C1	B	38	TEST/SCL_C2	B	54	OVCUR2#_C1	I_5V
7	NC	-	23	DP3_C1	B	39	OVCUR4#_C2	I_5V	55	OVCUR1#_C2	I_5V
8	GND	P	24	DM3_C2	B	40	OVCUR4#_C1	I_5V	56	OVCUR1#_C1	I_5V
9	DM1_C2	B	25	DP3_C2	B	41	OVCUR3#_C2	I_5V	57	SDA_C2	B
10	DP1_C2	B	26	AVDD	P	42	OVCUR3#_C1	I_5V	58	SDA_C1	B
11	AVDD	P	27	DM4_C1	B	43	GREEN3_C2	B	59	GREEN1_C2	B
12	DM2_C2	B	28	DP4_C1	B	44	GREEN3_C1	B	60	GREEN1_C1	B
13	DP2_C2	B	29	DM4_C2	B	45	DVDD	P	61	AMBER1_C2	B
14	RREF_C2	A	30	DP4_C2	B	46	GND	P	62	V5	P/I
15	RREF_C1	A	31	GND	P	47	DVDD	P	63	V33	P/O
16	AVDD	P	32	GND	P	48	GREEN2_C1	B	64	V33	P/O

3.3 Pin Descriptions

Table 3.2 - Pin Descriptions

USB Interface			
Pin Name	**Pin Number**	**I/O Type**	**Description**
DM0 DP0	1, 2	B	USB signals for USPORT
DM1_C1 DP1_C1	3, 4	B	USB signals for DSPORT1 of 1-tier hub
DM3_C1 DP3_C1	22, 23	B	USB signals for DSPORT3 of 1-tier hub
DM4_C1 DP4_C1	27, 28	B	USB signals for DSPORT4 of 1-tier hub
DM1_C2 DP1_C2	9,10	B	USB signals for DSPORT1 of 2-tier hub
DM2_C2 DP2_C2	12,13	B	USB signals for DSPORT2 of 2-tier hub
DM3_C2 DP3_C2	24, 25	B	USB signals for DSPORT3 of 2-tier hub

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DM4_C2 DP4_C2	29, 30	B	USB signals for DSPORT4 of 2-tier hub
RREF_C1 RREF_C2	15, 14	A	Ref. resistor for 1-tier and 2-tier hub. (C1=1-tier, C2=2-tier) Resistor value of 680Ω should be connected between RREF pin and ground (GND).

Note: USB signals must be carefully handled in PCB routing. For detailed information, please refer to **USB 2.0 Hub Design Guide**.

Hub Interface			
Pin Name	**Pin Number**	**I/O Type**	**Description**
OVCUR1#~4#_C1	56, 54, 42, 40	I_5V	Active low. Over current indicator for 1-tier hub's DSPORT1~4 OVCUR1# is the only over current flag for GANG mode. *In reset state: OVCUR1#_C1 will be 1-tier hub's SMC; OVCUR2#_C1 will be 1-tier hub's SMD Pulled-high to enable port, pulled-down to disable port, and floating to set non-removable port
OVCUR1#~4#_C2	55, 53, 41, 39	I_5V	Active low. Over current indicator for 2-tier hub's DSPORT1~4 OVCUR1# is the only over current flag for GANG mode. *In reset state: OVCUR1#_C2 will be 2-tier hub's SMC; OVCUR2#_C2 will be 2-tier hub's SMD Pulled-high to enable port, pulled-down to disable port, and floating to set non-removable port
GREEN1~4_C1	60, 48, 44, 34	B (pd)	Green LED indicator for 1-tier hub's DSPORT1~4
GREEN1~4_C2	59, 49, 43, 35	B (pd)	Green LED indicator for 2-tier hub's DSPORT1~4
PSELF	50	I_5V (pu)	Self-powered detection for 1-tier and 2-tier hub. * PSELF should be pull-high concurrently
PGANG_C1 PGANG_C2	52 51	B	Strapping pin for gang / individual mode selection. (input mode) Host Suspend notification output pin (output mode) Gang input:1, output: 0@normal, 1@suspend Individual input:0, output: 1@normal, 0@suspend * Details please check: Chapter 5, 5.2

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Others Interface			
Pin Name	**Pin Number**	**I/O Type**	**Description**
X1	19	I	Crystal / OSC clock input (for 1-tier hub)
X2	20	O	Crystal clock output. (for 1-tier hub)
CLKOUT	33	O	On-chip PLL output (12MHz output)
CLKIN_C2	18	I	OSC clock input (for 2-tier hub)
RESET#	36	I_5V	Active low. External reset input, default pull high 10KΩ When RESET# = low, whole chip is reset to the initial state
TEST/SCL_C1 SDA_C1	37, 58	B	I2C EEPROM interface for 1-tier hub *TEST/SCL pin cannot pull-high during initial stage to prevent hub get into test mode
TEST/SCL_C2 SDA_C2	38, 57	B	I2C EEPROM interface for 2-tier hub *TEST/SCL pin cannot pull-high during initial stage to prevent hub get into test mode
NC	6,7	-	Reserved *Not connected

Power / Ground			
Pin Name	**Pin Number**	**I/O Type**	**Description**
AVDD	5,11,16, 26	P	3.3V analog power input for analog circuits.
DVDD	45,47	P	3.3V digital power input for digital circuits
GND	8,17,21,31, 32,46,	P	Ground
V5	62	P/I	5V Power input. This pin should be provided 3.3V while using external regulator.
V33	63,64	P/O	5V-to-3.3V regulator Vout & 3.3 input

*Note: Analog circuits are quite sensitive to power and ground noise. PCB layout must take care the power routing and the ground plane. For detailed information, please refer to **USB 2.0 Hub Design Guide**.

Notation:

Type	**O**	Output
	I	Input
	I_5V	Input_5V tolerance
	B	Bi-directional
	P	Power / Ground
	pu	Internal pull up
	pd	Internal pull down
	P/I	Power input
	P/O	Power output

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CHAPTER 4 BLOCK DIAGRAM

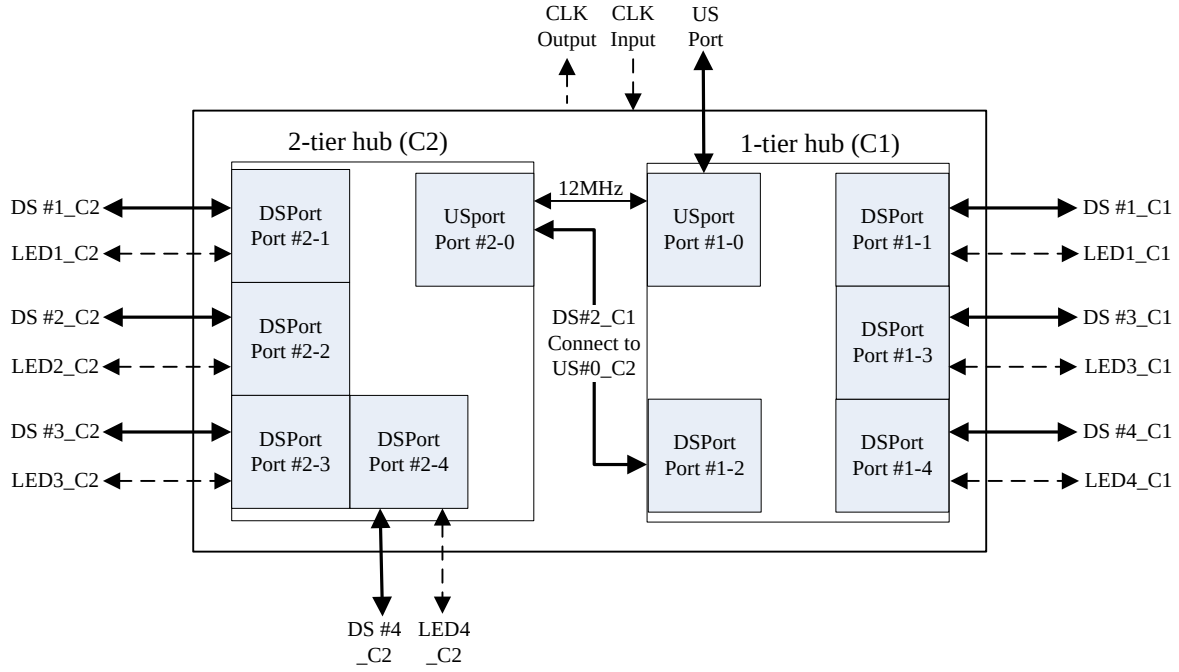

Figure 4.1 - GL854G Block Diagram (Multiple TT)

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CHAPTER 5 FUNCTION DESCRIPTION

5.1 General Hub Functions

5.1.1 MCP Architecture

GL854G leverages multi-chip package (MCP) technology that incorporates two USB 4-port hubs onto a standard 7x7mm 64 pin LQFP package to provide 7 downstream ports that fully compliant to USB 2.0 specifications. The 1-tier hub's PLL integrates on-chip clock output for 2-tier hub's reference clock, therefore, only one external 12MHz crystal is required for GL854G whole chip operation.

5.1.2 USB Transceiver

USB transceiver is the analog circuit to support USB electrical requirements. GL854G integrated all USPORT (upstream port) and DSPORT (downstream port) transceivers into single chip.

USPORT supports both full-speed and high-speed electrical characteristics defined in chapter 7 of USB specification Revision 2.0. USPORT transceiver will operate in full-speed electrical signaling when GL854G is plugged into a 1.1 host/hub. USPORT transceiver will operate in high-speed electrical signaling when GL854G is plugged into a 2.0 host/hub.

DSPORT supports high-speed, full-speed, and low-speed electrical characteristics defined in chapter 7 of USB specification Revision 2.0. In addition, each DSPORT transceiver accurately controls its own squelch level to detect the detachment and attachment of devices.

5.1.3 Multiple-TT Architecture

Transaction Translator (TT) implements the control logic defined in section 11.14 ~ 11.22 of USB specification Revision 2.0. TT basically handles the unbalanced traffic speed between the USPORT (operating in HS) and DSPORTS (operating in FS/LS) of hub. GL854G implements multiple-TT architecture that provide dedicated TT and control logic to each downstream (DS) ports, which guarantee Full-Speed(FS) data passing bandwidth when multiple FS device perform heavy loading operations.

5.1.4 Port Power Control

An USB hub is required to report DSPORT power status to host in case of any over-current event occurs. GL854G can support either individual mode or gang mode over-current detection scheme. (Please check 5.2.2 for gang/individual mode configuration) For individual mode, one DSPORT over-current event does not affect other ports. The OVCUR# pin corresponding to each downstream port should be connected to a power fuse with 500mA+ max current tolerance. For gang mode, multiple ports share the same power protection circuit. For 7-port application, there are two options to gang power fuse: (1) One 1.5A+ power fuse for 1-tier hub DSPORT (port2~4_C1) and One 2A+ power fuse for 2-tier (port1~4_C2).

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5.1.5 Port Indicator

GL854G controls the LED lighting according to the flow defined in section 11.5.3 of Universal Serial Bus Specification Revision2.0. Both manual mode and Automatic mode are supported in GL854G. When GL854G is globally suspended, GL854G will turn off the LED to save power.

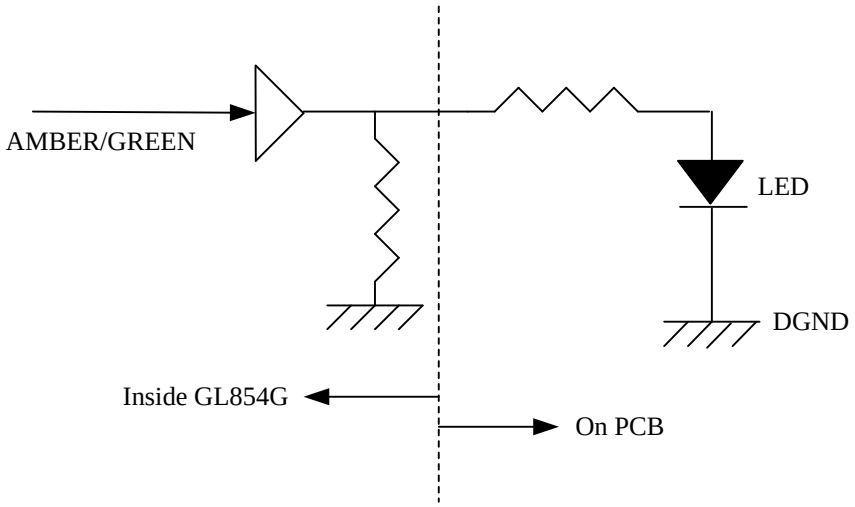

Figure 5.1 - LED Connection

5.1.6 Operation Scheme

5.1.6.1 Connected to USB 1.1 Host/Hub

If an USB 2.0 hub is connected to the downstream port of an USB 1.1 host/hub, it will operate in USB 1.1 mode. For an USB 1.1 hub, both upstream direction traffic and downstream direction traffic are passing through REPEATER. That is, the REPEATER/TT routing logic will route the traffic channel to the REPEATER.

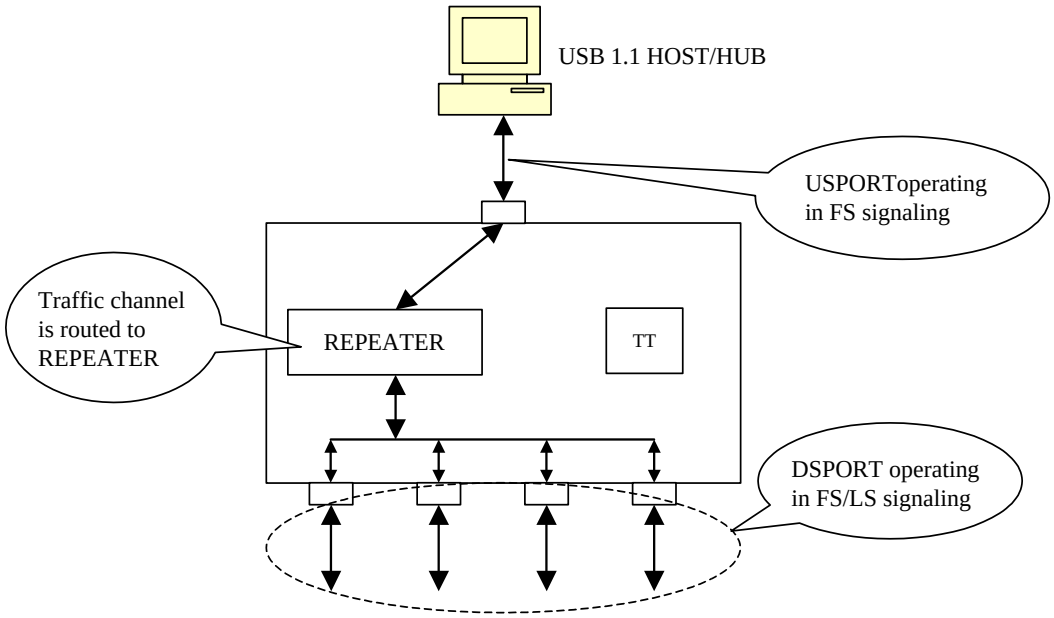

Figure 5.2 - Operating in USB 1.1 Scheme

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5.1.6.2 Connected to USB 2.0 Host/Hub

If an USB 2.0 hub is connected to an USB 2.0 host/hub, it will operate in USB 2.0 mode. The upstream port signaling is in high speed with bandwidth of 480 Mbps under this environment. The traffic channel will then be routed to the REPEATER when the device connected to the downstream port is signaling also in high speed. On the other hand, the traffic channel will then be routed to TT when the device connected to the downstream port is signaling in full/low speed.

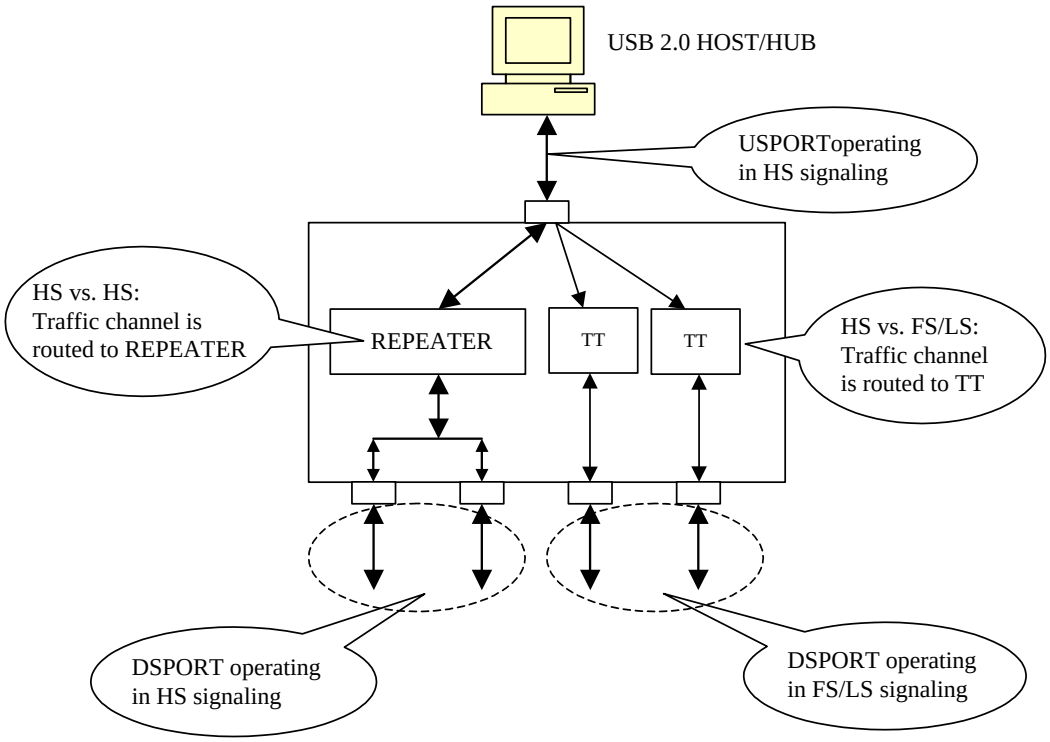

Figure 5.3 - Operating in USB 2.0 Scheme

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5.2 Configuration and I/O Settings

5.2.1 RESET Setting

GL854G's power on reset can either be triggered by external reset or internal power good reset circuit. The external reset pin, RESETJ, is connected to upstream port Vbus (5V) to sense the USB plug / unplug or 5V voltage drop. The reset trigger voltage can be set by adjusting the value of resistor R1 and R2 (Suggested value refers to schematics) GL854G's internal reset is designed to monitor silicon's internal core power (3.3V) and initiate reset when unstable power event occurs. The power on sequence will start after the power good voltage has been met, and the reset will be released after approximately 110~210 uS after power good.

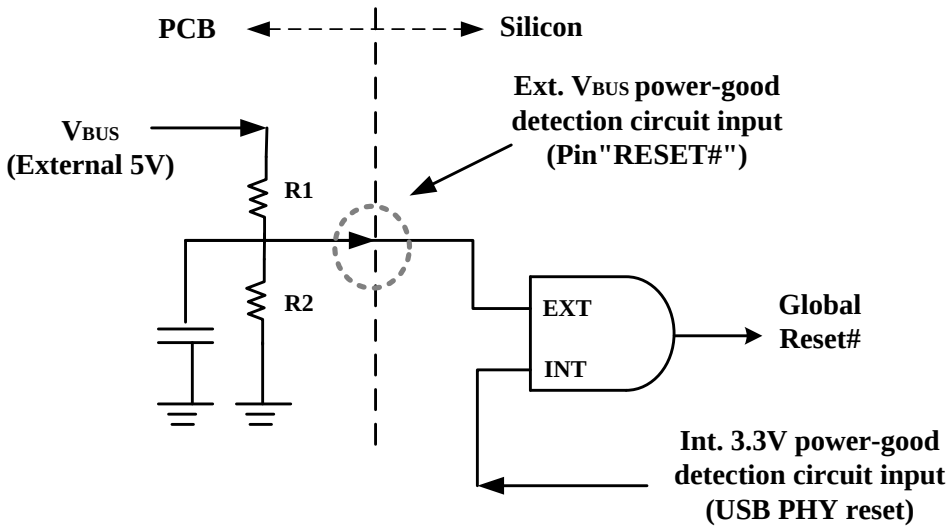

Figure 5.4 - Power on Reset Diagram

To fully control the reset process of GL854G, we suggest the reset time applied in the external reset circuit should longer than that of the internal reset circuit. Timing of POR is illustrated as below figure.

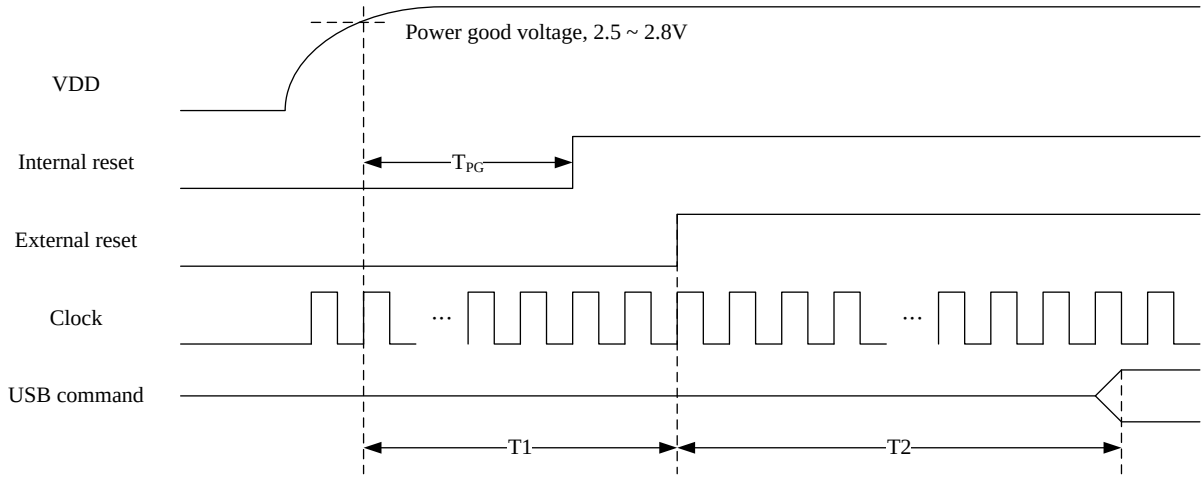

Figure 5.5 - Power on Sequence of GL854G

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Table 5.1 - Reset Timing

Symbol	Parameter	Min.	Max.	Unit
T_{PG}	VDD power up to internal reset (power good) assert	110	210	μs
T1	VDD power up to external reset (RESET#) assert	220	-	μs
T2	RESET assert to respond USB command ready	70	-	ms

To fully control the reset process of GL854G, we suggest the reset time applied in the external reset circuit should longer than that of the internal reset circuit.

5.2.2 PGANG/SUSPND Setting

To save pin count, GL854G uses the same pin to decide individual/gang mode as well as to output the suspend flag. The individual/gang mode is decided within 20us after power on reset. Then, about 50ms later, this pin is changed to output mode (as indicated in Figure 5.6). GL854G outputs the suspend flag once it is globally suspended. To setup individual mode, a pull-down resister should be placed, while gang mode on the contrary requires a pull high resister. The resistor value should be greater than 100KΩ. Figure 5.7 illustrate gang strapping and suspend LED indicator reference schematics. It should be noticed that the polarity of LED must be followed to prevent unwanted driving during host suspend.

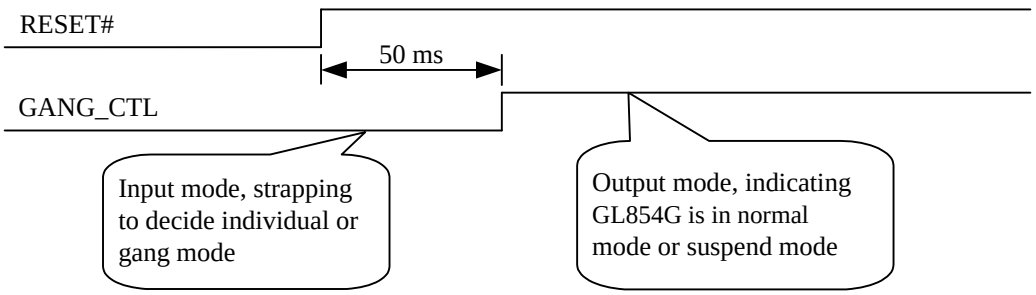

Figure 5.6 - Timing of PGANG/SUSPND Strapping

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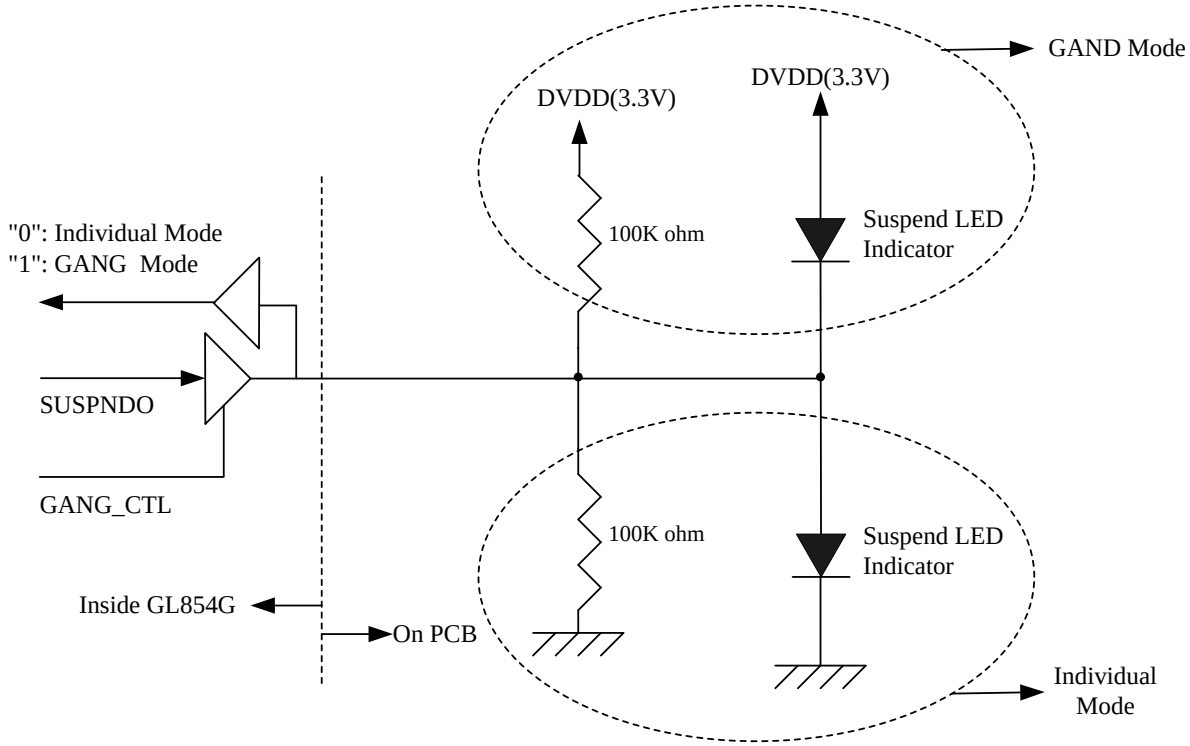

Figure 5.7 - GANG Mode Setting

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5.2.3 Power Control

GL854G targets 7-DFP hub application. It can only operate under self-power mode due to UFP Vbus maximum power supply (500mA) is not enough to support 7 DFPs operate concurrently (100/500mA per port x 7). To configure 1-tier and 2-tier hub into self-power mode, PSELF pin must be configured as a self-power hub (pull-high). Please check GL854G reference schematics for additional in formations.

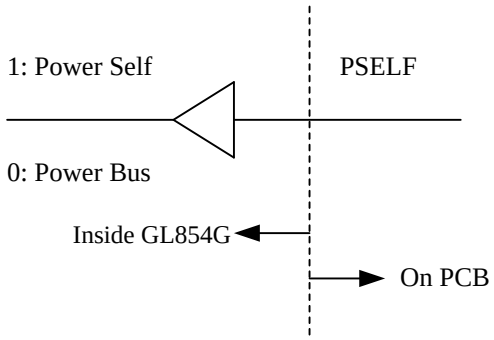

Figure 5.8 - SELF/BUS Power Setting

5.2.4 EEPROM Setting

GL854G provides flexibility to reply host with customer oriented PID/VID or desired hub settings through a low-cost 24C02 EEPROM. GL854G verifies the check sum after power on reset to make sure EEPROM content follows Genesys required format. If the check sum is correct, GL854G will take the configuration table that stored in EEPROM as part of the descriptor contents. In absence of external EEPROM, GL854G replies to host commands by the default settings in the internal ROM. The detail setting information please refers to the **USB 2.0 Hub AP Note_EEPROM Info** document.

5.2.5 Port Configuration

Downstream port can be configured (disabled) in following three ways:

1. I/O Strapping:

When OVCUR# pin of a downstream port is pulled or tied low to GND, the downstream port is disabled. Then, GL854G-65 will automatically rearrange logical port number and port order according to strapping results. Allowable port number configuration of GL854G-65 is shown in the following table.

Table 5.1 - Port Configuration

Physical Port Position		Port 1	Port 2	Port 3	Port 4
Logical Downstream Port Number	4 Ports Case	1	2	3	4
	3 Ports Case	1	2	3	Disabled
		1	2	Disabled	3
		1	Disabled	2	3
		Disabled	1	2	3
	2 Ports Case	1	2	Disabled	Disabled

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		1	Disabled	2	Disabled
		1	Disabled	Disabled	2
		Disabled	1	2	Disabled
		Disabled	1	Disabled	2
		Disabled	Disabled	1	2
	1 Port Case	1	Disabled	Disabled	Disabled
		Disabled	1	Disabled	Disabled
		Disabled	Disabled	1	Disabled
		Disabled	Disabled	Disabled	1
	0 Port Case (Illegal Case)	1	2	3	4

2. SMBUS (Refer to Chapter 5.2.7)
3. EEPROM (Refer to Chapter 5.2.4)

5.2.6 Non-removable Port Configuration

Non-removable setting of downstream port can be configured in following ways:

1. Pin-strapping, if OVCUR pin is floating, the port is set as non-removable.
2. SMBUS (Refer to Chapter 5.2.7)
3. EEPROM (Refer to Chapter 5.2.4)

5.2.7 SMBUS Mode (SMBUS Slave Address=0x2C)

GL854G-65 has two tiers of USB2 hubs cascading inside the chip. If using SMBUS to configure GL854G hub, both hubs need to be set separately. GL854G-65 enters SMBUS mode since Power-On occurs, and RESET# pin is asserted as well. After that, GL854G-65 will define OVCUR1# as SMC and OVCUR2# as SMD. GL854G-65 will exit the SMBUS mode since the RESET# pin is de-asserted. The more complicated settings such as PID, VID, power saving, port number, port non/removable, and downstream port electrical tuning can be configured by SMBUS.

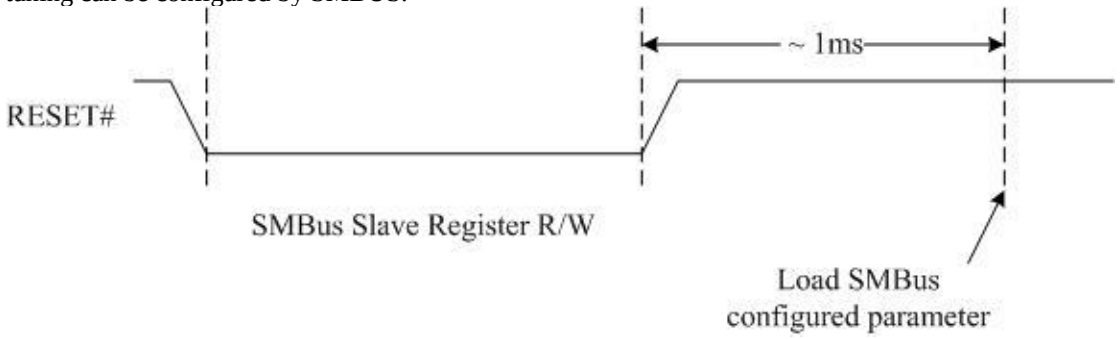

Figure 0.9 - SMBus Timing Diagram

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5.2.7.1 Internal Register Set

Table 0.3 - Internal Register Set

Address	Mnemonic	Register Description
00h	**VIDL**	Vendor ID LSB
01h	**VIDH**	Vendor ID MSB
02h	**PIDL**	Product ID LSB
03h	**PIDH**	Product ID MSB
04h	**CONFIG**	Hub non-removable configuration
08h	**VC_SR_JK_U**	Logical Upstream port HSTX electrical tuning option
09h	**VC_SR_JK_D1**	Logical Downstream port 1 HSTX electrical tuning option
0Ah	**VC_SR_JK_D2**	Logical Downstream port 2 HSTX electrical tuning option
0Bh	**VC_SR_JK_D3**	Logical Downstream port 3 HSTX electrical tuning option
0Ch	**VC_SR_JK_D4**	Logical Downstream port 4 HSTX electrical tuning option
0Dh	**DSCT_SQ_U**	Logical Upstream port HSRX electrical tuning option
0Eh	**DSCT_SQ_D1**	Logical Downstream port 1 HSRX electrical tuning option
0Fh	**DSCT_SQ_D2**	Logical Downstream port 2 HSRX electrical tuning option
10h	**DSCT_SQ_D3**	Logical Downstream port 3 HSRX electrical tuning option
11h	**DSCT_SQ_D4**	Logical Downstream port 4 HSRX electrical tuning option
2Bh	**DP12_PORT**	Physical Downstream port 1 & 2 enable/disable option
2Ch	**DP34_PORT**	Physical Downstream port 3 & 4 enable/disable option

5.2.7.2 VIDL – Vendor ID LSB

- Address: 00h
- Default value: E3h

Bit	Description
7:0	**VID[7:0]**, least significant byte of the Vendor ID

5.2.7.3 VIDH – Vendor ID MSB

- Address: 01h
- Default value: 05h

Bit	Description
7:0	**VID[15:8]**, most significant byte of the Vendor ID

5.2.7.4 PIDL – Product ID LSB

- Address: 02h
- Default value: 10h

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Bit	Description
7:0	**PID[7:0]**, least significant byte of the Product ID

5.2.7.5 PIDH – Product ID MSB

- Address: 03h
- Default value: 06h

Bit	Description
7:0	**PID[15:8]**, most significant byte of the Product ID

5.2.7.6 CONFIG – Hub non-removable Configuration

- Address: 04h
- Default value: 00h

Bit	Description
7:4	Reserved
3:0	Physical Downstream Port non-removable configuration '0' – Removable '1' – Non-removable Bit0: control physical downstream port 1 Bit1: control physical downstream port 2 Bit2: control physical downstream port 3 Bit3: control physical downstream port 4

5.2.7.7 VC_SR_JK_U – Logical Upstream Port HSTX Electrical Tuning Option

- Address: 08h
- Default value: 46h

Bit	Description
7	Logical Upstream port high speed transmitter D+/D- cross over point tuning option Default value: 1'b0
6:4	Logical Upstream port high speed transmitter slew rate control Default value: 3'b100
3:0	Logical Upstream port high speed transmitter JK level control Default value: 4'b0110

5.2.7.8 VC_SR_JK_D1 – Logical Downstream Port 1 HSTX Electrical Tuning Option

- Address: 09h
- Default value: 46h

Bit	Description
7	Logical Downstream port 1 high speed transmitter D+/D- cross over point tuning option Default value: 1'b0

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6:4	Logical Downstream port 1 high speed transmitter slew rate control Default value: 3'b100
3:0	Logical Downstream port 1 high speed transmitter JK level control Default value: 4'b0110

5.2.7.9 VC_SR_JK_D2 – Logical Downstream Port 2 HSTX Electrical Tuning Option

- Address: 0Ah
- Default value: 46h

Bit	Description
7	Logical Downstream port 2 high speed transmitter D+/D- cross over point tuning option Default value: 1'b0
6:4	Logical Downstream port 2 high speed transmitter slew rate control Default value: 3'b100
3:0	Logical Downstream port 2 high speed transmitter JK level control Default value: 4'b0110

5.2.7.10 VC_SR_JK_D3 – Logical Downstream Port 3 HSTX Electrical Tuning Option

- Address: 0Bh
- Default value: 46h

Bit	Description
7	Logical Downstream port 3 high speed transmitter D+/D- cross over point tuning option Default value: 1'b0
6:4	Logical Downstream port 3 high speed transmitter slew rate control Default value: 3'b100
3:0	Logical Downstream port 3 high speed transmitter JK level control Default value: 4'b0110

5.2.7.11 VC_SR_JK_D4 – Logical Downstream Port 4 HSTX Electrical Tuning Option

- Address: 0Ch
- Default value: 46h

Bit	Description
7	Logical Downstream port 4 high speed transmitter D+/D- cross over point tuning option Default value: 1'b0
6:4	Logical Downstream port 4 high speed transmitter slew rate control Default value: 3'b100
3:0	Logical Downstream port 4 high speed transmitter JK level control Default value: 4'b0110

5.2.7.12 DSCT_SQ_U – Logical Upstream Port HSRX Electrical Tuning Option

- Address: 0Dh
- Default value: B0h

Bit	Description

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7:5	Logical Upstream port high speed receiver high disconnect level control Default value: 3’b101
4:0	Logical Upstream port high speed receiver Squelch level control Default value: 4’b10000

5.2.7.13 DSCT_SQ_D1 – Logical Downstream Port 1 HSRX Electrical Tuning Option

- Address: 0Eh
- Default value: B0h

Bit	Description
7:5	Logical Downstream port 1 high speed receiver high disconnect level control Default value: 3’b101
4:0	Logical Downstream port 1 high speed receiver Squelch level control Default value: 4’b10000

5.2.7.14 DSCT_SQ_D2 – Logical Downstream Port 2 HSRX Electrical Tuning Option

- Address: 0Fh
- Default value: B0h

Bit	Description
7:5	Logical Downstream port 2 high speed receiver high disconnect level control Default value: 3’b101
4:0	Logical Downstream port 2 high speed receiver Squelch level control Default value: 4’b10000

5.2.7.15 DSCT_SQ_D3 – Logical Downstream Port 3 HSRX Electrical Tuning Option

- Address: 10h
- Default value: B0h

Bit	Description
7:5	Logical Downstream port 3 high speed receiver high disconnect level control Default value: 3’b101
4:0	Logical Downstream port 3 high speed receiver Squelch level control Default value: 4’b10000

5.2.7.16 DSCT_SQ_D4 – Logical Downstream Port 4 HSRX Electrical Tuning Option

- Address: 11h
- Default value: B0h

Bit	Description
7:5	Logical Downstream port 4 high speed receiver high disconnect level control Default value: 3’b101
4:0	Logical Downstream port 4 high speed receiver Squelch level control Default value: 4’b10000

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5.2.7.17 DP12_PORT – Physical Downstream Port 1 & 2 enable/disable Option

- Address: 2Bh
- Default value: A9h

Bit	Description
7	Physical Downstream port 2 enable/disable option '1' – Enable '0' – Disable
6:4	Reserved
3	Physical Downstream port 1 enable/disable option '1' – Enable '0' – Disable
2:0	Reserved

5.2.7.18 DP34_PORT – Physical Downstream Port 3 & 4 enable/disable Option

- Address: 2Ch
- Default value: CBh

Bit	Description
7	Physical Downstream port 4 enable/disable option '1' – Enable '0' – Disable
6:4	Reserved
3	Physical Downstream port 3 enable/disable option '1' – Enable '0' – Disable
2:0	Reserved

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5.2.8 SMBus Protocol

Fig. 5.9 shows the SMBus topology. The VDD power is 3.3V +/- 10% and the pull high resistor is 1KΩ. Both SMBCLK and SMBDAT lines are bi-directional, connected to 3.3V supply voltage through a pull high resistor. The operating frequency is 10~100 KHz.

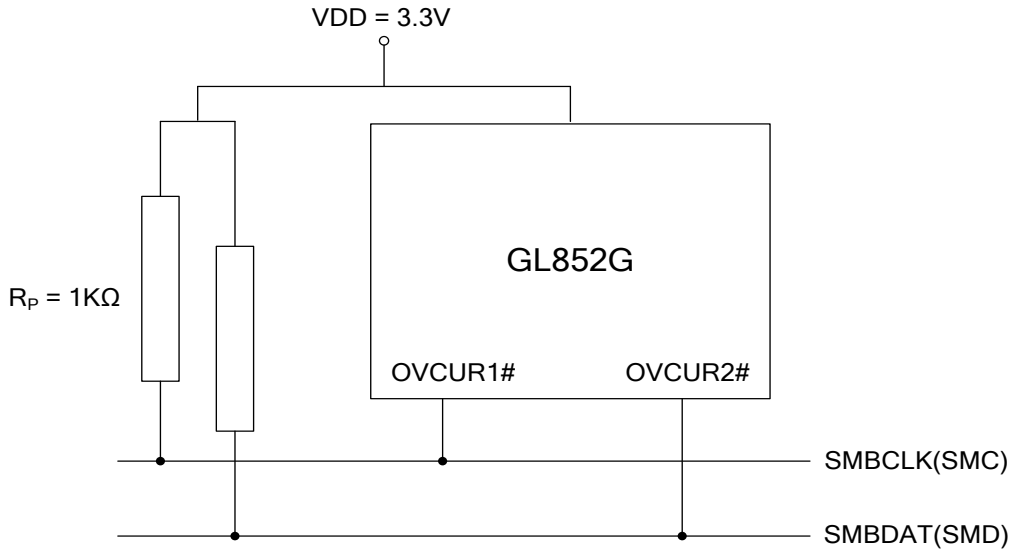

Figure 0.1 - SMBus Topology

SMBus uses fixed voltage levels to define the logic "ZERO" and logic "ONE" on the bus respectively. The data on SMBDAT must be stable during the "HIGH" period of the clock. Data can change state only when SMBCLK is low. Fig. 5.10 illustrates the relationships.

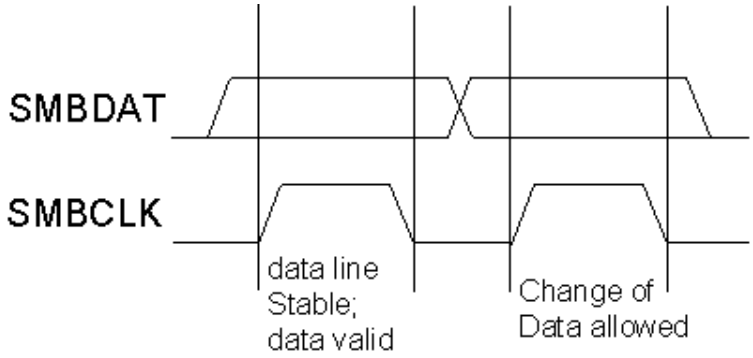

Figure 0.2 - Data Validity

Two unique bus situations define the messages of START and STOP conditions.
1. START condition: A HIGH to LOW transition of the SMBDAT line while SMBCLK is HIGH
2. STOP condition: A LOW to HIGH transition of the SMBDAT line while SMBCLK is HIGH

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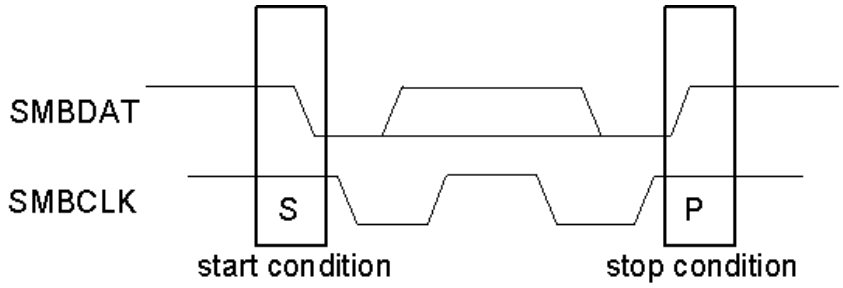


Figure 0.3 - START and STOP Condition

Every byte consists of 8 bits. Each byte transferred on the bus must be followed by an acknowledge bit. Bytes are transferred with the most significant bit (MSB) first. Fig. 5.12 illustrates the positioning of acknowledge (ACK) and not acknowledge (NACK) pulses relative to other data.

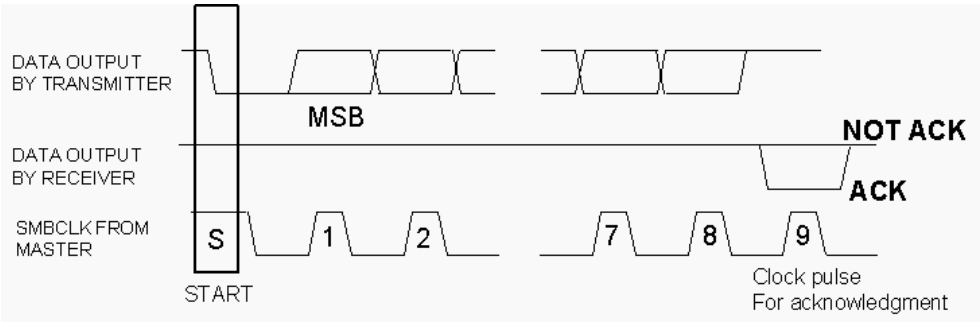
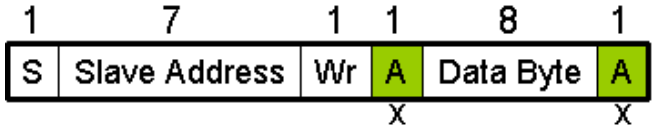


Figure 0.4 - ACK and NACK Signaling of SMBus

There is an element key for the SMBus protocol diagrams below.



S Start Condition
Sr Repeated Start Condition
Rd Read (bit value of 1)
Wr Write (bit value of 0)
x Shown under a field indicates that that field is required to have the value of 'x'
A Acknowledge (this bit position may be 0' for an ACK or '1' for a NACK)
P Stop Condition
Master-to-Slave
Slave-to-Master

Figure 0.5 - SMBus Packet Protocol Diagram Element Key

Fig 5.14 shows a Write Byte Protocol. The first byte of a Write Byte access is the command code and next byte is the data to be written. In this example the master asserts slave address followed by the write bit. The slave acknowledges and the master delivers the command code. The slave acknowledges again before the

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master sends the data byte. The slave acknowledges the data byte, and the entire transaction is finished with a STOP condition.

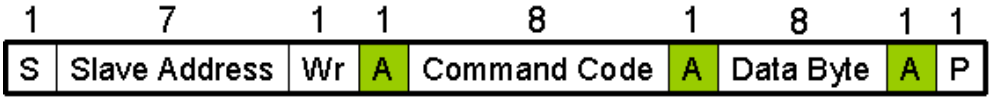

Figure 0.6 - Write Byte Protocol

Reading data is slightly more complicated than writing data. Firstly, the host has to write a command to slave, and the host must follow that command with a repeated START condition to denote a read from slave address. And the slave then returns one byte of data.
Please note there is no STOP condition before the repeated START condition, and a NACK signifies the end of the read transfer.

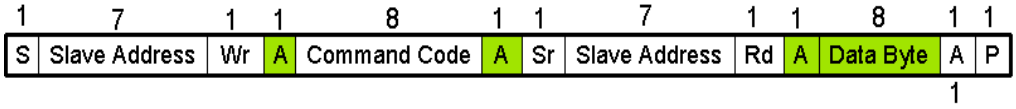

Figure 0.7 - Read Byte Protocol

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CHAPTER 6 ELECTRICAL CHARACTERISTICS

6.1 Maximum Ratings

Table 6.1 - Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V5	5V Power Supply	-0.5	+6.0	V
VDD	3.3V Power Supply	-0.5	+3.6	V
VIN	Input Voltage for digital I/O pins	-0.5	+3.6	V
VINOD	Open-drain input pins(Ovcur1~4#,Pself,Reset)	-0.5	+5.5	V
VINUSB	Input Voltage for USB signal (DP, DM) pins	-0.5	+3.6	V
TS	Storage Temperature under bias	-55	+100	ºC
FOSC	Frequency	12 MHz ± 0.05%		

6.2 Operating Ranges

Table 6.2 - Operating Ranges

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_5	5V Power Supply	4.75	5.0	5.25	V
V_{DD}	3.3V Power Supply	3.0	3.3	3.6	V
V_{IN}	Input Voltage for digital I/O pins	-0.5	-	3.6	V
V_{INOD}	Open-drain input pins(Ovcur1~4#,Pself,Reset)	-0.5	-	5.0	V
V_{INUSB}	Input Voltage for USB signal (DP, DM) pins	0.5	-	3.6	V
T_A	Ambient Temperature	0	-	70	ºC
T_J	Absolute maximum junction temperature	0	-	125	ºC
θ_{JA}	Thermal Characteristics 64 LQFP	-	83.86	-	ºC/W

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6.3 DC Characteristics

Table 6.3 - DC Characteristics except USB Signals

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	LOW level input voltage	-	-	0.8	V
V_{IH}	HIGH level input voltage	2.0	-	-	V
V_{TLH}	LOW to HIGH threshold voltage	1.48	1.55	1.6	V
V_{THL}	HIGH to LOW threshold voltage	1.13	1.21	1.27	V
V_{OL}	LOW level output voltage when I_{OL}=8mA	-	-	0.4	V
V_{OH}	HIGH level output voltage when I_{OH}=8mA	2.4	-	-	V
$R_{UP_OVCUR\#}$	OVCUR# pin internal pull high resister	440	890	2000	KΩ
$R_{DN_GRE_AMB}$	GREEN/AMBER pin internal pull down resister	440	890	2000	KΩ
R_{DN_TEST}	TEST pin internal pull down resister	33	51	102	KΩ
R_{UP_PSELF}	PSELF pin internal pull high resister	148	222	359	KΩ

Table 6.4 - DC Characteristics of USB Signals under FS/LS Mode

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OL}	DP/DM FS static output LOW(R_L of 1.5K to 3.6V)	0	-	0.3	V
V_{OH}	DP/DM FS static output HIGH (R_L of 15K to GND)	2.8	-	3.6	V
V_{DI}	Differential input sensitivity	0.2	-	-	V
V_{CM}	Differential common mode range	0.8	-	2.5	V
V_{SE}	Single-ended receiver threshold	0.2	-	-	V
C_{IN}	Transceiver capacitance	-	-	20	pf
I_{LO}	Hi-Z state data line leakage	-10	-	+10	μA
Z_{DRV}	Driver output resistance	28	-	44	Ω

Table 6.5 - DC Characteristics of USB Signals under HS Mode

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OL}	DP/DM HS static output LOW(R_L of 1.5K to 3.6V)	-	-	0.1	V
C_{IN}	Transceiver capacitance	4	4.5	5	pf
I_{LO}	Hi-Z state data line leakage	-5	0	+5	μA
Z_{DRV}	Driver output resistance for USB 2.0 HS	42	45	48	Ω

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6.4 Power Consumption

Table 6.6 - GL854G-65 power consumption

Symbol	Condition			Config.	Read / Write	Unit
	Active ports	Host	Device			
I_{SUSP}	Suspend			1.4	-	mA
I_{CC}	7	H	H	168	199	mA
	6	H	H	162	192	mA
	5	H	H	155	183	mA
	4	H	H	150	174	mA
	3	H	H	143	162	mA
	2	H	H	136	153	mA
	1	H	H	130	140	mA
	Upstream Port Configured	H	N/A	124	-	mA

*: H: High-Speed

Note:

Test result was measured by 5V input (it will be lower by 3.3V input), and represents silicon level operating current, without considering additional power consumption contributed by external over-current protection circuit such as power switch or polyfuse.

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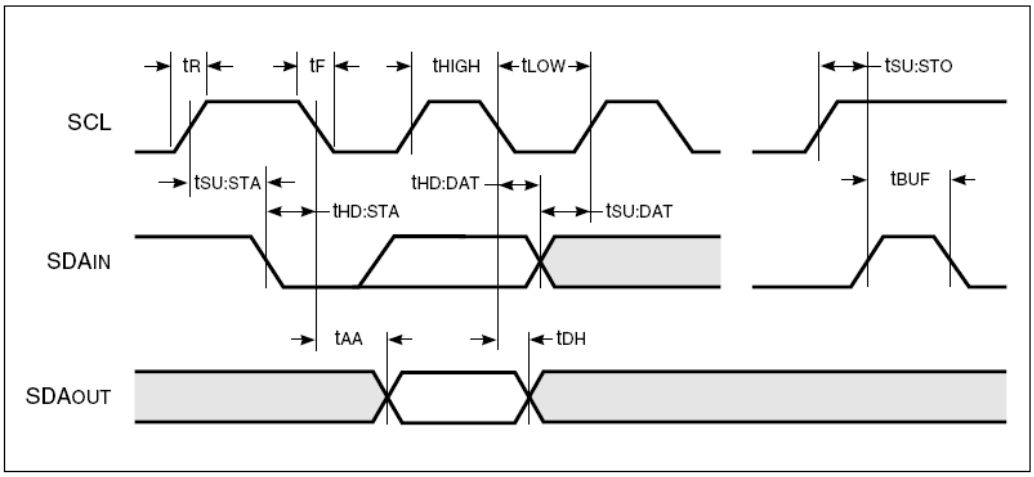
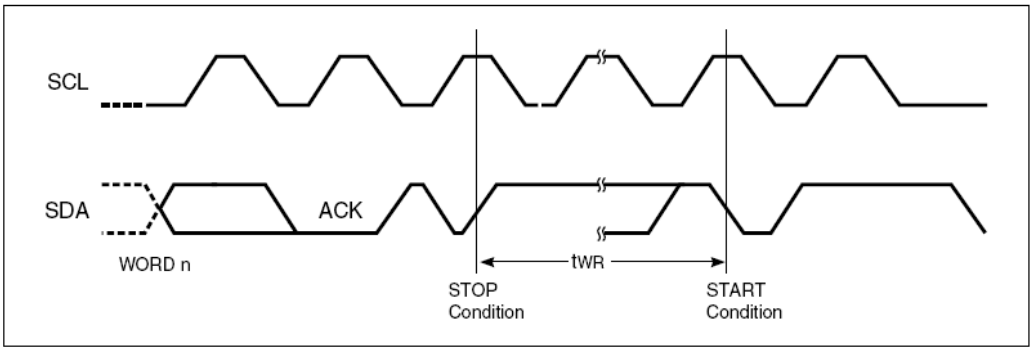
6.5 AC Characteristics

GL854G- supports 24C02 type EEPROM for customized VID/PID or hub configuration settings. AC characteristics of 24C02 interface summarized as below figures and tables.



Bus Timing



Write Cycle Timing

Table 6.7 - AC Characteristics of EEPROM Interface (24C02)

Symbol	Parameter	Test Conditions	1.8V-5.5V Min.	1.8V-5.5V Max.	2.5V-5.5V Min.	2.5V-5.5V Max.	Unit
f_{SCL}	SCL Clock Frequency		0	100	0	400	KHz
T	Noise Suppression Time(1)		—	100	—	50	ns
t_{LOW}	Clock LOW Period		4.7	—	1.2	—	µs
t_{HIGH}	Clock HIGH Period		4	—	0.6	—	µs
t_{BUF}	Bus Free Time Before New Transmission(1)		4.7	—	1.2	—	µs
$t_{SU:STA}$	Start Condition Setup Time		4.7	—	0.6	—	µs
$t_{SU:STO}$	Stop Condition Setup Time		4.7	—	0.6	—	µs
$t_{HD:STA}$	Start Condition Hold Time		4	—	0.6	—	µs
$t_{HD:STO}$	Stop Condition Hold Time		4	—	0.6	—	µs
$t_{SU:DAT}$	Data In Setup Time		200	—	100	—	ns
$t_{HD:DAT}$	Data In Hold Time		0	—	0	—	ns
t_{DH}	Data Out Hold Time	SCL LOW to SDA Data Out Change	100	—	50	—	ns
t_{AA}	Clock to Output	SCL LOW to SDA Data Out Valid	0.1	4.5	0.1	0.9	µs
t_R	SCL and SDA Rise Time(1)		—	1000	—	300	ns
t_F	SCL and SDA Fall Time(1)		—	300	—	300	ns
t_{WR}	Write Cycle Time		—	10	—	5	ms

Note:
1. This parameter is characterized but not 100% tested.

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CHAPTER 7 PACKAGE DIMENSION

SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	---	---	1.60 (63.0)
A1	0.05 (2.0)	---	0.15 (5.9)
A2	1.35 (53.1)	1.40 (55.1)	1.45 (57.1)
b	0.13 (5.1)	0.18 (7.1)	0.23 (9.1)
b1	0.13 (5.1)	0.16 (6.3)	0.19 (7.5)
c	0.09 (3.5)	---	0.20 (7.9)
c1	0.09 (3.5)	---	0.16 (6.3)
D	9.00 (354.3) BSC		
D1	7.00 (275.6) BSC		
e	0.40 (15.7) BSC		
E	9.00 (354.3) BSC		
E1	7.00 (275.6) BSC		
L	0.45 (17.7)	0.60 (23.6)	0.75 (29.5)
L1	1.00 (39.4) REF		
R1	0.08 (3.1)	---	---
R2	0.08 (3.1)	---	0.20 (7.9)
S	0.20 (7.9)	---	---
aaa	0.20 (7.9)		
bbb	0.20 (7.9)		
ccc	0.08 (3.1)		
ddd	0.07 (2.8)		
θ	0°	3.5°	7°
θ1	0°	---	---
θ2	11°	12°	13°
θ3	11°	12°	13°

NOTE: 1. REFER TO JEDEC MS-026/BBD
2. ALL DIMENSIONS IN MILLIMETERS.

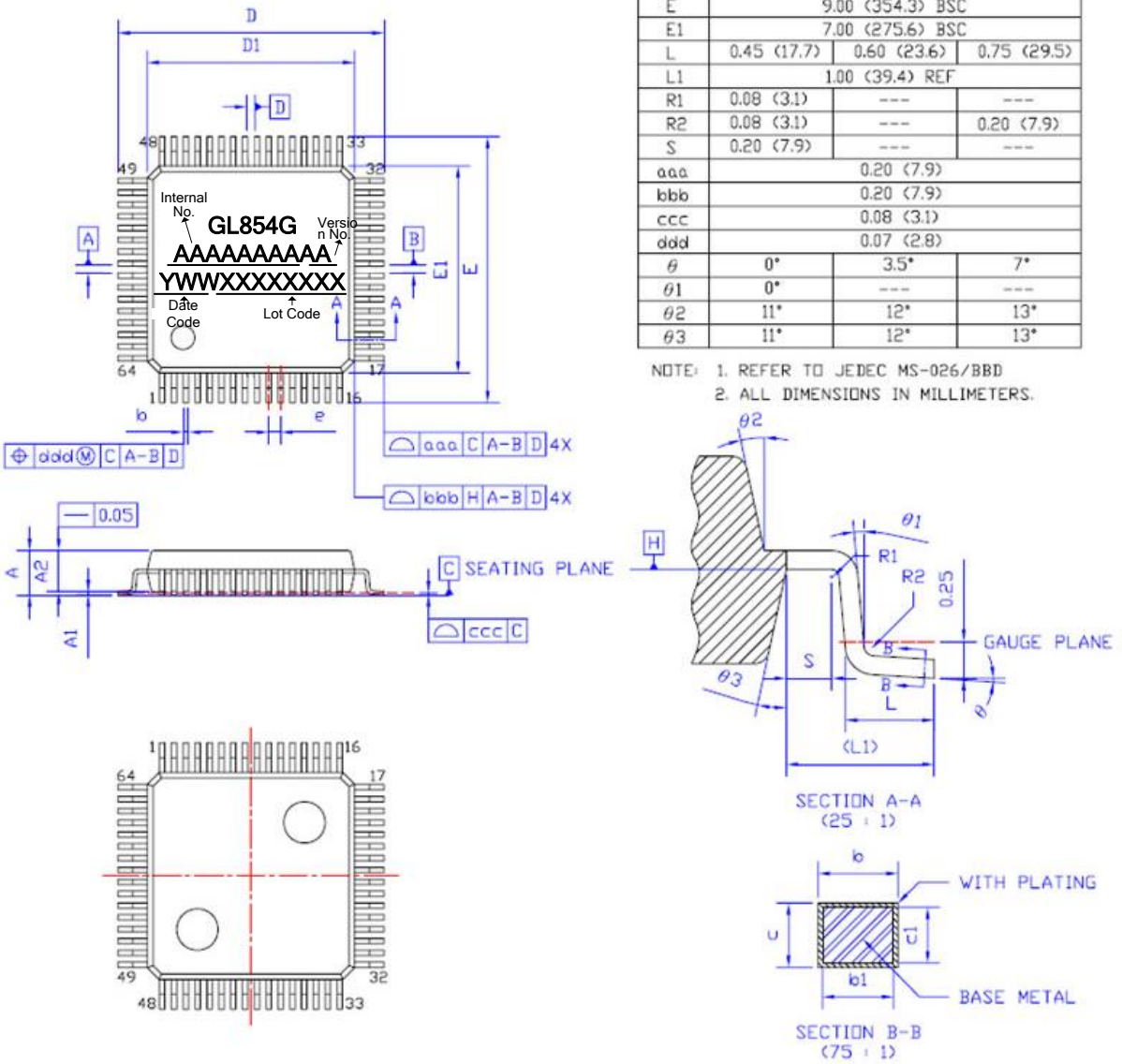

Figure 7.1 - GL854G 64 Pin LQFP Package

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CHAPTER 8 ORDERING INFORMATION

Table 8.1 - Ordering Information

Part Number	Package	Green/Wire Material	Version	Status
GL854G –MSY65	LQFP 64	Green Package	65	Available

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