RTD2525BR-VS-CG

MULTI-FUNCTION DISPLAY CONTROLLER

DATASHEET

(CONFIDENTIAL: Development Partners Only)

Rev. 1.0
15 July 2022

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2022/07/15	First release.

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1. General Description

The Realtek RTD2525BR-VS-CG monitor controller combines an analog RGB input interface, a HDMI 1.4a compliant digital input interface with HDCP1.4, and a DP1.2 digital input interface with HDCP1.4. The embedded MCU is based on an industrial standard 8051 core with external serial flash.

The RTD2525BR-VS-CG is suitable for multiple market segments and display applications, such as monitor, All in One PC, and embedded applications.

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2. Features

General

- RTD2525BR-VS-CG supports input format up to 1920x1080 @ 100Hz via HDMI and DisplayPort.
- Embedded 3DDC with DDC1/2B/CI
- Zoom scaling up and down
- Embedded one MCU with SPI flash controller.
- It contains 4 ADCs in key pad application
- Require only one crystal to generate all timing.
- Programmable internal low-voltage-reset (LVR)
- High resolution 4 channels PWM output, and wide range selectable PWM frequency.
- Support input format up to FHD.

Crystal

- Support 14.318MHz crystal type

Analog RGB Input Interface

- 1 Analog input supported
- Integrated 8-bit triple-channel 210MHz ADC/PLL
- Embedded programmable Schmitt trigger of HSYNC
- Support Sync-On-Green (SOG) and various kinds of composite sync modes
- On-chip high-performance hybrid PLLs
- High resolution true 64 phase ADC PLL
- YPbPr support up to HDTV 1080p resolution

HDMI 1.4a Compliant Digital Input Interface with HDCP 1.4

- HDMI Input with embedded high speed switch
- Single link on-chip TMDS receiver up to 225MHz.
- Support long cable
- Adaptive algorithm for TMDS capability
- Data enable only mode support
- High-Bandwidth Digital Content Protection (HDCP 1.4)
- Enhanced protection of HDCP secret key
- Capable of 2-channel I2S/SPDIF output in HDMI application
- ATC Lab certification pass HDMI1.4a compliance test
- Support FreeSync

DisplayPort 1.2 Digital Input Interface with HDCP 1.4

- Support 4 lanes digital input, each lanes speed up to 1.62Gbps and 2.7Gbps
- Support 6-bit, 8-bit, 10-bit, and 12-bit color depth transport
- High-Bandwidth Digital Content Protection (HDCP 1.4)
- Capable of 2-channel I2S/SPDIF output in DP application

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- Support VESA Adaptive Sync

Embedded MCU

- Industrial standard 8051 core with external serial flash
- Low speed ADC for various application
- I2C Master hardware supported

Auto Detection /Auto Calibration

- Input format detection
- Compatibility with standard VESA mode and support user-defined mode
- Smart engine for Phase/Image position/Color calibration

Scaling

- Fully programmable zoom ratios
- Independent horizontal/vertical scaling
- Advanced zoom algorithm provides high image quality
- Sharpness/Smooth filter enhancement
- Support non-linear scaling from 4:3 to 16:9 or 16:9 to 4:3

Color Processor

- xvYCC supported
- sRGB compliance
- Dynamic overshoot-smear canceling engine
- Brightness and contrast control
- Programmable 10-bit gamma support
- Peaking/Coring function for video sharpness
- dithering function for the fewer panel color depth

VividColorTM

- Independent color management (ICM)
- Dynamic contrast control (DCC)
- Precise color mapping (PCM)
- Support Ultra-Vivid function to enhance image quality

Output Interface

- Fully programmable display timing generator
- Flexible data pair swapping for easier system design.
- Display clock supports up to 120MHz for Single LVDS and 240MHz for Dual LVDS
- LVDS -output interface on single PCB
- Support 8-bit LVDS output
- Spread-Spectrum DPLL to reduce EMI
- Fixed Last Line output for perfect panel capability

Embedded OSD

- Embedded 24K SRAM dynamically stores OSD command and fonts
- Support multi-color RAM font, 1, 2 and 4-bit per pixel
- 64 color palette
- Maximum 18 window with alpha-blending /

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- gradient / gradient target color / gradient reversed color/ dynamic fade-in/fade-out, bordering/ shadow
- Rotate 90,270 degree
- OSD-made internal pattern generator for factory mode
- Support 12x18 ~ 4x18 proportional font
- Hardware decompression for OSD font
- Support OSD scrolling
- Support 2 independent font based OSD

Audio

- Output: IIS , SPDIF
- Embedded Audio DAC
- Embedded headphone amp

Power Supply

- 3.3V / 0.9V power supply
- Low standby current (<10mA)

LiveShowTM Function

- High-performance RTC (response time compensation).

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3. System Applications

- Display System on Motherboard, Monitor
- Display System for All in One PCs and embedded applications

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4. Block Diagram

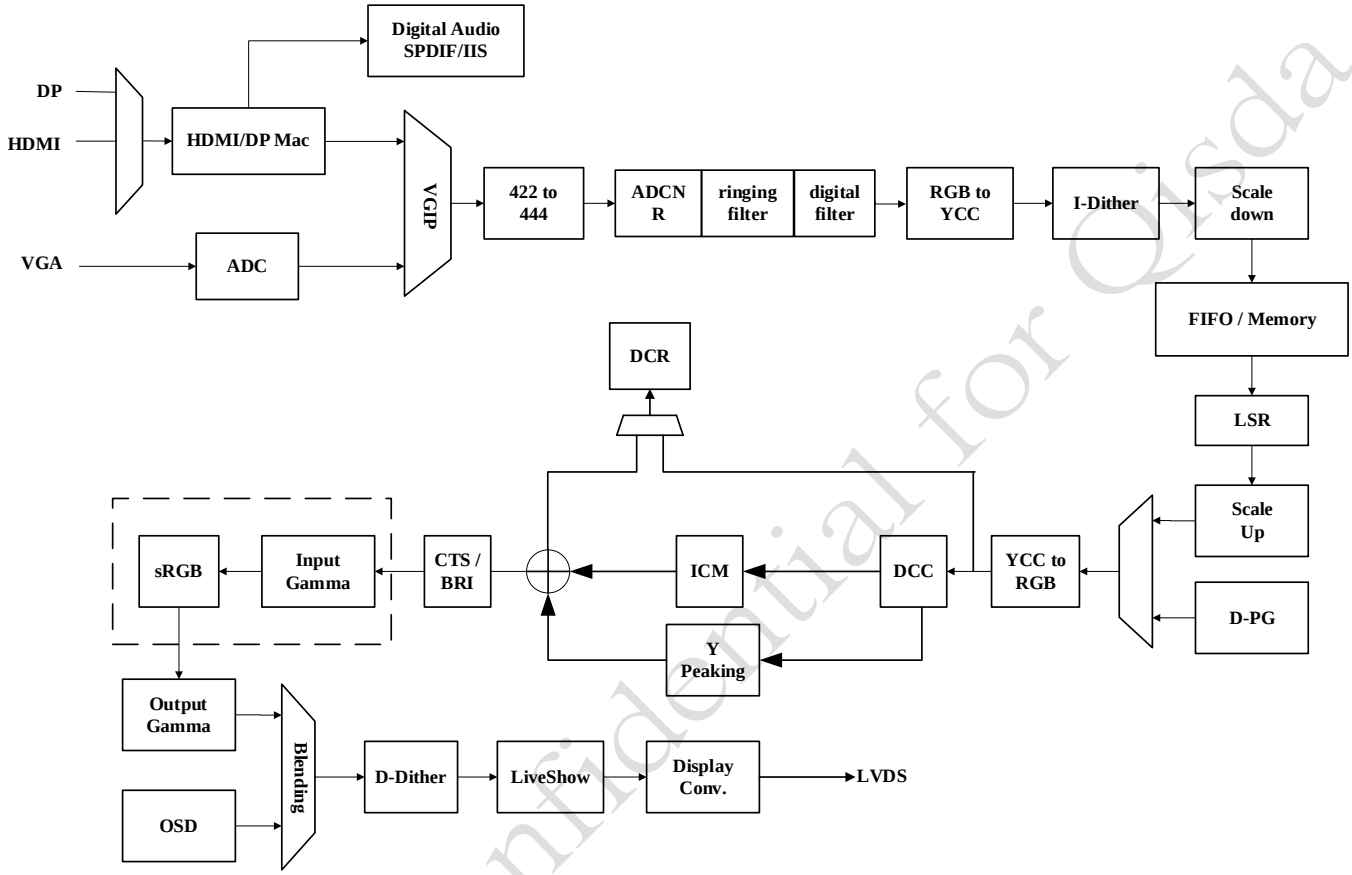

Figure 1. Data Path

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5. Pin Assignments

128 Pin LT128

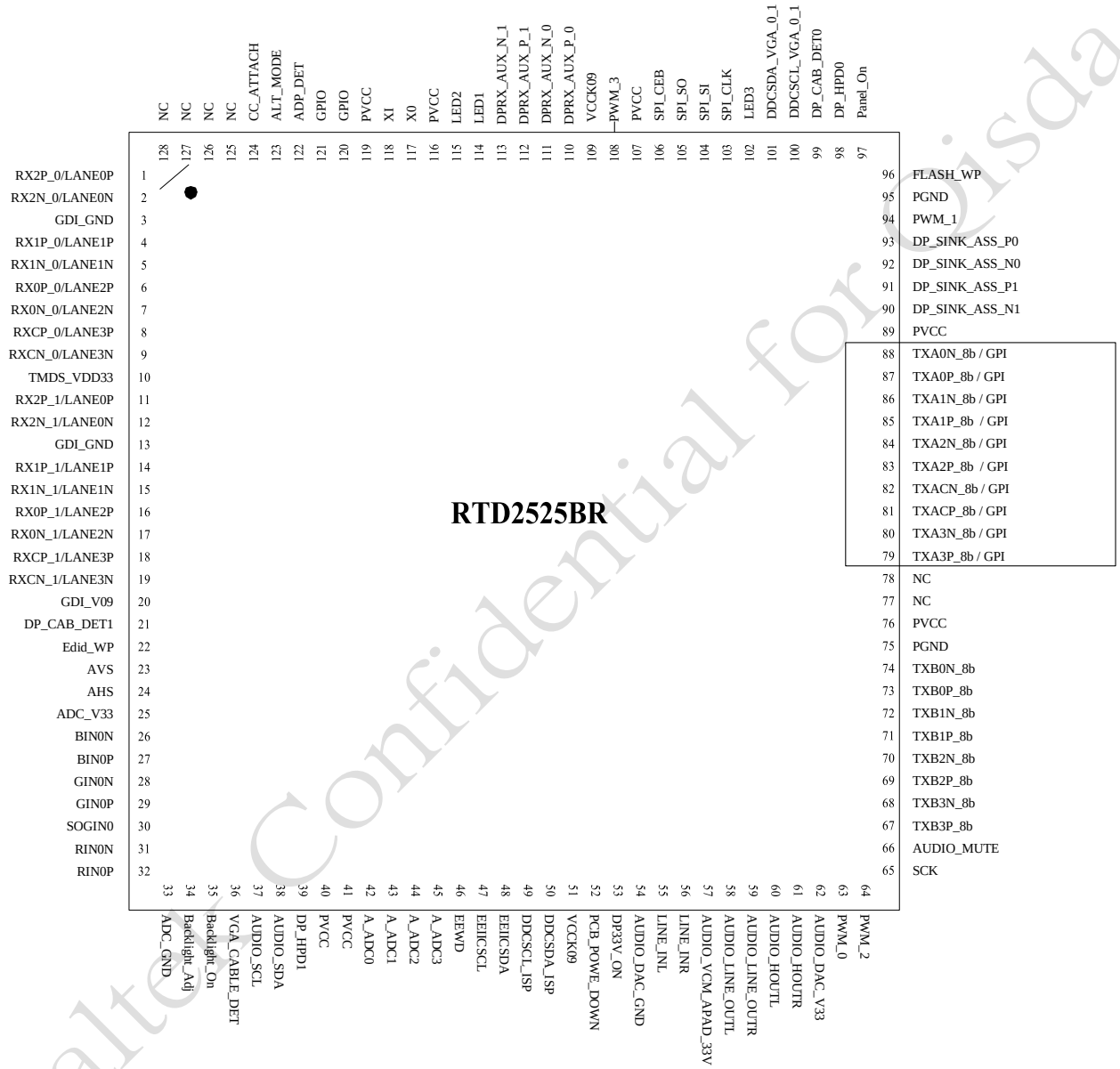

Figure 2. Pin Assignments

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6. Pin Assignments Table

I/O Legend: A = Analog, I = Input, O = Output, P = Power, G = Ground

Note Legend:

3(OFF) = 3.3V Tolerance even when power off

5(OFF) = 5V Tolerance even when power off

5(ON) = 5V Tolerance only when power on

IO Type Legend:

▲= GPIO can work only when power normal

Signals Pin Assignment

Table 1. Signals Pin Assignment

Pin Name	I/O	Pin #	Description	IO Type	Note
RX2P_0/LANE0P	AI	1	DP/TMDS Differential Signal Input		3(OFF)
RX2N_0/LANE0N	AI	2	DP/TMDS Differential Signal Input		3(OFF)
RX1P_0/LANE1P	AI	4	DP/TMDS Differential Signal Input		3(OFF)
RX1N_0/LANE1N	AI	5	DP/TMDS Differential Signal Input		3(OFF)
RX0P_0/LANE2P	AI	6	DP/TMDS Differential Signal Input		3(OFF)
RX0N_0/LANE2N	AI	7	DP/TMDS Differential Signal Input		3(OFF)
RXCP_0/LANE3P	AI	8	DP/TMDS Differential Signal Input		3(OFF)
RXCN_0/LANE3N	AI	9	DP/TMDS Differential Signal Input		3(OFF)
RX2P_1/LANE0P	AI	11	DP/TMDS Differential Signal Input		3(OFF)
RX2N_1/LANE0N	AI	12	DP/TMDS Differential Signal Input		3(OFF)
RX1P_1/LANE1P	AI	14	DP/TMDS Differential Signal Input		3(OFF)
RX1N_1/LANE1N	AI	15	DP/TMDS Differential Signal Input		3(OFF)
RX0P_1/LANE2P	AI	16	DP/TMDS Differential Signal Input		3(OFF)
RX0N_1/LANE2N	AI	17	DP/TMDS Differential Signal Input		3(OFF)
RXCP_1/LANE3P	AI	18	DP/TMDS Differential Signal Input		3(OFF)
RXCN_1/LANE3N	AI	19	DP/TMDS Differential Signal Input		3(OFF)
DP_CAB_DET	IO	21	DP_CAB_DET1(App) / PWM_0 / IHS / DHS / TCON[7] / GPIO / Test12b		5(OFF)
Edid_WP	IO	22	Edid_WP(App) / PWM_1 / TCON[8] / DCLK / GPIO / Test12b		5(OFF)
AVS	AI	23	ADC vertical sync input		5(OFF)
AHS	AI	24	ADC horizontal sync input		5(OFF)
BIN0N	AI	26	Negatice Blue analog input (Pb-)		3(OFF)
BIN0P	AI	27	Negatice Blue analog input (Pb+)		3(OFF)
GIN0N	AI	28	Negatice Green analog input (Y-)		3(OFF)
GIN0P	AI	29	Negatice Green analog input (Y+)		3(OFF)
SOGIN0	AI	30	Sync-On-Green		3(OFF)

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RIN0N	AI	31	Positive RED analog input (Pr-)		3(OFF)
RIN0P	AI	32	Positive RED analog input (Pr+)		3(OFF)
Backlight_Adj	IO	34	Backlight_Adj(App) / PWM_0 / MCK / CLKO / TCON[9] / GPIO / Test12b / TTS_SPI_CEB		5(OFF)
Backlight_On	IO	35	Backlight_On(App) / PWM_1 / IICSCL_0_3 / SCK / IRQB / TCON[13] / GPIO / Test12b		5(OFF)
VGA_CABLE_DET	IO	36	VGA_CABLE_DET(App) / PWM_2 / IICSDA_0_3 / CLKO / WS / TCON[13] / GPIO / Test12b		5(OFF)
AUDIO_SCL	IO	37	AUDIO_SCL(App) / PWM_3 / IICSCL_0_0 / UART_RX_0_0 / SD0 / SPDIF0 / TCON[11] / GPIO / Test12b		5(OFF)
AUDIO_SDA	IO	38	AUDIO_SDA(App) / PWM_2 / IICSDA_0_0 / UART_TX_0_0 / TCON[12] / GPIO / Test12b		5(OFF)
DP_HPD1	IO	39	DP_HPD1(App) / PWM_3 / TCON[13] / DCLK / GPIO / Test12b		5(OFF)
A_ADC0	AIO	42	A_ADC0(App) / SARADC_0 / TCON[9] / GPIO / Test12b		3(OFF)
A_ADC1	AIO	43	A_ADC1(App) / SARADC_1 / TCON[12] / GPIO / Test12b		3(OFF)
A_ADC2	AIO	44	A_ADC2(App) / SARADC_2 / GPIO / Test12b		3(OFF)
A_ADC3	AIO	45	A_ADC3(App) / SARADC_3 / CLKO / GPIO / Test12b		3(OFF)
EEWD	IO	46	EEWD (App) / PWM_1 / TCON[7] / TCON[13] / GPIO / Test12b / TTS_SPI_CLK		5(OFF)
EEIICSCL	IO	47	EEIICSCL / IICSCL_AUX / TCON[8] / TCON[12] / GPIO / Test12b		5(OFF)
EEIICSDA	IO	48	EEIICSDA / IICSDA_AUX / GPIO / Test12b		5(OFF)
DDCSCL_ISP	IO	49	DDCSCL_ISP / DDCSCL_VGA_0_0 / UART_RX_0_1 / GPIO / Test12b		5(OFF)
DDCSDA_ISP	IO	50	DDCSDA_ISP / DDCSDA_VGA_0_0 / UART_TX_0_1 / TCON[11] / TCON[13] / GPIO / Test12b		5(OFF)
PCB_POWE_DOWN	IO	52	PCB_POWE_DOWN(App) / PWM_0 / TCON[9] / GPIO / Test12b		5(OFF)
DP33V_ON	IO	53	DP33V_ON(App) / PWM_3 / TCON[12] / GPIO / Test12b		5(OFF)
LINE_INL	AIO	55	LINE_INL / PWM_0 / MCK / GPIO / Test12b		3(OFF)
LINE_INR	AIO	56	LINE_INR / SCK / GPIO / Test12b		3(OFF)
AUDIO_VCM_APAD_33V	AIO	57	AUDIO_VCM_APAD_33V(App) / AUDIO_REF / WS / TCON[13] / GPIO / Test12b		3(OFF)
AUDIO_LINE_OUTL	AIO	58	AUDIO_LINE_OUTL(App) / AUDIO_SOUTL / SD0 / SPDIF0 / GPIO / Test12b		3(OFF)
AUDIO_LINE_OUTR	AIO	59	AUDIO_LINE_OUTR(App) / AUDIO_SOUTR / GPIO / Test12b		3(OFF)
AUDIO_HOUTL	AIO	60	AUDIO_HOUTL / IICSCL_0_1 / UART_RX_0_2 / GPIO / Test12b		3(OFF)

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AUDIO_HOUTR	AIO	61	AUDIO_HOUTR / IICSDA_0_1 / UART_TX_0_2 / GPIO / Test12b		3(OFF)
PWM_0	IO	63	PWM_0 / PMW_3 / PWM_IN_0_1 /CLKO / INT1_0 / T2 / IHS / TCON[7] / GPIO / Test12b / TTS_SPI_SI		5(OFF)
PWM_2	IO	64	PWM_2 / PWM_OUT_0_1 / CLKO / INT0_0 / IENA / TCON[8] / GPIO / Test12b / TTS_SPI_SO		5(OFF)
SCK	IO	65	SCK / PWM_2 / TCON[9] / DCLK / GPIO / Test12b		5(OFF)
AUDIO_MUTE	IO	66	AUDIO_MUTE(App) / PWM_3 / MCK / IENA / DENA / TCON[11] / GPIO / Test12b		5(OFF)
TXB3P_8b	AO	67	LVDS		3(OFF)
TXB3N_8b	AO	68	LVDS		3(OFF)
TXB2P_8b	AO	69	LVDS		3(OFF)
TXB2N_8b	AO	70	LVDS		3(OFF)
TXB1P_8b	AO	71	LVDS		3(OFF)
TXB1N_8b	AO	72	LVDS		3(OFF)
TXB0P_8b	AO	73	LVDS		3(OFF)
TXB0N_8b	AO	74	LVDS		3(OFF)
NC	-	77	NC		-
NC	-	78	NC		-
TXA3P_8b / GPI	AIO	79	LVDS / GPI	▲	3(OFF)
TXA3N_8b / GPI	AIO	80	LVDS / GPI	▲	3(OFF)
TXACP_8b / GPI	AIO	81	LVDS / GPI	▲	3(OFF)
TXACN_8b / GPI	AIO	82	LVDS / GPI	▲	3(OFF)
TXA2P_8b / GPI	AIO	83	LVDS / GPI	▲	3(OFF)
TXA2N_8b / GPI	AIO	84	LVDS / GPI	▲	3(OFF)
TXA1P_8b / GPI	AIO	85	LVDS / GPI	▲	3(OFF)
TXA1N_8b / GPI	AIO	86	LVDS / GPI	▲	3(OFF)
TXA0P_8b / GPI	AIO	87	LVDS / GPI	▲	3(OFF)
TXA0N_8b / GPI	AIO	88	LVDS / GPI	▲	3(OFF)
DP_SINK_ASS_N	IO	90	DP_SINK_ASS_N1(App) / PWM_0 / TCON[12] / GPIO / Test12b		5(OFF)
DP_SINK_ASS_P1	IO	91	DP_SINK_ASS_P1(App) / PWM_1 / TCON[13] / GPIO / Test12b		5(OFF)
DP_SINK_ASS_N0	IO	92	DP_SINK_ASS_N0(App) / PWM_3 / TCON[7] / GPIO / Test12b		5(OFF)

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DP_SINK_ASS_P0	IO	93	DP_SINK_ASS_P0(App) / PWM_2 / TCON[8] / GPIO / Test12b		5(OFF)
PWM_1	IO	94	PWM_1 / TCON[9] / DCLK / GPIO / Test12b		5(OFF)
FLASH_WP	IO	96	FLASH_WP (App) / IVS / DVS / CLKO / INT0_1 / TCON[11] / GPIO / Test12b		5(OFF)
Panel_On	IO	97	Panel_On(App) / PWM_2 / PWM_3 / IICSCL_0_2 / UART_TX_0_3 / INT1_1 / IVS / TCON[11] / DCLK / DHS / GPIO / Test12b		5(OFF)
DP_HPD0	IO	98	DP_HPD0(App) / PWM_3 / IICSDA_0_2 / UART_RX_0_3 / T0 / DENA / TCON[9] / GPIO / Test12b		5(OFF)
DP_CAB_DET0	IO	99	DP_CAB_DET0(App) / PWM_2 / PMW_3 / T1 / IHS / DHS / TCON[13] / GPIO / Test12b / MCK		5(OFF)
DDCSCL_VGA_0_1	IO	100	DDCSCL_VGA_0_1 / PWM_IN_0_0 / AUX_D2 / DCLK / TCON[8] / T2EX / GPIO / Test12b		5(OFF)
DDCSDA_VGA_0_1	IO	101	DDCSDA_VGA_0_1 / PWM_0 / PWM_OUT_0_0 / AUX_D1 / DVS / TCON[7] / GPIO / Test12b		5(OFF)
LED3	IO	102	LED3(App) / PWM_0 / TCON[12] / DCLK / GPIO / Test12b		5(OFF)
SPI_CLK	IO	103	Flash SPI_CLK		3(OFF)
SPI_SI	IO	104	Flash SPI_SI		3(OFF)
SPI_SO	IO	105	Flash SPI_SO		3(OFF)
SPI_CEB	IO	106	Flash SPI_CEB		3(OFF)
PWM_3	IO	108	PWM_3 / PWM_1 / TCON[13] / GPIO / Test12b		5(OFF)
DPRX_AUX_P_0	AIO	110	DPRX_AUX_P_0 / DDCSCL_0 / GPIO / Test12b		5(OFF)
DPRX_AUX_N_0	AIO	111	DPRX_AUX_N_0 / DDCSDA_0 / GPIO / Test12b		5(OFF)
DPRX_AUX_P_1	AIO	112	DPRX_AUX_P_1 / DDCSCL_1 / GPIO / Test12b		5(OFF)
DPRX_AUX_N_1	AIO	113	DPRX_AUX_N_1 / DDCSDA_1 / GPIO / Test12b		5(OFF)
LED1	IO	114	LED1(App) / PWM_2 / TCON[11] / GPIO / Test12b		5(OFF)
LED2	IO	115	LED2(App) / PWM_1 / IRQB / TCON[12] / GPIO / Test12b		5(OFF)
XO	AO	117	XO		3(OFF)
XI	AI	118	XI		3(OFF)
GPIO	AIO	120	PWM_2 / DENA / DCLK / GPIO / Test12b		3(OFF)
GPIO	AIO	121	PWM_3 / IVS / DVS / DCLK / GPIO / Test12b		3(OFF)
ADP_DET	IO	122	ADP_DET(App) / PWM_1/ PWM_0 / MCK / TCON[7] / TCON[13] / GPIO / Test12b		5(OFF)
ALT_MODE	IO	123	ALT_MODE(App) / PWM_2 / PWM_OUT_0_2 / TCON[8] / GPIO / Test12b		5(OFF)

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CC_ATTACH	IO	124	CC_ATTACH(App) / PWM_0 / PMW_3 / PWM_IN_0_2 / TCON[7] / GPIO / Test12b / TCON[9]		5(OFF)
NC	--	125	NC		--
NC	--	126	NC		--
NC	--	127	NC		--
NC	--	128	NC		--

Power / Ground Pin Assigment

Table 2. Power / Ground Pin Assignment

P/G Pin Name	I/O	Pin #	Description	Note
PVCC	P	40, 41, 76, 89, 107, 116, 119	Pad Power	
TMDS_VDD33	AP	10	3.3V Analog Power	
ADC_V33	AP	25	3.3V Analog Power	
AUDIO_DAC_V33	AP	62	3.3V Analog Power	
VCCK09	P	51, 109	0.9V Core Power	
GDI_V09	AP	20	0.9V Analog Power	
PGND	G	75, 95	Digital Ground	
GDI_GND	AG	3, 13	GDI Ground	
ADC_GND	AG	33	ADC Ground	
AUDIO_DAC_GND	AG	54	Audio DAC Ground	

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7. Electrical Specifications

DC Characteristics

7.1. Recommended Operating Conditions

Table 3. Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Voltage on Input (5V tolerance)	V_{IN}	-0.3		5.5	V
Voltage on Input (3.3V tolerance)	V_{IN}	-0.3		3.63	V
Supply Voltage	PVCC	3.14	3.30	3.47	V
Core Power	VCCK	0.855	0.9	0.945	V
Electrostatic Discharge	V_{ESD}			±2.5	kV
Latch-Up	I_{LA}			±100	mA
Ambient Operating Temperature	T_A	0		70	ºC
Storage Temperature (plastic)	T_{STG}	-55		125	ºC
Thermal Resistance (Junction to Air)	θ_{JA}		57.2		ºC/W
Thermal Resistance (Junction to Case)	θ_{JC}		17		ºC/W
Junction Acceptable Temperature	T_j			125	ºC

7.2. Absolute Maximum Ratings

Table 4. Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Supply Voltage	PVCC			3.6	V
	VCCK			0.99	V
Storage Temperature (plastic)	T_{STG}			150	ºC
Junction Acceptable Temperature	T_j			150	ºC

Note : Operation under the absolute maximum ratings does not imply well-functioning. Long-term stress to the absolute maximum ratings would probably affect the device reliability or further cause permanent damage.

7.3. Reset Period

Table 5. Reset Period

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Reset Pulse Period	Trst-en[1]	1120			ns
Power-on-Reset Period	Tpor-rst[2]	145	146.5	148	ms

1. 16 * Xtal_cycle(1/14.3Mhz)
2. 65536*16*2*Xtal_cycle(1/14.3Mhz)

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8. Mechanical Specifications

Low Profile Plastic Quad Flat Package 128 Leads 14x14mm2 Outline

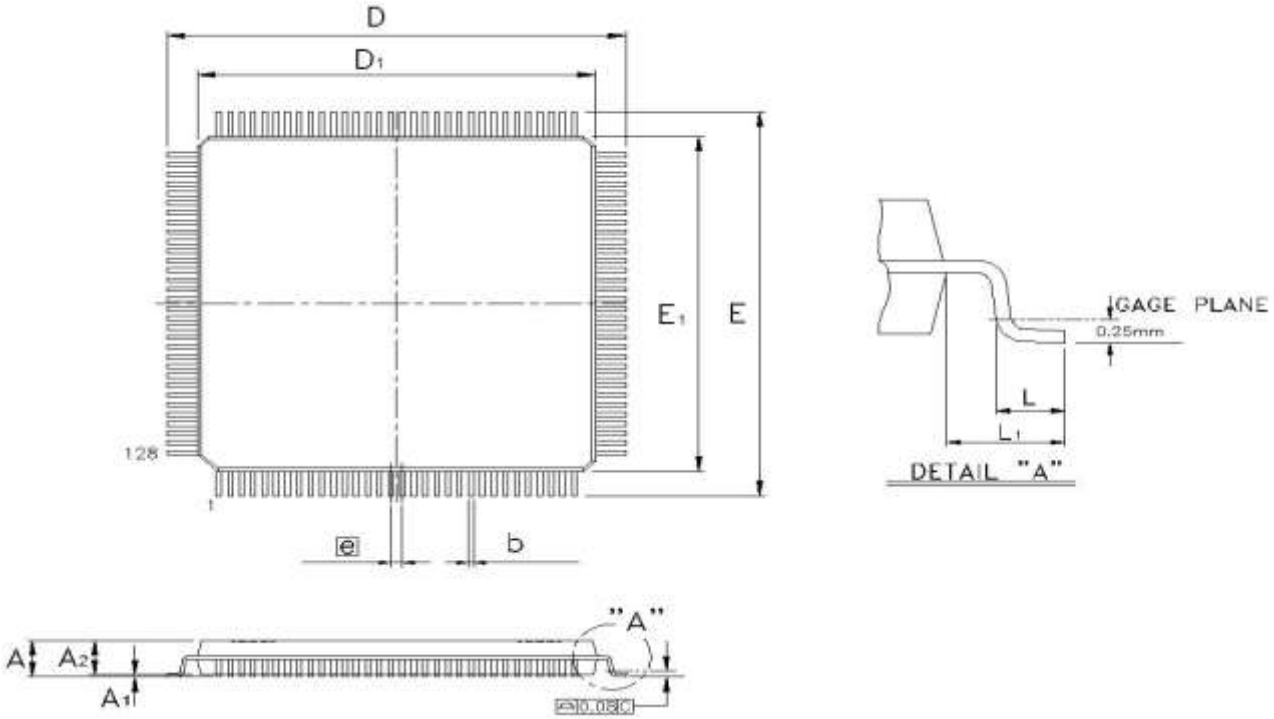

Figure 3. Mechanical Specification of 128 pin package

Table 6. Mechanical Specification of 128 pin package

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.09
D/E	16.00BSC			0.630BSC		
D_1/E_1	14.00BSC			0.551BSC		
e	0.40BSC			0.016BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		

Notes：

1. CONTROLLING DIMENSION：MILLIMETER(mm).
2. REFERENCE DOCUMENTL：JEDEC MS-026.

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9. Ordering Information

Table 7. Ordering Information

Part No.	VGA	HDMI	DP	HDCP	Audio DAC	OD	FRC	Max. Resolution	Output	PKG
RTD2525BR-VS-CG	Yes (210MHz)	Y	Y	Y	Y	Y	N	1920*1200	Dual-LVDS	LT128 (green package)

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