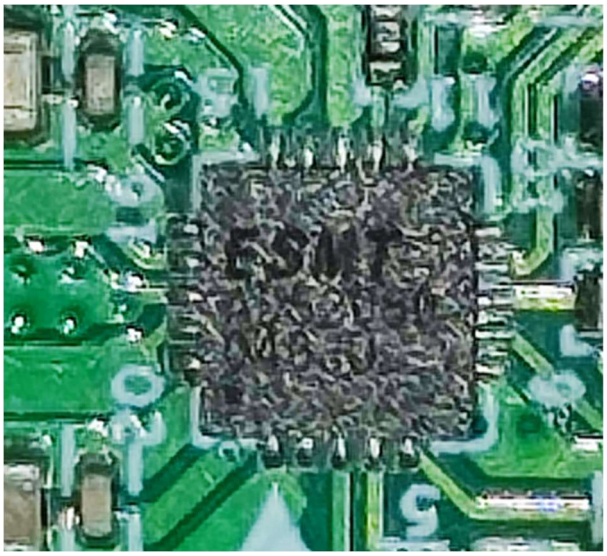

設計驗證
工程課
2025 -04- 08
發行

CONQUER
港晟國際股份有限公司
CONQUER Semiconductor International Corp.
3F., No.159, Sanmin Rd., Luzhou Dist., New Taipei City 247, Taiwan (R.O.C.)
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承　認　書

公司名稱: 鈺緯科技開發股份有限公司

品　　名: AD52080-HI20NRR
封裝方式: TQFN-20L

品牌名稱: ESMT
產品名稱:3W Stereo Class-D Audio Amplifier with Headphone Driver
客戶料號 :3AAD520801Y(A0559)

日　　期: 2025/04/07

承認單位		
		設計驗證 工程課 2025 -04- 08 發行 鈺緯科技開發股份有限公司

3W Stereo Class-D Audio Amplifier with Headphone Driver

Features

- Supply voltage range: 3.0 V to 5.8 V
- Max. 2.5W AGC non-clip function
- <12mA static operation current
- <1uA shutdown current
- 64 steps DC volume control from -60dB to +20dB
- High Efficiency >87% into 4Ω, and >92% into 8Ω loudspeaker
- Over current, under voltage, and over temperature, fully protection
- Loudspeaker output power @ 10% THD+N
  - 1.7W/CH into 8Ω loudspeaker
  - 3W/CH into 4Ω loudspeaker
- Headphone output power @ 1% THD+N
  - 80mW/CH into 32Ω headphone

Applications

- Monitor audio
- Portable multimedia devices
- Mobile phone

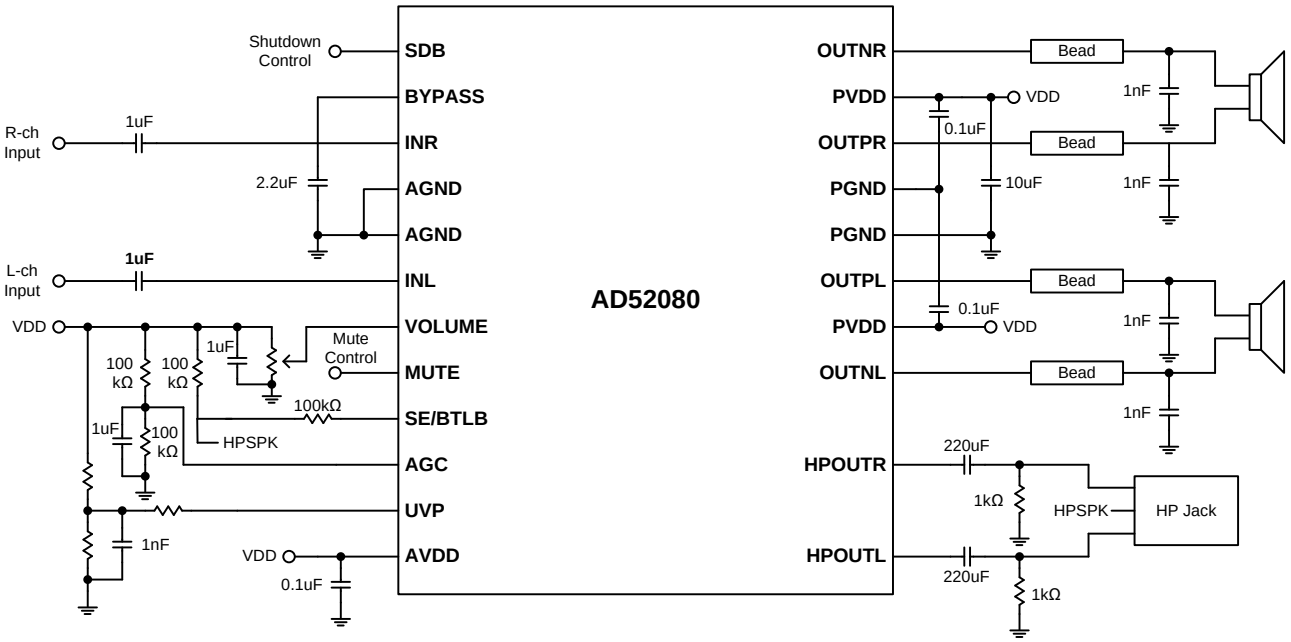
Description

The AD52080 is a stereo, filter-less Class-D audio amplifier with a Class-AB headphone driver also. Operating with 3.0V~5.8V wide power supply range, it delivers 3W/CH power into 4Ω loudspeaker within 10% THD+N or 80mW/CH power into 32Ω headphone within 1% THD+N

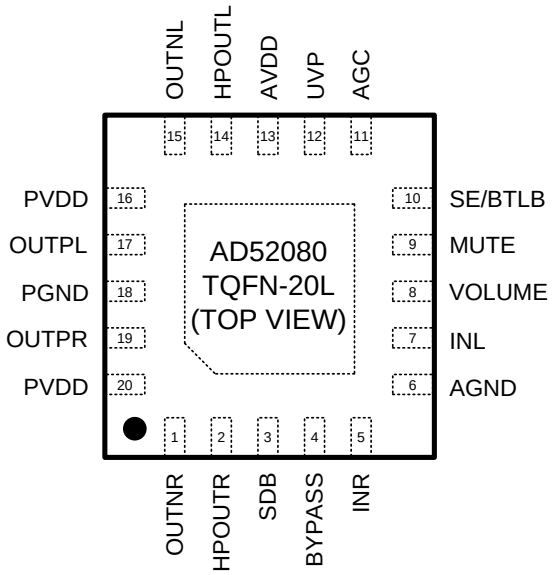
The AD52080 has not only a 64-step DC volume controller, also with a 2.5W power limiter, which implement with an automatic gain controller (AGC) internally.

The AD52080 is a stereo audio amplifier with high efficiency, which leads to longer battery life, less heat sink, smaller board size, lower system cost, and suitable for the notebook and portable multimedia devices application.

Typical Application Circuit



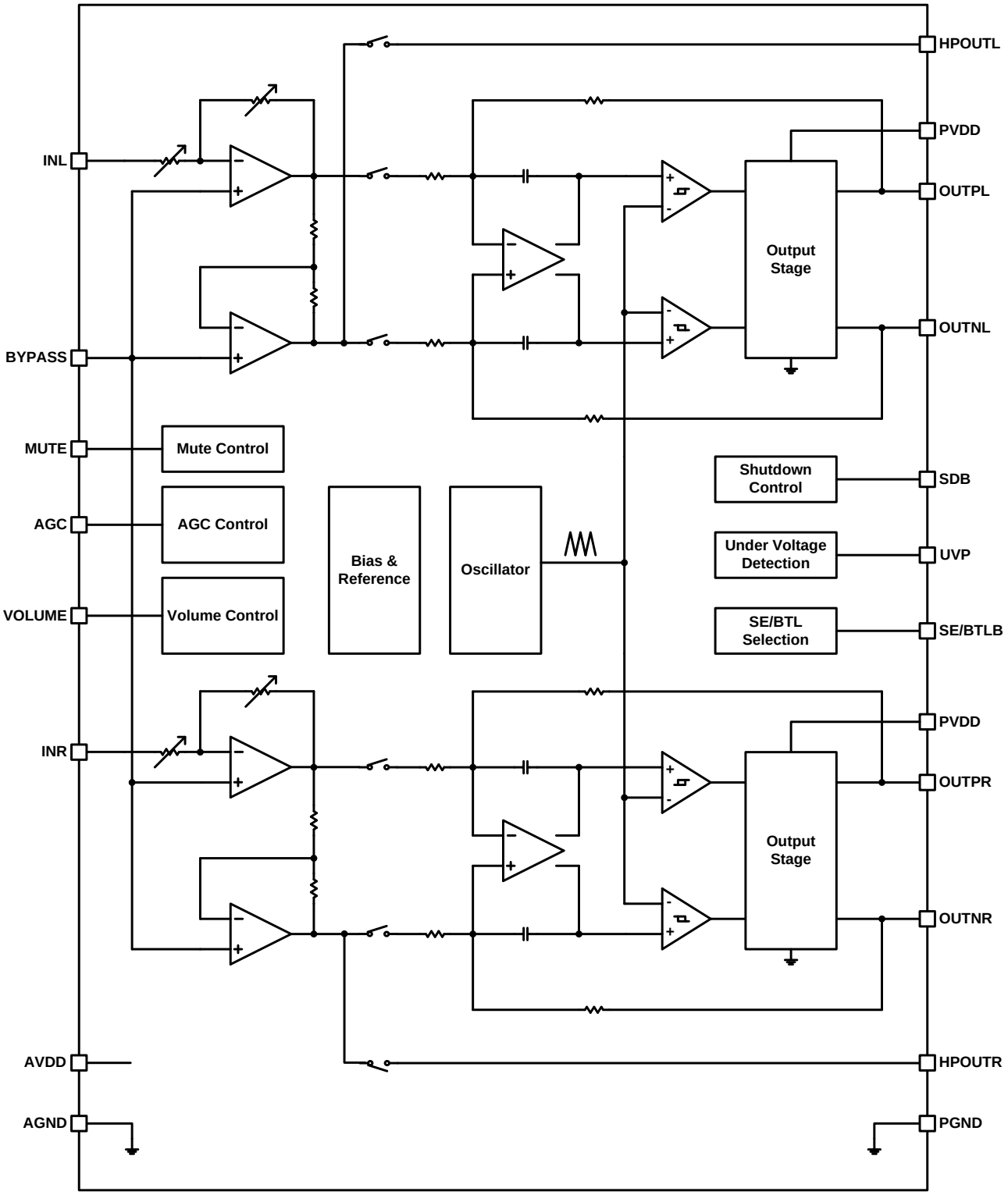
Pin Assignments



Pin Description

PIN NAME	QFN-20L	DESCRIPTION
OUTNR	1	Right channel negative output.
HPOUTR	2	Right channel headphone output.
SDB	3	Shut-down control, 0=shutdown.
BYPASS	4	Bias voltage for power amplifiers.
INR	5	Input of right channel power amplifier.
AGND	6	Analog circuit's ground.
INL	7	Input of left channel power amplifier.
VOLUME	8	Internal gain setting input.
MUTE	9	Mute control, high active.
SE/BTLB	10	Output mode control, 1=SE mode, 0=BTL mode.
AGC	11	Maximum power output setting.
UVP	12	Under voltage protection unit.
AVDD	13	Power supply.
HPOUTL	14	Left channel headphone output.
OUTNL	15	Left channel negative output.
PVDD	16	Power supply.
OUTPL	17	Left channel positive output.
PGND	18	Power amplifier's ground.
OUTPR	19	Right channel positive output.
PVDD	20	Power supply.

Functional Block Diagram



Ordering Information

Product ID	Package	Packing / MPQ	Comments
AD52080-HI20NRY	TQFN-20L	490 Units / Tray 4900 Units / Small Box	Green
AD52080-HI20NRR		5000 Units / Reel 10000 Units / Small Box	Green

Available Package

Package Type	Device No.	θ_{JA}(℃/W)	θ_{JT} (℃/W)	Ψ_{JT} (℃/W)	Exposed Thermal Pad
TQFN-20L (4mm x 4mm)	AD52080	46	52.8	1.3	Yes (Note 1)

Note 1.1: The thermal pad is located at the bottom of the package. To optimize thermal performance, soldering the thermal pad to the PCB's ground plane is necessary.

Note 1.2: θ_{JA} is simulated on a room temperature (T_A=25℃), natural convection environment test board, which is constructed with a thermally efficient, 4-layers PCB (2S2P). The measurement is simulated using the JEDEC51-5 thermal measurement standard.

Note 1.3: θ_{JT} represents the thermal resistance for the heat flow between the chip junction and the package's top surface. It's extracted from the simulation data with obtaining a cold plate on the package top.

Note 1.4: Ψ_{JT} represents the thermal parameter for the heat flow between the chip junction and the package's top surface center. It's extracted from the simulation data for obtainingθ_{JA}, using a procedure described in JESD51-5.

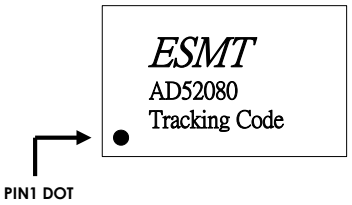
Marking Information

AD52080

Line 1 : LOGO

Line 2 : Product no.

Line 3 : Tracking Code



Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
AVDD	Power supply for analog circuits	3.0	6	V
PVDD	Power supply for loudspeaker driver	3.0	6	V
	Input voltage	-0.3	AVDD	V
T_{stg}	Storage temperature	-65	150	°C
T_J	Operating junction temperature range	-40	150	°C
T_A	Ambient operating temperature	-40	85	°C
R_L	Minimum Load Resistance for speaker	3.2		Ω
	Minimum Load Resistance for headphone	16		
ESD	Human Body Model		±2k	V
	Charged Device Model		±500	

General Electrical Characteristics

- T_A=25°C (unless otherwise noted)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
VDD	Supply voltage	AVDD and PVDD	3		5.8	V
VIH	Input high threshold	SDB, MUTE and SE/BTLB	1.4			V
VIL	Input low threshold	SDB, MUTE and SE/BTLB			0.6	V
IQ	Quiescent current	BTL, no load		6	12	mA
		SE, no load		2	4	mA
I_{mute}	Mute current	BTL, no load		2	6	mA
		SE, no load		2	4	mA
Isd	Shutdown current	BTL mode, unmute			1	uA
Iin	Input current_Vin=2V	SDB, MUTE, VOLUME and SE/BTLB		1.5		uA
Fosc	Switching frequency	VDD=3.0V to 5.5V	400	500	600	kHz
Ri	Input Resistance	BTL, Gain=20dB		35		kΩ
		SE, Gain=3.5dB		59		kΩ
Ron	Static drain-source on-state resistance	PMOS, VDD=5.5V, IL=0.8A		200		mΩ
		NMOS, VDD=5.5V, IL=0.8A		200		mΩ
Tstart	Start-up time from	CBYASS=2.2uF		1.4		Sec
OTP	Over temperature			170		°C
OTP_Hys	Over temperature			35		°C

Electrical Characteristics and Specifications of Loudspeaker Driver

- VDD=5V, R_L=4Ω, Gain=20dB , T_A=25°C (unless otherwise noted)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Po	Output power	THD+N=1%, RL=4Ω	2.2	2.5		W
		THD+N=1%, RL=8Ω		1.42		W
		THD+N=10%, RL=4Ω		3.0		W
		THD+N=10%, RL=8Ω		1.74		W
n	Efficiency	RL=4Ω, Po=3W		87		%
		RL=8Ω, Po=1.7W		92		%
THD+N	Total harmonic distortion plus noise	Fin=1kHz, RL=4Ω, Po=1.7W		0.08		%
		Fin=1kHz, RL=8Ω, Po=1W		0.09		%
XTLK	Crosstalk, channel	Po=0.2W, RL=4Ω, Fin=1kHz		-100		dB
PSRR	Power supply rejection ratio	RL=4Ω, Fin=100Hz		-70		dB
		RL=4Ω, Fin=1kHz		-70		dB
SNR	Signal to noise ratio	Vi=1Vrms, RL=8Ω, with		95		dB
Att(mute)	Mute attenuation	Fin=1kHz, RL=8Ω,		-105		dB
Att(shutdown)	Shutdown attenuation	Fin=1kHz, RL=8Ω,		-120		dB
Vn	Output noise voltage	with A-weighting filter,		50		uVrms
Vos_spk	Offset voltage	RL=4Ω, Gain=20dB		5	30	mV

- VDD=3.6V, R_L=4Ω, Gain=20dB , T_A=25°C (unless otherwise noted)

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Po	Output power	THD+N=1%, RL=4Ω		1.25		W
		THD+N=1%, RL=8Ω		0.73		W
		THD+N=10%, RL=4Ω		1.55		W
		THD+N=10%, RL=8Ω		0.89		W
n	Efficiency	RL=4Ω, Po=1.4W		84.5		%
THD+N	Total harmonic distortion plus noise	Fin=1kHz, RL=4Ω, Po=0.8W		0.11		%
		Fin=1kHz, RL=8Ω, Po=0.5W		0.1		%
XTLK	Crosstalk, channel	Po=0.2W, RL=4Ω, Fin=1kHz		-100		dB
PSRR	Power supply rejection ratio	RL=4Ω, Fin=100Hz		-70		dB
		RL=4Ω, Fin=1kHz		-70		dB
SNR	Signal to noise ratio	Vi=1Vrms, RL=8Ω, with		94		dB
Att(mute)	Mute attenuation	Fin=1kHz, RL=8Ω, Vin=1Vrms		-100		dB
Att(shutdown)	Shutdown attenuation	Fin=1kHz, RL=8Ω, Vin=1Vrms		-120		dB
Vn	Output noise voltage	with A-weighting filter,		50		uVrms
Vos	Offset voltage	RL=4Ω, Gain=20dB		5	30	mV

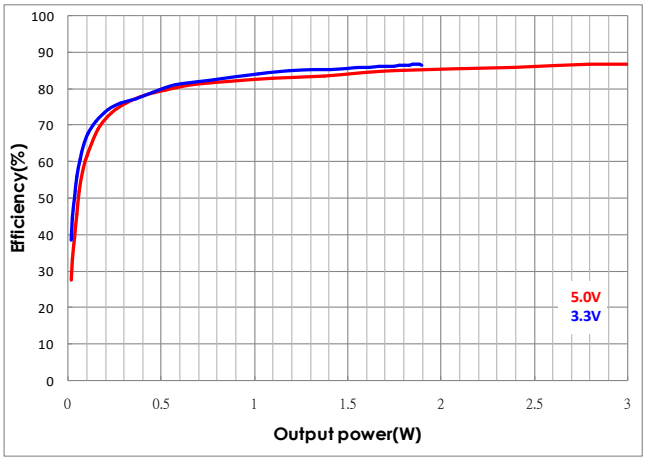
Electrical Characteristics and Specifications of Headphone Driver

- VDD=5V, R_L=32Ω, Gain=3.5dB, T_A=25°C (unless otherwise noted)

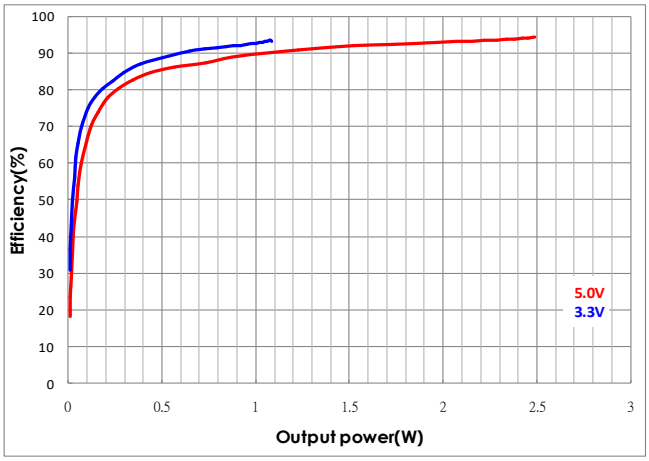
SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Po	Output power	THD+N=1%, RL=32Ω		90		mW
		THD+N=10%, RL=32Ω		110		mW
THD+N	Total harmonic distortion	Fin=1kHz, RL=32Ω, Po=42.5mW		0.013		%
XTLK	Crosstalk, channel	Po=6mW, RL=32Ω, Fin=1kHz		-102		dB
PSRR	Power supply rejection ratio	RL=32Ω, Fin=100Hz		-70		dB
		RL=32Ω, Fin=1kHz		-70		dB
SNR	Signal to noise ratio	Vo=1Vrms, RL=32Ω, with		96		dB
Att(mute)	Mute attenuation	Fin=1kHz, RL=32Ω, Vin=1Vrms		-85		dB
Att(shutdown)	Shutdown attenuation	Fin=1kHz, RL=32Ω, Vin=1Vrms		-75		dB
Vn	Output noise voltage	with A-weighting filter,		13		uVrms

Typical Characteristics

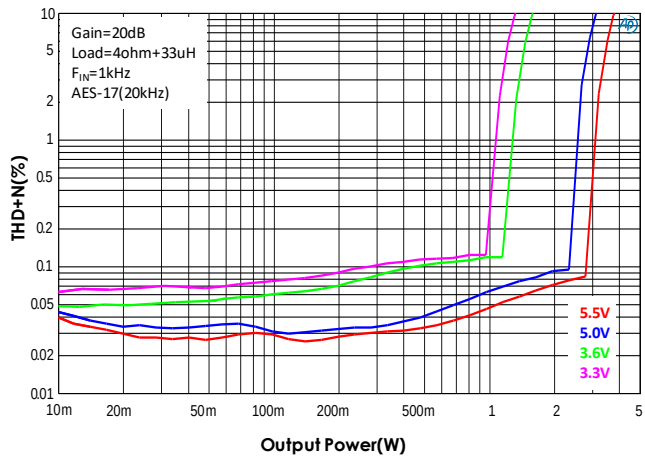
Efficiency (Stereo 4Ω load) / 2ch



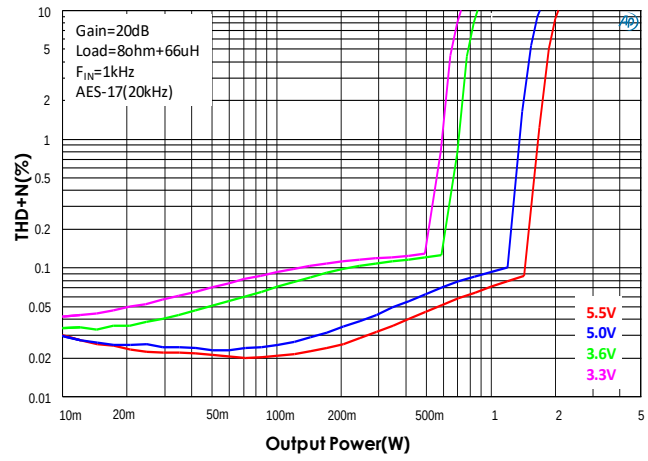
Efficiency (Stereo 8Ω load) / 2ch



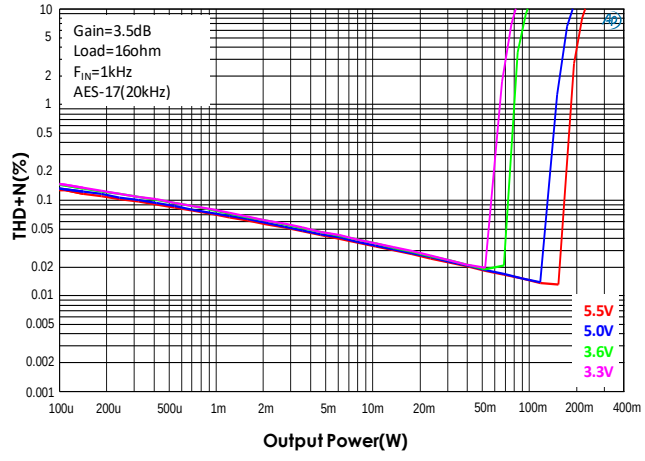
THD+N vs. Output Power, 4Ω load (BTL Mode)



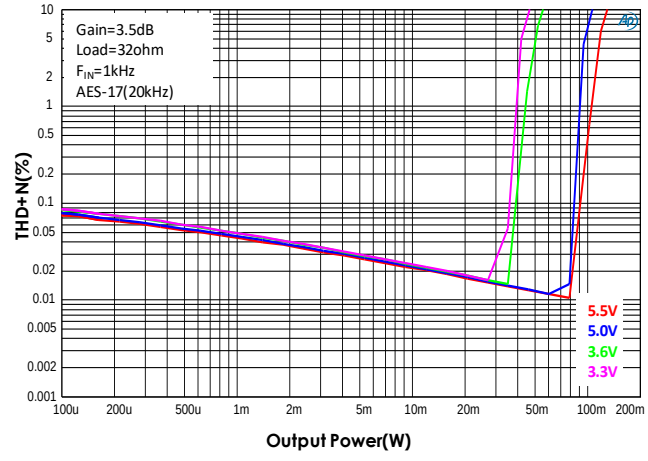
THD+N vs. Output Power, 8Ω load (BTL Mode)



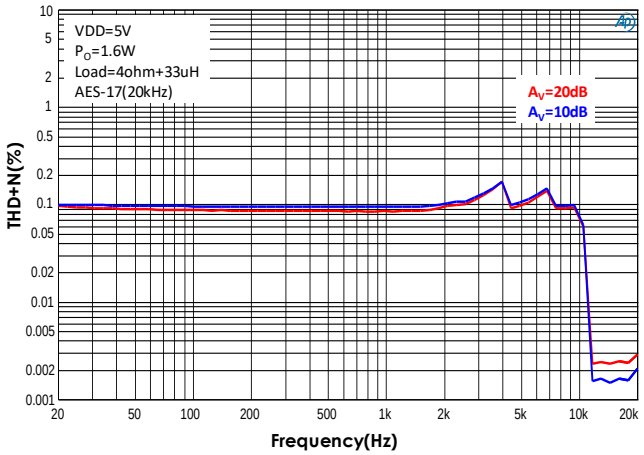
THD+N vs. Output Power, 16Ω load (SE Mode)



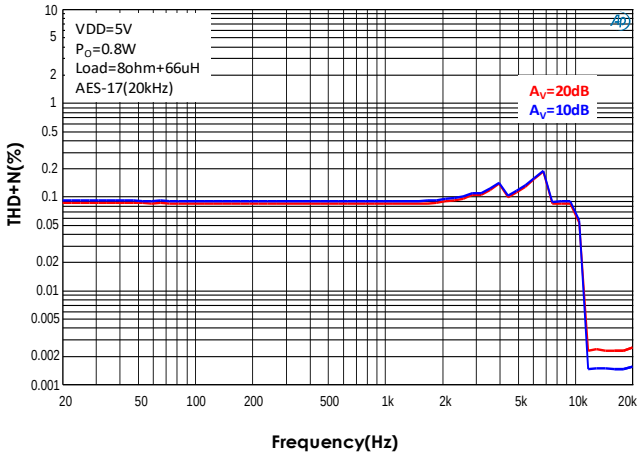
THD+N vs. Output Power, 32Ω load (SE Mode)



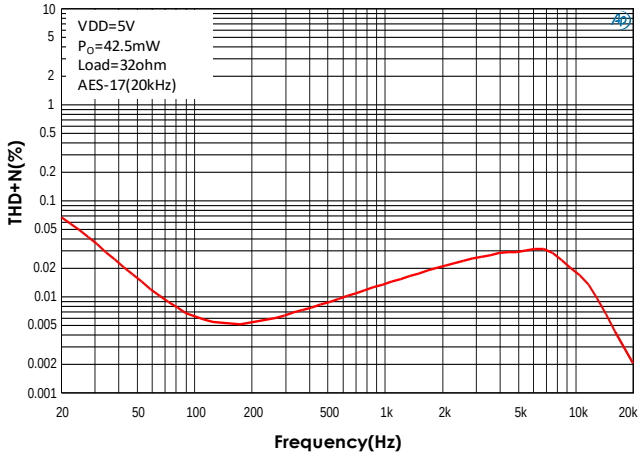
THD + N (%) vs. Frequency, 4Ω load (BTL Mode)



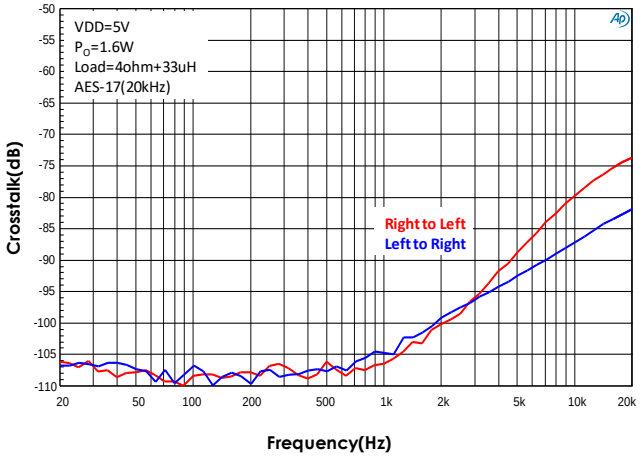
THD + N (%) vs. Frequency, 8Ω load (BTL Mode)



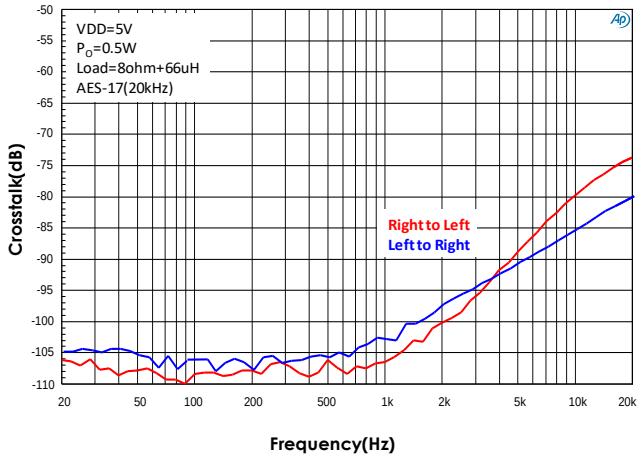
THD + N (%) vs. Frequency, 32Ω load (SE Mode)



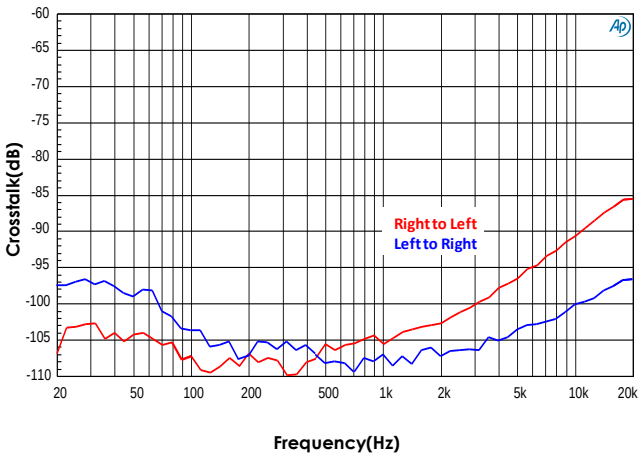
Cross-Talk ,4Ω load (BTL Mode)



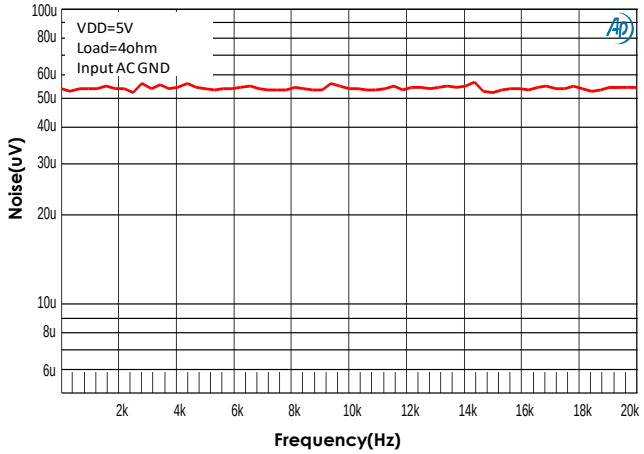
Cross-Talk ,8Ω load (BTL Mode)



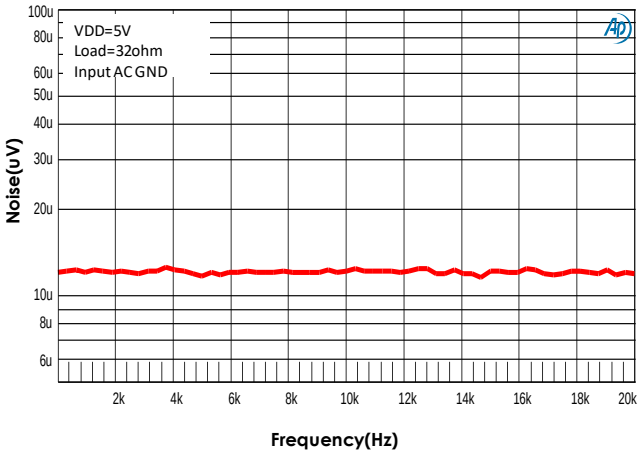
Cross-Talk ,32Ω load (SE Mode)



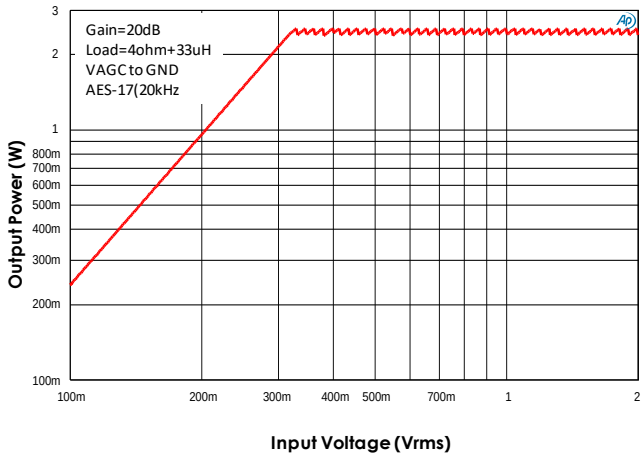
Noise, 4Ω load (BTL Mode)



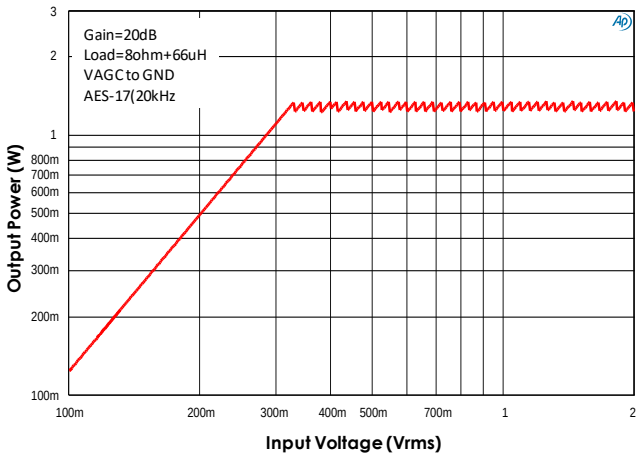
Noise, 8Ω load (SE Mode)



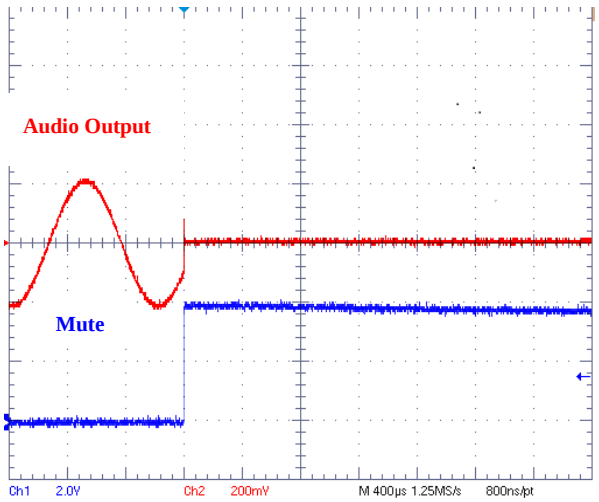
AGC Function
Output Power vs. Input AC, 4 load



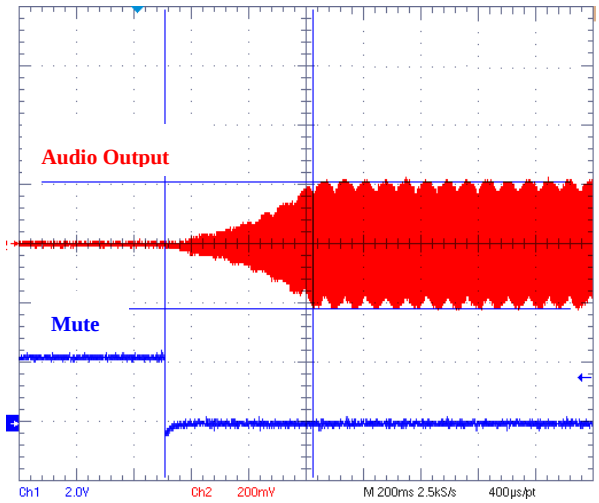
AGC Function
Output Power vs. Input AC, 8 load



Mute Enable (Gain=20dB)



Mute Release (Gain=20dB)



Operation Descriptions

●Volume Control Table

AD52080 has built-in a 64-steps DC volume controller, and the volume level is set by VOLUME pin which is ratio of AVDD.

AVDD=5V, T_A=25°C, no load

Step	BTL Gain(dB)	SE Gain(dB)	Recommended Voltage(V)	% of AVDD
1	20	3.5	0	0
2	19.6	3.2	0.14	2.8
3	19.2	2.9	0.21	4.2
4	18.8	2.6	0.29	5.8
5	18.4	2.3	0.37	7.4
6	18	2	0.45	9
7	17.6	1.7	0.52	10.4
8	17.2	1.4	0.6	12
9	16.8	1.1	0.68	13.6
10	16.4	0.8	0.76	15.2
11	16	0.5	0.83	16.6
12	15.6	0.1	0.91	18.2
13	15.2	-0.2	0.99	19.8
14	14.8	-0.5	1.07	21.4
15	14.4	-0.8	1.14	22.8
16	14	-1.2	1.22	24.4
17	13.6	-1.5	1.3	26
18	13.2	-1.8	1.38	27.6
19	12.8	-2.2	1.45	29
20	12.4	-2.5	1.53	30.6
21	12	-2.9	1.61	32.2
22	11.6	-3.2	1.69	33.8
23	11.2	-3.6	1.76	35.2
24	10.8	-3.9	1.84	36.8
25	10.4	-4.3	1.92	38.4
26	10	-4.6	2	40
27	9.6	-5	2.07	41.4
28	9.2	-5.4	2.15	43
29	8.8	-5.7	2.23	44.6
30	8.4	-6.1	2.31	46.2
31	8	-6.4	2.38	47.6
32	7.6	-6.8	2.46	49.2
33	7.2	-7.2	2.54	50.8

34	6.8	-7.5	2.62	52.4
35	6.4	-7.9	2.69	53.8
36	6	-8.3	2.77	55.4
37	5.6	-8.6	2.85	57
38	5.2	-9	2.93	58.6
39	4.8	-9.4	3	60
40	4.4	-9.8	3.08	61.6
41	4	-10.1	3.16	63.2
42	3.6	-10.5	3.24	64.8
43	3.2	-10.9	3.31	66.2
44	2.8	-11.3	3.39	67.8
45	2.4	-11.6	3.47	69.4
46	2	-12	3.55	71
47	1.6	-12.4	3.62	72.4
48	1.2	-12.8	3.7	74
49	0.8	-13.1	3.78	75.6
50	0.4	-13.5	3.86	77.2
51	0	-13.9	3.93	78.6
52	-1	-14.9	4.01	80.2
53	-2	-15.8	4.09	81.8
54	-3	-16.8	4.17	83.4
55	-5	-18.8	4.24	84.8
56	-7	-20.7	4.32	86.4
57	-9	-22.7	4.4	88
58	-11	-24.7	4.48	89.6
59	-17	-30.7	4.55	91
60	-23	-36.9	4.63	92.6
61	-29	-43	4.71	94.2
62	-35	-49.3	4.79	95.8
63	-41	-55.3	4.86	97.2
64	-60	-60	5	100

- AGC Non-clip Function

AD52080 support AGC non-clip function to keep power amplifier performs high quality audio into speakers and to prevent the speakers from damage when higher volume level is selected. Using AGC pin to set the power limited threshold.

AGC Setting	Limited Output Power
0.45x AVDD ~ AVDD or floating	Disable AGC function
0.27x AVDD ~ 0.45xAVDD	$Po = \frac{8\times(\frac{AVDD}{2}-AGC)^2}{RL} X0.95$
0V ~ 0.27xAVDD	Po(max)= 2.5W into 4Ω Po(max)= 1.35W into 8Ω

- Short-circuit Protection

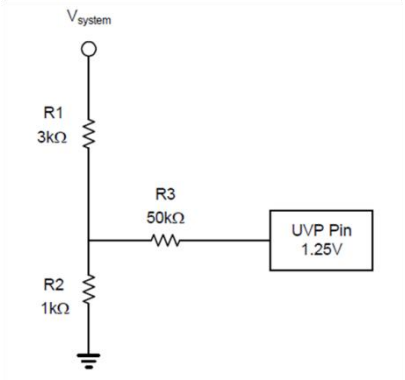
To protect loudspeaker drivers from over-current damage, AD52080 has built-in short-circuit protection circuit. When the wires connected to loudspeakers are shorted to each other, GND or power supply, overload detectors may activate. Once short circuit is detected, AD52080 would auto recovery while short-circuit is removed.

- Over Temperature Protection

If the internal junction temperature is higher than 170°C, the outputs of loudspeaker drivers will be disabled and at low state. The temperature hysteresis for AD52080 to return to normal operation is about 30°C.

- Under Voltage Protection (UVP)

Under voltage protection can be used to shutdown AD52080 by external circuit to set the AVDD threshold. Below equations shows how to design the UVP threshold.



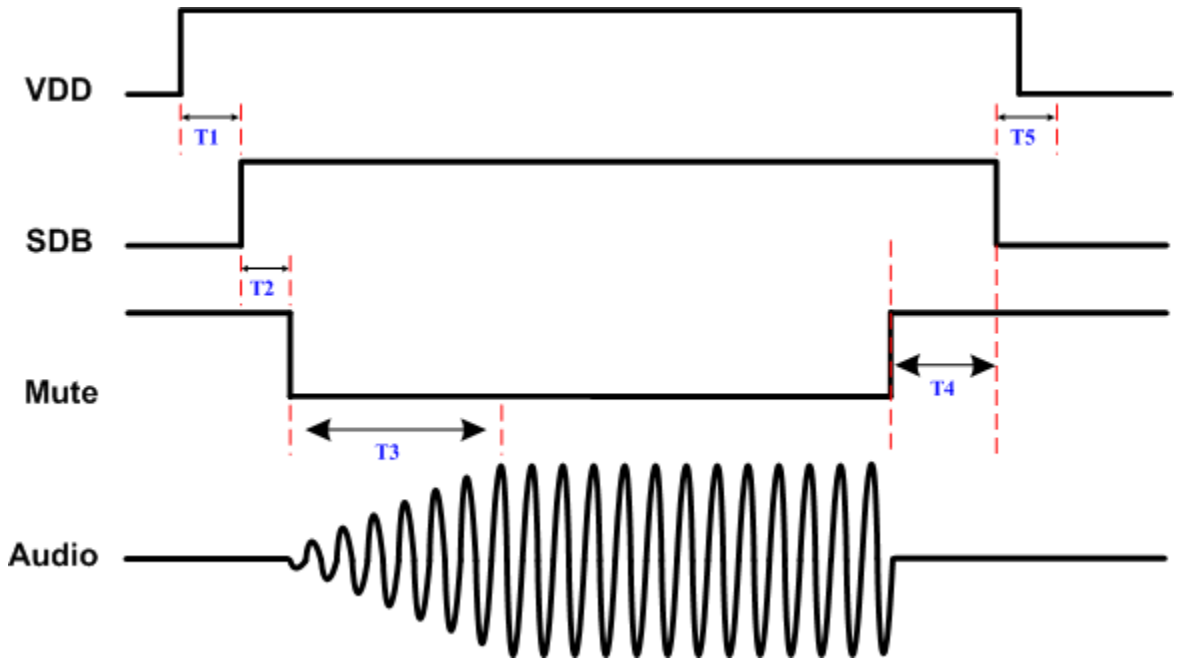
With the condition: R3 >> R1//R2

$$UVP\ threshold = [1.25\text{-}(6\mu A \times R3)] \times \frac{R1+R2}{R2}$$

$$Hysteresis = 5\mu A \times R3 \times \frac{R1+R2}{R2}$$

- Mute control (MUTE)

  Like shutdown mode, AD52080 ceases output driver, but keeps parts of internal circuits still working. That could provide lower standby current, quick disable and enable power amplifier. AD52080 with volume fade-in/fade-out design during mute process, the relative mute timing diagrams are shown below.



Symbol	Min. (ms)	Typ. (ms)	Max. (ms)
t1	0	-	-
t2	0	-	-
t3	Depend on Gain setting	528 (gain=20dB)	972
t4	-	-	1
t5	0	-	-

- Bypass Voltage

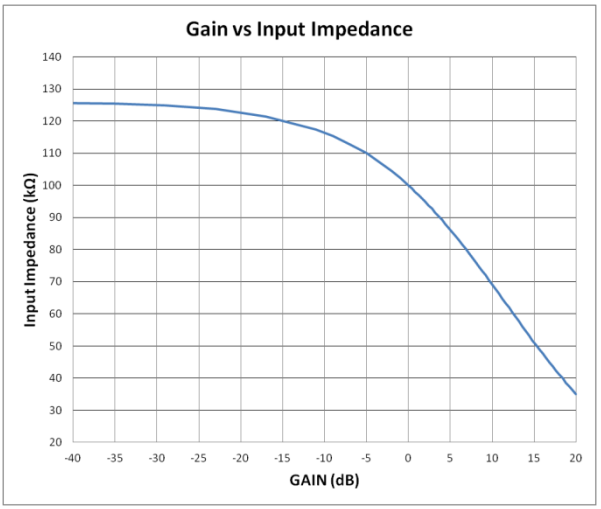
  Bypass voltage of AD52080 is equal to AVDD/2. The external capacitor for this referenced voltage is a critical component and serves several performances.

Application information

- Input capacitors (C_{in})

  The performance at low frequency (bass) is affected by the corner frequency (f_c) of the high-pass filter composed of input resistors (R_{in}) and input capacitors (C_{in}), determined in equation (a). And, the resistance of input resistors is different at different volume gain. But there is 20% variation in input resistance from 20% process variation in actual resistance of the input resistors. Typically, a 0.47μF or 1μF ceramic capacitor is suggested.

$$f_c = \frac{1}{2\pi R_{in} C_{in}} \ (Hz) \quad \cdots\cdots\cdots (a)$$



- Capacitor on BYPASS (C_{Byp})

  In order to reduce low-frequency noise produced by power supply, the capacitor (C_{Vref}) on Vref, which is the mid-rail voltage of AVDD, is necessary. It is also good for PSRR. And, to have less annoying pop, the recommended C_{Vref} is the same with Cin.

- Decoupling capacitor

  Because of the power loss on the trace, which is between the device and decoupling capacitor, the decoupling capacitor should be placed as close to the device PVDDL (PVDDR) and PGNDL (PGNDR) to reduce any parasitic resistor or inductor between them. And, a low ESR ceramic capacitor, typically 1μF, is suggested for high frequency transients and as close to AD52080 as possible. For filtering audio band noise signal, a 10μF or greater capacitor (tantalum or electrolytic type) is suggested.

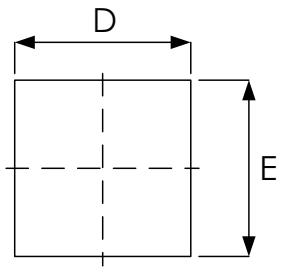
- Headphone DC decoupling capacitors (C_{hp})

  The DC decoupling capacitors (C_{hp}) between headphone and HPL/HPR pins are used to remove the DC voltage on the headphone from HPL/HPR. The high pass filter, which is composed of the headphone resistance and the DC decoupling capacitor, attenuates the low frequency audio performance. For 16Ω headphone, the electrolytic or tantalum capacitor with 100μF or greater is suggested. The relationship between f_{hc}, R_{hp} and C_{hp} is shown in the below equation (b).

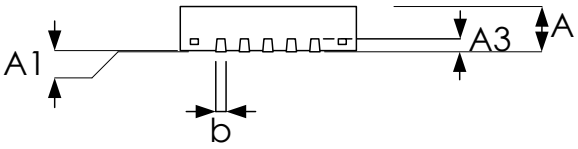
$$f_{hc} = \frac{1}{2\pi R_{hp} C_{hp}} \ (Hz) \quad \cdots\cdots\cdots (b)$$

Package Dimensions

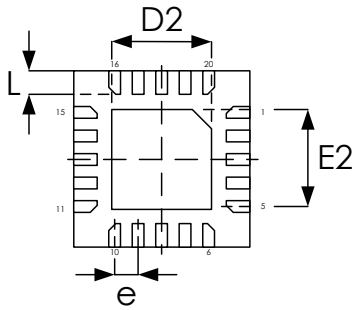
- **TQFN-20L (4mmx4 mm)**



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Symbol	Dimension in mm	
	Min	Max
A	0.70	0.85
A1	0.00	0.05
A3	0.18	0.03
b	0.18	0.30
D	3.90	4.10
E	3.90	4.10
e	0.50 BSC	
L	0.30	0.50

	Dimention in mm	
	Min	Max
D2	1.90	2.05
E2	1.90	2.05

Revision History

Revision	Date	Description
0.1	2019.04.15	Initial version.
0.2	2020.02.18	Update typical characteristics. Update operation descriptions. Update pin description.
1.0	2020.05.18	Remove" Preliminary" and revision to 1.0
1.1	2020.09.24	Update features. Update typical characteristics. Update operation descriptions.

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