

設計驗證
工程課
2025 -06- 06
發行

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AIT group

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APPROVAL SHEET

CUSTOMER: 鈺緯科技開發股份有限公司

BRAND: **MPS**

PART NUMBER: **MP8856GQE-0000-Z**

CUSTOMER P/N: **3AMP885601Y** (A0562)

DATE: **2025/5/28**

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零件承認	
核准	負責人
ASIAN INFORMATION TECHNOLOGY INC. 詮鼎科技股份有限公司	
承認日期	年 月 日

詮鼎科技股份有限公司
Asian Information Technology Inc.
業務人員：陳文豪

MP8856

36V,140W Hybrid Buck Converter Integrates Low Side MOSFET Supports 100% Duty and IMON

PRELIMINARY SPECIFICATIONS SUBJECT TO CHANGE

DESCRIPTION

The MP8856 is a synchronous, low-side switch integrated step-down converter capable of regulating the output voltage from wide input voltage range with high efficiency. It can deliver 5A output current with excellent load and line regulation. The integrated output voltage scaling and adjustable output current limit functions meet the USB Power Delivery (PD) and PPS requirement.

The MP8856 supports 100% duty cycle function to reduce the Vin to Vout dropout voltage meanwhile provides high efficiency. It also provides output isolation switch gate driver.

The MP8856 implements PMBUS interface, which supports flexible design for different applications. It provides programmable accurate input and output constant current (CC) limit, adjustable reference voltage from 0.1V to 2.147V, selectable PFM/PWM mode, programmable Line drop compensation, soft-start and EN shutdown discharge, which supports flexible design for different applications.

Internal feedback resistor ratio VOUT/VFB (FB_RATIO)=10, supporting 1V to 21.47V output voltage range with 10mV resolution through PMBus interface; Internal feedback resistor ratio VOUT/VFB (FB_RATIO)=16, supporting 1.6V to 28V output voltage range with 16mV resolution through PMBus interface.

Full protection features include OCP, OVP, UVP and thermal shutdown protection.

The MP8856 is available in a 16-pin QFN (3mmx3mm) package.

FEATURES

- IEC62368-1 Certified
- Buck Converter with Low-side MOSFET Integrated
- Wide 4V to 36V Operation Input Voltage
- Supports 1V to 21.47V or 1.6V to 28V VOUT Range
- Support True 100% Duty Cycle Operation
- Up to 99.55% Peak Efficiency in 100% Duty
- Meet USB-PD Peak Current Capability
- Integrated High-side Switch Gate Driver
- Output Isolation NMOSFET Gate Driver
- 5% Accurate Output CC Current Limit
- 5% Accurate Input CC Current Limit
- Output Bias function for VCC supply
- 450kHz/950kHz Switching Frequency with Frequency Dithering
- Output OVP/OCP/SCP Protection
- Over Temperature Warning and Shutdown
- PMBus Programmable Parameters Include:
  - Input/output CC Current limit
  - Line Drop Compensation
  - PFM/PWM
  - Frequency
  - EN Shutdown Discharge
- Available in QFN-16 (3mmx3mm) Package with Wettable Flank

MPL Optimized Performance with MPS Inductor MPL-AY Series

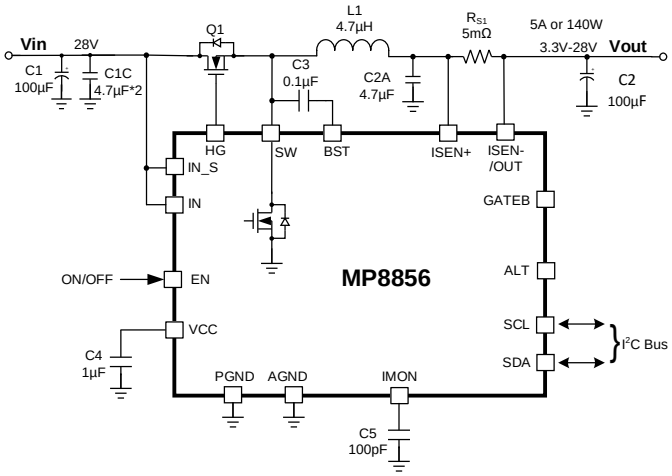
APPLICATIONS

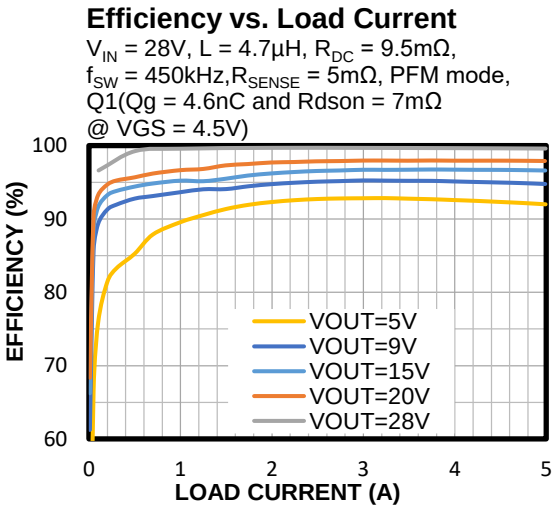
- USB Type-C and USB PD3.1 Multi-ports Adapter
- USB Type-C PD Monitors and Docking Stations
- High Power DC/DC Converter

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TYPICAL APPLICATION





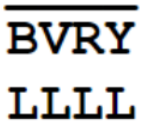
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ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL
MP8856GQE-xxxx **	QFN-16 (3mmx3mm)	*See Below*	1
MP8856GQE-00A0			
MP8856GQE-00A1			
EVKT-MP8856	Evaluation kit		

*For Tape & Reel, add suffix -Z (e.g. MP8856GQE-xxxx-Z).
** "xxxx" is the configuration code identifier for the register setting stored in the OTP. The default number is "0000", which is already preprogrammed by MPS factory. User can't reprogram it. MP8856-00A0 supports 1.6V to 28V output voltage, can be used for 140W EPR application. MP8856-00A1 supports 1V to 21.47V output voltage, can be used for ≤100W SPR application. Each "x" can be a hexadecimal value between 0 and F. Please work with an MPS FAE to create this unique number, even if ordering the "0000" code.

TOP MARKING

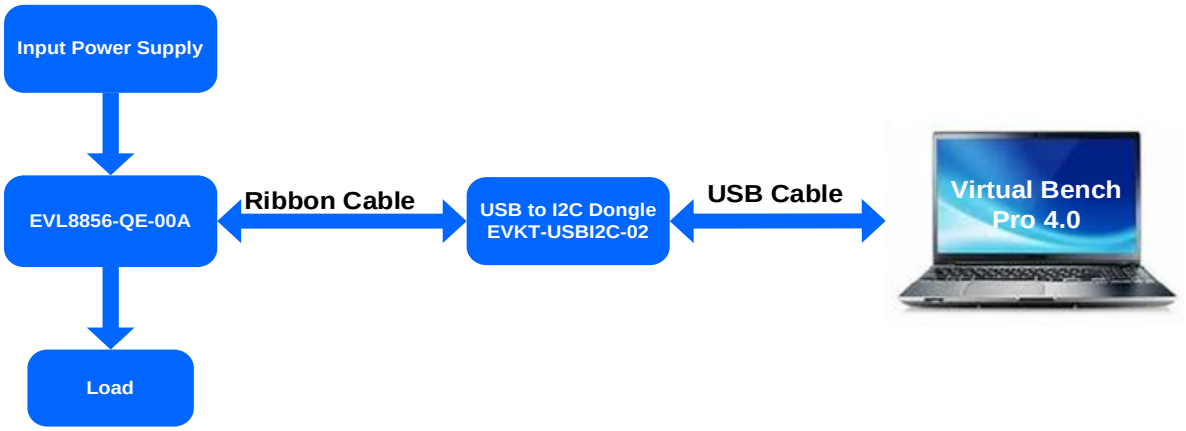


BVR: Product code of MP8856GQE
Y: Year code
LLLL: Lot number

Evaluation Kit EVKT-MP8856

EVKT-MP8856 Kit contents:

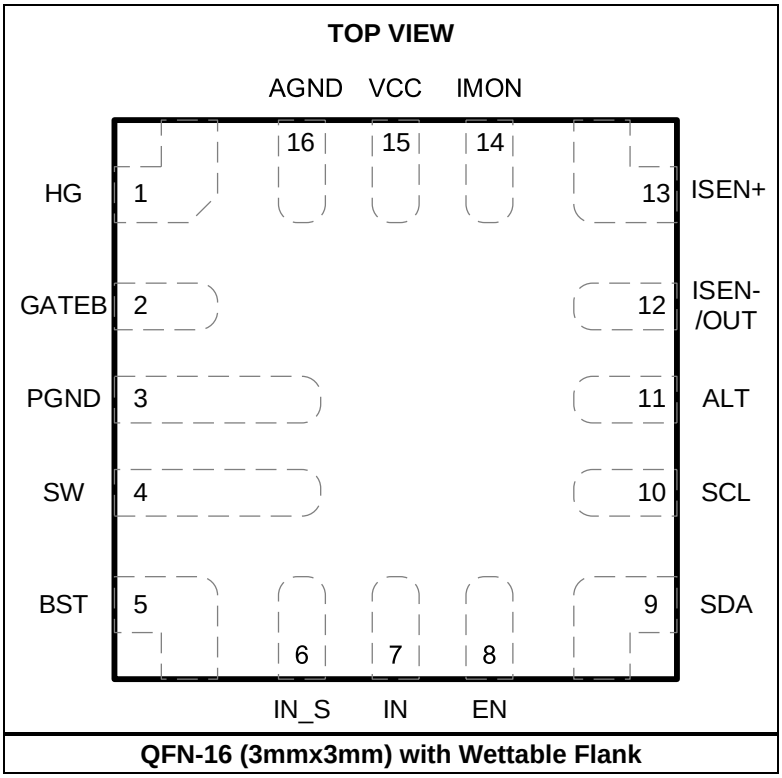
#	Part Number	Item	Quantity
1	EVL8856-QE-00A	MP8856GQE Evaluation Board	1
2	EVKT-USBI2C-02	USB to I2C Communication interface device, USB Cable and Ribbon Cable	1
3	MP8856GQE-0000	IC with default configuration	2



EVKT-MP8856 Evaluation Kit Set-Up

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PACKAGE REFERENCE



QFN-16 (3mmx3mm) with Wettable Flank

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PIN FUNCTIONS

Pin #	Name	Description
1	HG	**External high-side MOSFET driver.** Connect it to the gate of high-side power MOSFET with wide and short trace.
2	GATEB	**Output isolation switch's gate drive.** Connect this pin to the gate of isolation NMOSFET.
3	PGND	**Power Ground.** PGND requires extra care during PCB layout. Connect to GND with copper traces and vias.
4	SW	**Switch node of the Buck.** Use a wide PCB trace to make the connection.
5	BST	**Bootstrap**. A 0.1µF capacitor is connected between SW and BST to form a floating supply across the high-side switch driver. R_{BST} must be 0Ω when V_{IN}-V_{OUT}≤1V.
6	IN_S	**Negative input of current-sense.** Connect it to Vin when input current sense is not needed. It can't be floated or connected to GND.
7	IN	**Supply voltage.** IN is the power supply to the entire chip. The MP8856 operates from a 4V to 36V input voltage. Put a 0.1µF capacitor (CIN) close to this pin.
8	EN	**Enable input.** Apply logic high to enable the chip; Apply logic low to disable the chip. EN is a high voltage pin, which can connect to Vin directly.
9	SDA	**PMBus Serial Data.** If not used, SDA should be pulled up to VCC.
10	SCL	**PMBus Serial Clock.** If not used, SCL should be pulled up to VCC.
11	ALT	**PMBus alert.** Open drain output, active low.
12	ISEN-/OUT	**Negative node of Current sense signal input.** A current sense resistor should be placed on output trace to sense the DC current. Then connect ISEN- pin to the right side of sensing resistor. This pin is also used as output voltage sense.
13	ISEN+	**Positive node of output current sense signal input.** A current sense resistor should be placed on output trace to sense the DC current. Then connect ISEN+ pin to the left side of sensing resistor.
14	IMON	**Output current monitor.** This pin indicates the output current.
15	VCC	**Internal 5.25V LDO Regulator Output.** Decouple with a 1µF capacitor between VCC and AGND.
16	AGND	**Analog Ground.** Connect AGND to PGND.

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ABSOLUTE MAXIMUM RATINGS(1)

Supply Voltage V_{IN} ,V_{IN_S}..... -0.4V to +40V
V_{SW} .....
-0.3V (-5V for <10ns) to V_{IN} + 0.3V (42V for <10ns)
$V_{BST, HG}$ .....V_{SW} + 6V
$V_{GATEB, ISEN+, ISEN-/OUT}$, V_{EN}..... -0.3V to +40V
All Other Pins..... -0.3V to +6V
Continuous Power Dissipation (T_A = +25°C) (2) (5)
QFN-16 (3mmx3mm).....3.6W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature..... -65°C to +150°C

ESD Rating (3)

All pins (HBM) .....±1.5kV
All pins (CDM) .....±750V

Recommended Operating Conditions (4)

Supply Voltage V_{IN}..... 4V to 36V
Output Voltage V_{OUT}..... 1V to 28V
Output Current/Output Power 5A/140W
Operating Junction Temp.(T_J).. -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

EVL8856-QE-00A (5).....34.6…10.7 °C/W
QFN-16 (3mmx3mm) (6).....50…..12…°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature TJ (MAX), the junction-to-ambient thermal resistance θJA, and the ambient temperature TA. The maximum allowable continuous power dissipation at any ambient temperature is calculated by PD (MAX) = (TJ (MAX)-TA)/θJA. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) HBM, per JEDEC specification JESD22-A114; CDM, per JEDEC specification JESD22-C101. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on MP8856 test board, four layer PCB.
6) Measured on JESD51-7, 4-layer PCB. The value of θJA given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{EN} = 5V, T_J= -40°C to 125°C(7), Typical values is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Current (Shutdown)	I_{Q_STD}	V_{EN}=0V		1	5	μA
Supply Current (Quiescent)	I_{Q1}	No switching, EN on, Vout apply 5V, T_J=+25°C		400	600	μA
	I_{Q2}	No switching, EN on, Vout apply 5V, T_J=-40°C to +125°C		600	1000	μA
	I_{Q3}	I2C set Operation=off, EN on		120	250	μA
EN Rising Threshold	V_{EN_Rising}		1.2	1.3	1.4	V
EN Hysteresis	$V_{EN_Falling}$			150		mV
EN Pull-down Resistor	R_{EN}	EN=2V		2		MΩ
Thermal Shutdown(8)	T_{STD}			165		°C
Thermal Hysteresis(8)	T_{STD_HYS}			25		°C
VCC Regulator	V_{CC}		4.85	5.25	5.35	V
VCC Load Regulation	V_{CC_LOG}	I_{CC}=50mA		2	6	%
V_{IN} Under-Voltage Lockout Threshold Rising	$V_{IN_UVLO_R}$		3.4	3.6	3.8	V
V_{IN} Under-Voltage Lockout Falling Threshold	V_{UVLO_F}			3.3		V
Buck Converter						
Output Voltage	V_{OUT1}		-3%	3.3	+3%	V
	V_{OUT2}		-2.5%	5.1	+2.5%	V
	V_{OUT3}		-1.5%	20	+1.5%	V
Output Over-Voltage Protection	V_{OVP_R}			118		%
Output OVP Recovery	V_{OVP_F}			105		%
Input OVP Rising	V_{INOVP_R}		36.2	39	41	V
LS Switch On Resistance	R_{DSON_LS}			20		mΩ
Dead Time (8)	TD_{HS_RISE}			20		ns
	TD_{HS_FALL}			20		ns
Output Discharge Resistor	R_{DISCHG}			220		Ω
Switch Leakage	SW_{LKG}	V_{EN}=0V, V_{SW}=36V, T_J=+25°C			1	μA
		V_{EN}=0V, V_{SW}=36V, T_J=-40°C to +125°C (8)			5	
		V_{EN}=0V, V_{SW}=36V, T_J=-40°C to +150°C			50	
Hiccup Off Timer	T_{hiccup}	V_{OUT}=5V		400		ms

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_J= -40°C to 125°C(7), Typical values is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Oscillator Frequency	f_{SW1}		700	950	1200	kHz
	f_{SW2}		380	450	520	
Frequency Dithering Span	FS_{Range}			±6		%
Soft-Start Time	t_{SS}	Output from 10% to 90%, V_{OUT}=5V Constant slew rate for other Vref	0.5	1.2	1.9	ms
Max Duty Cycle	D_{MAX}			100		%
Min On Time(8)	T_{ON_MIN}			80		ns
Min Off Time(8)	T_{OFF_MIN}			80		ns
ISEN+/- OC Threshold	Ioc1	OC threshold=1A, 5mΩ Rsens, T_J=+25°C	4.25	5	5.75	mV
		OC threshold=1A, 5mΩ Rsens, T_J=-40°C to +150°C	3.7	5	7	mV
	Ioc2	OC threshold=3.6A, 5mΩ Rsens, T_J=+25°C	17.1	18	18.9	mV
		OC threshold=3.6A, 5mΩ Rsens, T_J=-40°C to +150°C	16.2	18	20	mV
ISEN+/- OC Blank Timer	t_{OCISEN}		-20%	19	+20%	ms
ISEN+/- 2nd OC	Ioc3			20		A
Input OC Threshold	Ioci1	OC threshold=1A, 5mΩ Rsens	4.25	5	5.75	mV
	Ioci2	OC threshold=3.6A, 5mΩ Rsens	-5%	18	+5%	mV
IIN Peak Current Limit	t_{INCC3}			27		A
Low-side Valley Current Limit	I_{LIMIT1}		6	8	12	A
Low-side Negative Current Limit	I_{LIMIT2}			-4		A
Line Drop Compensation	V_{DROP}	Vout compensates 300mV@3A Iout, I_{OUT}=1A, T_J=-40°C to +150°C	65	100	120	mV
Imon Gain	Gmon	5mΩ Rsens, I_{OUT}=3A or 5A, T_J=+25°C	-3%	56	+3%	V/V
Vbus Isolation Switch Gate Driver - GATEB						
Output Voltage	V_{GATEB}	V_{IN}=20V, V_{CC}=5.25V		25		V
Source Current	I_{Source}			40		µA
External high-side MOSFET driver - HG						
HG Gate Source Current Capability(8)	I_{HG_SRC}	5.2V_{BST-SW}, 4.7nF load		1		A
HG Gate Sink Current Capability(8)	I_{HG_SINK}	5.2V_{BST-SW}, 4.7nF load		1.6		A
HG Gate Source Resistance	R_{HG_SRC}	5.2V_{BST-SW}		1.5	2.5	Ω
HG Gate Sink Resistance	R_{HG_SINK}	5.2V_{BST-SW}		1	1.5	Ω
ALT pin leakage	I_{ALT_LKG}	V_{ALT}=5V			0.1	µA

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 12V, V_{EN} = 5V, T_J= -40°C to 125°C(7), Typical values is tested at T_J = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
ALT pin Pull Low Resistance	R_{ALT}			15		Ω
Status Register Threshold						
PG Lower Rising Threshold	V_{PG_R}	PG switches high	87%	92%	97%	VFB
PG Lower Falling Threshold	V_{PG_F}	PG switches low		81%		VFB
VOUT_UV_FAULT_Rising	$VOUT_{UV_F_R}$		60%	65%	70%	VFB
VOUT_UV_FAULT Hysteresis	$VOUT_{UV_HYS}$			5%		VFB
PMBus Interface Specifications (Hs-Mode) (8)						
Input Logic High	V_{IH}		1.4			V
Input Logic Low	V_{IL}				0.6	V
Output Voltage Logic Low	V_{OUT_L}				0.4	V
SCL Clock Frequency	f_{SCL}			400	1000	kHz
SCL High Time	t_{HIGH}		60			ns
SCL Low Time	t_{LOW}		160			ns
Data Setup Time	$t_{SU.DAT}$		10			ns
Data Hold Time	$t_{HD.DAT}$		0	60		ns
Setup Time for (Repeated) Start Condition	$t_{SU.STA}$		160			ns
Hold Time for (repeated) Start Condition	$t_{HD.STA}$		160			ns
Bus Free Time between a Start and a Stop Condition	t_{BUF}		160			ns
Setup Time for Stop Condition	$T_{SU.STO}$		160			ns
Rise Time of SCL and SDA	t_R		10		300	ns
Fall Time of SCL and SDA	t_F		10		300	ns
Pulse width of Suppressed Spike	t_{SP}		0		50	ns
Capacitance for Each Bus Line	C_B				400	pF

Notes:

7) All minimum and maximum parameters are tested at T_J = 25°C. Over-temperature limits are guaranteed by characterization and correlation.

8) Not tested in production and guaranteed by design and characterization.

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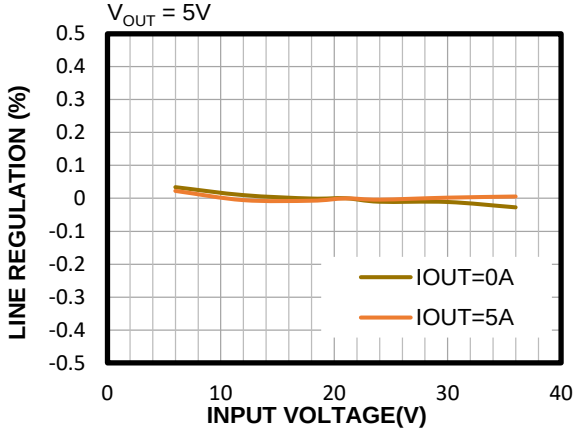
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TYPICAL CHARACTERISTICS

V_{IN} = 20V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 450kHz, Auto PFM/PWM mode, T_A = 25°C, unless otherwise noted.

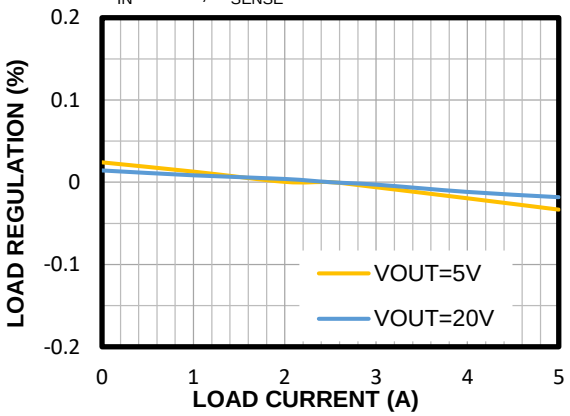
Line Regulation

V_{OUT} = 5V



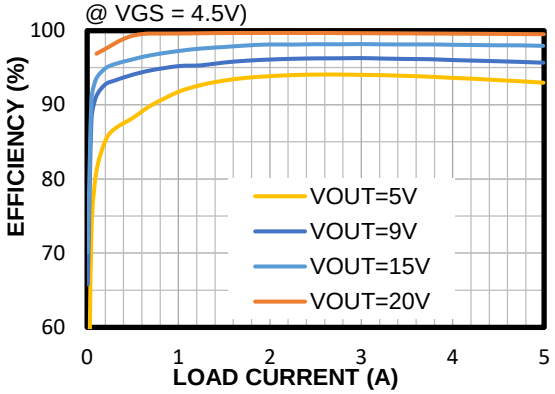
Load Regulation

V_{IN} = 24V, R_{SENSE} = 5mΩ



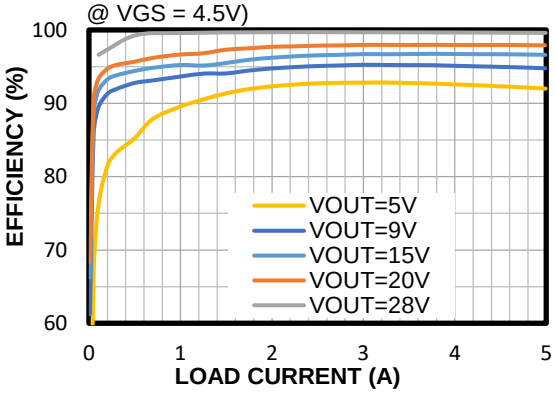
Efficiency vs. Load Current

V_{IN} = 20V, L = 4.7µH,R_{DC} = 9.5mΩ,
f_{SW} = 450kHz, R_{SENSE} = 5mΩ, PFM mode,
Q1(Qg = 4.6nC and Rdson = 7mΩ
@ VGS = 4.5V)



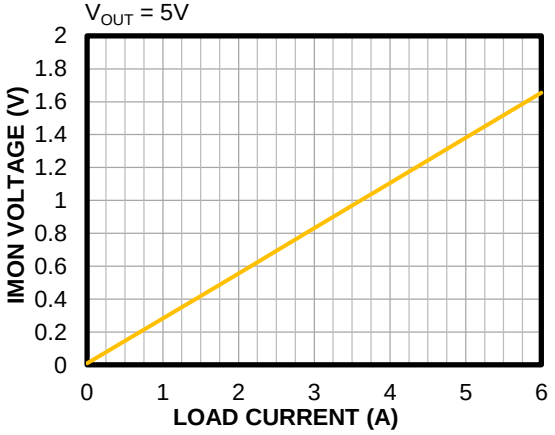
Efficiency vs. Load Current

V_{IN} = 28V, L = 4.7µH, R_{DC} = 9.5mΩ,
f_{SW} = 450kHz,R_{SENSE} = 5mΩ, PFM mode,
Q1(Qg = 4.6nC and Rdson = 7mΩ
@ VGS = 4.5V)



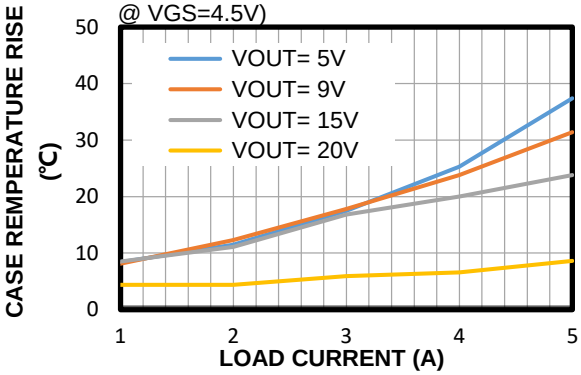
IMON Voltage vs. Load Current

V_{OUT} = 5V



Case Temperature Rise

V_{IN} = 20V, V_{OUT} = 5V/9V/15V/20V,
f_{SW} = 450kHz, L = 4.7µH, RDC = 9.5mΩ,
based on 6.35cm*6.35cm board,
Q1(Qg = 4.6nC and Rdson = 7mΩ
@ VGS=4.5V)



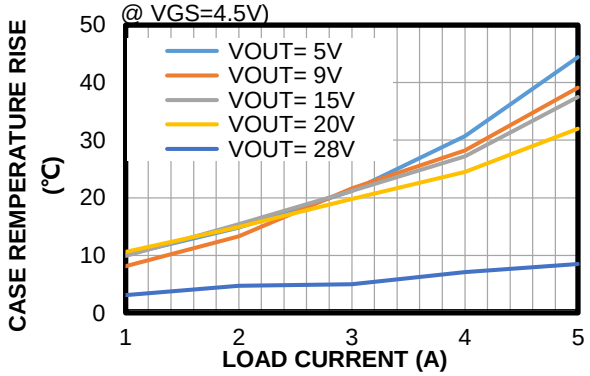
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TYPICAL CHARACTERISTICS *(continued)*

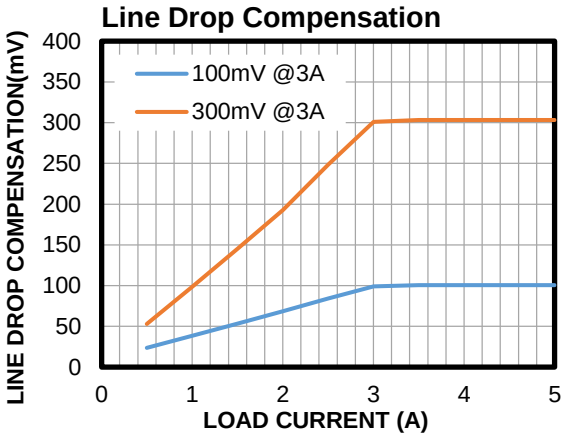
V_{IN} = 20V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 450kHz, Auto PFM/PWM mode, T_A = 25°C, unless otherwise noted.

Case Temperature Rise

V_{IN} = 28V, V_{OUT} = 5V/9V/15V/20/28V,
f_{SW} = 450kHz, L = 4.7µH, RDC = 9.5mΩ,
based on 6.35cm*6.35cm board,
Q1(Qg = 4.6nC and Rdson = 7mΩ
@ VGS=4.5V)



Line Drop Compensation



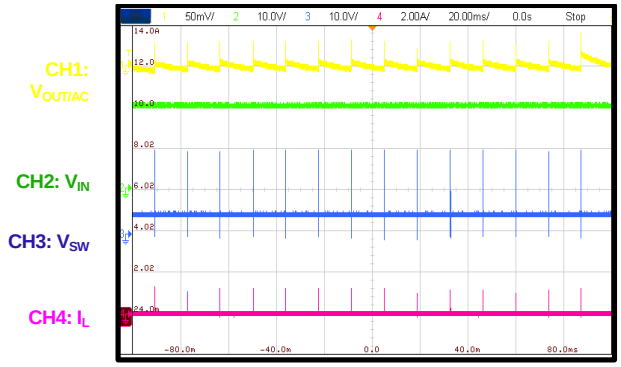
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TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 20V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 450kHz, Auto PFM/PWM mode, T_A = 25°C, unless otherwise noted.

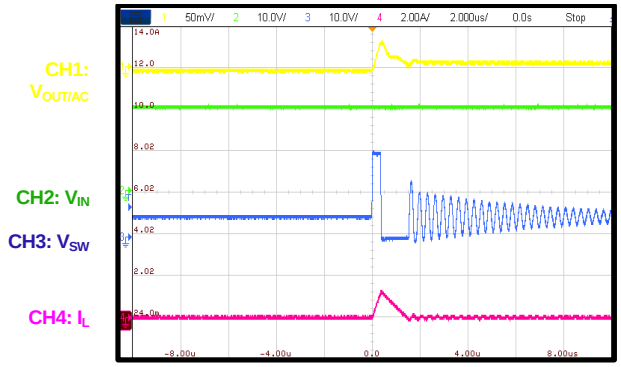
Steady State

V_{OUT} = 5V, f_{SW} = 450kHZ , I_{OUT} = 0A



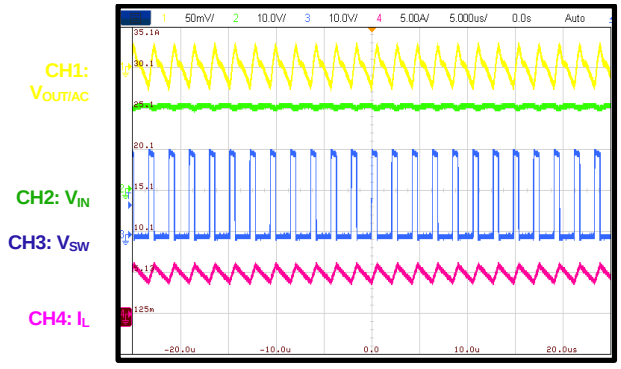
Steady State

V_{OUT} = 5V, f_{SW} = 450kHZ , I_{OUT} = 0A
zoom in



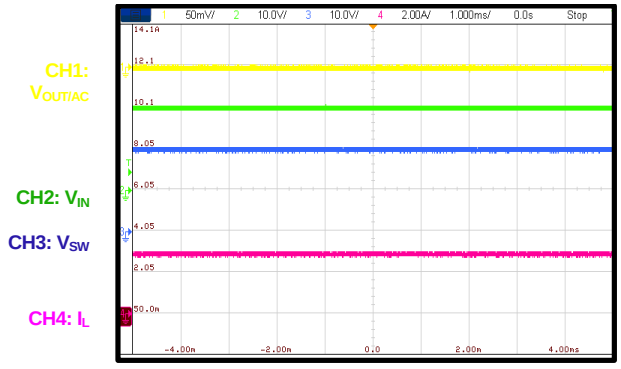
Steady State

V_{OUT} = 5V, f_{SW} = 450kHZ , I_{OUT} = 5A



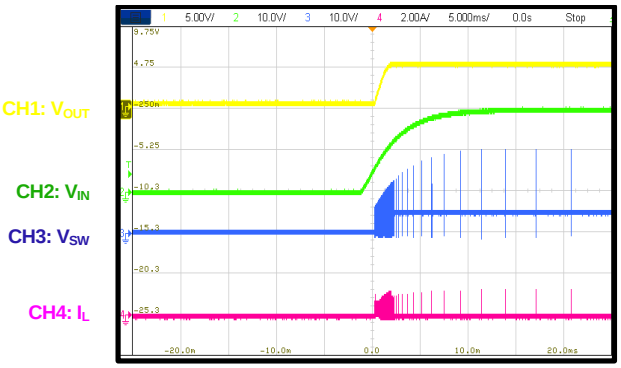
Steady State

V_{OUT} = 20V, f_{SW} = 450kHZ , I_{OUT} = 5A,
100%duty



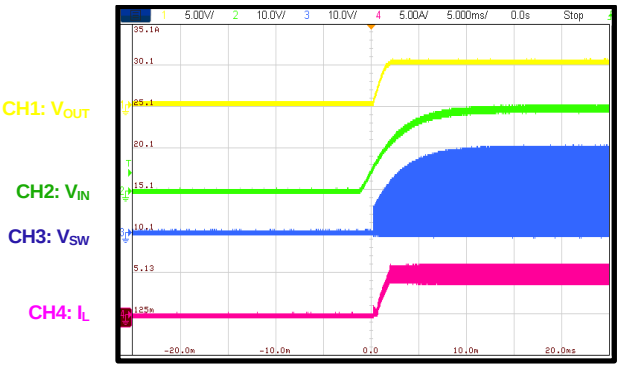
Power Start-up

V_{OUT} = 5V, I_{OUT} = 0A



Power Start-up

V_{OUT} = 5V, I_{OUT} = 5A



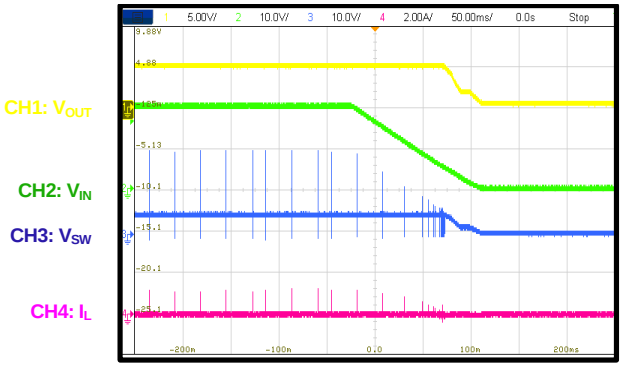
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 20V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 450kHz, Auto PFM/PWM mode, T_A = 25°C, unless otherwise noted.

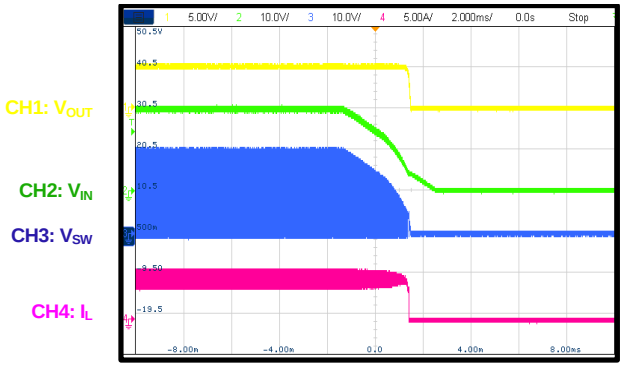
Power Shutdown

V_{OUT} = 5V, I_{OUT} = 0A



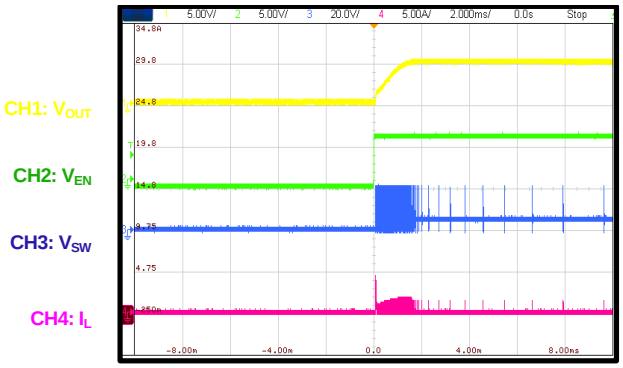
Power Shutdown

V_{OUT} = 5V, I_{OUT} = 5A



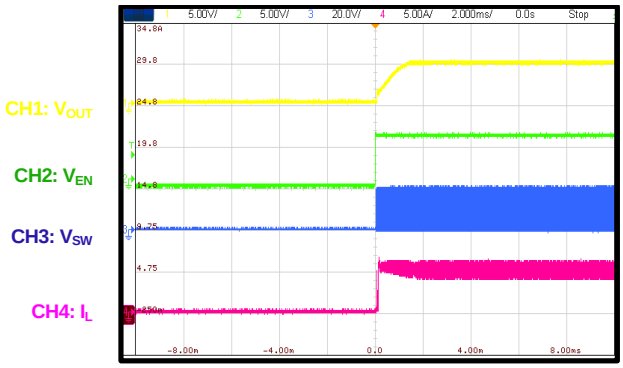
EN Start-up

V_{OUT} = 5V, I_{OUT} = 0A



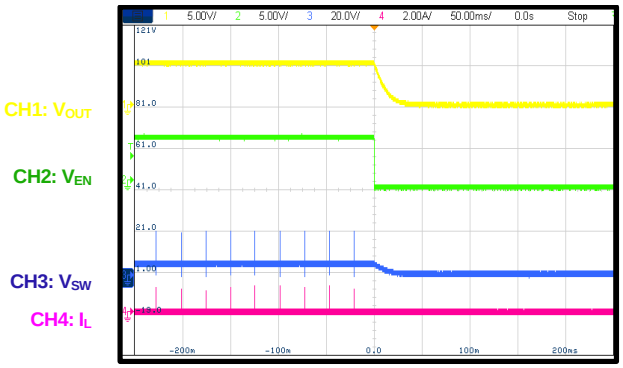
EN Start-up

V_{OUT} = 5V, I_{OUT} = 5A



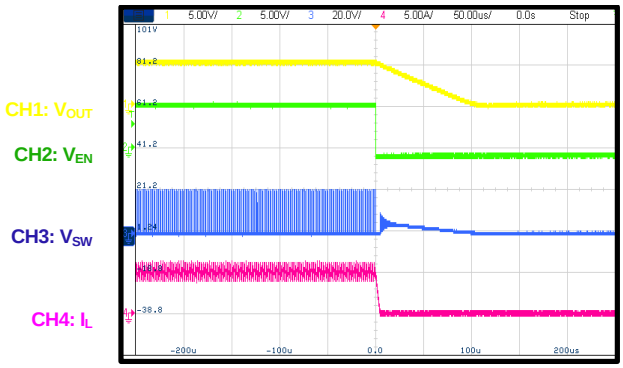
EN Shutdown

V_{OUT} = 5V, I_{OUT} = 0A



EN Shutdown

V_{OUT} = 5V, I_{OUT} = 5A



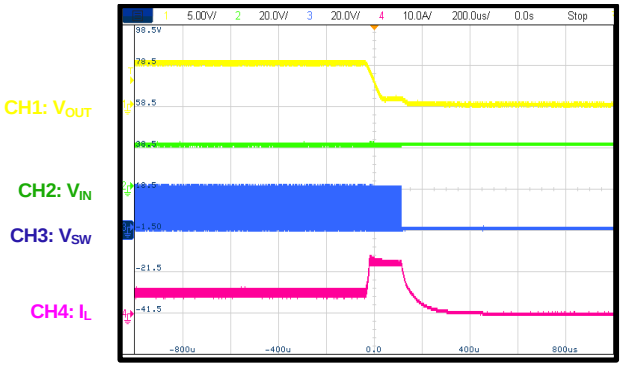
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 20V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 450kHz, Auto PFM/PWM mode, T_A = 25°C, unless otherwise noted.

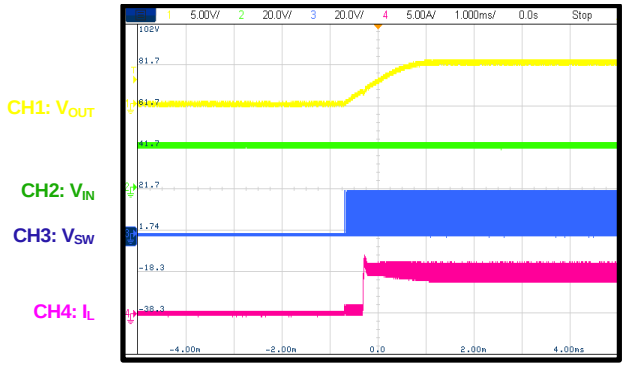
SCP Entry

V_{OUT} = 5V, I_{OUT} = 5A



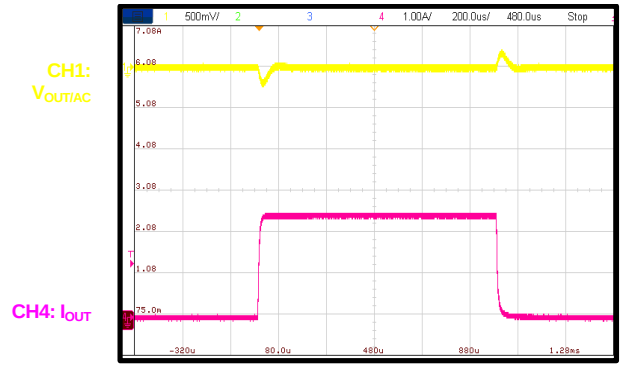
SCP Recovery

V_{OUT} = 5V, I_{OUT} = 5A



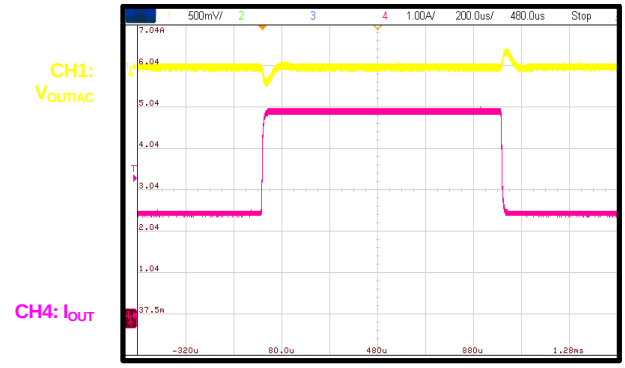
Load Transient Response

V_{OUT} = 5V, I_{OUT} = 0A to 2.5A,
slew rate = 300mA/µs, forced PWM mode



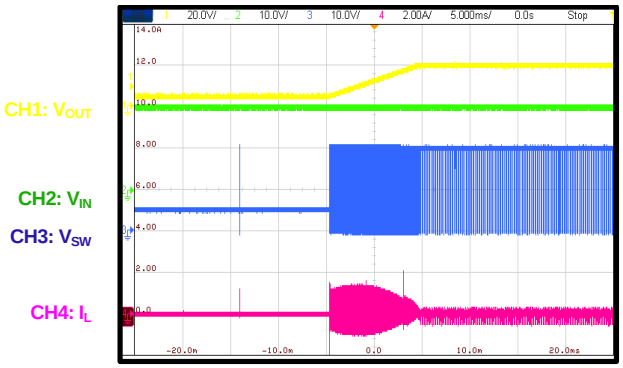
Load Transient Response

V_{OUT} = 5V, I_{OUT} = 2.5A to 5A,
slew rate = 300mA/µs, forced PWM mode



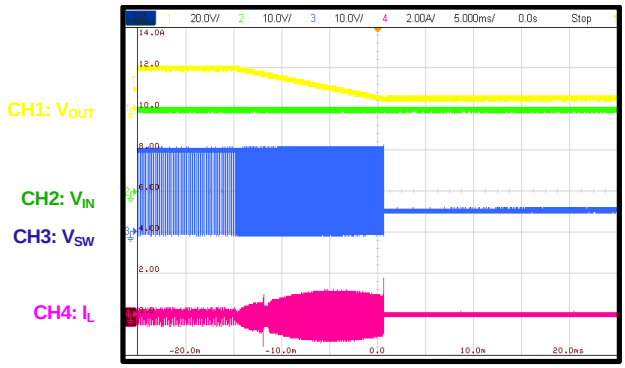
Output Voltage Transition

V_{OUT} = 5V to 20V, I_{OUT} = 0A



Output Voltage Transition

V_{OUT} = 20V to 5V, I_{OUT} = 0A



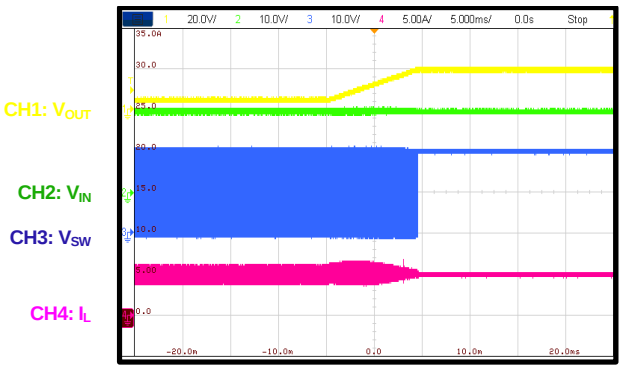
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TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 20V, V_{OUT} = 5V, L = 4.7µH, f_{SW} = 450kHz, Auto PFM/PWM mode, T_A = 25°C, unless otherwise noted.

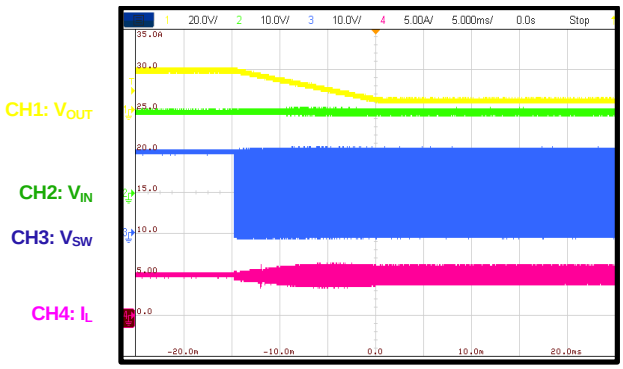
Output Voltage Transition

V_{OUT} = 5V to 20V, I_{OUT} = 5A



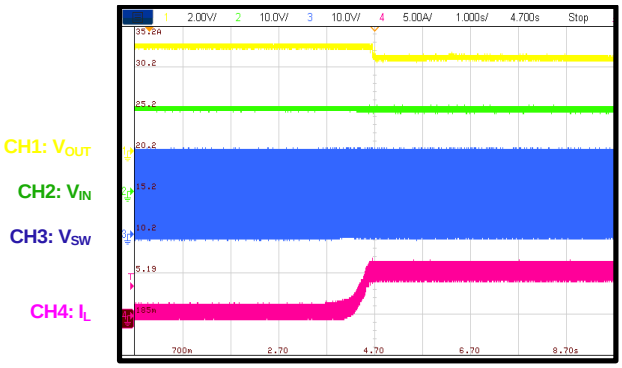
Output Voltage Transition

V_{OUT} = 20V to 5V, I_{OUT} = 5A



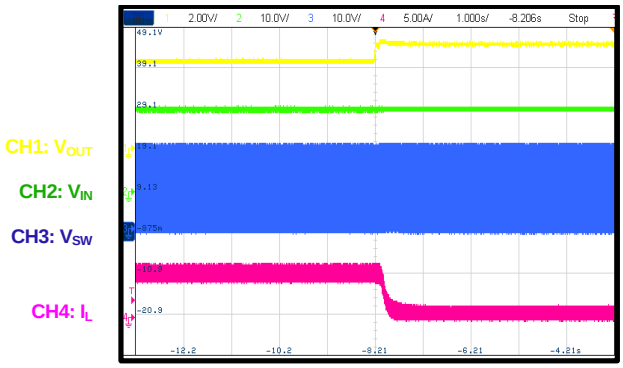
CC Entry

CC limit = 5.4A



CC Exit

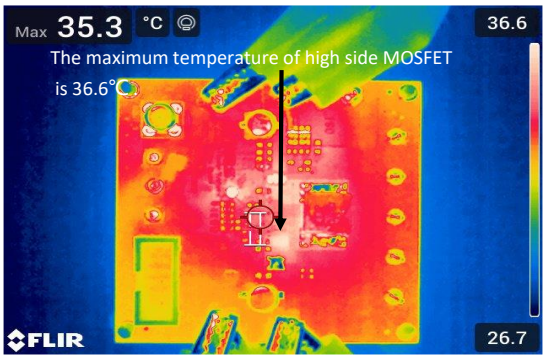
CC limit = 5.4A



Case Temperature

V_{IN} = 20V, V_{OUT} = 20V, I_{OUT} = 5A, f_{SW} = 450KHz, L = 4.7µH, RDC = 9.5mΩ, 6.35cm*6.35cm PC board. Top/Bottom Layer: 2Oz, Middle Layer 1 and 2: 1Oz.

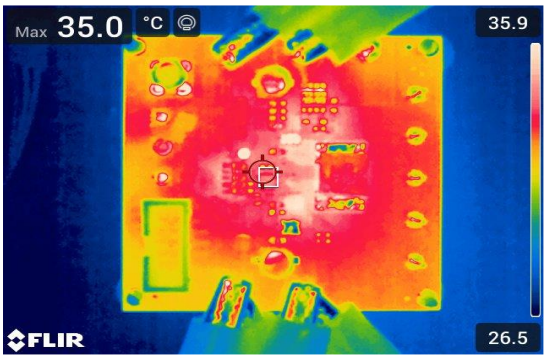
T_A = 26.7°C



Case Temperature

V_{IN} = 28V, V_{OUT} = 28V, I_{OUT} = 5A, f_{SW} = 450KHz, L = 4.7µH, RDC = 9.5mΩ, 6.35cm*6.35cm PC board. Top/Bottom Layer: 2Oz, Middle Layer 1 and 2: 1Oz.

T_A = 25°C



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FUNCTIONAL BLOCK DIAGRAM

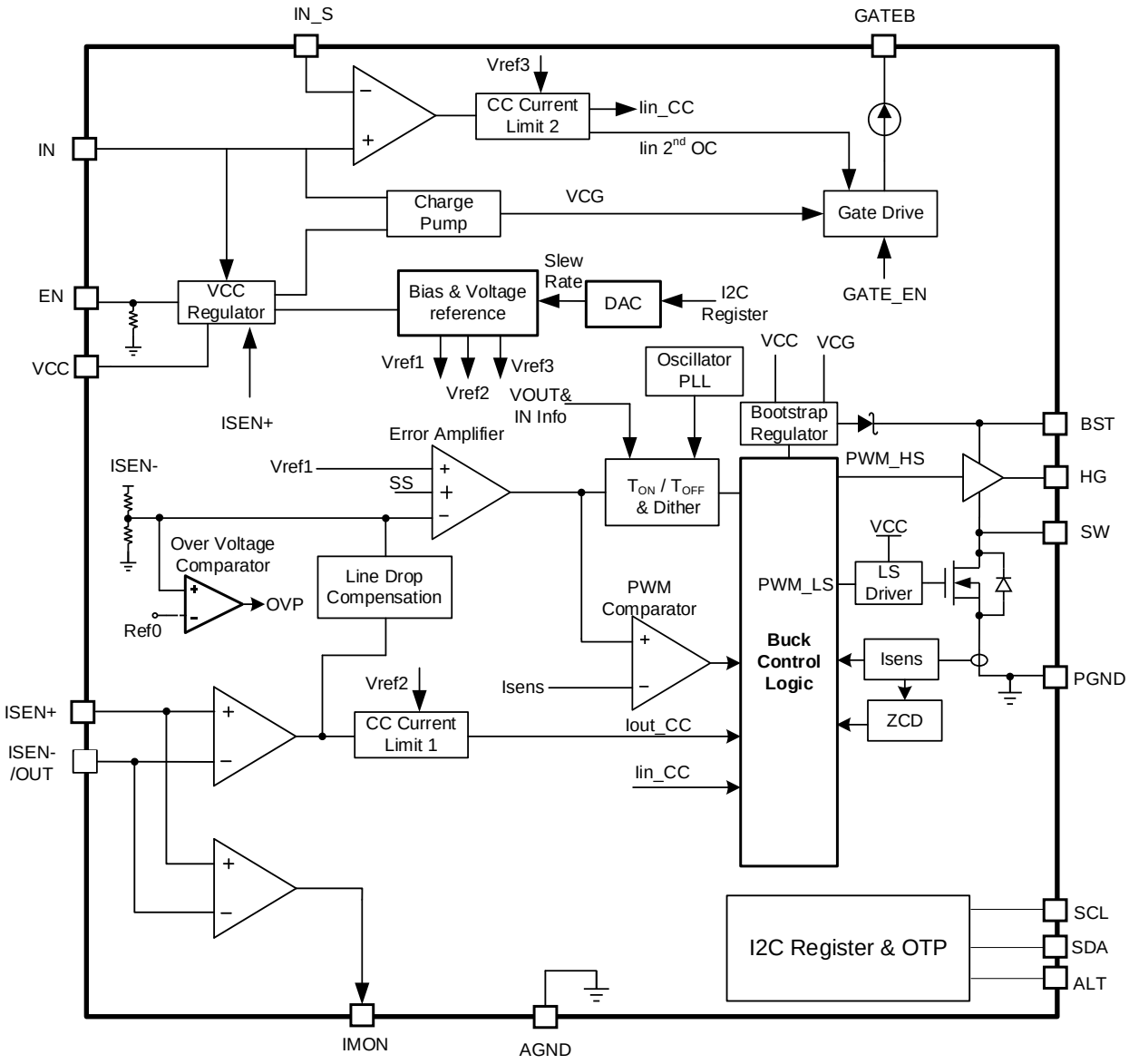


Figure 1: Functional Block Diagram

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OPERATION

The MP8856 is a step-down converter with integrated low-side power switch. It offers a compact solution from a wide input-supply range with excellent load and line regulation.

The step-down converter of the MP8856 operates in a fixed-frequency, valley-current–mode control to regulate the output voltage.

Error Amplifier (EA)

The error amplifier (EA) compares the internal feedback voltage against the internal reference (REF) and outputs a COMP voltage. This COMP voltage controls the power MOSFET current. The optimized, internal compensation network minimizes the external component count and simplifies the control loop design.

Power Supply

MP8856 internal circuit is powered by VCC, including high-side switch gate driver. VCC regulator takes either the VOUT or VIN as supply. When V_{IN} power is supplied and EN is high, MP8856 tries to regulate VCC at 5.25V. When output voltage is established and higher than 6.8V, VCC regulator uses VOUT power to save LDO power loss. When MP8856 enters output CC mode, VCC regulator uses VIN as supply regardless of output voltage.

100% Duty Cycle Operation

MP8856 integrates a charge pump, which enables it work in 100% duty cycle mode to minimize the Vin-to-Vout voltage drop meanwhile maximize converter efficiency. When the Vin is close to Vout voltage, the switching frequency gradually decrease until Vout is 140mV lower than Vout target. When Vout is 140mV lower than Vout target, MP8856 will enter 100% duty mode. Vout target-Vout =140mV is the critical point for entering and exiting 100% duty mode (For feedback resistor ratio = 16 parts, the value is 224mV). In the 100% duty cycle mode, the high-side switch is always on and low-side switch is always off. Internal charge pump provides HG driver voltage to maintain the Vgs of high-side NMOS FET.

MP8856 exits 100% duty mode quickly once Vout drops due to short circuitry happens. MP8856 exits 100% duty mode when Vout target-Vout is lower than 140mV. After exiting 100% duty mode, the low-side valley current limit will take effect immediately to limit the output power.

Enable Control (EN)

The MP8856 has an enable control pin (EN). Pull EN high to enable the IC. Pull EN low or float EN to disable the IC.
The MP8856 EN is a high voltage pin, it can be connected to VIN directly or through a resistor.

It also can program EN divider resistor to set VIN on/off threshold.

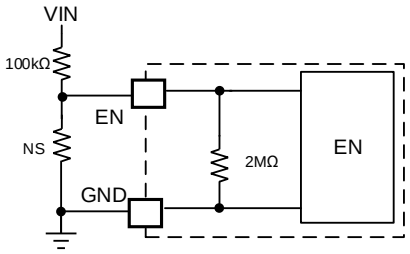


Figure 2: EN connection

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. The UVLO comparator monitors the input and VCC voltage. MP8856 is enabled when VCC voltage is higher than its rising UVLO threshold; MP8856 stops working when either VIN or VCC below its UVLO falling threshold.

Internal Soft-Start (SS)

The soft-start (SS) prevents the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a SS voltage that ramps up from 0V to 5V. When SS is lower than REF, the error amplifier uses SS as the reference. When SS is higher than REF, the error amplifier uses REF as the reference.

If the output of the MP8856 is pre-biased to a certain voltage during start-up, the IC disables the switching of both the high-side and low-side switches until the voltage on the internal SS capacitor exceeds the internal feedback voltage.

Input and Output CC Mode Over-Current-Protection

The MP8856 provides both input current and output current limit function. It senses the current

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by IN/IN_S and ISEN+/- pins, if I_{OUT} current or Iin current exceeds the set current-limit threshold,

MP8856 will enter constant current limit mode (CC mode). In this mode the current amplitude is limited and output voltage will decrease.

I_{OUT} over current protection has programmable OC blank timer, 300us/2.5ms/9.5ms/19ms. The ALT pin will pull-low to report OC event after this blank timer finishes. It allows a transient load current work in a short period without trigger OCP protection. The input CC limit function can be disabled by IIC.

As the reducing of load resistance, output voltage drops until feedback voltage falls below the under voltage (UV) threshold. Once UV triggers and Vout voltage is lower than 3V, the MP8856 enters hiccup mode to periodically restart the part. This protection mode is especially useful when the output is dead-shorted to ground. This greatly reduces the average short circuit current, alleviates thermal issues, and protects the regulator. The MP8856 exits hiccup mode once the over current condition is removed.

Hiccup entry condition: hit CC or OC threshold (LS valley), Vout<3V and SS ready and FB UV (<65%).

Output Over-Voltage Protection (OVP)

The MP8856 has output over-voltage protection (OVP). If the output is higher than 118% of Vref, the power switches turn-off. There is a discharge path from ISEN+ pin to ground which will turn-on. When the feedback voltage drops to 110% of Vref, the chip returns to normal operation. If the OVP happens and not in i2c VID period, the GATEB will be disabled.

Start-Up and Shutdown

If both VIN and EN exceed their respective thresholds, the chip is enabled. The reference block starts first, generating a stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides a stable supply for the remaining circuitries.

Several events can shut down the chip: EN low, VIN low, and thermal shutdown. In shutdown, the signaling path is blocked to avoid any fault triggering. Then the COMP voltage and the internal supply rail are pulled down. The floating driver is not subject to this shutdown command.

Floating Driver and Bootstrap Charging

An external bootstrap capacitor powers the floating power MOSFET driver. This floating driver has its own UVLO protection. The UVLO's rising threshold is 2.7V with a hysteresis of 200mV. The bootstrap capacitor voltage is regulated internally by VCC through D1, D2, M1, and C4 (see Figure 3). The charge pump, whose output voltage up to VIN+VCC, can also charge the BST capacitor with 10µA output capacity.

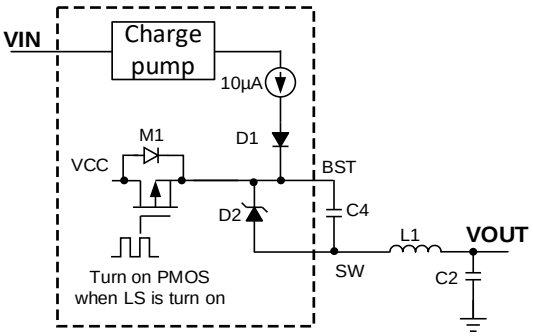


Figure 3: Floating power MOSFET driver

EN Shutdown Discharge

When the EN pin is pull low or "OFF" bit is set, MP8856 will enter output discharge mode. The discharge path is on for 230ms timer. The discharge resistor is from ISEN- to PGND. The GATEB is still on until output discharge is finished.

GATEB Driver

The GATEB driver outputs 20µA source current up to VIN+VCC voltage. Once the MP8856 is enabled (Vin and EN are active), GATEB output is enabled.

In output OCP/SCP fault conditions, the GATEB is still turn-on.

During IC in thermal shutdown the GATEB is turn-off.
During EN off, the GATEB is still on until output discharge finishes.

Output Line Drop Compensation

The MP8856 is capable of compensating an output voltage drop, such as high impedance caused by a long trace, to keep a fairly constant load-side voltage. The output current information

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is sampled from ISEN+/- pins. Refer to register table for detail line drop compensation amplitude.

Current Monitor Output

The MP8856 senses the average load current through one sensing resistor, and the device outputs a voltage signal on the IMON pin. This signal is amplified by the voltage difference between ISEN+ and ISEN-, IMON Gain is 56. For example, the IMON pin is 280mV (output sense resistor is 5mΩ), it indicates that output current is $\frac{280mV}{56\times5\text{m}\Omega}$ = 1A. Load current of IMON pin should be ⩽3μA for accuracy. The IMON pin maximum output voltage can be estimated with Equation (1) .

$$V_{IMON_MAX}(mV) = I_{OUT_OC}(A) \times 280 + 100 \quad (1)$$

Where:
Iout_OC (A) is determined by the register 0xD1 D[6:0].

It is recommended to place a 100pF capacitor from IMON to AGND.

System Thermal Shutdown (TSD)

Thermal shutdown prevents the chip from operating at exceedingly high temperatures. When the silicon die temperature exceeds 165°C, it shuts down the entire chip. When the temperature falls below its lower threshold, 140°C typically, the chip is enabled.

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PMBUS INTERFACE

PMBus Serial Interface Description

The power management bus (PMBus) is an open-standard power management protocol that defines a means of communication with power conversion and other devices.

The PMBus is a two-wire, bidirectional serial interface, consisting of a data line (SDA) and a clock line (SCL). The lines are pulled to a bus voltage externally when they are idle. When connecting to the lines, a master device generates an SCL signal and device address, and arranges the communication sequence. This is based on I^2C operation principles.

Start and Stop Conditions

The start and stop conditions are signaled by the master device, which signifies the beginning and end of the PMBus transfer. The start condition is defined as the SDA signal transitioning from high to low while the SCL is high. The stop condition is defined as the SDA signal transitioning from low to high while the SCL is high (see Figure 4).

The master then generates the SCL clocks and transmits the device address and the read/write direction bit (R/W) on the SDA line. Data is transferred in 8-bit bytes by the SDA line. Each byte of data is followed by an acknowledge bit (ACK).

PMBus Update Sequence

The MP8856 requires a start condition, a valid PMBus address, a register address byte, and a data byte for a single data update. The device acknowledges receipt of each byte by pulling the SDA line low during the high period of a single clock pulse. A valid PMBus address selects the MP8856. The device performs an update on the falling edge of the LSB byte.

PMBus Bus Message Format

In the tables in Figure 5, unshaded cells indicate that the bus host is driving the bus actively, and shaded cells indicate that the MP8856 is driving the bus.

S = Start condition

Sr = Repeated start condition

P = Stop condition

R = Read bit

$\overline{W}$ = Write bit c

A = Acknowledge bit (0)

$\overline{A}$ = Acknowledge bit (1)

“A” represents the acknowledge bit. The ACK bit is typically active low (logic 0) if the transmitted byte is received successfully by a device.

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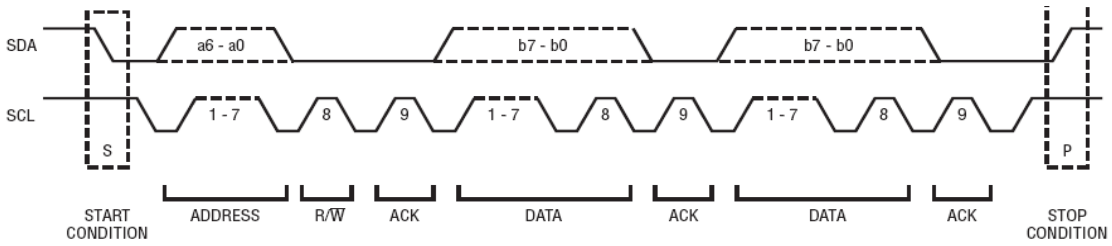


Figure 4: Data Transfer Over the PMBus

a) Send Byte

1	7	1	1	8	1	1
S	Slave Address	Wr	A	Data Byte	A	P

b) Write Byte

1	7	1	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	Data Byte	A	P

c) Write Word

1	7	1	1	8	1	8	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	Data Byte Low	A	Data Byte High	A	P

d) Read Byte

1	7	1	1	8	1	1	7	1	1	8	1	1
S	Slave Address	Wr	A	Command Code	A	S	Slave Address	Rd	A	Data Byte	NA	P

e) Read Word

1	7	1	1	8	1	1	7	1	1	8	1
S	Slave Address	Wr	A	Command Code	A	S	Slave Address	Rd	A	Data Byte Low	A

8	1	1
Data Byte High	NA	P

Figure 5: PMBus Message Format

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REGISTER DESCRIPTION

I2C/PMBUS Register

The I2C is active once VIN and EN both are higher than UVLO threshold. The default value is based on MP8856-0000.

Command Name	Command code	Description	Type	Data Format	Unit	OTP	Default Value
OPEARTION	0x01	ON/OFF	R/W Byte	Reg		Y	ON
CLEAR_FAULTS	0x03		Send/Write Byte	Reg		N	
VOUT_COMMAND	0x21		R/W Word	Linear L16*	V	Y	5.1V
STATUS_WORD	0x79		R Word	Reg		N	
STATUS_TEMPERATURE	0x7D		R Byte	Reg		N	
MFR_CTRL1	0xD0		R/W Byte	Reg		Y	0x0C
MFR_IOUT_LIMIT	0xD1	Set CC current limit continuously	R/W Byte	Reg		Y	6.35A
MFR_CTRL2	0xD2	Set line drop compensation	R/W Byte	Reg		Y	0x01
MFR_CTRL3	0xD3		R/W Byte	Reg		Y	0xAC
MFR_CTRL4	0xD4		R/W Byte	Reg		Y	0x07
MFR_IIN_LIMIT	0xD5	Set CC current limit continuously	R/W Byte	Reg		Y	0xFF
MFR_STATUS_MASK	0xD8	Mask the ALT# pin indication	R/W Byte	Reg		Y	0xBF
ID1	0xD9	OTP configuration code	R/W Byte	Reg		Y	
ID2	0xDA	OTP software revision	R/W Byte	Reg		Y	

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PMBUS COMMAND INTRODUCTION

OPERATION

The OPERATION command is used to configure the operational state of the converter. Bold font is the default.

Bits	Description	Bit Value	Meaning
7	ON/OFF State. Note the "EN" pin has higher control priority than this bit.	0	The output is off.
		1	**The output is on.**
6:0	Reserved		

CLEAR_FAULTS

The CLEAR_FAULTS command is used to clear any fault bits that have been set. This command clears all bits in all status registers simultaneously. At the same time, the device negates (clears, releases) its ALT# signal output if the device is asserting the ALT# signal.

The CLEAR_FAULTS command does not cause an unit that has latched off for a fault condition to restart.

If the fault is still present when the bit is cleared, the fault bit shall immediately be set again and the host notified by the usual means. **This command is write only.** Send byte to clear fault. Refer to Send Byte format in figure 5.

VOUT_COMMAND

The VOUT_COMMAND sets the output voltage. It follows the L16 linear data format.

Command Name	VOUT_COMMAND															
Format	Linear															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Data Byte High								Data byte Low							
Default value (5.1V)	5222 Decimal															

The Vout, in volts is calculated from the equation below:

$V_{OUT} = V \times 2^{-10}$,

Where:

V is a 16 bit unsigned binary integer of VOUT_COMMAND[15:0];

The valid Vout range is from 1V to 21.47V. The internal feedback resistor ratio Vout/Vfb=10. The VOUT_COMMAND resolution is 10mV. Internal reference voltage equals to Vout/10. Internal reference voltage range is from 0.1V to 2.147V with 1mV step (total 2047 steps, 11 bit DAC, when DAC input is 11 bit “0”, DAC output is 0.1V). Table 1 shows the V_{OUT} options when FB_RATIO is 10.

Table 1: VOUT_COMMAND Setting Table (FB_RATIO = 10)

V_{OUT}	V_{REF}	VOUT_COMMAND
5V	0.5V	1400h
9V	0.9V	2400h
15V	1.5V	3C00h
20V	2V	5000h

MP8856 can support output voltage from 1.6V to 28V after trimming the internal feedback resistor ratio Vout/Vfb to 16 by factory, the VOUT_COMMAND resolution is 16mV, internal reference voltage

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range is from 0.1V to 2.147V with 1mV step (total 2047 steps, 11 bit DAC, when DAC input is 11 bit “0”, DAC output is 0.1V).

The Vout(FB resistor ration = 16), in volts is calculated from the equation below:

$$V_{OUT} = V \times 2^{-10} \times 1.6.$$

Table 2 shows the V_{OUT} options when FB_RATIO is 16.

Table 2: VOUT_COMMAND Setting Table (FB_RATIO = 16)

V_{OUT}	V_{REF}	VOUT_COMMAND
5V	0.3125V	0C80h
9V	0.5625V	1680h
15V	0.9375V	2580h
20V	1.25V	3200h
28V	1.75V	4600h

STATUS_WORD

The STATUS_WORD command returns two bytes of information with a summary of the unit’s fault condition. Based on the information in these bytes, the host can get more information by reading the appropriate status registers.

Byte	Bits	Status Bit Name	Description
Low	7	Reserved	0
	6	IIN_OC_FAULT	An input over current fault has occurred. Either enter CC current limit, peak current limit, this bit will be set.
	5	VOUT_OV_FAULT	An output overvoltage fault has occurred.
	4	IOUT_OC_FAULT	An output over current fault has occurred. Either enter CC current limit, peak current limit or enter hiccup mode, this bit will be set.
	3	Reserved	0
	2	TEMPERATURE	A temperature fault or warning has occurred.
	1	Reserved	0
	0	Reserved	0
High	7	VOUT	An output voltage fault or warning has occurred.
	6	IOUT/POUT	An output current fault has occurred. Either enter CC current limit or enter hiccup mode, this bit will be set.
	5	Reserved	0
	4	OC_EXIT	Output current exits the CC current limit. This bit is only set high when Iout changes from CC (before enter hiccup) to non-CC. Recovery from hiccup will NOT set this bit.
	3	PG_STATUS#	The POWER_GOOD signal, if present, is negated. When this bit is set ‘1”, the output voltage is not good. when this bit is clear, the output voltage is power good. PG: 91% rising, 81% falling;
	2	Reserved	0
	1	Reserved	0
	0	Reserved	0

The exception to the rule that status bit remain set is the PG_STATUS# bits. This bit always reflects the current state of the POWER_GOOD signal (if present).

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STATUS_TEMPERATURE

The STATUS_TEMPERATURE command returns one data byte with contents as follows:

Bit	Description
7	OT_FAULT (Overtemperature Fault). OTP entry threshold 165degC
6	OT_WARNING (Overtemperature Warning). Enter threshold is 135C, 20degC hysteresis
5	Reserved
4	Reserved
3	OT_WARNNING Exit. The OT_warning falling edge set this bit high;
2	Reserved
1	Reserved
0	

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I2C Register Map

Name	REG(0x)	R/W	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
MFR_CTRL1	D0	R/W	Dither Enable	FREQ	Disable_GATEB	Disable_Charge_Pump	Output OVP EN	Output Discharge EN	PFM/PWM Mode	
MFR_IOUT_LIMIT	D1	R/W	Disable_LDC	Constant Current Limit(1A-6.35A/50mA STEP)						
MFR_CTRL2	D2	R/W	Reserved					Line Drop Compensation		
MFR_CTRL3	D3	R/W	CC_BLANK_TIMER		Disable_OTW	SLEW RATE Rise		SLEW RATE Fall		Reserved
MFR_CTRL4	D4	R/W	Reserved	Disable_IIN_Peak_LIM	Reserved	I2C Address(A4-A0)				
MFR_IIN_LIMIT	D5	R/W	Disable_IIN_CC	Constant Current Limit(1A-6.35A/50mA STEP)						
MFR_STATUS_MASK	D8	R/W	Mask the ALT# pin indication when fault or event happens							
ID1	D9	R/W	OTP CONFIGURE CODE							
ID2	DA	R/W	OTP SOFTWARE REVISION							

1) I2C Slave "ADDRESS":

The I2C slave address: **67H** Default. I2C Slave Address is determined by 7-bit binary data, A6 and A5 are fixed 1, A4-A0 is controlled by MFR_CTRL4_D[4:0].

I2C Address A4:A0	
Binary	Hex
00 111 (Default)	67H
I2C/OTP adjustable for A4-A0. Set by MFR_CTRL4_D[4:0]	

2) Register "MFR_CTRL1":

Address: 0xD0
Reset value: Set by OTP.
Type: Read and Write

Bits	Bit Name	Description
7	Dither Enable	**"0" no dither;** "1" enable frequency spread spectrum function.
6	FREQ	Set Buck switching frequency at CCM. Default is "0". "**0": 450kHz** "1": 950kHz
5	Disable_GATEB	GATEB output enable control: **“0”: The GATEB function is enabled;** “1”: Disable the GATEB output. Default is “0”
4	Disable_Charge_Pump	Internal charge pump enable control: **“0”: The charge pump function is enabled;** “1”: Disable the charge pump. If this bit is set, the GATEB will be no function. Default is “0”
3	Output OVP EN	Output OVP enable or disable control bit. **"1": enable;** "0": no output OVP function. Default value is "1".
2	Output Discharge EN	Output discharge function enable bit. **"1" enable the output discharge function during EN or i2c OFF;** "0" disable the output discharge function during IC off. Default value is "1". It’s an ISEN+ to ground passive discharge resistor turn-on. During IC EN/i2c turn-off, this discharge works until Vfb<25mV or maximum 230ms timer ends.

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1:0	PFM/PWM Mode	Set Buck work mode: Auto PFM/PWM mode, Forced PWM mode. **"00": auto PFM/PWM mode;** "01" Forced PWM mode; “10” Reserved “11” Reserved Default value: "00".

3) Register "MFR_IOUT_LIMIT":
Address: 0xD1
Reset value: Set by MTP.
Type: Read and Write
Set the output constant current (CC) limit threshold.

Bit Name	Line Drop Disable	IOUT_LIM						
Format	Direct, unsigned binary integer							
Bits	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Default value (6.35A)	0	108 Integer						

When change the IOUT_LIM, internal IREF have some slew rate control. Ramp slew is 50us/50mA.
The real world Iout_OC, in Ampere is calculated from the equation below:
Iout_OC (A)= IOUT_LIM*0.05,
Where:
IOUT_LIM is a 7 bit unsigned binary integer of IOUT_LIM D[6:0];

The Iout_OC resolution or minimum step is 50mA. Maximum value **is** 6.35A.

D[7] is the line drop compensation enabled control bit:

D[7]=0 means the line drop compensation is controlled by 0xD2 register; D[7]=1 means the line drop compensation is disabled. Default value is “0”.

4) Register "MFR_CTRL2":
Address: 0xD2
Reset value: Set by OTP.
Type: Read and Write

Bits	Bit Name	Description
2:0	Line Drop Compensation	Set output voltage compensation vs load feature: 000: no compensation **001: Vout compensates 100mV@3A Iout** 010: Vout compensates 300mV@3A Iout 011: Vout compensates 600mV@3A Iout 100: Vout compensates 900mV@3A Iout Above compensation amplitude is fixed for any output voltage. Line drop comp is only enabled for 5V and above Vout. Line drop compensation will clamp for >3A load current, for example, “001” configuration, the compensation voltage is clamped to 100mA for >3A Iout. Above compensation amplitude is for parts with feedback resistor ratio=10. For parts with feedback resistor ratio=16, the compensation amplitude(feedback resistor ratio is 16) = compensation amplitude(feedback resistor ratio is 10) * 1.6 Default: “001”.

5) Registers "MFR_CTRL3":
Address: 0xD3
Reset value: Set by OTP.
Type: Read and Write

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Bits	Bit Name	Description
7:6	CC_BLANK_TIMER	Set the Iout CC blank timer. “00”: 300us; “01”: 2.5ms; **“10”: 9.5ms;** “11”: 19ms.
5	Disable OTW	Disable OTW enter and exit function 0: not disable; **1: disable.**
4:3	SLEW RATE Rise	Set the Vout adjust rising slew rate. '00": 0.08mv/us **Vref** rising slew rate; **'01": 0.16mv/us Vref rising slew rate;;** '10": 0.4mv/us Vref rising slew rate; '11": 0.8mv/us Vref rising slew rate; Default is "01". Vout_Slew rate=Vref_slew rate * Feedback Ratio. Feedback Ratio=10.
2:1	SLEW RATE Fall	Set the Vout adjust falling slew rate: '00": "0.02mv/us" Vref falling slew rate; '01": "0.04mv/us" Vref falling slew rate; **'10": "0.1mv/us" Vref falling slew rate;** '11": "0.2mv/us" Vref falling slew rate; Default is "10". Vout_Slew rate=Vref_slew rate * Feedback Ratio. Feedback Ratio=10.

6) Register "MFR_CTRL4":
Address: 0xD4
Reset value: Set by OTP.
Type: Read and Write

Bits	Bit Name	Description
Disable_IIN_Peak_LIM	D[6]	Input peak current limit disable bit. Input peak current limit: the function needs input current sense resistor, once the input current is greater than or equal to IIN peak current limit value(20A), the chip will turn off for 500ms, after 500ms, restart with soft-start. **0: Enable input peak current limit.** 1: Disable input peak current limit Default “0”.
4:0	I2C Address	Set I2C slave address A4-A0 bit. I2C address is Default is "00111".

7) Register "MFR_IIN_LIMIT":
Address: 0xD5
Reset value: Set by MTP.
Type: Read and Write
Set the IIN constant current (CC) limit threshold.

Bit Name	Disable_ IIN_CC	IIN_LIM					
Format	Direct, unsigned binary integer						
Bits	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Default value (6.35A)	1	127 Integer					

The real world IIN_OC, in Ampere is calculated from the equation below:
IIN_OC (A)= IIN_LIM*0.05,
Where:
IIN_LIM is a 7 bit unsigned binary integer of IIN_LIM D[6:0];

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The Iin_OC resolution or minimum step is 50mA. Maximum value is 6.35A.

D[7] is the Iin CC current limit function disable control bit:

“0”: Iin CC function is enabled;

“1”: Iin CC function is disabled. Default is “1”.

8) Registers "MFR_STATUS_MASK":
Address: 0xD8
Reset value: Set by OTP.
Type: Read and Write
This register only can mask off the ALT# pin behavior, but the STATUS register still indicate each event.

Bits	Bit Name	Description
7	VOUT MSK	0: Not mask **1: Mask Enabled**
6	IOUT/POUT MSK	**0: Not mask.** This bit mask IOUT_OC_FAULT, IOUT/POUT and OC_EXIT. 1: Mask Enabled
5	IIN_OC MSK	0: Not mask **1: Mask Enabled**
4	TEMP MSK	Temperature related mask bit. 0: Not mask **1: Mask Enabled**
3	PG_STATUS# MSK	Higher level PG mask off control bit. 0: Not mask **1: Mask Enabled**
2	PG_ALT_EDGE MSK	0: Not mask. ALT pin will indicate both PG_STATUS# rising and falling edges; **1: Mask Enabled.** ALT pin only indicate PG_STATUS# Falling edge, which means the output voltage from not good to good transition.
1	Reserved	Reserved
0	UNKNOWN MSK(dummy)	0: Not mask. **1: Mask Enabled**

9) Registers "MFR_OTP_CONFIGURATION_CODE":
Address: 0xD9
Reset value: Set by OTP.
Type: Read and Write

Bits	Bit Name	Description
7:0	OTP_CONFIGURATION_CODE	OTP configuration code, defined by MPS.

10) Registers "MFR_OTP_REVISION_NUMBER":
Address: 0xDA
Reset value: Set by OTP.
Type: Read and Write

Bits	Bit Name	Description
7:0	OTP_REVISION_NUMBER	OTP software revision number, defined by MPS.

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APPLICATION INFORMATION

Selecting the Input Capacitor

The input current of the step-down converter is discontinuous and therefore requires a capacitor to supply the AC current to the step-down converter while maintaining the DC input voltage. For the best performance, use low ESR capacitors. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. Make sure place the input ceramic capacitor as close to the isolation NMOSFET as possible.

Since C_{IN} absorbs the input switching current, it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated with Equation (2):

$$I_{CIN} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}})} \quad (2)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (3):

$$I_{CIN} = \frac{I_{OUT}}{2} \quad (3)$$

For simplification, choose the input capacitor with RMS current rating greater than half of the maximum load current.

The input capacitance value determines the input voltage ripple. Select input capacitor that meets the input voltage ripple requirement in the system. The input voltage ripple can be estimated with Equation (4):

$$\Delta V_{IN} = \frac{I_{OUT}}{F_{SW} \times C_{IN}} \times \frac{V_{OUT}}{V_{IN}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (4)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (5):

$$\Delta V_{IN} = \frac{1}{4} \times \frac{I_{OUT}}{F_{SW} \times C_{IN}} \quad (5)$$

Selecting the Output Capacitor

The output capacitor is required to maintain the DC output voltage. Ceramic or POSCAP capacitors are recommended. The output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times (R_{ESR} + \frac{1}{8 \times F_{SW} \times C_{OUT}}) \quad (6)$$

For ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times F_{SW}^{2} \times L \times C_{OUT}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (7)$$

When using capacitors with a larger ESR (e.g. POSCAP), the ESR dominates the switching frequency impedance. The output voltage ripple can be determined by the ESR values. For simplification, the output ripple can be estimated as:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \times R_{ESR} \quad (8)$$

Larger output capacitor not only reduces output ripple, but also provides better load transient response. However, the maximum output capacitance limitation should be also considered in design application. If the output capacitor value is too large, the output voltage cannot reach the target value during soft-start time, and then it fails to regulate. The maximum output capacitor C_{O_MAX} can be limited approximately by:

$$C_{O_MAX} = (I_{LIM_AVG} - I_{OUT}) \times T_{ss} / V_{OUT} \quad (9)$$

Where, I_{LIM_AVG} is the average start-up current during soft-start period. T_{SS} is the soft-start time.

Selecting the Inductor

The inductor is necessary to supply constant current to the output load while being driven by the high frequency voltage. A larger value inductor results in less ripple current and lower output voltage ripple, but also has a larger physical size, higher series resistance and lower saturation current. A good rule for determining the inductance value is to allow the peak-to-peak ripple current in the inductor to be 30% to 50% of the maximum output load current. The inductance value can be estimated as:

$$L = \frac{V_{OUT}}{F_{SW} \times \Delta I_{L}} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (10)$$

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Where ΔI_L is the peak-to-peak inductor ripple current.

Choose an inductor that will not saturate under the maximum inductor peak current. The peak inductor current can be estimated as:

$$I_{LP} = I_{OUT} + \frac{V_{OUT}}{2 \times f_{SW} \times L} \times (1 - \frac{V_{OUT}}{V_{IN}}) \quad (11)$$

External MOSFET Selection

The MP8856 requires an external N-channel power MOSFET.

The critical parameters of selecting a MOSFET are:

1. Maximum drain to source voltage, $V_{DS(MAX)}$

   The MOSFET needs to withstand the maximum input voltage. In addition they must withstand the transient spikes at SW during switching. Therefore it is better select the MOSFET with 1.5 times of input voltage.

2. Maximum current, $I_{D(MAX)}$
3. V_{TH}: The driver voltages of MP8856 is supplied by VCC, V_{TH} of the MOSFETs should be smaller than the minimum VCC voltage of the converter, and otherwise the MOSFETs may not fully enhance during startup or overload conditions. Recommended $V_{TH} \leqslant 2.5V$.
4. On-resistance, $R_{DS(ON)}$
5. $t_{d(off)}$ and t_f: The sum of maximum turn-off delay time and maximum fall time needs to be lower than 15ns at MP8856 driver condition.

Assume that the MOSFET thermal resistance from junction to ambient is 50°C/W (this is determined by the board power dissipation), and the maximum acceptant temperature rise is 50°C, thus, the maximum power loss is 1W.

$$P_{C_Loss(SWA)} < 1W$$

Based on above calculate equation, we can select the MOSFET Ron.

The conduction and switching loss of MOSFET can be calculated by:

$$P_{C_Loss(SWA)} = \frac{V_{OUT}}{V_{IN}} \times I_o^2 \times R_{DSON(SWA)}$$

$$P_{SW_Loss(SWA)} = \frac{1}{2} V_{IN} \times I_{OUT} \times (t_{on} + t_{off}) \times f_{sw}$$

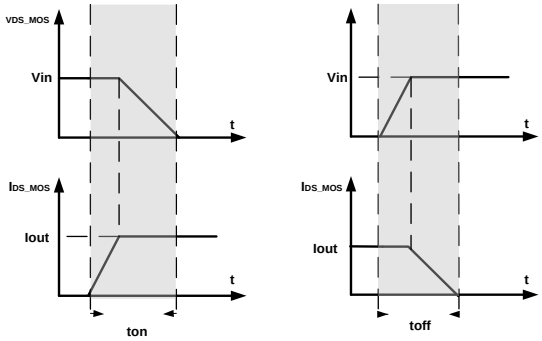


Figure 6: Switch On/Off State

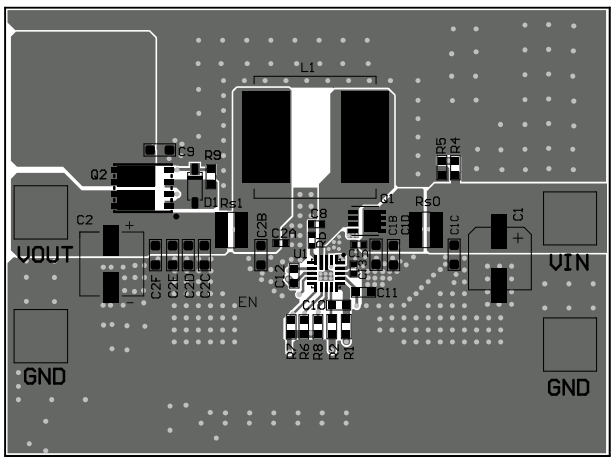
The switch on time (t_{on}) and the switch off time (t_{off}) are based on the MOSFET datasheet information.

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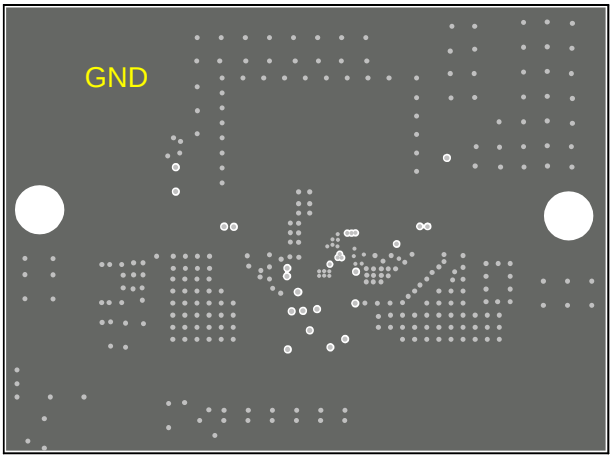
PCB Layout Guidelines

An optimized PCB layout is critical for reliable operation. For best result, refer to Figure 7 and follow the guidelines below:

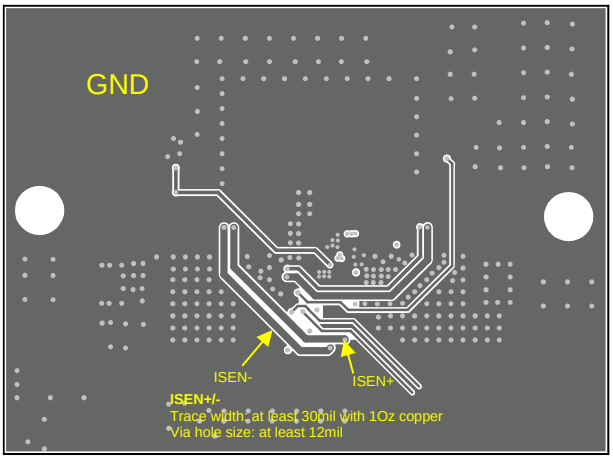
1. Place the input MLCC capacitors as close to the external high side MOSFET as possible.
2. Place at least one 0.1µF ceramic cap close to the external high side MOSFET.
3. Trace width of ISEN+/- needs to be at least 30mil with 1Oz copper. Via hole size of ISEN+/- needs to be at least 12mil.
4. Kelvin connections between Rs0/Rs1 if IC are needed for current sense.
5. Maximize the VIN and PGND copper plane to minimize parasitic impedance.
6. Ensure that the high-current paths (PGND, IN, and OUT) have short and wide traces.
7. Place as many PGND vias as possible close to the pin to minimize parasitic impedance and thermal resistance.
8. Place the VCC decoupling capacitor close to VCC and AGND pin and connect AGND and PGND at the point of the VCC capacitor's ground.
9. Place the BST capacitor as close to BST and SW as possible.
10. Avoid routing sensitive traces close to input plane and SW node.



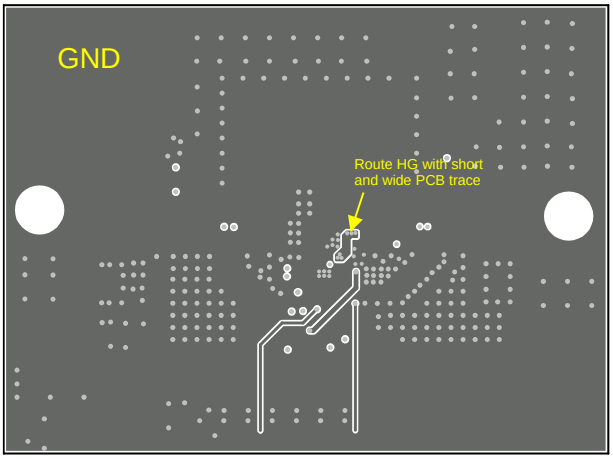
Top Layer



Middle Layer 1



Middle Layer 2



Bottom Layer

Figure 7: PC Board layout(9)

Notes:

9) The recommended layout is based on the typical application circuit (see Figure 8).

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TYPICAL APPLICATION CIRCUITS

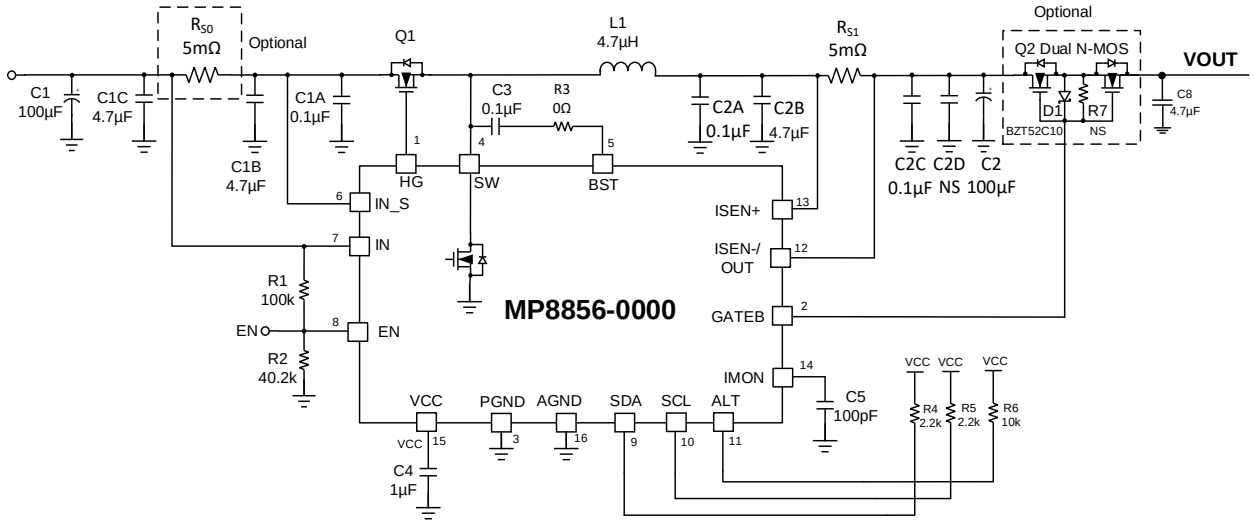
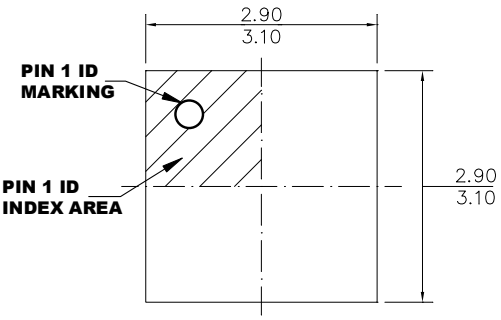


Figure 8: Typical Application Circuit (V_{IN} = 4V-36V, V_{OUT} = 3.3V-21V, 5.1V default, I_{OUT} = 5A, f_{SW}=450kHz)

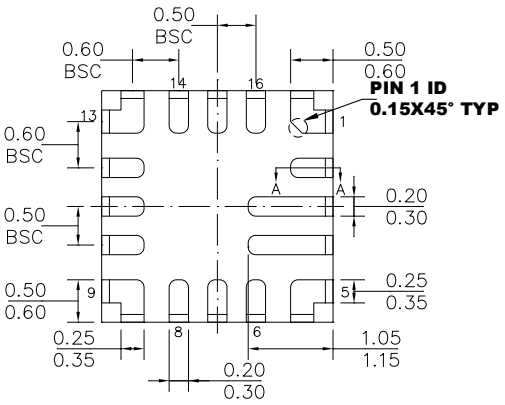
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PACKAGE INFORMATION

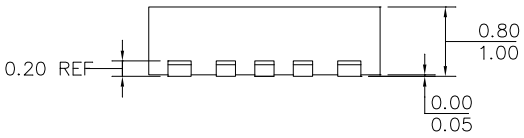
QFN-16 (3mmx3mm)
Wettable Flank



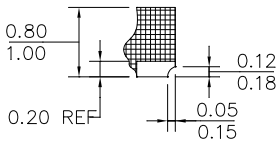
TOP VIEW



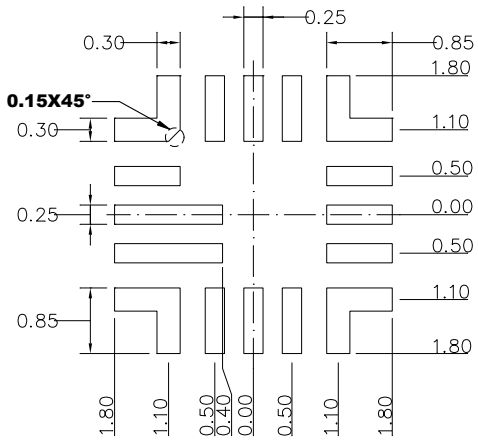
BOTTOM VIEW



SIDE VIEW



SECTION A-A



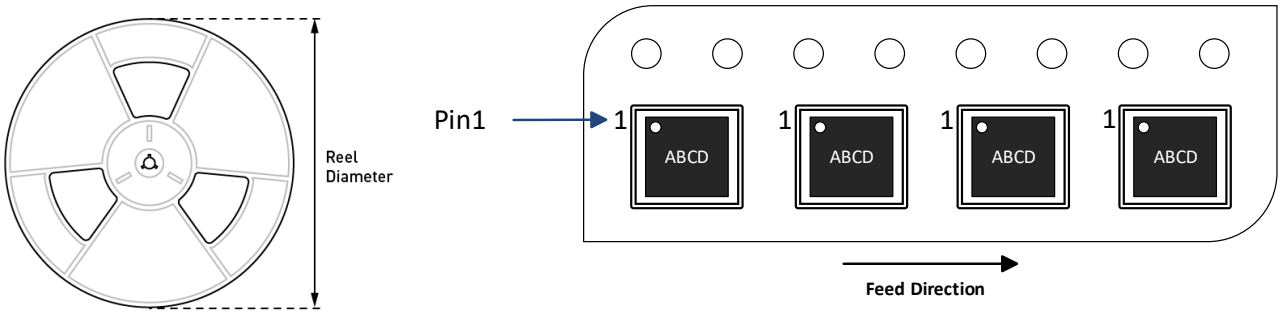
RECOMMENDED LAND PATTERN

NOTE:

1) THE LEAD SIDE IS WETTABLE.
2) ALL DIMENSIONS ARE IN MILLIMETERS.
3) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantiy/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP8856GQE-xxxx-Z	QFN-16 (3mmx3mm)	5000	N/A	N/A	13 in.	12 mm	8 mm

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