Genesys Logic, Inc.

GL850G-60

USB 2.0 Hub Controller

Datasheet

Revision 1.10
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1.00	01/05/2018	Formal release
1.10	01/11/2021	Add QFN24 package information

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CHAPTER 1 GENERAL DESCRIPTION

GL850G-60 is Genesys Logic's advanced STT hub solutions which fully comply with Universal Serial Bus Specification Revision 2.0. GL850G-60 inherits Genesys Logic's cutting edge technology on cost and power efficient serial interface design. GL850G-60 has proven compatibility, lower power consumption figure and better cost structure above all USB2.0 hub solutions worldwide.

GL850G-60 provides multiple advantages to simplify board level design that help achieving lowest BOM (Bill of Material) for system integrator. GL850G-60 integrates both 5V to 3.3V and 3.3V to 1.8V low dropout voltage regulator into single chip, therefore no external LDO required.

GL850G-60 embeds an 8-bit RISC processor to manipulate the control/status registers and respond to the requests from USB host. Firmware of GL850G-60 will control its general purpose I/O (GPIO) to access the external EEPROM and then respond to the host the customized PID and VID configured in the external EEPROM. Default settings in the internal mask ROM is responded to the host without having external EEPROM. GL850G-60 provides better design flexibility for customers. The complicated settings such as PID, VID, and number of downstream ports settings…etc. are easily achieved by programming the external EEPROM or SMBUS mode (please refer to to Chapter 5).

GL850G-60 is a full function solution which supports both Individual and Gang (4 ports as a group) mode for power management (Individual mode is only available in QFN28 package). Number of downstream ports and non/removable downstream port can be configured by different ways, such as EEPROM, SMBUS or I/O strapping. For the detailed configuration methods, please refer to the following table.

Package Type	# of DS Ports	Port # Config.	Non-removable Declaration	Power Mgmt.	EEPROM
QFN 28	4	EEPROM, SMBUS	EEPROM, SMBUS, I/O strapping	Individual/Gang	24C02
SSOP 28	4	EEPROM, SMBUS	EEPROM, SMBUS	Gang	24C02
QFN24	2	EEPROM, SMBUS	EEPROM, SMBUS	Individual/Gang	24C02

*TT (transaction translator) is the main traffic control engine in an USB 2.0 hub to handle the unbalanced traffic speed between the upstream port and the downstream ports.

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CHAPTER 2 FEATURES

- Compliant to USB Specification Revision 2.0
  - Upstream port supports both high-speed (HS) and full-speed (FS) traffic
  - Downstream ports support HS, FS, and low-speed (LS) traffic
  - 1 control pipe (endpoint 0, 64-byte data payload) and 1 interrupt pipe (endpoint 1, 1-byte data payload)
  - Backward compatible to *USB specification Revision 1.1*
- On-chip 8-bit micro-processor
  - RISC-like architecture
  - USB optimized instruction set
  - Performance: 6 MIPS @ 12MHz
  - With 64-byte RAM and 4K mask ROM
  - Support customized PID, VID by external EEPROM/ SMBUS/
  - Support downstream port configuration by external EEPROM/ SMBUS/
- Single Transaction Translator (STT)
  - Single TT shares the same TT control logics for all downstream port devices. This is the most cost effective solution for TT.
- Integrate USB 2.0 transceiver
  - Improve output drivers with slew-rate control for EMI reduction
  - Internal power-fail detection for ESD recovery
- Low BOM cost
  - Built-in 5V to 3.3V regulator
  - Built-in upstream 1.5KΩ pull high and downstream 15KΩ pull-down
  - Built-in PLL supports external 12 MHz crystal / Oscillator clock input
  - Embed serial resister for USB signals
- Low power support
  - Support Selective Suspend
  - Support LPM L1 with EEPROM
- Smart power mode
  - Support both individual and gang modes of power management and over-current detection for downstream ports (Individual mode is not supported by SSOP 28 package)
  - Conform to bus power requirements
- Flexible design
  - Number of Downstream port can be configured by SMBUS / EEPROM/
  - Compound-device (non-removable in downstream ports) could be configured by I/O strapping/ SMBUS / EEPROM/
  - Automatic switching between self-powered and bus-powered modes
- Available package:
  - 28 pin QFN (5x5mm)
  - 28 pin SSOP (209mil)
  - 24 pin QFN (4x4mm)
- Applications:
  - Standalone USB hub
  - NB / Tablet / Motherboard / Docking Station
  - Gaming console
  - LCD monitor hub
  - Any compound device to support USB hub function

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CHAPTER 3 PIN ASSIGNMENT

3.1 Pinouts



Figure 3.1 - GL850G-60 SSOP28 Pinout Diagram

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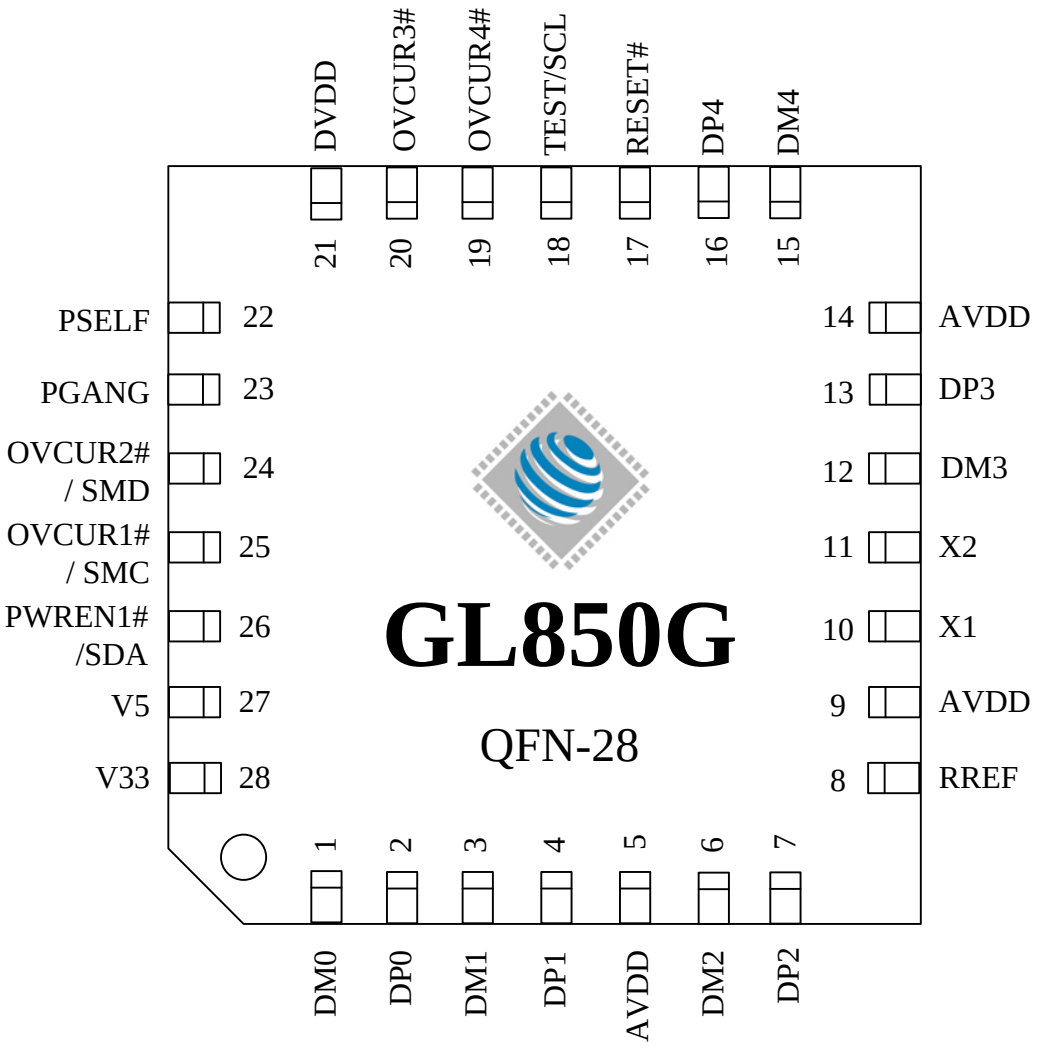

Figure 3.2 - GL850G-60 QFN28 Pinout Diagram

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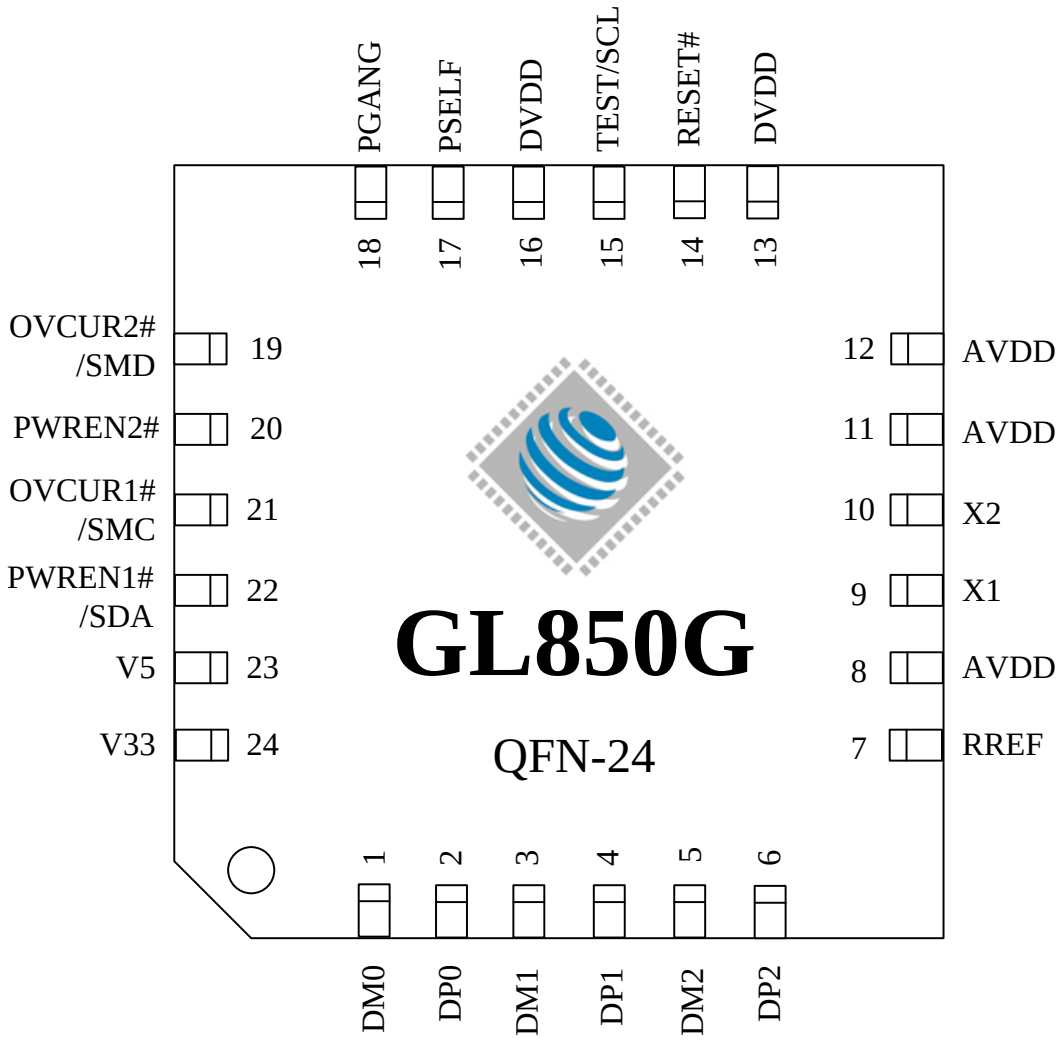

Figure 3.3 - GL850G-60 QFN24 Pinout Diagram

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3.2 Pin List

Table 3.1 - GL850G-60 SSOP 28 Pin List

Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type
1	AVDD	P	8	DM3	B	15	GND	P	22	PWREN1# /SDA	O/B
2	DM2	B	9	DP3	B	16	DVDD	P	23	V5	P
3	DP2	B	10	AVDD	P	17	PSELF	I_5V	24	V33	P
4	RREF	A	11	DM4	B	18	PGANG	B	25	DM0	B
5	AVDD	P	12	DP4	B	19	OVCUR2# /SMD	I/B	26	DP0	B
6	X1	I	13	RESET#	I_5V	20	PWREN2#	O	27	DM1	B
7	X2	O	14	TEST/SCL	I/B	21	OVCUR1# /SMC	I_5V	28	DP1	B

Table 3.2 - GL850G-60 QFN 28 Pin List

Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type
1	DM0	B	8	RREF	A	15	DM4	B	22	PSELF	I_5V
2	DP0	B	9	AVDD	P	16	DP4	B	23	PGANG	B
3	DM1	B	10	X1	I	17	RESET#	I_5V	24	OVCUR2# /SMD	I/B
4	DP1	B	11	X2	O	18	TEST/SCL	I/B	25	OVCUR1# /SMC	I_5V
5	AVDD	P	12	DM3	B	19	OVCUR4#	I_5V	26	PWREN1# /SDA	B
6	DM2	B	13	DP3	B	20	OVCUR3#	I_5V	27	V5	P
7	DP2	B	14	AVDD	P	21	DVDD	P	28	V33	P

Table 3.3 - GL850G-60 QFN 24 Pin List

Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type	Pin#	Pin Name	Type
1	DM0	B	7	RREF	A	13	DVDD	P	19	OVCUR2# /SMD	I/B
2	DP0	B	8	AVDD	P	14	RESET#	I_5V	20	PWREN2#	O/B
3	DM1	B	9	X1	I	15	TEST/SCL	I/B	21	OVCUR1# /SMC	I_5V
4	DP1	B	10	X2	O	16	DVDD	P	22	PWREN1# /SDA	O/B
5	DM2	P	11	AVDD	P	17	PSELF	I_5V	23	V5	P
6	DP2	B	12	AVDD	P	18	PGANG	B	24	V33	P

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Table 3.4 - Pin Descriptions

USB Interface					
Pin Name	**GL850G-60**			**I/O Type**	**Description**
	SSOP 28 Pin	**QFN 28 Pin**	**QFN 24 Pin**		
DM0,DP0	25,26	1,2	1,2	B	USB signals for USPORT
DM1,DP1	27,28	3,4	3,4	B	USB signals for DSPORT1
DM2,DP2	2,3	6,7	5,6	B	USB signals for DSPORT2
DM3,DP3	8,9	12,13	-	B	USB signals for DSPORT3
DM4,DP4	11,12	15,16	-	B	USB signals for DSPORT4
RREF	4	8	7	A	A 680Ω resister must be connected between RREF and analog ground (AGND)

Note: USB signals must be carefully handled in PCB routing. For detailed information, please refer to **USB 2.0 Hub Design Guide**.

Hub Interface					
Pin Name	**GL850G-60**			**I/O Type**	**Description**
	SSOP 28 Pin	**QFN 28 Pin**	**QFN 24 Pin**		
OVCUR1~4#	21,19	25,24, 20,19	21,19	I_5V	Active low. Over current indicator for DSPORT1~4. *Over current flag On when OVCUR= low over 3ms. OVCUR1# is the only over current flag for GANG mode. *In reset state : OVCUR1# will be SMC, OVCUR2# will be SMD OVCUR pin has strapping for configuration, pulled-high to enable port; pulled-down to disable port; floating to set non-removable port.
PWREN1~2#	22,20	-	22,20	O	Active low. Power enable output for DSPORT1~2 PWREN1# is the only power-enable output for GANG mode
PSELF	17	22	17	I_5V	0: GL850G-60 is bus-powered 1: GL850G-60 is self-powered

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PGANG	18	23	18	B	This pin is default put in input mode after power-on reset. Individual/gang mode is strapped during this period. After the strapping period, this pin will be set to output mode, and then output high for normal mode. When GL850G-60 is suspended, this pin will output low. *For detailed explanation, please see Chapter 5 Gang input:1, output: 0@normal, 1@suspend Individual input:0, output: 1@normal, 0@suspend *Note: Individual mode only available for QFN28 package.

Clock and Reset Interface					
Pin Name	**GL850G-60**			**I/O Type**	**Description**
	SSOP 28 Pin	**QFN 28 Pin**	**QFN 24 Pin**		
X1	6	10	9	I	12MHz crystal clock input
X2	7	11	10	O	12MHz crystal clock output
RESET#	13	17	14	I_5V	Active low. External reset input, default pull high 10KΩ When RESET# = low, whole chip is reset to the initial state

System Interface					
Pin Name	**GL850G-60**			**I/O Type**	**Description**
	SSOP 28 Pin	**QFN 28 Pin**	**QFN 24 Pin**		
TEST/SCL	14	18	15	I/B	TEST: 0: Normal operation. 1: Chip will be put in test mode. I2C: clock output pin; only for EEPROM use
SDA	22	26	22	B	I2C: data pin; only for EEPROM use
SMC	21	25	21	B	SMBUS clock
SMD	19	24	19	B	SMBUS data

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Power / Ground					
Pin Name	GL850G-60			I/O Type	Description
	SSOP 28 Pin	QFN 28 Pin	QFN 24 Pin		
AVDD	1,5,10	5,9,14	8,11,12	P	3.3V analog power input for analog circuits
DVDD	16	21	13,16	P	3.3V digital power input for digital circuits
GND	15	Bottom Ground Pad	Bottom Ground Pad	P	Ground Exposed pad is connected to GND
V5	23	27	23	P	5V Power input. This pin should be provided 3.3V while using external regulator
V33	24	28	24	P	5V-to-3.3V regulator Vout & 3.3V input

Note: Analog circuits are quite sensitive to power and ground noise. PCB layout must takes care the power routing and the ground plane. For detailed information, please refer to **USB 2.0 Hub Design Guide**.

Notation:

Type	**O**	Output
	I	Input
	I_5V	5V tolerant input
	B	Bi-directional
	B/I	Bi-directional, default input
	B/O	Bi-directional, default output
	P	Power / Ground
	A	Analog
	SO	Automatic output low when suspend
	pu	Internal pull high
	pd	Internal pull down
	odpu	Open drain with internal pull high

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CHAPTER 4 BLOCK DIAGRAM

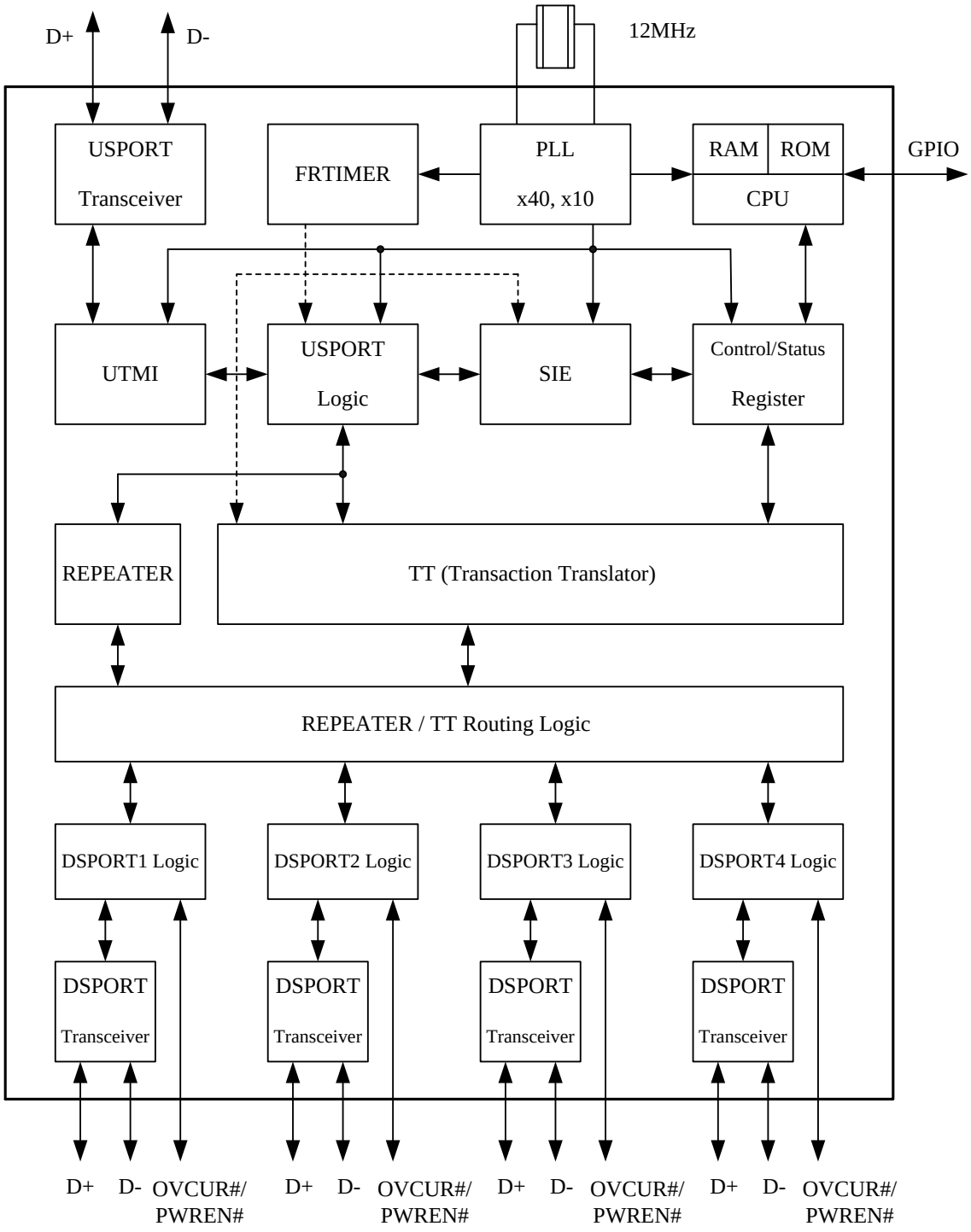

Figure 4.1 - GL850G-60 4-DFP Block Diagram

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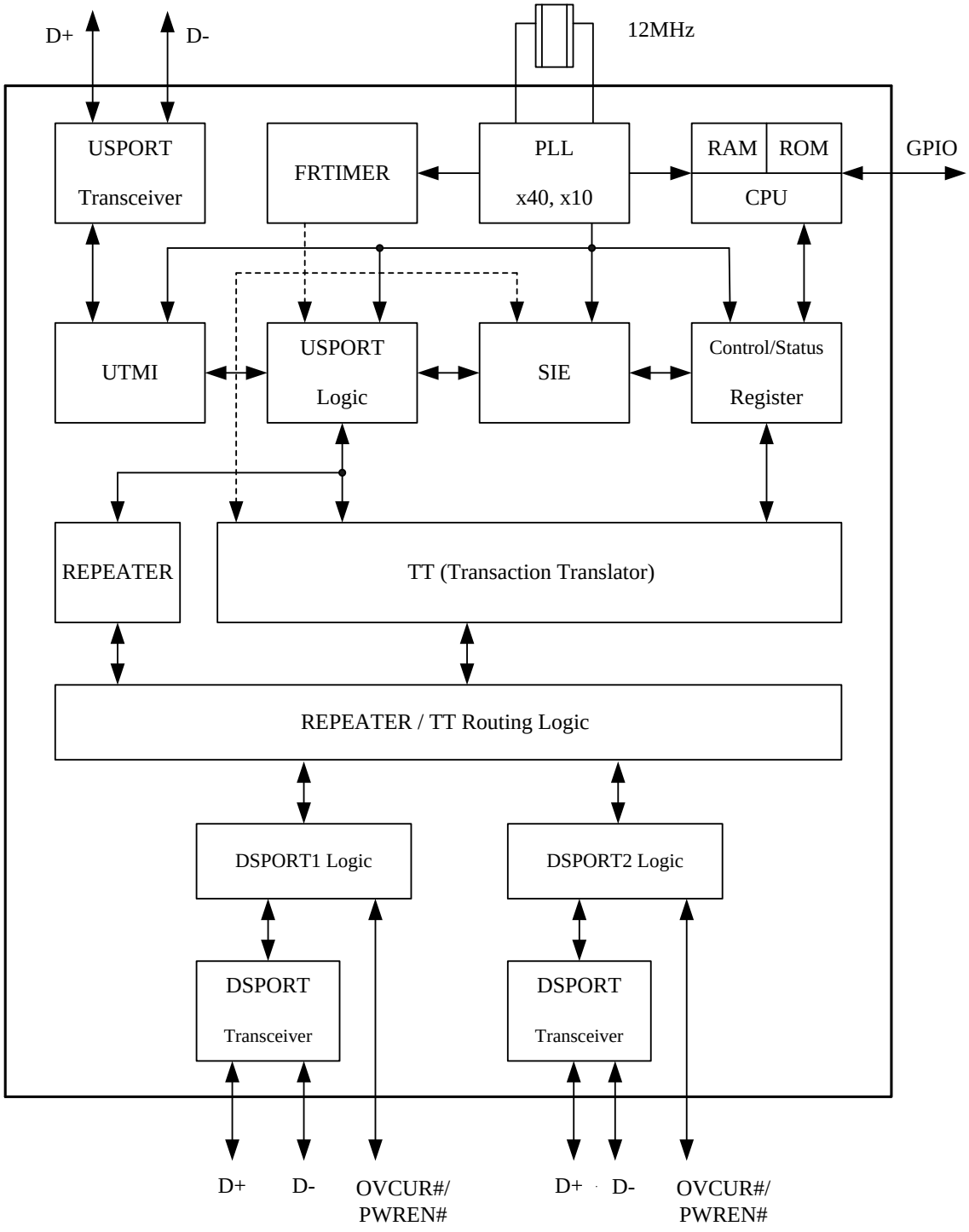

Figure 4.2 - GL850G-60 2-DFP Block Diagram

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CHAPTER 5 FUNCTION DESCRIPTION

5.1 General Description

5.1.1 USPORT Transceiver

USPORT (upstream port) transceiver is the analog circuit that supports both full-speed and high-speed electrical characteristics defined in chapter 7 of *USB specification Revision 2.0*. USPORT transceiver will operate in full-speed electrical signaling when GL850G-60 is plugged into a 1.1 host/hub. USPORT transceiver will operate in high-speed electrical signaling when GL850G-60 is plugged into a 2.0 host/hub.

5.1.2 PLL (Phase Lock Loop)

GL850G-60 contains a 40x PLL. PLL generates the clock sources for the whole chip. The generated clocks are proven quite accurate that help in generating high speed signal without jitter.

5.1.3 FRTIMER

This module implements hub (micro) frame timer. The (micro) frame timer is derived from the hub's local clock and is synchronized to the host (micro) frame period by the host generated Start of (micro) frame (SOF). FRTIMER keeps tracking the host's SOF such that GL850G-60 is always safely synchronized to the host. The functionality of FRTIMER is described in section 11.2 of *USB Specification Revision 2.0*.

5.1.4 µC

µC is the micro-processor unit of GL850G-60. It is an 8-bit RISC processor with 4K ROM and 64 bytes RAM. It operates at 6MIPS of 12MHz clock to decode the USB command issued from host and then prepares the data to respond to the host. In addition, µC can handle GPIO (general purpose I/O) settings and reading content of EEPROM to support high flexibility for customers of different configurations of hub. These configurations include self/bus power mode setting, individual/gang mode setting, downstream port number setting, device removable/non-removable setting, port electrical tuning and PID/VID setting.

5.1.5 UTMI (USB 2.0 Transceiver Microcell Interface)

UTMI handles the low level USB protocol and signaling. It's designed based on the Intel's UTMI specification 1.01. The major functions of UTMI logic are to handle the data and clock recovery, NRZI encoding/decoding, Bit stuffing /de-stuffing, supporting USB 2.0 test modes, and serial/parallel conversion.

5.1.6 USPORT Logic

USPORT implements the upstream port logic defined in section 11.6 of USB specification Revision 2.0. It mainly manipulates traffics in the upstream direction. The main functions include the state machines of Receiver and Transmitter, interfaces between UTMI and SIE, and traffic control to/from the REPEATER and TT.

5.1.7 SIE (Serial Interface Engine)

SIE handles the USB protocol defined in chapter 8 of USB specification Revision 2.0. It co-works with Mc to play the role of the hub kernel. The main functions of SIE include the state machine of USB protocol flow, CRC check, PID error check, and timeout check. Unlike USB 1.1, bit stuffing/de-stuffing is implemented in UTMI, not in SIE.

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5.1.8 Control/Status Register

Control/Status register is the interface register between hardware and firmware. This register contains the information necessary to control endpoint0 and endpoint1 pipes. Through the firmware based architecture, GL850G-60 possesses higher flexibility to control the USB protocol easily and correctly.

5.1.9 REPEATER

Repeater logic implements the control logic defined in section 11.4 and section 11.7 of *USB specification Revision 2.0*. REPEATER controls the traffic flow when upstream port and downstream port are signaling in the same speed. In addition, REPEATER will generate internal resume signal whenever a wakeup event is issued under the situation that hub is globally suspended.

5.1.10 TT (Transaction Translator)

TT implements the control logic defined in section 11.14 ~ 11.22 of *USB specification Revision 2.0*. TT basically handles the unbalanced traffic speed between the USPORT (operating in HS) and DSPORTS (operating in FS/LS) of hub. GL850G-60 adopts the single TT architecture to provide the most cost effective solution. Single TT shares the same buffer control module for each downstream port. GL852G adopts multiple TT architecture to provide the most performance effective solution. Multiple TT provides control logics for each downstream port respectively. Please refer to GL852G datasheet for more detailed information.

5.1.11 REPEATER/TT Routing Logic

REPEATER and TT are the major traffic control machines in the USB 2.0 hub. Under situation that USPORT and DSPORT are signaling in the same speed, REPEATER/TT routing logic switches the traffic channel to the REPEATER. Under situation that USPORT is in the high speed signaling and DSPORT is in the full/low speed signaling, REPEATER/TT routing logic switches the traffic channel to the TT.

5.1.11.1 Connected to USB 1.1 Host/Hub

If an USB 2.0 hub is connected to the downstream port of an USB 1.1 host/hub, it will operate in USB 1.1 mode. For an USB 1.1 hub, both upstream direction traffic and downstream direction traffic are passing through REPEATER. That is, the REPEATER/TT routing logic will route the traffic channel to the REPEATER.

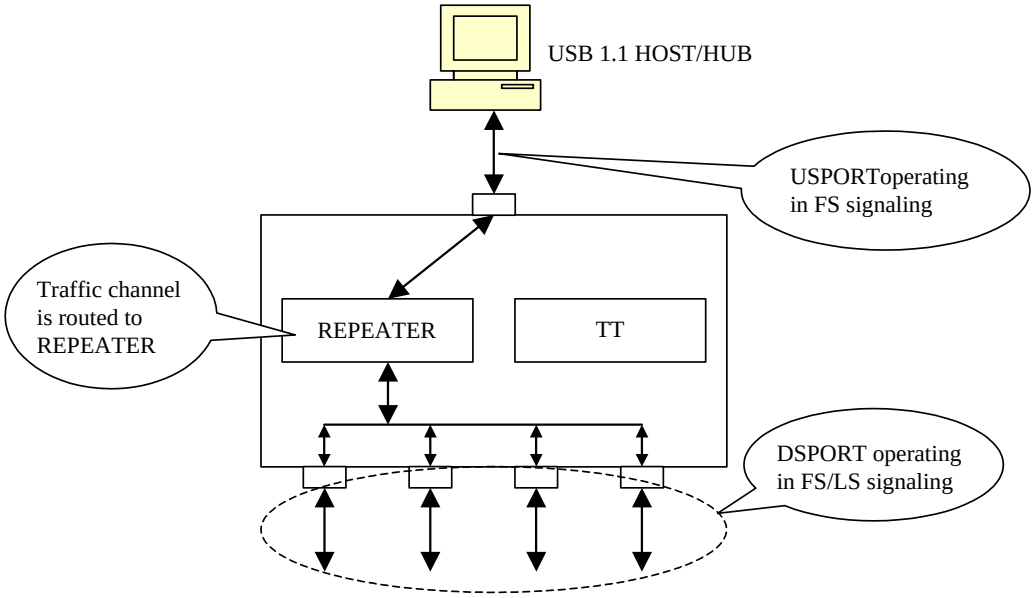

Figure 5.1 - Operating in USB 1.1 Scheme

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5.1.11.2 Connected to USB 2.0 Host/Hub

If an USB 2.0 hub is connected to an USB 2.0 host/hub, it will operate in USB 2.0 mode. The upstream port signaling is in high speed with bandwidth of 480 Mbps under this environment. The traffic channel will then be routed to the REPEATER when the device connected to the downstream port is signaling also in high speed. On the other hand, the traffic channel will then be routed to TT when the device connected to the downstream port is signaling in full/low speed.

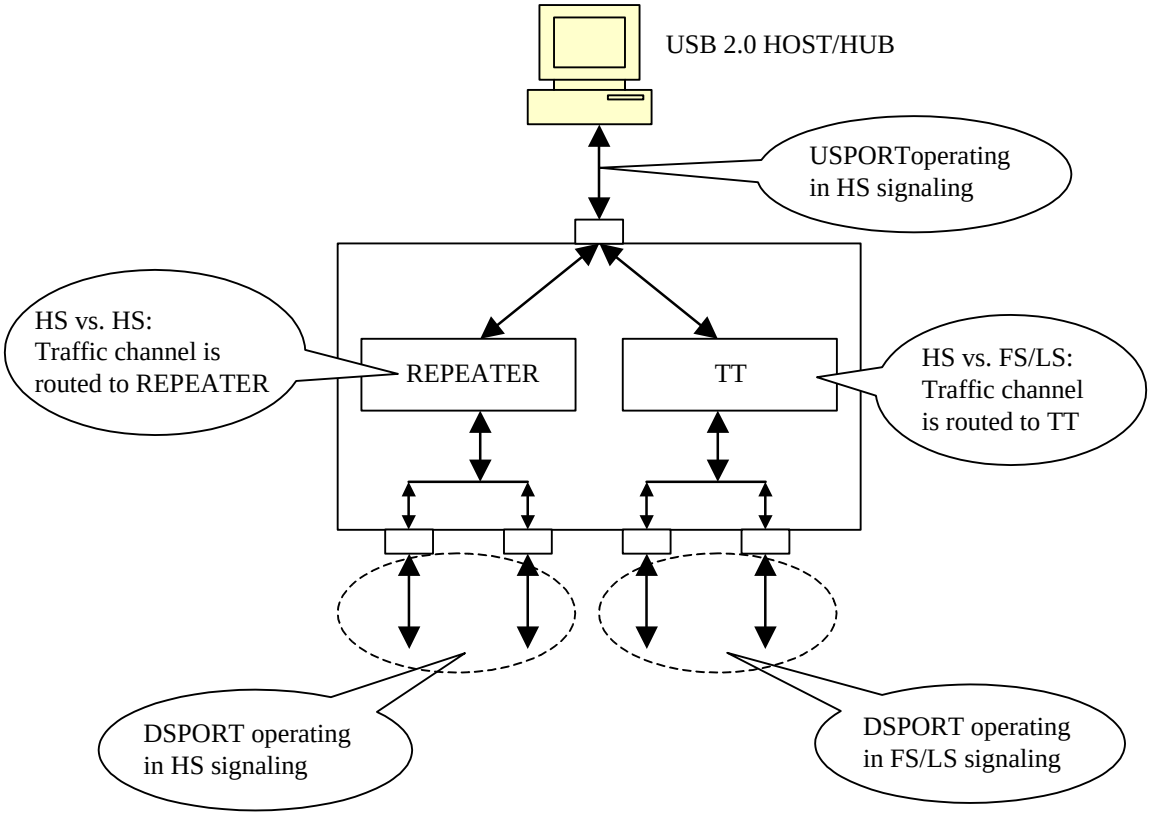

Figure 5.2 - Operating in USB 2.0 Scheme

DSPORT (downstream port) logic implements the control logic defined in section 11.5 of *USB specification Revision 2.0.* It mainly manipulates the state machine, the connection/disconnection detection, over current detection and power enable control, and the status LED control of the downstream port. Besides, it also output the control signals to the DSPORT transceiver.

5.1.13 DSPORT Transceiver

DSPORT transceiver is the analog circuit that supports high-speed, full-speed, and low-speed electrical characteristics defined in chapter 7 of *USB specification Revision 2.0.* In addition, each DSPORT transceiver accurately controls its own squelch level to detect the detachment and attachment of devices.

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5.2 Configuration and I/O Settings

5.2.1 RESET Setting

GL850G-60's power on reset can either be triggered by external reset or internal power good reset circuit. The external reset pin, RESET#, is connected to upstream port Vbus (5V) to sense the USB plug / unplug or 5V voltage drop. The reset trigger voltage can be set by adjusting the value of resistor R1 and R2 (Suggested value refers to schematics) GL850G-60's internal reset is designed to monitor silicon's internal core power (3.3V) and initiate reset when unstable power event occurs. The power on sequence will start after the power good voltage has been met, and the reset will be released after approximately 110~210 uS after power good.

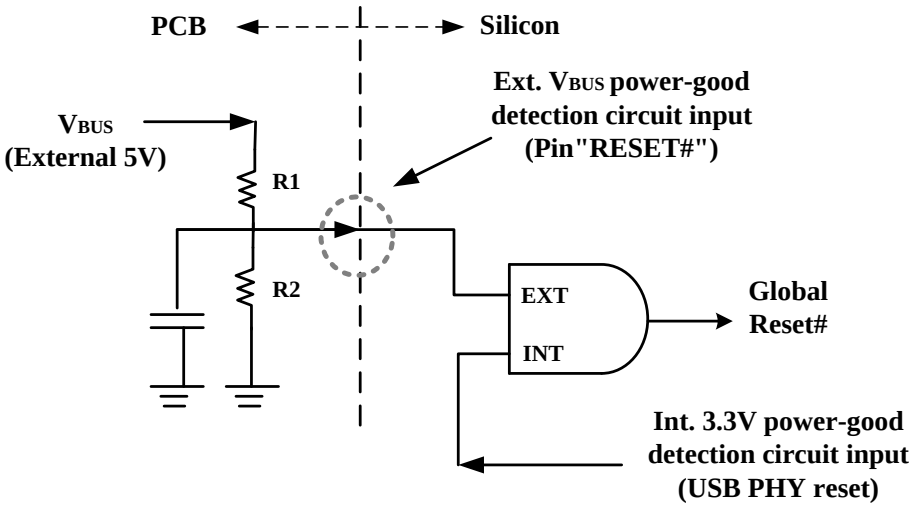

Figure 5.3 - Power on Reset Diagram

GL850G-60 internally contains a power on reset circuit as depicted in the picture above.

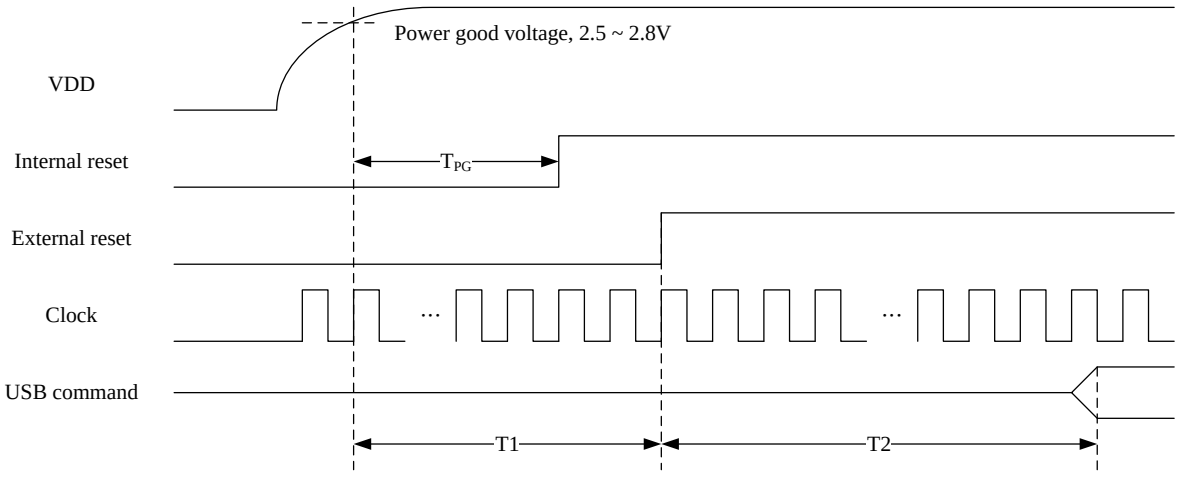

Figure 5.4 - Power on Sequence of GL850G-60

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Table 5.1 - Reset Timing

Symbol	Parameter	Min.	Max.	Unit
T_{PG}	VDD power up to internal reset (power good) assert	110	210	μs
T1	VDD power up to external reset (RESET#) assert	220	-	μs
T2	RESET assert to respond USB command ready	70	-	ms

To fully control the reset process of GL850G-60, we suggest the reset time applied in the external reset circuit should longer than that of the internal reset circuit.

5.2.2 PGANG/SUSPND Setting

To save pin count, GL850G-60 uses the same pin to decide individual/gang mode as well as to output the suspend flag. The individual/gang mode is decided within 20us after power on reset. Then, about 50ms later, this pin is changed to output mode. GL850G-60 outputs the suspend flag once it is globally suspended. For individual mode, a pull low resister greater than 100KΩ should be placed. For gang mode, a pull high resister greater than 100KΩ should be placed. In figure 5.5, we also depict the suspend LED indicator schematics. It should be noticed that the polarity of LED must be followed, otherwise the suspend current will be over spec limitation (2.5mA).

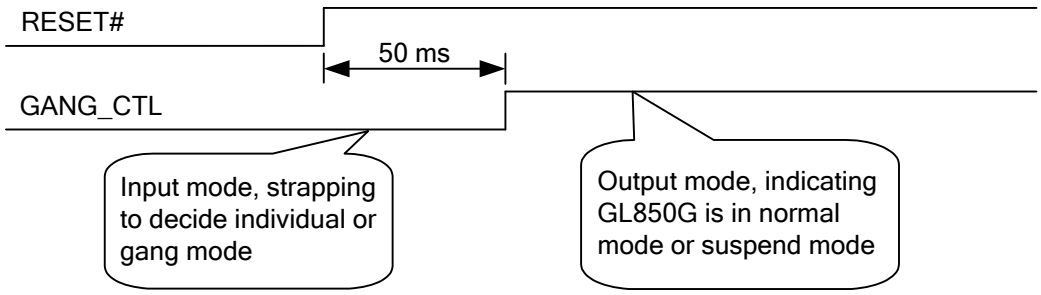

Figure 5.5 - Timing of PGANG/SUSPEND Strapping

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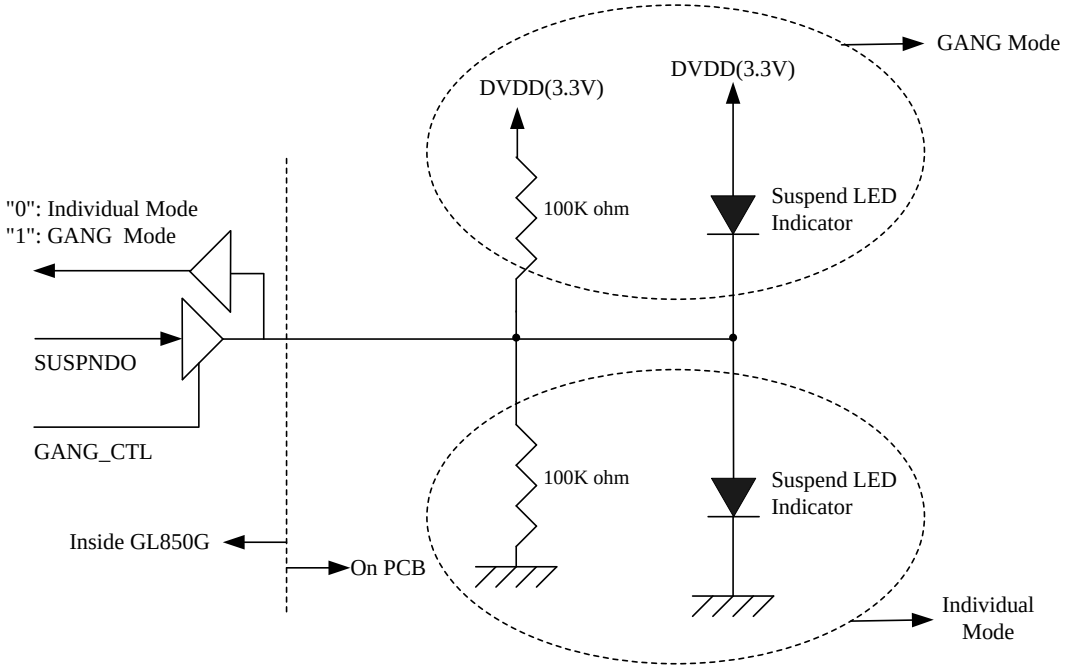

Figure 5.6 - Individual/GANG Mode Setting

5.2.3 SELF/BUS Power Setting

GL850G-60 can operate under bus power and conform to the power consumption limitation completely (suspend current < 2.5 mA, normal operation current < 100 mA). By setting PSELF, GL850G-60 can be configured as a bus-power or a self-power hub.

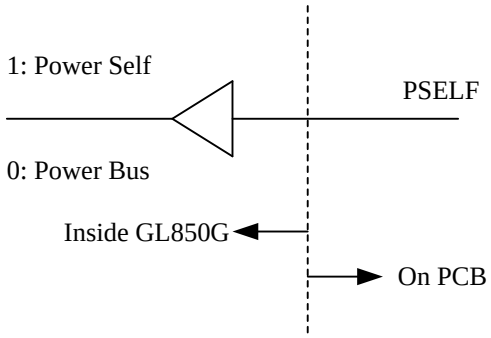

Figure 5.7 - SELF/BUS Power Setting

5.2.4 EEPROM Setting

GL850G-60 replies to host commands by default settings in the internal ROM. GL850G-60 also offers the ability to reply to host according to the settings in the external EEPROM (24C02). Please refer to **GL850G-5x Hub AP Note_EEPROM Info** document for the detailed setting information.

Please note that EEPROM and power switch cannot be used at the same time because PWREN1# and SDA are shared pin.

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5.2.5 Port Configuration

Downstream port can be configured (disabled) in following three ways:

1. I/O Strapping:

When OVCUR# pin of a downstream port is pulled or tied low to GND, the downstream port is disabled. Then, GL850G-60 will automatically rearrange logical port number and port order according to strapping results. Allowable port number configuration of GL850G-60 is shown in the following table.

Table 5.2 - Port Configuration

Physical Port Position		Port 1	Port 2	Port 3	Port 4
Logical Downstream Port Number	4 Ports Case	1	2	3	4
	3 Ports Case	1	2	3	Disabled
		1	2	Disabled	3
		1	Disabled	2	3
		Disabled	1	2	3
	2 Ports Case	1	2	Disabled	Disabled
		1	Disabled	2	Disabled
		1	Disabled	Disabled	2
		Disabled	1	2	Disabled
		Disabled	1	Disabled	2
		Disabled	Disabled	1	2
	1 Port Case	1	Disabled	Disabled	Disabled
		Disabled	1	Disabled	Disabled
		Disabled	Disabled	1	Disabled
		Disabled	Disabled	Disabled	1
	0 Port Case (Illegal Case)	1	2	3	4

For SSOP28 package, there is no pin-out for OVCUR3# and OVCUR4# which are always floating internally, so physical downstream port 3 and 4 are always not disabled by I/O Strapping. And more, in order to keep over current detection function, SSOP28 package cannot disable physical port 1 & 2 at the same time in gang mode.

2. SMBUS (Refer to Chapter 5.2.8)
3. EEPROM (Refer to Chapter 5.2.4)

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5.2.6 Non-removable Port Configuration (Not Available for SSOP28)

For compound application or embedded system, downstream ports that always connected inside the system can be set as non-removable based on the state of pin OVCUR1# ~ 4#. If the pin is floating, the corresponding port will be set as non-removable. Non-removable port also can be configured by SMBUS or EEPROM.

.

Table 5.3 - QFN 28 Non-removable Port Configurations

OVCURn#	Non-removable Configuration of Portn
Floating	Non-removable
Pull high	Removable

5.2.7 SMBUS Mode (SMBUS Slave Address=0x2C)

GL850G-60 enters SMBUS mode since Power-On occurs, and RESET# pin is asserted as well. After that, GL850G-60 will define OVCUR1# as SMC and OVCUR2# as SMD. GL850G-60 will exit the SMBUS mode since the RESET# pin is de-asserted. The more complicated settings such as PID, VID, power saving, port number, port non/removable, and downstream port electrical tuning can be configured by SMBUS.

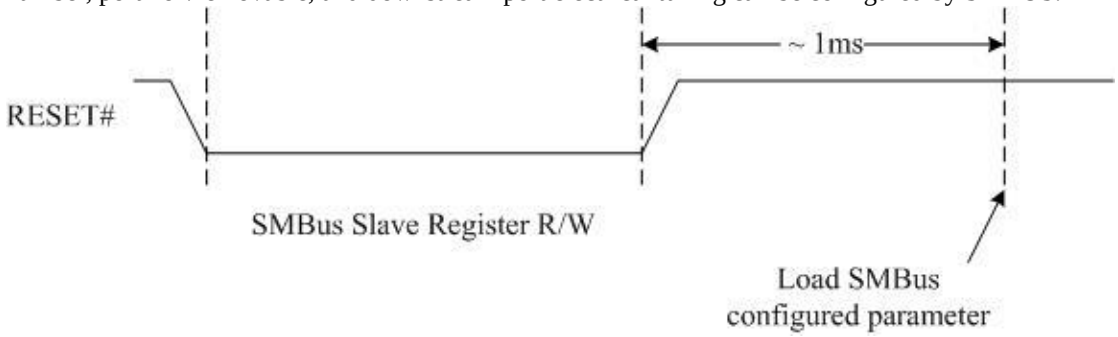

Figure 5.8 - SMBus Timing Diagram

5.2.7.1 SMBus Internal Register Set

Table 5.4 - Internal Register Set

Address	Mnemonic	Register Description
00h	**VIDL**	Vendor ID LSB
01h	**VIDH**	Vendor ID MSB
02h	**PIDL**	Product ID LSB
03h	**PIDH**	Product ID MSB
04h	**ELECTRICAL1**	Upstream and Logical Downstream port electrical tuning option
05h	**CONFIG**	Hub non-removable configuration
07h	**ELECTRICAL2**	Logical Downstream port 1 & 2 electrical tuning option
08h	**ELECTRICAL3**	Logical Downstream port 3 & 4 electrical tuning option
2Bh	**DP12_PORT**	Physical Downstream port 1 & 2 enable/disable option

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2Ch	**DP34_PORT**	Physical Downstream port 3 & 4 enable/disable option

5.2.7.1.1 VIDL – Vendor ID LSB

- Address: 00h
- Default value: E3h

Bit	Description
7:0	**VID[7:0]**, least significant byte of the Vendor ID

5.2.7.1.2 VIDH – Vendor ID MSB

- Address: 01h
- Default value: 05h

Bit	Description
7:0	**VID[15:8]**, most significant byte of the Vendor ID

5.2.7.1.3 PIDL – Product ID LSB

- Address: 02h
- Default value: 08h

Bit	Description
7:0	**PID[7:0]**, least significant byte of the Product ID

5.2.7.1.4 PIDH – Product ID MSB

- Address: 03h
- Default value: 06h

Bit	Description
7:0	**PID[15:8]**, most significant byte of the Product ID

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5.2.7.1.5 ELECTRICAL – Downstream Port Electrical Tuning Option

- Address: 04h
- Default value: 40h

Bit	Description
7:5	Upstream port high speed transmitter JK level control Default value: 3'b010
4:0	Upstream port and Downstream port 1 ~ 4 high speed transmitter slew rate control '0' – normal '1' – improved Bit0: control downstream port 1 Bit1: control downstream port 2 Bit2: control downstream port 3 Bit3: control downstream port 4 Bit4: control upstream port

5.2.7.1.6 CONFIG – Hub non-removable Configuration

- Address: 05h
- Default value: 00h

Bit	Description
7:4	Reserved
3:0	Port non-removable configuration '0' – Removable '1' – Non-removable Bit0: control downstream port 1 Bit1: control downstream port 2 Bit2: control downstream port 3 Bit3: control downstream port 4

5.2.7.1.7 ELECTRICAL2 –Downstream Port 1 & 2 Electrical Tuning Option

- Address: 07h
- Default value: 44h

Bit	Description
7:5	Downstream port 2 high speed transmitter JK level control Default value: 3'b010
4	Reserved
3:1	Downstream port 1 high speed transmitter JK level control Default value: 3'b010
0	Reserved

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5.2.7.1.8 ELECTRICAL3 –Downstream Port 3 & 4 Electrical Tuning Option

- Address: 08h
- Default value: 44h

Bit	Description
7:5	Downstream port 4 high speed transmitter JK level control Default value: 3'b010
4	Reserved
3:1	Downstream port 3 high speed transmitter JK level control Default value: 3'b010
0	Reserved

5.2.7.1.9 DP12_PORT - Physical Downstream Port 1 & 2 enable/disable Option

- Address: 2Bh
- Default value: A9h

Bit	Description
7	Physical Downstream port 2 enable/disable option '1' – Enable '0' – Disable
6:4	Reserved
3	Physical Downstream port 1 enable/disable option '1' – Enable '0' – Disable
2:0	Reserved

5.2.7.1.10 DP34_PORT - Physical Downstream Port 3 & 4 enable/disable Option

- Address: 2Ch
- Default value: CBh

Bit	Description
7	Physical Downstream port 4 enable/disable option '1' – Enable '0' – Disable
6:4	Reserved
3	Physical Downstream port 3 enable/disable option '1' – Enable '0' – Disable
2:0	Reserved

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5.2.7.2 SMBus Protocol

Fig. 5.9 shows the SMBus topology. The VDD power is 3.3V +/- 10% and the pull high resistor is 1KΩ. Both SMBCLK and SMBDAT lines are bi-directional, connected to 3.3V supply voltage through a pull high resistor. The operating frequency is 10~100 KHz.

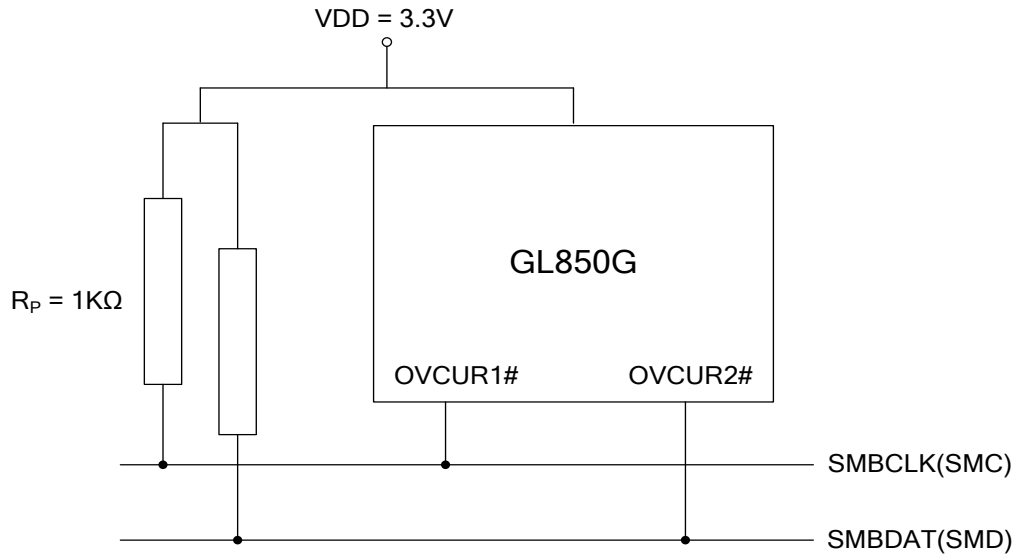

Figure 5.9 - SMBus Topology

SMBus uses fixed voltage levels to define the logic "ZERO" and logic "ONE" on the bus respectively. The data on SMBDAT must be stable during the "HIGH" period of the clock. Data can change state only when SMBCLK is low. Fig. 5.10 illustrates the relationships.

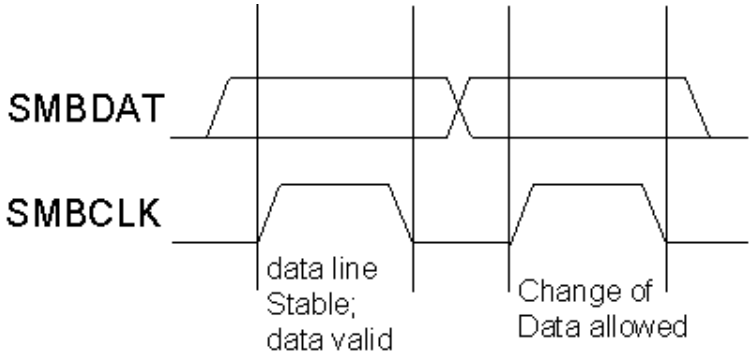

Figure 5.10 - Data Validity

Two unique bus situations define the messages of START and STOP conditions.
1. START condition: A HIGH to LOW transition of the SMBDAT line while SMBCLK is HIGH
2. STOP condition: A LOW to HIGH transition of the SMBDAT line while SMBCLK is HIGH

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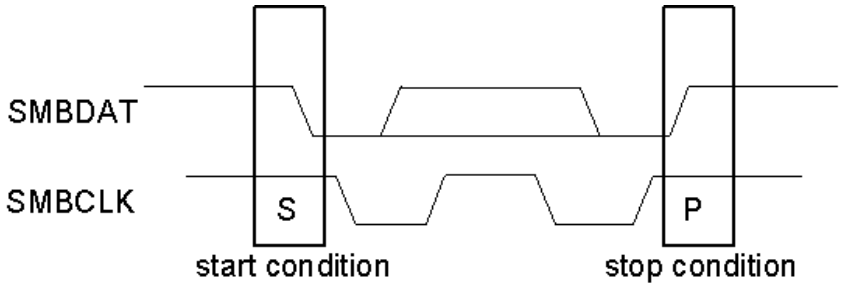

Figure 5.11 - START and STOP Condition

Every byte consists of 8 bits. Each byte transferred on the bus must be followed by an acknowledge bit. Bytes are transferred with the most significant bit (MSB) first. Fig. 5.12 illustrates the positioning of acknowledge (ACK) and not acknowledge (NACK) pulses relative to other data.

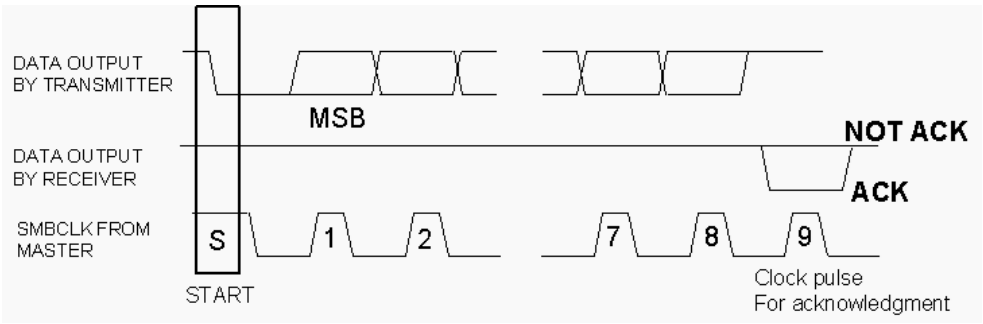

Figure 5.12 - ACK and NACK Signaling of SMBus

There is an element key for the SMBus protocol diagrams below.



S Start Condition
Sr Repeated Start Condition
Rd Read (bit value of 1)
Wr Write (bit value of 0)
x Shown under a field indicates that that field is required to have the value of 'x'
A Acknowledge (this bit position may be 0' for an ACK or '1' for a NACK)
P Stop Condition
Master-to-Slave
Slave-to-Master

Figure 5.13 - SMBus Packet Protocol Diagram Element Key

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Fig 5.14 shows a Write Byte Protocol. The first byte of a Write Byte access is the command code and next byte is the data to be written. In this example the master asserts slave address followed by the write bit. The slave acknowledges and the master delivers the command code. The slave acknowledges again before the master sends the data byte. The slave acknowledges the data byte, and the entire transaction is finished with a STOP condition.

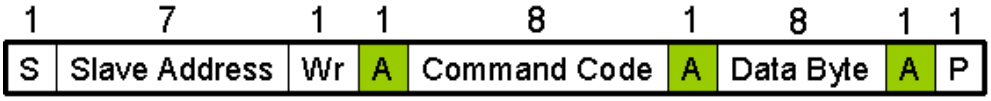

Figure 5.14 - Write Byte Protocol

Reading data is slightly more complicated than writing data. Firstly, the host has to write a command to slave, and the host must follow that command with a repeated START condition to denote a read from slave address. And the slave then returns one byte of data.
Please note there is no STOP condition before the repeated START condition, and a NACK signifies the end of the read transfer.

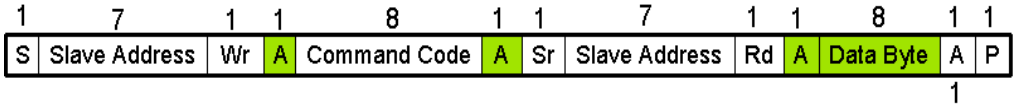

Figure 5.15 - Read Byte Protocol

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CHAPTER 6 ELECTRICAL CHARACTERISTICS

6.1 Maximum Ratings

Table 6.1 - Maximum Ratings

Symbol	Parameter	Min.	Max.	Unit
V5	5V Power Supply	-0.5	+6.0	V
VDD	3.3V Power Supply	-0.5	+3.6	V
VIN	Input Voltage for digital I/O pins	-0.5	+3.6	V
VINOD	Open-drain input pins(Ovcur1~4#,Pself,Reset)	-0.5	+5.5	V
VINUSB	Input Voltage for USB signal (DP, DM) pins	-0.5	+3.6	V
TS	Storage Temperature under bias	-55	+100	oC
FOSC	Frequency	12 MHz ± 0.05%		

6.2 Operating Ranges

Table 6.2 - Operating Ranges

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_5	5V Power Supply	4.5	5.0	5.5	V
V_{DD}	3.3V Power Supply	3.0	3.3	3.6	V
V_{IN}	Input Voltage for digital I/O pins	-0.5	-	3.6	V
V_{INOD}	Open-drain input pins(Ovcur1~4#,Pself,Reset)	-0.5	-	5.0	V
V_{INUSB}	Input Voltage for USB signal (DP, DM) pins	0.5	-	3.6	V
T_A	Ambient Temperature	0	-	70	ºC
T_J	Absolute maximum junction temperature	0	-	125	ºC
θ_{JA}	Thermal Characteristics 28 SSOP	-	65.65	-	ºC/W
	Thermal Characteristics 28 QFN	-	38.9	-	ºC/W

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6.3 DC Characteristics

Table 6.3 - DC Characteristics except USB Signals

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{IL}	LOW level input voltage	-	-	0.8	V
V_{IH}	HIGH level input voltage	2.0	-	-	V
V_{TLH}	LOW to HIGH threshold voltage	1.48	1.55	1.6	V
V_{THL}	HIGH to LOW threshold voltage	1.13	1.21	1.27	V
V_{OL}	LOW level output voltage when I_{OL}=8mA	-	-	0.4	V
V_{OH}	HIGH level output voltage when I_{OH}=8mA	2.4	-	-	V
$R_{UP_OVCUR\#}$	OVCUR# pin internal pull high resister	440	890	2000	KΩ
R_{DN_TEST}	TEST pin internal pull down resister	33	51	102	KΩ
R_{UP_PSELF}	PSELF pin internal pull high resister	148	222	359	KΩ

Table 6.4 - DC Characteristics of USB Signals under FS/LS Mode

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OL}	DP/DM FS static output LOW(R_L of 1.5K to 3.6V)	0	-	0.3	V
V_{OH}	DP/DM FS static output HIGH (R_L of 15K to GND)	2.8	-	3.6	V
V_{DI}	Differential input sensitivity	0.2	-	-	V
V_{CM}	Differential common mode range	0.8	-	2.5	V
V_{SE}	Single-ended receiver threshold	0.2	-	-	V
C_{IN}	Transceiver capacitance	-	-	20	pf
I_{LO}	Hi-Z state data line leakage	-10	-	+10	μA
Z_{DRV}	Driver output resistance	28	-	44	Ω

Table 6.5 - DC Characteristics of USB Signals under HS Mode

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{OL}	DP/DM HS static output LOW(R_L of 1.5K to 3.6V)	-	-	0.1	V
C_{IN}	Transceiver capacitance	4	4.5	5	pf
I_{LO}	Hi-Z state data line leakage	-5	0	+5	μA
Z_{DRV}	Driver output resistance for USB 2.0 HS	42	45	48	Ω

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6.4 Power Consumption

Table 6.6 –GL850G-60 power consumption

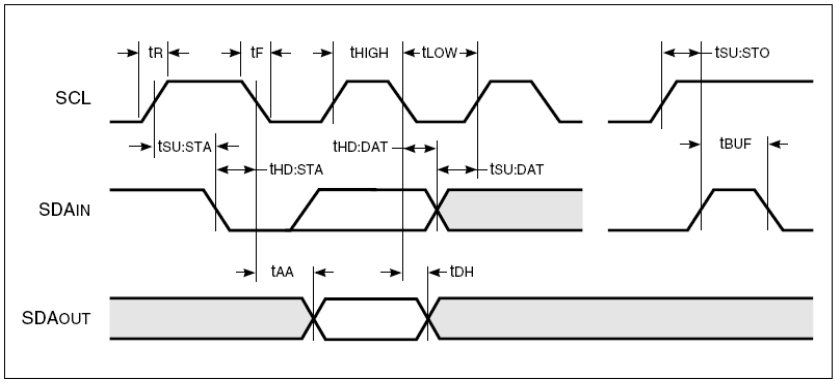
Symbol	Condition			Current	Unit
	Active ports	Host	Device		
I_{SUSP}	Suspend			**380**	uA
I_{CC}	4	H[*1]	H	**58.6**	mA
	3	H	H	**53.7**	mA
	2	H	H	**48.7**	mA
	1	H	H	**43.9**	mA
	Upstream Port Config.	H	N/A	**38.4**	mA

[*1]: H: High-Speed

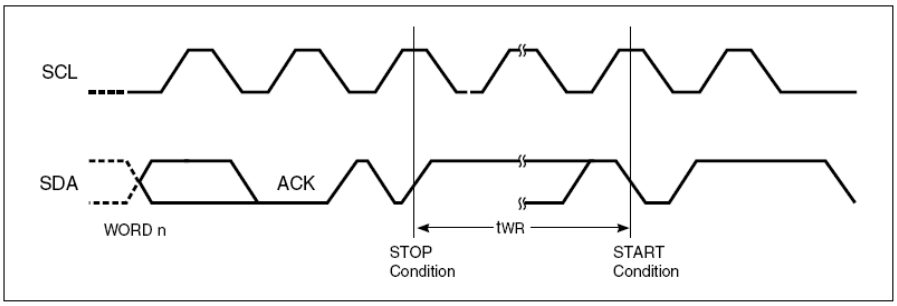
Note:

Test result was measured by 5V input (it will be lower by 3.3V input), and represents silicon level operating current, without considering additional power consumption contributed by external over-current protection circuit such as power switch or polyfuse.

6.5 EEPROM Interface



Bus Timing



Write Cycle Timing

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Table 6.7 - AC Characteristics of EEPROM Interface (24C02)

Symbol	Parameter	Test Conditions	1.8V-5.5V Min.	1.8V-5.5V Max.	2.5V-5.5V Min.	2.5V-5.5V Max.	Unit
f_{SCL}	SCL Clock Frequency		0	100	0	400	KHz
T	Noise Suppression Time(1)		—	100	—	50	ns
t_{LOW}	Clock LOW Period		4.7	—	1.2	—	µs
t_{HIGH}	Clock HIGH Period		4	—	0.6	—	µs
t_{BUF}	Bus Free Time Before New Transmission(1)		4.7	—	1.2	—	µs
$t_{SU:STA}$	Start Condition Setup Time		4.7	—	0.6	—	µs
$t_{SU:STO}$	Stop Condition Setup Time		4.7	—	0.6	—	µs
$t_{HD:STA}$	Start Condition Hold Time		4	—	0.6	—	µs
$t_{HD:STO}$	Stop Condition Hold Time		4	—	0.6	—	µs
$t_{SU:DAT}$	Data In Setup Time		200	—	100	—	ns
$t_{HD:DAT}$	Data In Hold Time		0	—	0	—	ns
t_{DH}	Data Out Hold Time	SCL LOW to SDA Data Out Change	100	—	50	—	ns
t_{AA}	Clock to Output	SCL LOW to SDA Data Out Valid	0.1	4.5	0.1	0.9	µs
t_R	SCL and SDA Rise Time(1)		—	1000	—	300	ns
t_F	SCL and SDA Fall Time(1)		—	300	—	300	ns
t_{WR}	Write Cycle Time		—	10	—	5	ms

Note:
1. This parameter is characterized but not 100% tested.

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6.6 On-Chip Power Regulator

GL850G-60 requires 3.3V source power for normal operation of internal core logic and USB physical layer (PHY). The integrated low-drop power regulator converts 5V power input from USB cable (Vbus) to 3.3V voltage for silicon power source. The 3.3V power output is guaranteed by an internal voltage reference circuit to prevent unstable 5V power compromise USB data integrity. The regulator's maximum current loading is 200mA, which provides enough tolerance for normal GL850G-60 operation (below 100mA).

On-chip Power Regulator Features:

- 5V to 3.3V low-drop power regulator
- 200mA maximum output driving capability
- Provide stable 3.3V output when Vin = 4.4V~5.5V
- Max. suspend current:266uA; typical suspend current 187uA

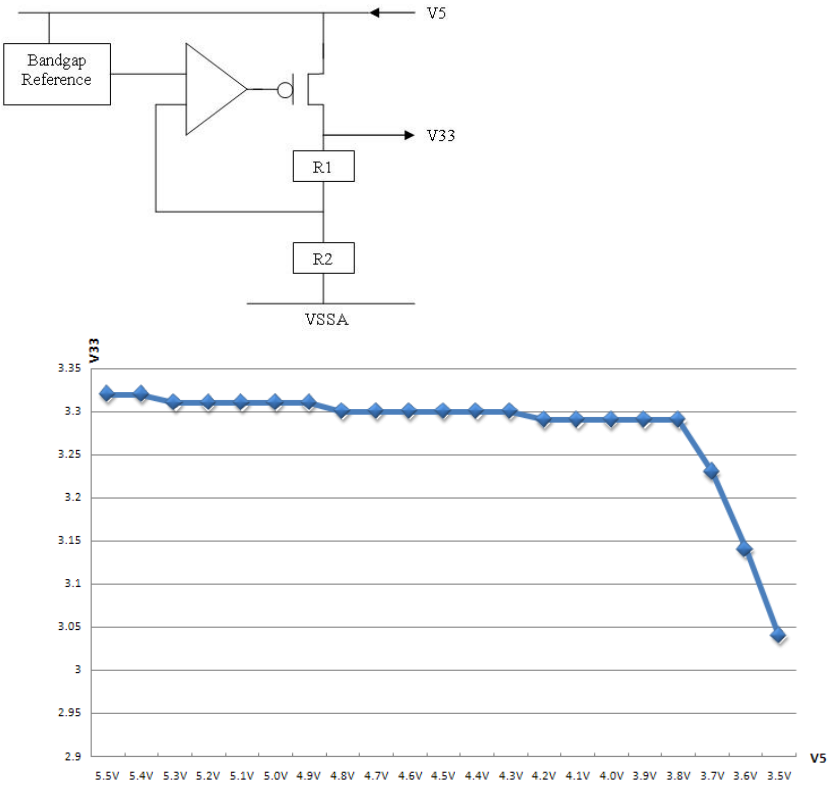

Figure 6.1 - Vin(V5) vs Vout(V33)*

*Note: Measured environment: Ambient temperature = 25℃ / Current Loading = 200mA

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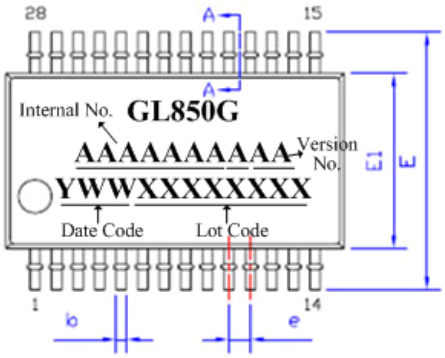
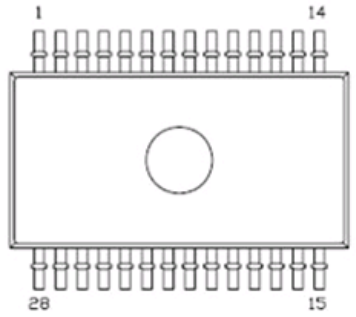
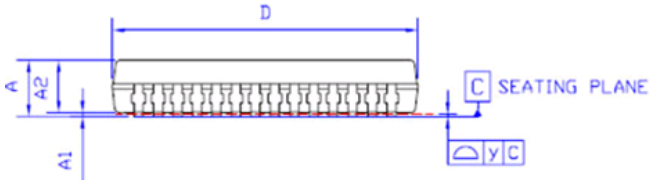
CHAPTER 7 PACKAGE DIMENSION

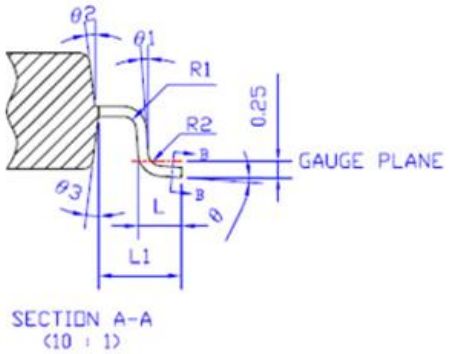


SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	---	---	2.00 (78.7)
A1	0.05 (2.0)	---	0.21 (8.3)
A2	1.65 (65.0)	1.75 (68.9)	1.85 (72.8)
b	0.22 (8.7)	---	0.38 (15.0)
b1	0.22 (8.7)	0.30 (11.8)	0.33 (13.0)
c	0.09 (3.5)	---	0.25 (9.8)
c1	0.09 (3.5)	---	0.21 (8.3)
D	10.20 (401.6) BSC		
e	0.65 (25.6) BSC		
E	7.80 (307.1) BSC		
E1	5.30 (208.7) BSC		
L	0.55 (21.7)	0.75 (29.5)	0.95 (37.4)
L1	1.25 (49.2) REF		
R1	0.15 (5.9)	0.20 (7.9)	0.25 (9.8)
R2	0.15 (5.9)	0.20 (7.9)	0.25 (9.8)
y	---	---	0.08 (3.1)
θ	0°	4°	8°
θ1	0°	---	---
θ2	7° TYP		
θ3	7° TYP		

NOTE: 1. REFER TO JEDEC MO-150
2. ALL DIMENSIONS IN MILLIMETERS.









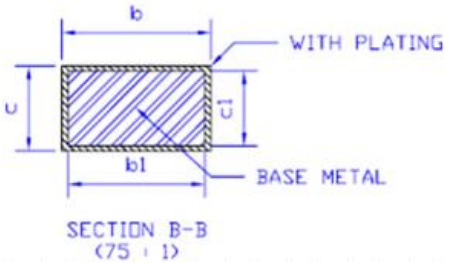


Figure 7.1 - GL850G-60 28 Pin SSOP Package

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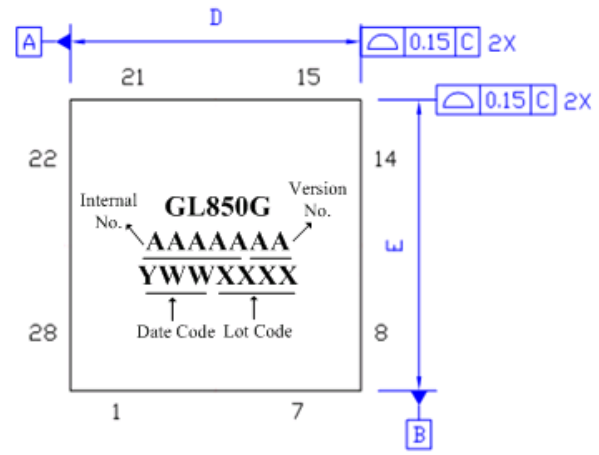
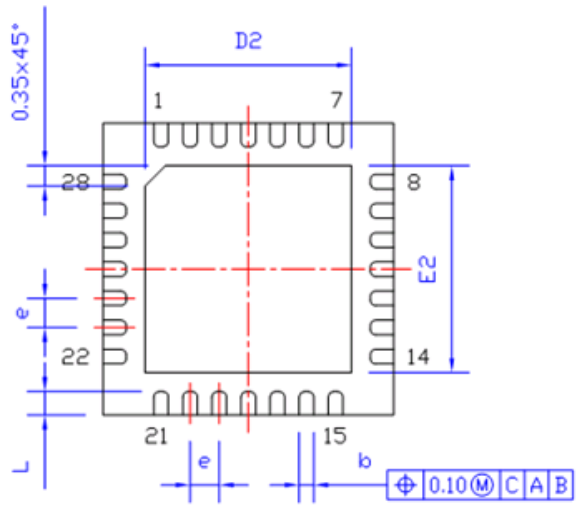


SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	0.70 (27.6)	0.75 (29.5)	0.80 (31.5)
A1	---	0.02 (0.8)	0.05 (2.0)
A3	0.203 (8.0) REF		
b	0.18 (7.1)	0.25 (9.8)	0.30 (11.8)
D	5.00 (196.9) BSC		
D2	3.40 (133.9)	3.55 (139.8)	3.70 (145.7)
E	5.00 (196.9) BSC		
E2	3.40 (133.9)	3.55 (139.8)	3.70 (145.7)
e	0.50 (19.7) BSC		
L	0.30 (11.8)	0.40 (15.7)	0.50 (19.7)

NOTE: 1. REFER TO JEDEC STD. MO-220
2. ALL DIMENSIONS IN MILLIMETERS.



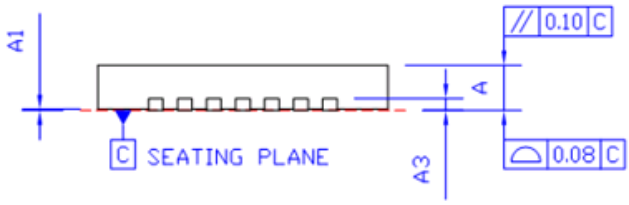


Figure 7.2 - GL850G-60 28 Pin QFN Package

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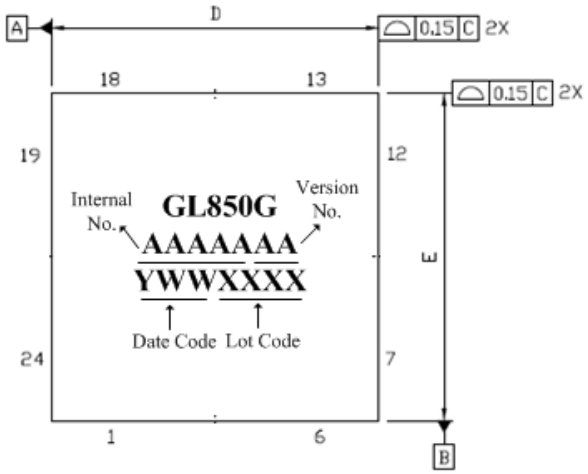

SYMBOL	DIMENSION MM (MIL)		
	MIN.	NOM.	MAX.
A	0.70 (27.6)	0.75 (29.5)	0.80 (31.5)
A1	---	0.02 (0.8)	0.05 (2.0)
A3	0.203 (8.0) REF		
b	0.18 (7.1)	0.25 (9.8)	0.30 (11.8)
D	4.00 (157.4) BSC		
D2	1.90 (74.8)	2.40 (94.5)	2.85 (112.2)
E	4.00 (157.4) BSC		
E2	1.90 (74.8)	2.40 (94.5)	2.85 (112.2)
e	0.50 (19.7) BSC		
L	0.30 (11.8)	0.40 (15.7)	0.50 (19.7)

NOTE: 1. REFER TO JEDEC STD. MO-220
2. ALL DIMENSIONS IN MILLIMETERS.

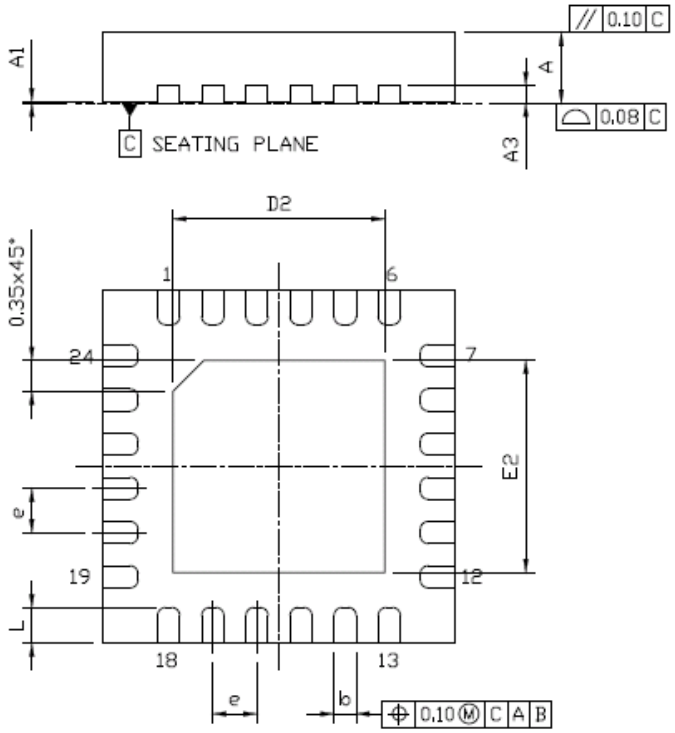

Figure 7.3 - GL850G-60 24 Pin QFN Package

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CHAPTER 8 ORDERING INFORMATION

Table 8.1 - Ordering Information

Part Number	Package	Package Type	Version	Status
GL850G-HHY60	SSOP 28	Green Package	60	Available
GL850G-OHY60	QFN 28	Green Package	60	Available
GL850G-OGY60	QFN 24	Green Package	60	Available

Note: The marking of "OHY" will not be shown on the IC due to QFN 28 package size limitation.

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