承認書

Specification Approval

CUSTOMER : DIVA Laboratories., Ltd.

BRAND:Nexperia

PART NO: 74LVC1G08GW

CUSTOMER PART NO: 3ALVC1G081Y

Checksum :

APPROVED BY: Edison Liu

DATE: 2025/7/16

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74LVC1G08

Single 2-input AND gate

Rev. 16.1 — 3 September 2024 Product data sheet

1. General description

The 74LVC1G08 is a single 2-input AND gate. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V applications.

Schmitt trigger action at all inputs makes the circuit tolerant of slower input rise and fall time.

This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- High noise immunity
- ±24 mA output drive (V_{CC} = 3.0 V)
- CMOS low power dissipation
- Direct interface with TTL levels
- Overvoltage tolerant inputs to 5.5 V
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance ≤ 250 mA
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8C (2.7 V to 3.6 V)
  - JESD36 (4.5 V to 5.5 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from −40 °C to +85 °C and −40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC1G08GW	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74LVC1G08GV	-40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	SOT753
74LVC1G08GM	-40 °C to +125 °C	XSON6	plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm	SOT886
74LVC1G08GN	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 0.9 × 1.0 × 0.35 mm	SOT1115
74LVC1G08GS	-40 °C to +125 °C	XSON6	extremely thin small outline package; no leads; 6 terminals; body 1.0 × 1.0 × 0.35 mm	SOT1202
74LVC1G08GX	-40 °C to +125 °C	X2SON5	plastic thermal enhanced extremely thin small outline package; no leads; 5 terminals; body 0.8 × 0.8 × 0.32 mm	SOT1226-3
74LVC1G08GZ	-40 °C to +125 °C	XSON5	plastic thermal enhanced extremely thin small outline package with side-wettable flanks (SWF); no leads; 5 terminals; body 1.1 × 0.85 × 0.5 mm	SOT8065-1

4. Marking

Table 2. Marking

Type number	Marking code [1]
74LVC1G08GW	VE
74LVC1G08GV	V08
74LVC1G08GM	VE
74LVC1G08GN	VE
74LVC1G08GS	VE
74LVC1G08GX	VE
74LVC1G08GZ	VE

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

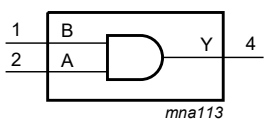

Fig. 1. Logic symbol



Fig. 2. IEC logic symbol

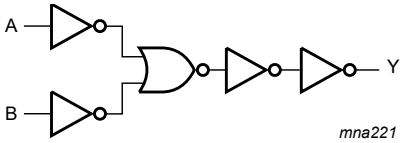

Fig. 3. Logic diagram

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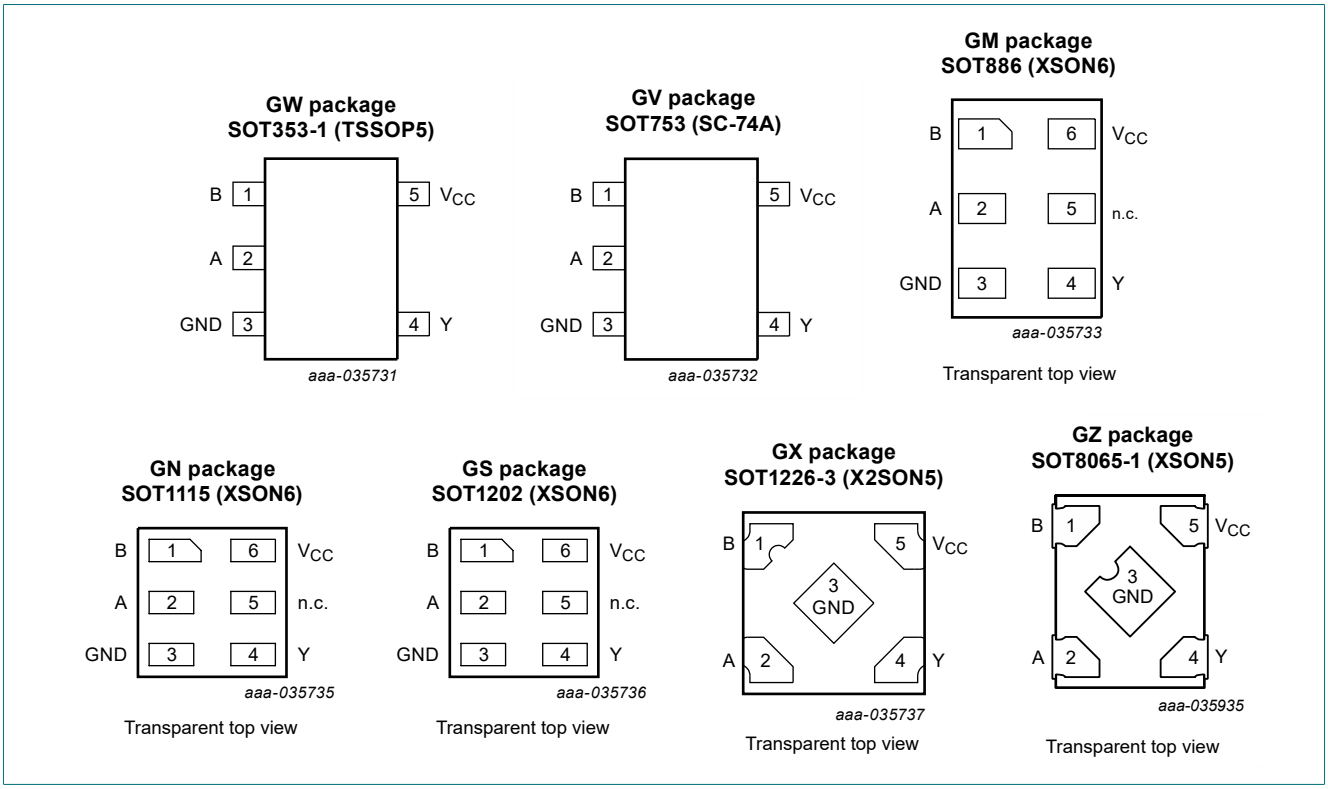
6. Pinning information

6.1. Pinning



6.2. Pin description

Table 3. Pin description

Symbol	Pin		Description
	TSSOP5, SC-74A , XSON5 and X2SON5	XSON6	
B	1	1	data input
A	2	2	data input
GND	3	3	ground (0 V)
Y	4	4	data output
n.c.	-	5	not connected
V_{CC}	5	6	supply voltage

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7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level.

Input		Output
A	**B**	**Y**
L	L	L
L	H	L
H	L	L
H	H	H

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V		-50	-	mA
V_I	input voltage		[1]	-0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage	Active mode	[1]	-0.5	V_{CC} + 0.5	V
		Power-down mode; V_{CC} = 0 V	[1]	-0.5	+6.5	V
I_O	output current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			-100	-	mA
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[2]	-	250	mW
T_{stg}	storage temperature			-65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT353-1 (TSSOP5) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.
For SOT753 (SC-74A) package: P_{tot} derates linearly with 3.8 mW/K above 85 °C.
For SOT886 (XSON6) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.
For SOT1115 (XSON6) package: P_{tot} derates linearly with 3.2 mW/K above 71 °C.
For SOT1202 (XSON6) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.
For SOT1226-3 (X2SON5) package: P_{tot} derates linearly with 3.0 mW/K above 67 °C.
For SOT8065-1 (XSON5) package: P_{tot} derates linearly with 3.2 mW/K above 72 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	5.5	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage	Active mode	0	-	V_{CC}	V
		Power-down mode; V_{CC} = 0 V	0	-	5.5	V
T_{amb}	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 1.65 V to 2.7 V	-	-	20	ns/V
		V_{CC} = 2.7 V to 5.5 V	-	-	10	ns/V

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10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.65 V to 1.95 V	0.65V_{CC}	-	-	0.65V_{CC}	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V_{CC} = 4.5 V to 5.5 V	0.7V_{CC}	-	-	0.7V_{CC}	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.65 V to 1.95 V	-	-	0.35V_{CC}	-	0.35V_{CC}	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V	-	-	0.3V_{CC}	-	0.3V_{CC}	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = -100 µA; V_{CC} = 1.65 V to 5.5 V	V_{CC} - 0.1	-	-	V_{CC} - 0.1	-	V
		I_O = -4 mA; V_{CC} = 1.65 V	1.2	-	-	0.95	-	V
		I_O = -8 mA; V_{CC} = 2.3 V	1.9	-	-	1.7	-	V
		I_O = -12 mA; V_{CC} = 2.7 V	2.2	-	-	1.9	-	V
		I_O = -24 mA; V_{CC} = 3.0 V	2.3	-	-	2.0	-	V
		I_O = -32 mA; V_{CC} = 4.5 V	3.8	-	-	3.4	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 100 µA; V_{CC} = 1.65 V to 5.5 V	-	-	0.10	-	0.10	V
		I_O = 4 mA; V_{CC} = 1.65 V	-	-	0.45	-	0.70	V
		I_O = 8 mA; V_{CC} = 2.3 V	-	-	0.30	-	0.45	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.40	-	0.60	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.55	-	0.80	V
		I_O = 32 mA; V_{CC} = 4.5 V	-	-	0.55	-	0.80	V
I_I	input leakage current	V_I = 5.5 V or GND; V_{CC} = 0 V to 5.5 V	-	±0.1	±1	-	±1	µA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O = 5.5 V	-	±0.1	±2	-	±2	µA
I_{CC}	supply current	V_I = 5.5 V or GND; I_O = 0 A; V_{CC} = 1.65 V to 5.5 V	-	0.1	4	-	4	µA
ΔI_{CC}	additional supply current	per pin; V_{CC} = 2.3 V to 5.5 V; V_I = V_{CC} - 0.6 V; I_O = 0 A	-	5	500	-	500	µA
C_I	input capacitance	V_{CC} = 3.3 V; V_I = GND to V_{CC}	-	5	-	-	-	pF

[1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

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11. Dynamic characteristics

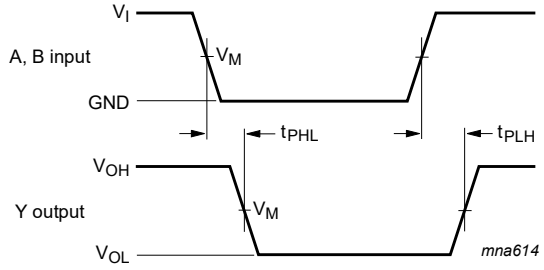
Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t_{pd}	propagation delay	A, B to Y; see Fig. 4 [2]						
		V_{CC} = 1.65 V to 1.95 V	1.0	3.4	8.0	1.0	10.5	ns
		V_{CC} = 2.3 V to 2.7 V	0.5	2.2	5.5	0.5	7.0	ns
		V_{CC} = 2.7 V	0.5	2.5	5.5	0.5	7.0	ns
		V_{CC} = 3.0 V to 3.6 V	0.5	2.1	4.5	0.5	6.0	ns
		V_{CC} = 4.5 V to 5.5 V	0.5	1.7	4.0	0.5	5.5	ns
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}; V_{CC} = 3.3 V [3]	-	16	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.
[2] t_{pd} is the same as t_{PLZ} and t_{PZL}.
[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11.1. Waveforms and test circuit



Measurement points are given in Table 9.
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 4. The input A, B to output Y propagation delays

Table 9. Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
1.65 V to 1.95 V	$0.5V_{CC}$	$0.5V_{CC}$
2.3 V to 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	$0.5V_{CC}$	$0.5V_{CC}$

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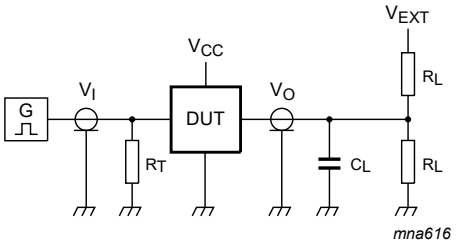

Test data is given in Table 10.

Definitions for test circuit:

R_L = Load resistance;

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator;

V_{EXT} = External voltage for measuring switching times.

Fig. 5. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load		V_{EXT}
V_{CC}	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}, t_{PHL}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 kΩ	open
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open

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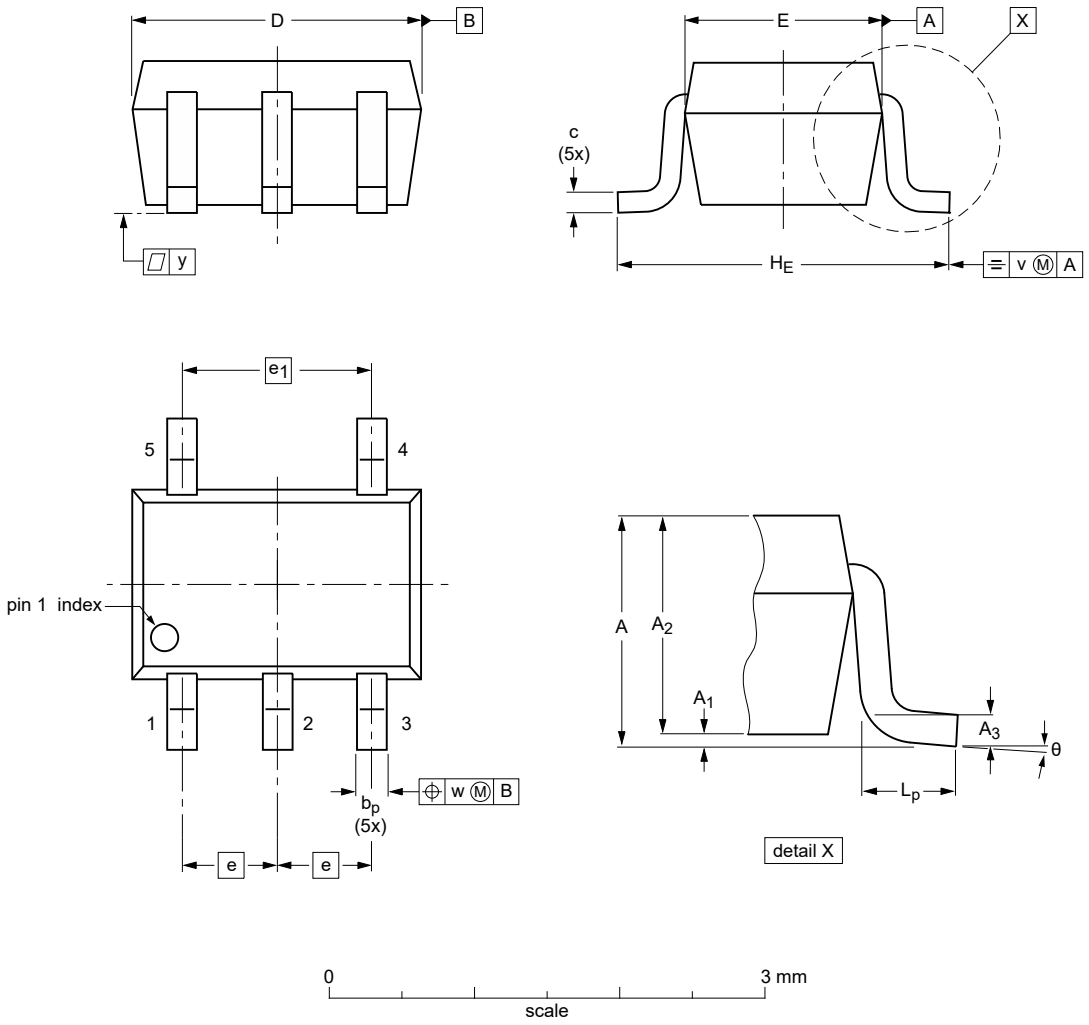
12. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm **SOT353-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	e_1	H_E	L_p	v	w	y	θ
mm	max	1.1	0.1	1.0	0.15	0.30	0.25	2.2	1.35	0.65	1.3	2.4	0.46	0.3	0.1	0.1	8°
	min	0.8	0	0.8		0.15	0.08	1.8	1.15			1.8	0.26				0°

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

sot353-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT353-1		MO-203	SC-88A			~~21-12-15~~ 21-12-16

Fig. 6. Package outline SOT353-1 (TSSOP5)

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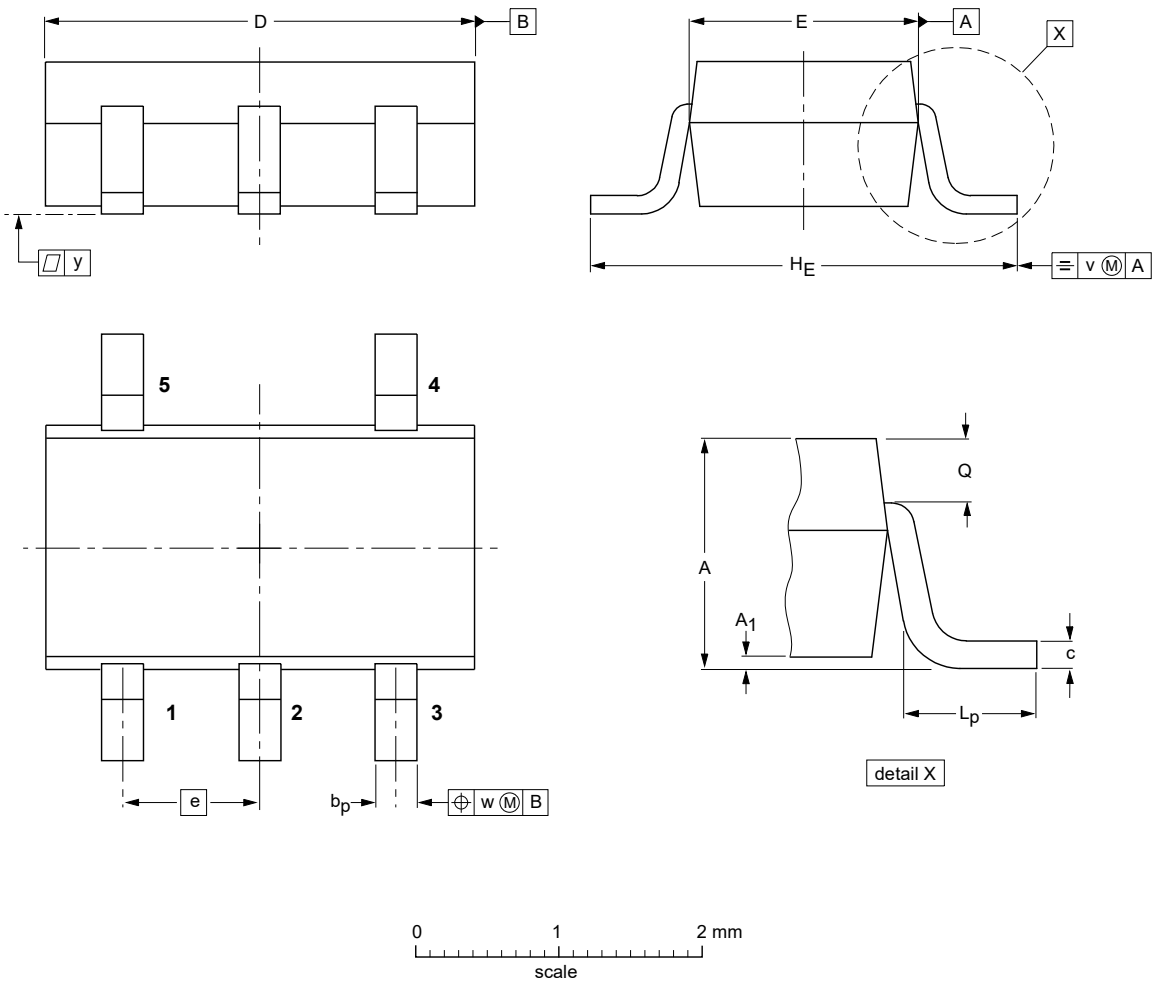
Plastic surface-mounted package; 5 leads **SOT753**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.100 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT753			SC-74A			~~02-04-16~~ 06-03-16

Fig. 7. Package outline SOT753 (SC-74A)

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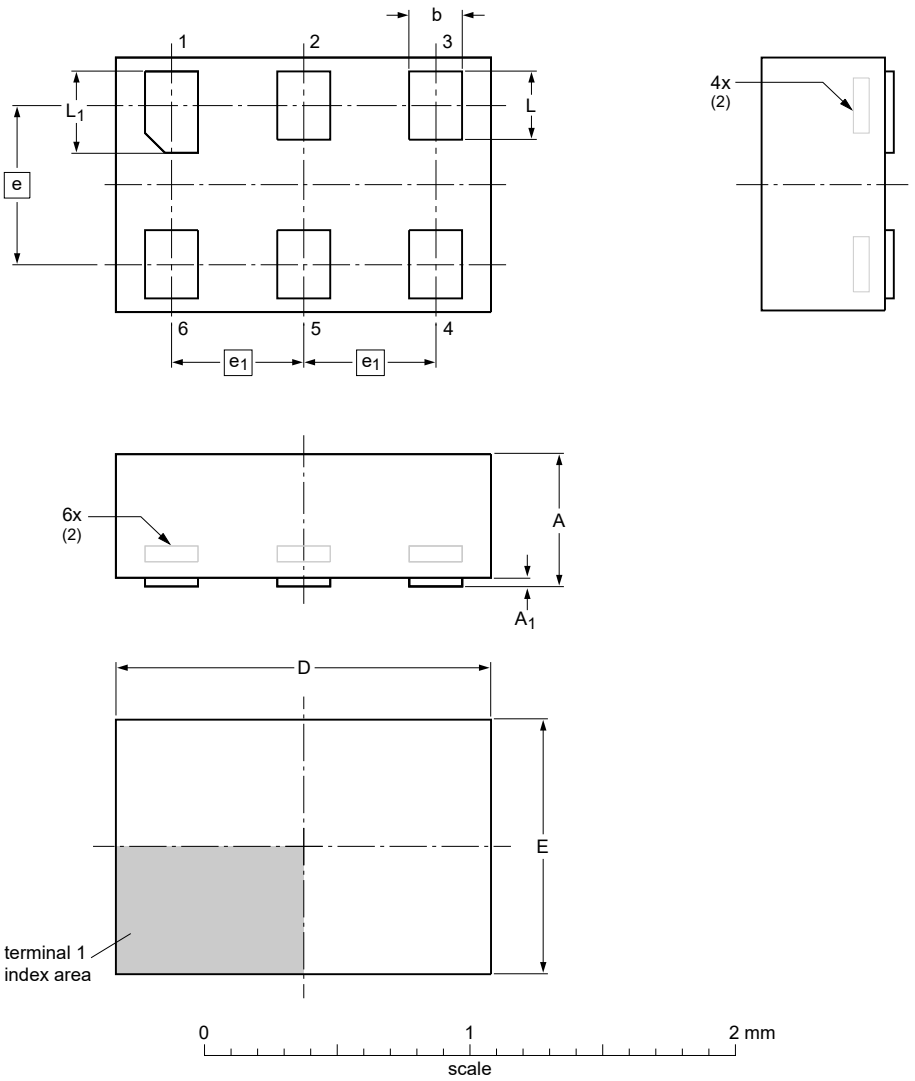
XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm SOT886



Dimensions (mm are the original dimensions)

Unit		A(1)	A_1	b	D	E	e	e_1	L	L_1
mm	max	0.5	0.04	0.25	1.50	1.05			0.35	0.40
	nom			0.20	1.45	1.00	0.6	0.5	0.30	0.35
	min			0.17	1.40	0.95			0.27	0.32

Notes
1. Including plating thickness.
2. Can be visible in some manufacturing processes.

sot886_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT886		MO-252				~~04-07-22~~ 12-01-05

Fig. 8. Package outline SOT886 (XSON6)

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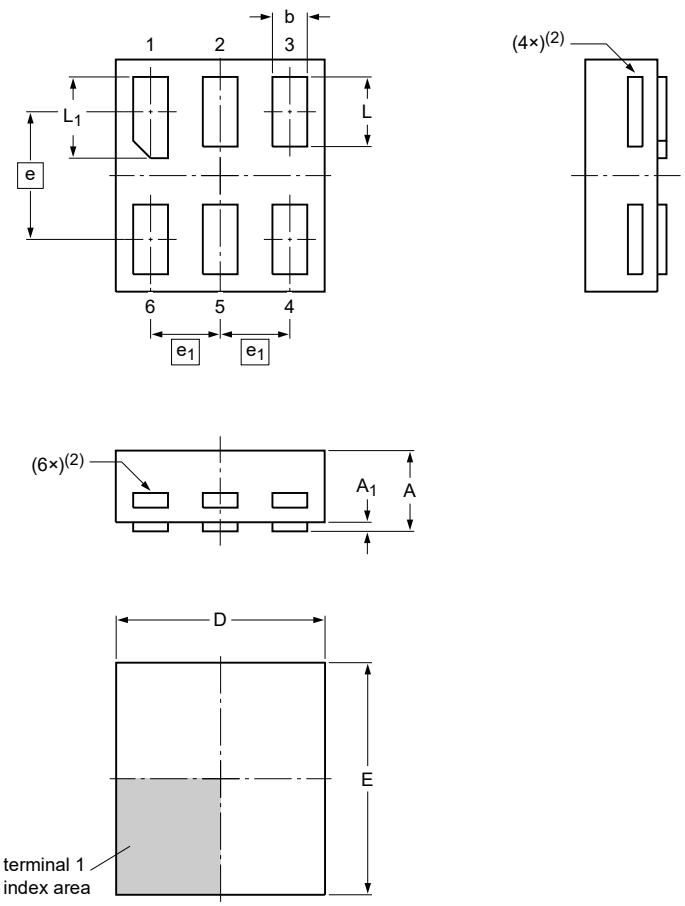
XSON6: extremely thin small outline package; no leads; 6 terminals; body 0.9 x 1.0 x 0.35 mm **SOT1115**



Dimensions

Unit		$A^{(1)}$	A_1	b	D	E	e	e_1	L	L_1
mm	max	0.35	0.04	0.20	0.95	1.05			0.35	0.40
	nom			0.15	0.90	1.00	0.55	0.3	0.30	0.35
	min			0.12	0.85	0.95			0.27	0.32

Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1115_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1115						~~10-04-02~~ 10-04-07

Fig. 9. Package outline SOT1115 (XSON6)

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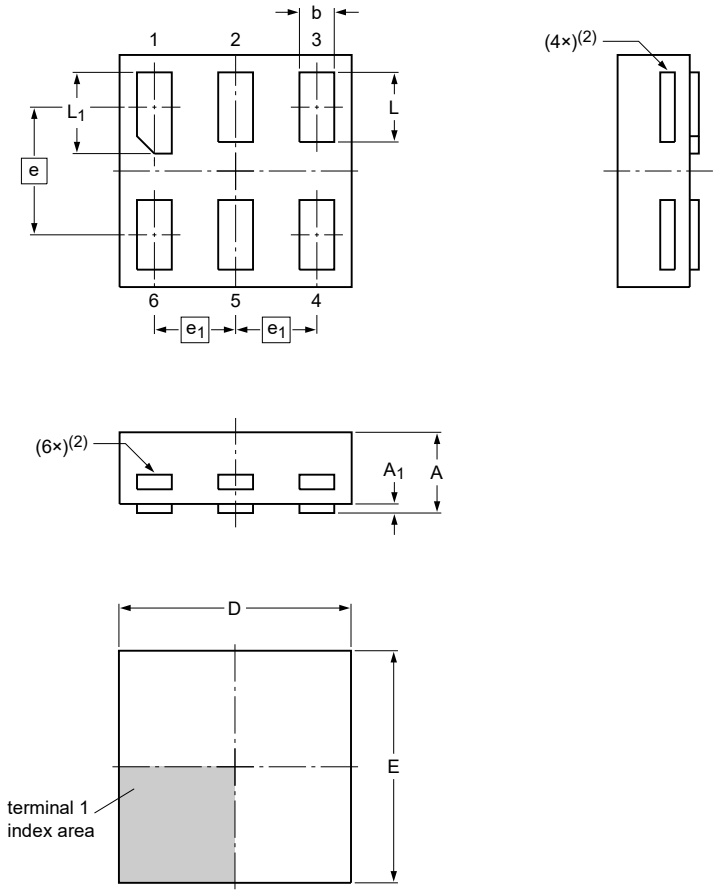
XSON6: extremely thin small outline package; no leads; 6 terminals; body 1.0 x 1.0 x 0.35 mm **SOT1202**



Dimensions

Unit		$A^{(1)}$	A_1	b	D	E	e	e_1	L	L_1
mm	max	0.35	0.04	0.20	1.05	1.05			0.35	0.40
	nom			0.15	1.00	1.00	0.55	0.35	0.30	0.35
	min			0.12	0.95	0.95			0.27	0.32

Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1202_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1202						~~10-04-02~~ 10-04-06

Fig. 10. Package outline SOT1202 (XSON6)

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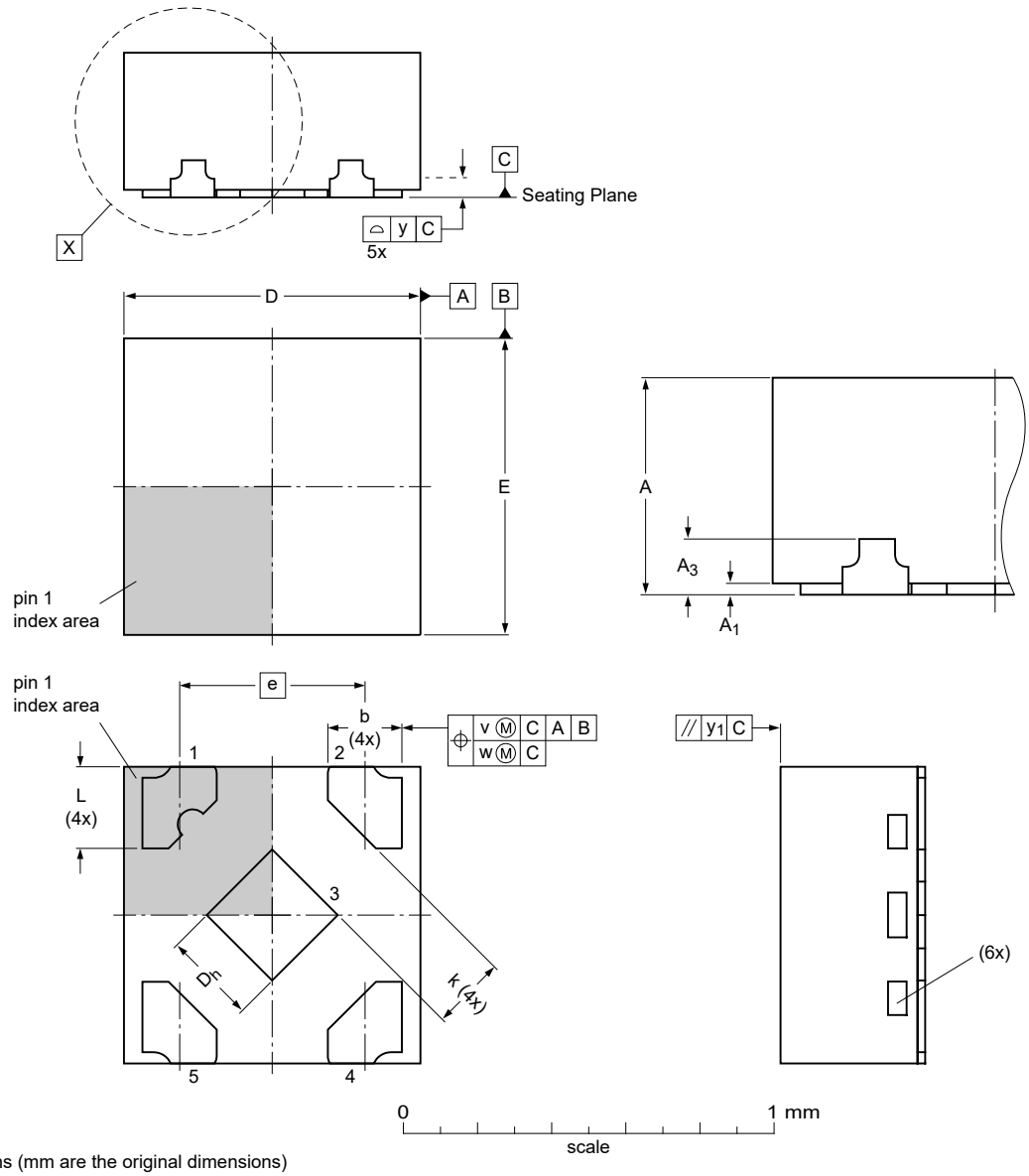
X2SON5: plastic thermal enhanced extremely thin small outline package; no leads; 5 terminals; body 0.8 x 0.8 x 0.32 mm **SOT1226-3**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_3	D	D_h	E	b	e	K	L	v	w	y	y_1
mm	max	0.35	0.04	0.10 (Typ.)	0.85	0.30	0.85	0.25	0.50		0.27	0.1	0.05	0.05	0.05
	nom	0.32	0.02		0.80	0.25	0.80	0.20			0.22				
	min	0.30	0.00		0.75	0.20	0.75	0.15		0.20	0.17				

sot1226-3_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	EIAJ			
SOT1226-3		---				~~19-11-06~~ 19-11-07

Fig. 11. Package outline SOT1226-3 (X2SON5)

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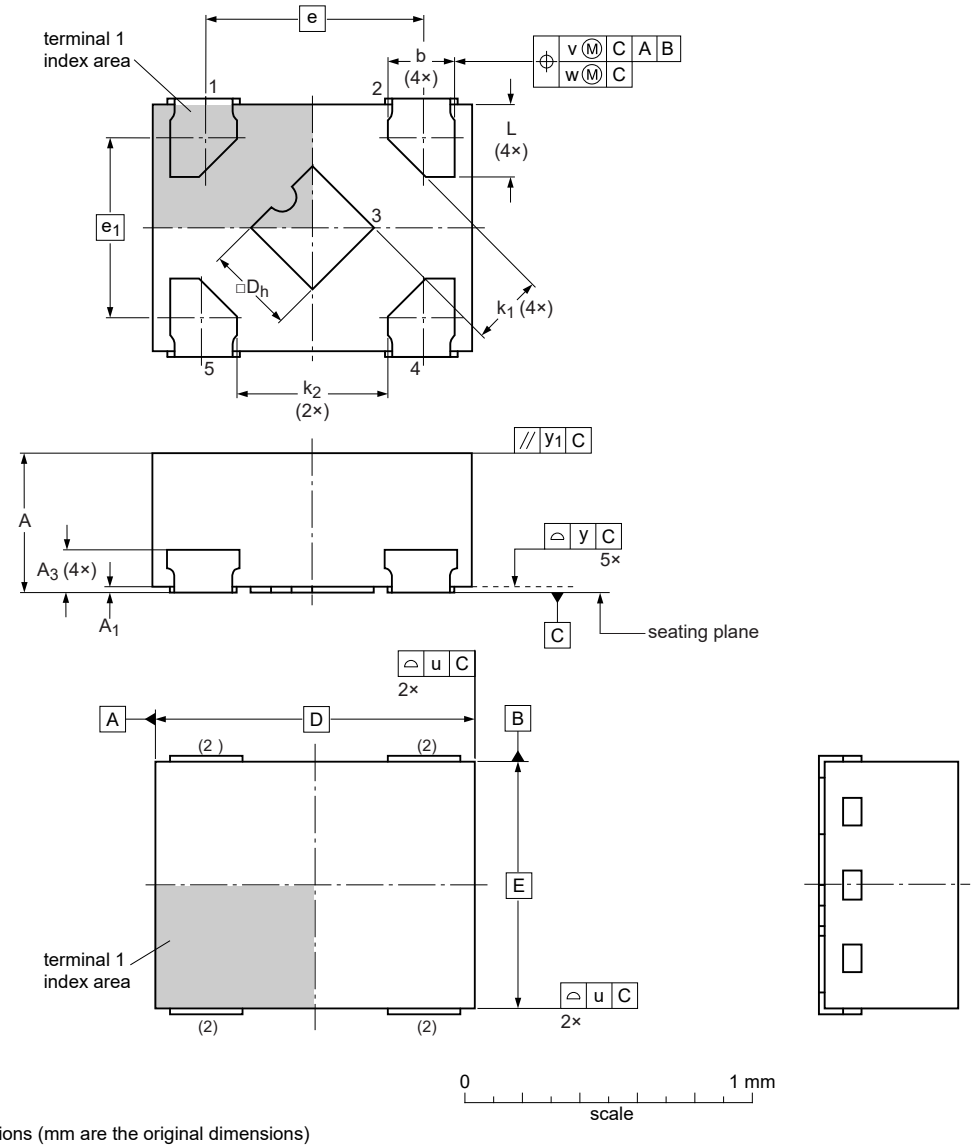
XSON5: Plastic thermal enhanced extremely thin small outline package with side-wettable flanks (SWF); no leads; 5 terminals; body 1.1 × 0.85 × 0.5 mm

SOT8065-1



Dimensions (mm are the original dimensions)

Unit		$A^{(1)}$	A_1	A_3	b	D[1]	D_h	E[1]	e	e_1	k_1	k_2	L	u	v	w	y	y_1
mm	max	0.50	0.040	0.135 (typ)	0.28	1.10	0.35	0.85	0.75	0.6		0.45	0.30	0.05	0.1	0.05	0.05	0.05
	nom	0.47	0.020		0.23		0.30				0.2		0.25					
	min	0.44	0.005		0.20		0.27						0.22					

Note:
1. Plastic or metal protrusions per side are not included.
2. Side wettable flanks (SWF), protrusion max. 0.02 mm.

sot8065-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8065-1		MO-340				~~24-07-09~~ 24-08-27

Fig. 12. Package outline SOT8065-1 (XSON5)

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13. Abbreviations

Table 11. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC1G08 v.16.1	20240903	Product data sheet	-	74LVC1G08 v.16
Modifications:	• Fig. 12: Added JEDEC reference MO-340 to SOT8065-1 package outline drawing.			
74LVC1G08 v.16	20240711	Product data sheet	-	74LVC1G08 v.15
Modifications:	• Type number 74LVC1G08GZ (SOT8065-1/XSON5) added. • Type number 74LVC1G08GF (SOT891/XSON6) removed.			
74LVC1G08 v.15	20230804	Product data sheet	-	74LVC1G08 v.14
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard.			
74LVC1G08 v.14	20220224	Product data sheet	-	74LVC1G08 v.13
Modifications:	• Package SOT1226 (X2SON5) changed to SOT1226-3 (X2SON5).			
74LVC1G08 v.13	20220209	Product data sheet	-	74LVC1G08 v.12
Modifications:	• Section 1 and Section 2 updated. • Table 5: Derating values for P_{tot} total power dissipation updated. • Fig. 6: Package outline drawing for SOT353-1 (TSSOP5) has changed.			
74LVC1G08 v.12	20180116	Product data sheet	-	74LVC1G08 v.11
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Pin configuration drawing of SOT1226 modified.			
74LVC1G08 v.11	20161128	Product data sheet	-	74LVC1G08 v.10
Modifications:	• Table 7: The maximum limits for leakage current and supply current have changed.			
74LVC1G08 v.10	20120629	Product data sheet	-	74LVC1G08 v.9
Modifications:	• Added type number 74LVC1G08GX (SOT1226) • Package outline drawing of SOT886 (Fig. 8) modified.			
74LVC1G08 v.9	20111209	Product data sheet	-	74LVC1G08 v.8
Modifications:	• Legal pages updated.			
74LVC1G08 v.8	20101019	Product data sheet	-	74LVC1G08 v.7

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15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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Date of release: 3 September 2024

Full Material Declaration for 74LVC1G08GW

Date	2025-07-08 09:32:49 CEST+0200
Package	SOT353-1 (UMT5): 0.9 mm × 1.25 mm × 2.1 mm
Description	Single 2-input AND gate
Datasheet	https://assets.nexperia.com/documents/data-sheet/74LVC1G08.pdf
OPNs	935268380125: 74LVC1G08GW,125 (RFS), MSL 1
Automotive-qualified	No
UL-94	https://iq.ulprospector.com/en/profile?e=558010



REACH	Compliant with Regulation 1907/2006/EC (REACH). Does not contain REACH SVHC substances exceeding 1000 ppm of the article.
EU RoHS	Compliant with Directive 2011/65/EU, amended by Directive 2015/863/EU, on the restriction of the use of certain hazardous substances in electrical and electronic equipment ('RoHS 2 amended') without exemptions.
CN RoHS	Compliant with Chinese ACPEIP (Administration on the Control of Pollution Caused by Electronic Information Products) (CN RoHS) without exemptions.
ELV	Compliant with Directive 2000/53/EC, amended by Directive 2023/533, on end of life vehicles (ELV) without exemptions.
PFAS	Does not contain any intentionally added per- and polyfluoroalkyl substances (PFAS).
CA Proposition 65	Contains California Proposition 65 substance(s) [at the article level]: substance 7439-92-1: 38 ppm; substance 1333-86-4: 1420 ppm;
IEC 62474	Contains IEC 62474 substance(s) [at the article level]: substance 7439-92-1: 38 ppm; substance 1333-86-4: 1420 ppm;
Precious Metals	Contains precious metals [Ag, Au, Pd, Pt; at the article level]: substance 7440-22-4: 3761 ppm;
GADSL	Contains 'Global Automotive Declarable Substances List' (GADSL) substances: substance 7440-22-4: 3761 ppm; substance 7440-50-8: 351794 ppm; substance 7439-92-1: 39 ppm;
RHF Indicator	D: Lead-free and halogen-free according to Nexperia's halogen-free definition.

Material	Mat. Group	Substance	CAS No.	Mass / mg	Mass-% of Material	Mass-% of Part
Adhesive	Filler	Silver (Ag)	7440-22-4	0.007776	80.000000	0.142118
Adhesive	Polymer	Resin system		0.001944	20.000000	0.035529
		Adhesive Total		**0.009720**	**100.000000**	**0.177647**
Die	Doped silicon	Silicon (Si)	7440-21-3	0.054704	100.000000	0.999795
		Die Total		**0.054704**	**100.000000**	**0.999795**
Lead Frame	Copper alloy	Copper (Cu)	7440-50-8	1.907748	96.840000	34.866868
Lead Frame	Copper alloy	Iron (Fe)	7439-89-6	0.045507	2.310000	0.831707
Lead Frame	Copper alloy	Zinc (Zn)	7440-66-6	0.002364	0.120000	0.043206
Lead Frame	Copper alloy	Phosphorus (P)	7723-14-0	0.001379	0.070000	0.025203
Lead Frame	Copper alloy	Lead (Pb)	7439-92-1	0.000197	0.010000	0.003600
		Base Alloy Total		*1.957195*	*99.350000*	*35.770584*
Lead Frame	Pure metal layer	Silver (Ag)	7440-22-4	0.012805	0.650000	0.234030
		Pre-Plating Total		*0.012805*	*0.650000*	*0.234030*
		Lead Frame Total		**1.970000**	**100.000000**	**36.004614**
Mould Compound	Filler	Silica fused	60676-86-0	1.363424	43.840000	24.918556
Mould Compound	Filler	Silica	7631-86-9	1.090677	35.070000	19.933708
Mould Compound	Polymer	o-Cresol-epichlorohydrin-formaldehyde copolymer	29690-82-2	0.311000	10.000000	5.683977
Mould Compound	Polymer	Formaldehyde-phenol copolymer	9003-35-4	0.309134	9.940000	5.649873
Mould Compound	Polymer	Polyethylene (PE) -wax-	9002-88-4	0.027990	0.900000	0.511558
Mould Compound	Pigment	Carbon black	1333-86-4	0.007775	0.250000	0.142099

Material	Mat. Group	Substance	CAS No.	Mass / mg	Mass-% of Material	Mass-% of Part
		Mould Compound Total		**3.110000**	**100.000000**	**56.839771**
Post-Plating	Tin solder	Tin (Sn)	7440-31-5	0.309969	99.990000	5.665134
Post-Plating	Impurity	Lead (Pb)	7439-92-1	0.000016	0.005000	0.000292
Post-Plating	Impurity	Antimony (Sb)	7440-36-0	0.000009	0.003000	0.000165
Post-Plating	Impurity	Bismuth (Bi)	7440-69-9	0.000003	0.001000	0.000055
Post-Plating	Impurity	Copper (Cu)	7440-50-8	0.000003	0.001000	0.000055
		Post-Plating Total		**0.310000**	**100.000000**	**5.665701**
Wire	Pure metal	Copper (Cu)	7440-50-8	0.017095	99.990000	0.312436
Wire	Impurity	Non-declarable		0.000002	0.010000	0.000036
		Wire Total		**0.017097**	**100.000000**	**0.312472**
		74LVC1G08GW Total		**5.471521**	**100.000000**	**100.000000**

部件名称 Material	有毒或有害物质和元素 (Toxic or hazardous substances and elements)					
	铅 (Pb)	镉 (Cd)	汞 (Hg)	六价铬 (Cr^{6+})	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
胶黏剂 (Adhesive)	○	○	○	○	○	○
半导体芯片 (Die)	○	○	○	○	○	○
基底合金 (Base Alloy)	○	○	○	○	○	○
预镀层 (Pre-Plating)	○	○	○	○	○	○
模封料 (Mould Compound)	○	○	○	○	○	○
后镀层 (Post-Plating)	○	○	○	○	○	○
导线 (Wire)	○	○	○	○	○	○

○ 表示该有害物质在该部件所有均质材料中的含量均在 GB/T 26572 规定的限量要求以下
Indicates that said hazardous substance contained in all of the homogeneous materials for this part is below the limit requirement of GB/T 26572.

× 表示该有害物质至少在该部件的某一均质材料中的含量超出 GB/T 26572 规定的限量要求
Indicates that said hazardous substance contained in at least one of the homogeneous materials used for this part is above the limit requirement of GB/T 26572.

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