

設計驗證
工程課
2026 -01- 20
發行

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承　認　書

SAMPLE　SPECIFICATION　REPORT

送 樣 廠 商 / VENDER　：　全 科 科 技 股 份 有 限 公 司

品　　名 / PART NAME　：　MT5080
Asynchronous Step-Up DC/DC Converter
with 50V 1A Integrated Switch

型　　號 / TYPE　：　MT5080NSBR

料　　號 / PART NO.　：　3AMT508001Y(A0573)

適 用 模 型 / MODEL NO.　：

申 請 單 編 號:

備　　註:　Sales: 葉源順 Ben Yeh　2026/1/16

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承 認 客 戶: 鈺緯科技開發股份有限公司
承 認 單 位:

研 究 開 發 部 R & D	品 保 工 程 師 Q A
設計驗證 工程課 2026 -01- 20 發行 鈺緯科技開發股份有限公司	

Asynchronous Step-Up DC/DC Converter with 50V 1A Integrated Switch

Description

The MT5080 is a current mode step-up converter operating at a fixed frequency of 1.5MHz. It can be configured as a boost, SEPIC or inverting converter consuming as low as 100μA of quiescent current. The internally compensated current mode architecture results in stable operation over a wide range of input and output voltages.

The 50V 1A internal switch makes the part perfect for boosting to voltages of 12V or greater. The MT5080 has a logic-level shutdown pin be used to reduce quiescent current and extend battery life. Protection is provided through cycle-by-cycle current limiting and thermal shutdown. The MT5080 is available in a low profile 5 leads SOT23 and 6 leads DFN 2mmx2mm package.

Features

- 2.7V to 6V Input Voltage Range
- +/-2% 1.25V Feedback Voltage Accuracy
- Output Voltage Up to 50V
- High Efficiency up to 92%
- Built it 1A 50V 280mΩ Power Switch
- 1.5MHz Constant Frequency Operation
- Internal Compensation and Soft-Start
- Thermal Shutdown
- Input Under-Voltage Lockout (UVLO)
- < 0.1μA Shutdown Current
- Available in Low Profile SOT23_5L and DFN2x2_6L Packages
- RoHS Compliant (100% Green available)

Applications

- Boost Conversions from 3.3V, 5V and 12V Rails
- ADP Bias for GPON and EPON
- Telecom
- Portable Instruments

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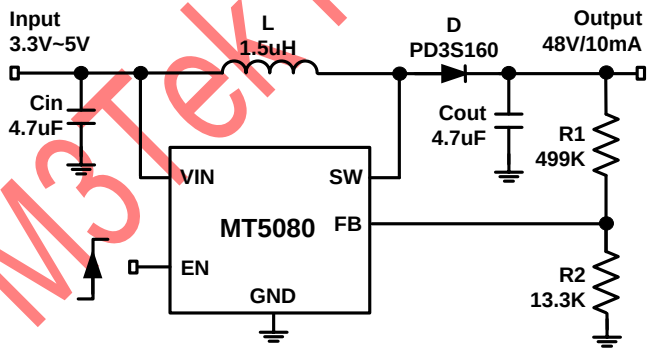
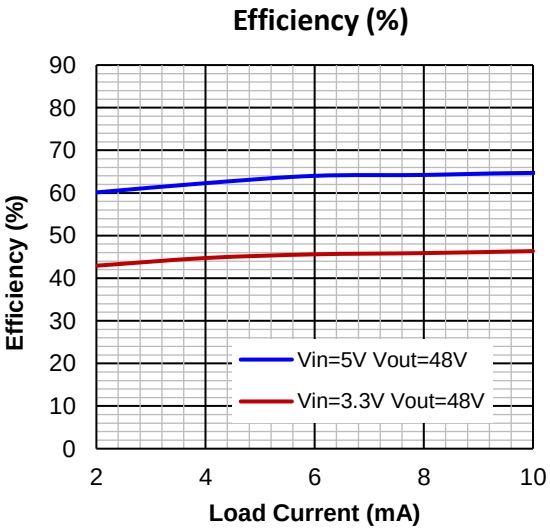
Typical Applications



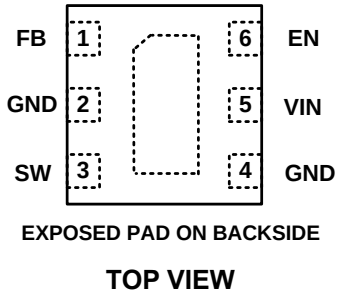


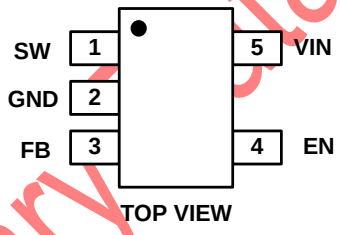
Ordering Information

Part No.	Marking	Temp. Range	Package	MOQ
MT5080NSBR	5080 YWWxx	-40°C ~+85°C	SOT23_5L	3000/Tape & Reel
MT5080NDER	5080 YWxx	-40°C ~+85°C	DFN2x2_6L	3000/Tape & Reel

Note: Y:Year, WW:Week, xx:Manufacture Code

Pin Configuration





Pin Description

SOT23_5L Pin No.	DFN2x2_6L Pin No.	Symbol	Description
1	3	SW	Power Switch Output. Minimize the metal trace area connected to this pin to reduce EMI.
2	2, 4	GND	Ground connection. The ground plane should be connected to large copper layers to spread heat dissipated by the MT5080.
3	1	FB	Voltage Regulation Feedback Pin. Connect this pin to a resistor divider between the output and GND.
4	6	EN	Regulator Enable Control Input. The MT5080 is shut down when this pin is low and active when this pin is high. If shutdown feature is not required, connect this pin to system input supply.
5	5	VIN	Input Supply. This pin must be locally bypassed. Be sure to place the positive terminal of the input capacitor as close as possible to the VIN pin, and the negative terminal as close as possible to the GND pin.

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Absolute Maximum Rating (Reference to GND) (Note 1)

Input Supply Voltage VIN ..... -0.3V to +6.5V
EN, FB Voltage ..... -0.3V to +6.5V
SW Voltage ..... -0.3V to +52V
SW Peak Current 2.5A
Junction Temperature Range ..... -20°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +260°C
ESD Classification ..... Class 2

Recommend Operating Conditions (Note 2)

Input Voltage (V_{IN}) ..... +2.7V to +6V
Operating Temperature Range ..... -40°C to +85°C

Thermal information (Note 3,4)

Maximum Power Dissipation (T_A=+25°C)
SOT23_5L 0.57W
DFN2x2_6L 1.3W
Thermal Resistance (θ_{JA}) SOT235 ..... 210°C/W
Thermal Resistance (θ_{JC}) SOT235 ..... 100°C/W
Thermal Resistance (θ_{JA}) DFN2x2 ..... 75°C/W
Thermal Resistance (θ_{JC}) DFN2x2 ..... 20°C/W

Note(1): Stress exceeding those listed "Absolute Maximum Ratings" may damage the device.
Note(2): The device is not guaranteed to function outside of the recommended operating conditions.
Note(3): Measured on JESD51-7, 4-Layer PCB.
Note(4): The maximum allowable power dissipation is a function of the maximum junction temperature T_{J_MAX}, the junction to ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_{D_MAX}= (T_{J_MAX}-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.

Electrical Characteristics

Recommended Operating Conditions; unless otherwise noted; V_{IN} = 3.3V, V_{OUT} = 12V; T_A = +25℃

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Voltage	V_{IN}		2.7		6	V
Output Voltage	V_{OUT}		3		50	V
Feedback Current	I_{VFB}		-100		100	nA
Feedback Voltage	V_{FB}		1.225	1.250	1.275	V
Shutdown Current	I_{SD}	V_{EN} = 0V		0.001	1	μA
Quiescent Current	I_Q	V_{FB} = 1.31V, No switching		100	160	μA
SW Leakage Current	I_{LEAK}	V_{EN} = 0V, V_{SW} = 50V	-2	0.1	2	μA
SW On Resistance	R_{DSON}	I_{SW} = 100mA		0.28		Ω
SW Current Limit	I_{PEAK}		1	1.45		A
Oscillator Frequency	f_{OSC}		1.2	1.5	1.8	MHz
Minimum Duty Cycle	D_{MIN}			15		%
Maximum Duty Cycle	D_{MAX}			88		%
Thermal Shutdown Temperature	T_{SD}			150		℃
EN Logic High Level	V_{ENH}		1.6			V
EN Logic Low Level	V_{ENL}				0.3	V
EN Input Current	I_{EN}	V_{EN} = 0V to 5.5V	-1		1	μA
Under Voltage Lockout	ULVO	V_{IN} Rising	2.85			V
Under Voltage Lockout		V_{IN} Falling			2.3	V

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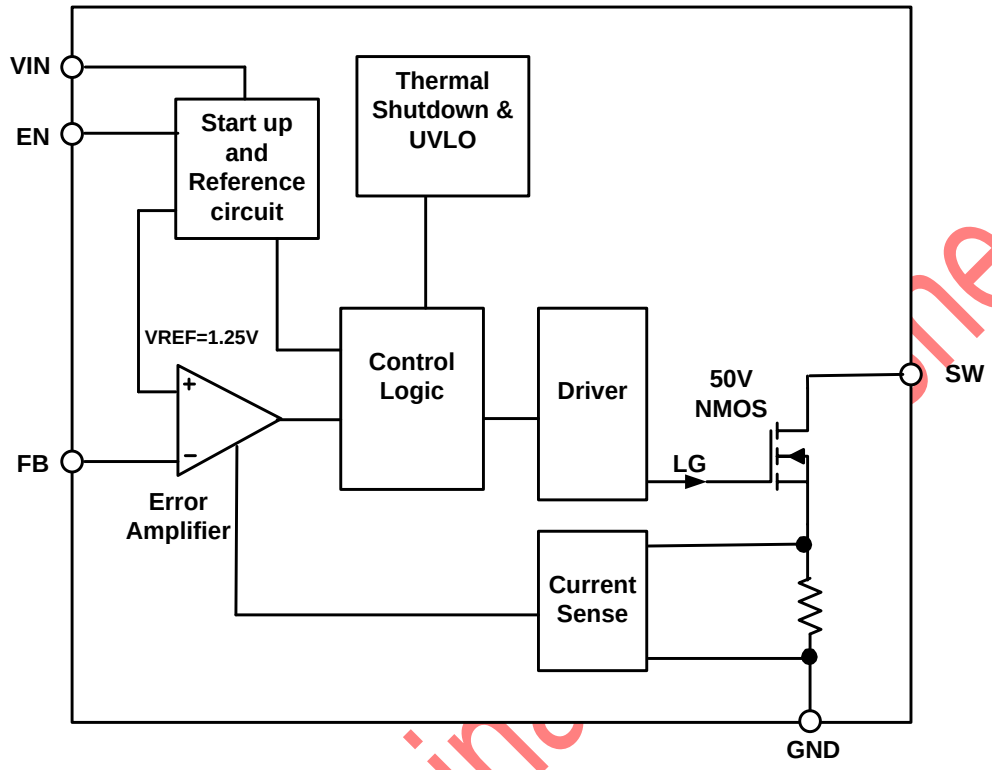
Functional Block Diagram



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TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=3.3V-5V, C_{IN}=4.7μF, C_{OUT}=4.7μF, L=1.5μH, T_A=+25℃

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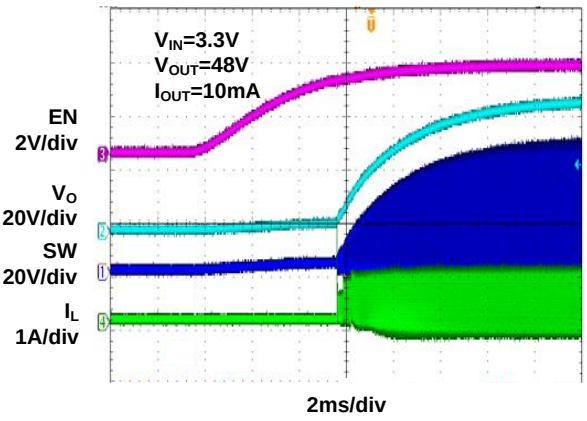

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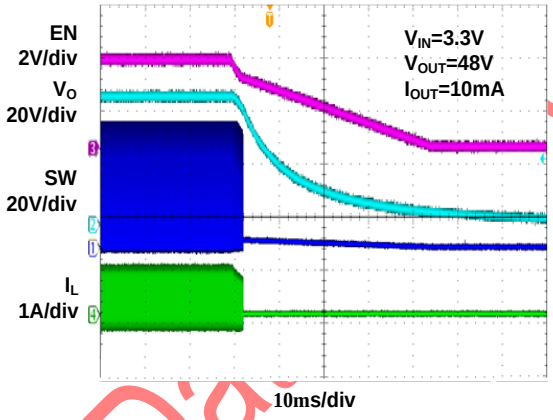

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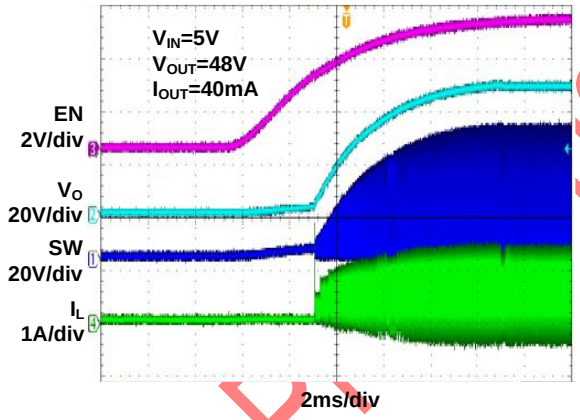

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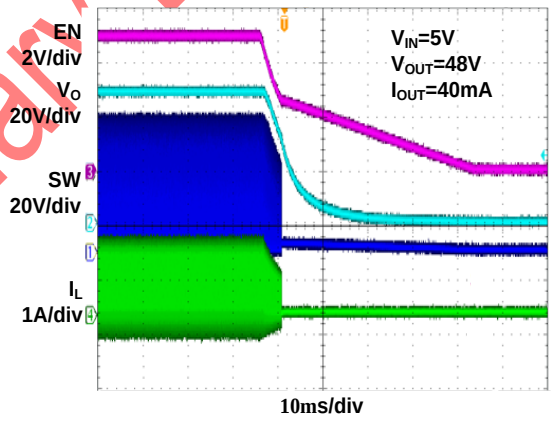
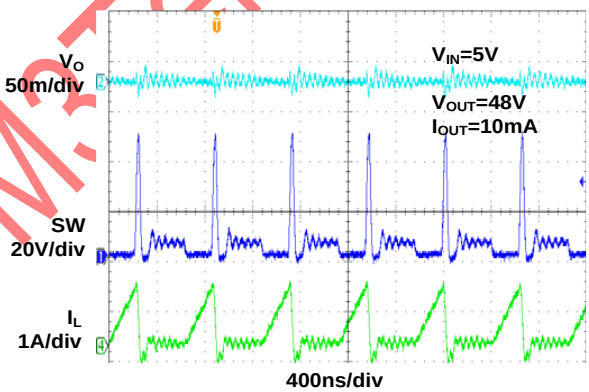


Steady State Test



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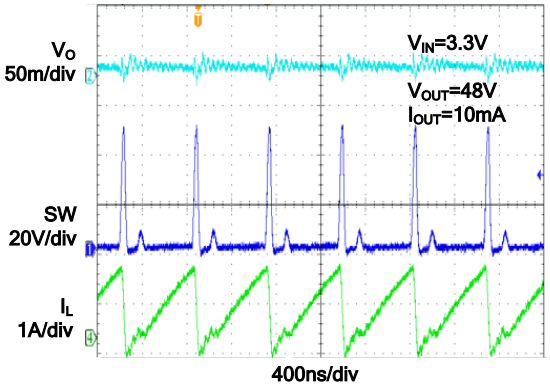
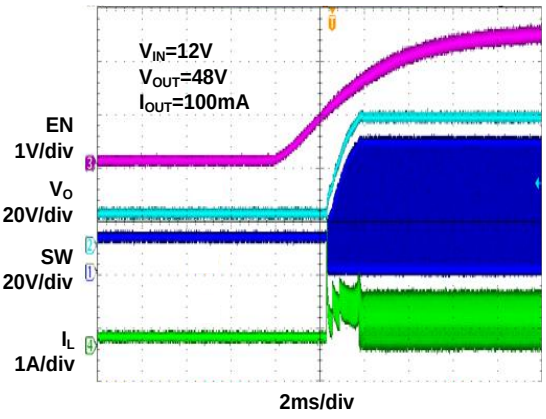


TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN}=12V, C_{IN}=4.7μF, C_{OUT}=10μF, L=10μH, T_A=+25℃

Enable On

Vin=12V, Vout=48V, Iout=100mA



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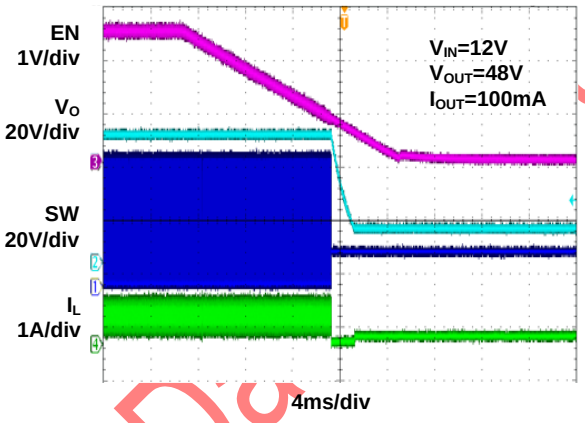
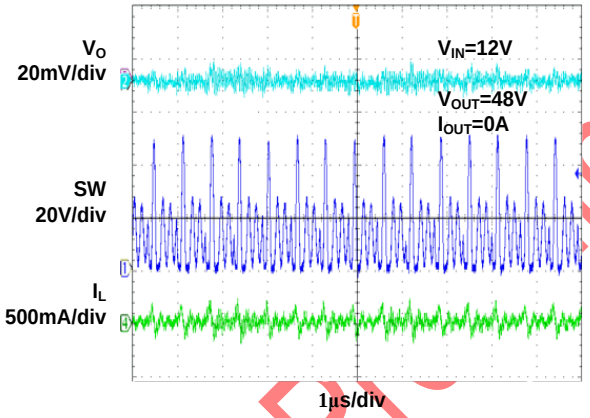
Vin=12V, Vout=48V, Iout=100mA





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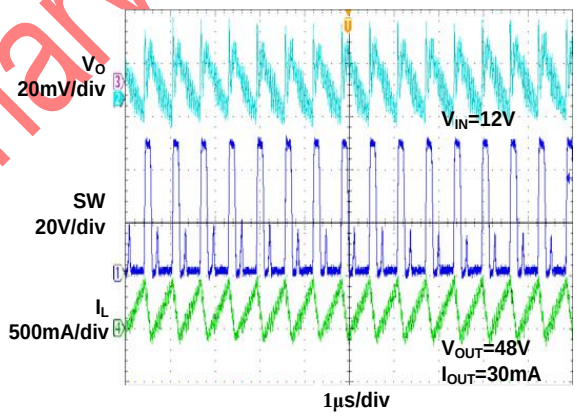

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Theory of Operation

The MT5080 is a switching converter IC that operates at a fixed frequency 1.5MHz using slope compensated current-mode control for fast transient response over a wide input voltage range and incorporates cycle-by-cycle current limiting protection. The PWM comparator modulates the power transferred to the load by changing the inductor peak current based on the feedback error voltage during each cycle. The main switch is turned on for a certain time to ramp the inductor current at each rising edge of the internal oscillator under normal operation whereas off when the peak inductor current is above the error voltage.

Application Information

Input and Output Capacitor Selection

For the most optimized application of MT5080, 4.7uF of the input ceramic capacitor and 4.7μF~10μF of output ceramic capacitor are recommended. Additionally, ceramic capacitors with low ESR are recommended for better voltage filtering. Regarding the ceramic type, multi-layer ceramic (MLC) type such as X5R or X7R is recommended to ensure good capacitance stability over the full operating temperature range. Ceramic capacitors have excellent low ESR characteristics but can have a DC Bias effect, which will have a strong influence on the final effective capacitance. Capacitance deratings for aging, temperature and dc bias increase the minimum value required. The voltage rating must be greater than the output voltage with some tolerance for output voltage ripple and overshoot in transient conditions. For this example 10μF, 25 V ceramic capacitors with 5 mΩ of ESR are used. The 40% derated capacitance is 6μF, approximately equal to the calculated minimum.

Inductor Selection

For the value of the inductor to achieve the most optimized application, it is recommended to select that ranging from 1uH to 10uH. The small size as well as better efficiency are the main concern for portable devices such as mobile phones. Therefore, low core loss at 1.5MHz and low DCR are required for the inductor to have better efficiency. Besides, the inductor saturation current rating should be considered to cover the inductor peak current.
If the boost converter remains in the discontinuous mode of operation, then the approximate peak inductor current, I_{LPEAK} (A), is represented by the formula below:

$$I_{LPEK} = \sqrt{\frac{2 \cdot T_S \cdot (V_{OUT} - V_{IN_MIN}) \cdot I_{OUT_MAX}}{\eta \cdot L}}$$

Use the following formula to calculate the lower bound of the inductor value at different output voltages and output currents. This is the minimum inductance value for discontinuous mode operation:

$$L_{MIN} = \frac{2 \cdot T_S \cdot I_{OUT} \cdot (V_{OUT} - V_{IN_MIN})}{\eta \cdot I^2_{PEAK_SW}}$$

Calculate the optimum value of $L_{OPTIMUM}$ to ensure the full output power without reaching the boundary between continuous-conduction mode (CCM) and discontinuous-conduction mode (DCM) using the following formula:

$$L_{MAX} = \frac{V^2_{IN_MIN} \cdot T_S \cdot \eta \cdot (V_{OUT} - V_{IN_MIN})}{2 \cdot V^2_{OUT} \cdot I_{OUT}}, \quad L_{OPTIMUM} = \frac{L_{MAX}}{2.25}$$

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where T_S (μsec) is the switching period in microseconds, V_{OUT} (V) is the output voltage, V_{IN_MIN} (V) is the minimum input voltage, I_{OUT_MAX} (A) is the maximum output current, I_{PEAK_SW} (A) is the peak switch current, L (μH) is the inductor value, and η is the efficiency of the boost converter.

Diode Selection

To get better efficiency, a Schottky diode is recommended to use with MT5080 because of its low forward voltage drop and fast reverse recovery. The high speed rectification is also a good characteristic of it for the high switching frequency. The current rating of the diode must meet the root mean square of the peak current and output average current multiplication as the following:

$$I_{D_RMS} \approx (I_{OUT} \times I_{PEAK})$$

The diode's reverse breakdown voltage should be larger than the output voltage. 40V rated Schottky diodes are recommended for outputs less than 30V, while 60V rated Schottky diodes are recommended for outputs greater than 35V.

Setting The Output Voltage

The output voltage is set using the FB pin and a resistor divider connected to the output as shown in Figure 1. The output voltage (V_{OUT}) can be calculated according to the voltage of the FB pin (V_{FB}) and ratio of the feedback resistors by the following equation, where (V_{FB}) is 1.25V (Typical):

$$V_{FB} = V_{OUT} \cdot (\frac{R_2}{R_1 + R_2})$$

Thus the output voltage is:

$$V_{OUT} = V_{FB} \cdot (\frac{R_1 + R_2}{R_2}), \quad V_{OUT} = 1.25V \cdot (\frac{R_1 + R_2}{R_2})$$

1% resistors are recommended to maintain output voltage accuracy.

Compensation

The MT5080 is internally compensated. The decision to use either low ESR (ceramic) capacitors or the higher ESR (tantalum or OS-CON) capacitors, for the output capacitor, can affect the stability of the overall system. The ESR of any capacitor, along with the capacitance itself, contributes a zero to the system. For the tantalum and OS-CON capacitors, this zero is located at a lower frequency due to the higher value of the ESR, while the zero of a ceramic capacitor is at a much higher frequency and can generally be ignored. A phase lead zero can be intentionally introduced by placing a feed-forward capacitor in parallel with the resistor R1 between VOUT and FB. By choosing the appropriate values for the resistor and capacitor, the zero frequency can be designed to improve the phase margin of the overall converter. The typical target value for the zero frequency is between 30kHz to 60kHz. A practical approach to compensation is to start with one of the circuits in this data sheet that is similar to your application. Optimize performance by adjusting the output capacitor and/or the feed forward capacitor (connected across the feedback resistor from output to FB pin).

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Duty Cycle Consideration

The MT5080 switching frequency (f_{OSC}), minimum duty cycles (D_{MIN}) and maximum duty cycles (D_{MAX}) of the converter are listed in the Electrical Characteristics table. The required switch duty cycle range for a Boost converter operating in continuous conduction mode (CCM) can be calculated as:

$$D_{MIN} = 1 - \frac{V_{IN_MAX}}{V_{OUT} + V_D}, \quad D_{MAX} = 1 - \frac{V_{IN_MIN}}{V_{OUT} + V_D}$$

Where V_D is the diode forward voltage drop. If the above duty cycle calculations for a given application violate the minimum (<15%) or maximum (>88%) allowed duty cycles for the MT5080, operation in discontinuous conduction mode (DCM) might provide a solution. For the same V_{IN} and V_{OUT} levels, operation in DCM does not demand as low a duty cycle as in CCM. DCM also allows higher duty cycle operation than CCM. The additional advantage of DCM is the removal of the limitations to inductor value and duty cycle required to avoid sub-harmonic oscillations and the right half plane zero (RHPZ). While DCM provides these benefits, the trade-off is higher inductor peak current, lower available output power and reduced efficiency.

Layout Consideration

The physical design of the PCB is the final stage in the design of power converter. If designed improperly, the PCB could radiate excessive EMI and contribute instability to the power converter. Therefore, following the PCB layout guidelines below can ensure better performance of MT5080. A suggested PCB layout for the MT5080 boost converter is shown in EVB Top Layer and EVB Bottom Layer below.

(1).The bold lines of AP Circuit below show the main power current paths. Keep the traces short and wide.
(2).To reduce resistive voltage drops and the number of via, MT5080 and power components (C_{IN}, C_{OUT} and L) should be placed on the component side of the board and power current traces routed on its component layer.
(3).SW node supports high frequency voltage swing (dv/dt). It should be routed small area.
(4).Place input capacitor C_{IN} as close as possible to the IC pins (VIN and GND).
(5).To prevent the switching noise from polluting MT5080's internal circuit, an additional high frequency bypass capacitor C_{IN1} (0.1μF) needs to be added between the analog ground pin (GND) and VIN pin.
(6).When laying out a board, minimize trace lengths between the IC and inductor, diode, input capacitor, and out capacitor.
(7).To minimize parasitical capacitor couplings and magnetic field-to-loop couplings, the power converter should be located away from other circuitry, especially from sensitive analog circuitry.
(8).For a typical 2-layer PCB layout, please refer to EVB Top Layer and EVB Bottom Layer below.

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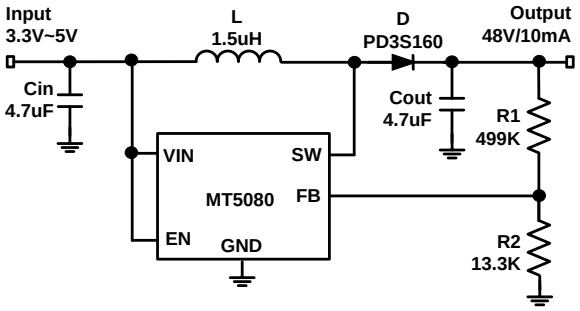
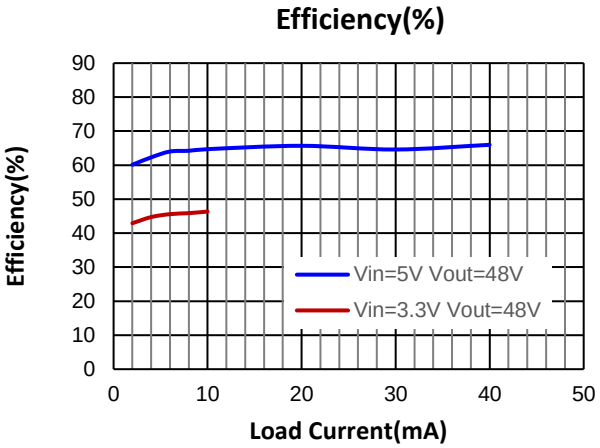
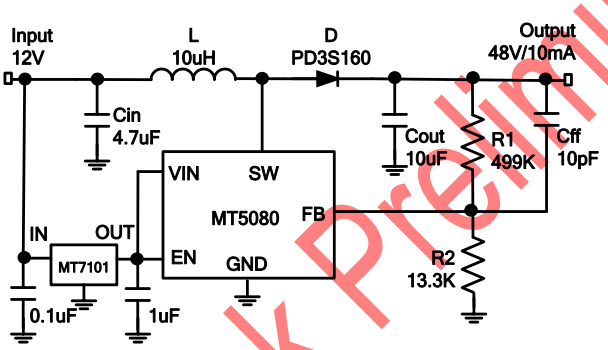
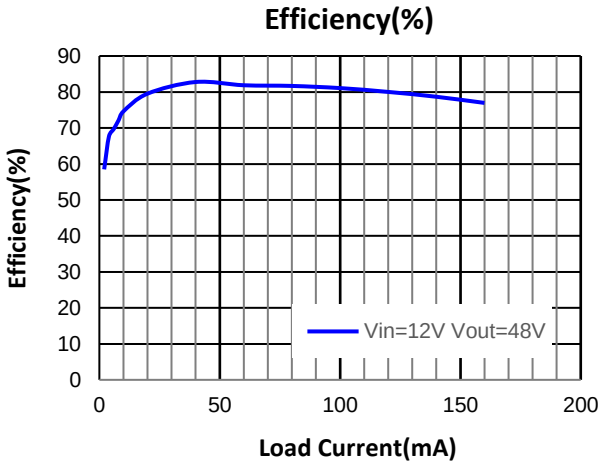
MT5080 Vin 3.3V/5V, Vout 48Vout Application Circuit





MT5080 Vin 12V, Vout 48Vout With MT7101 Application Circuit





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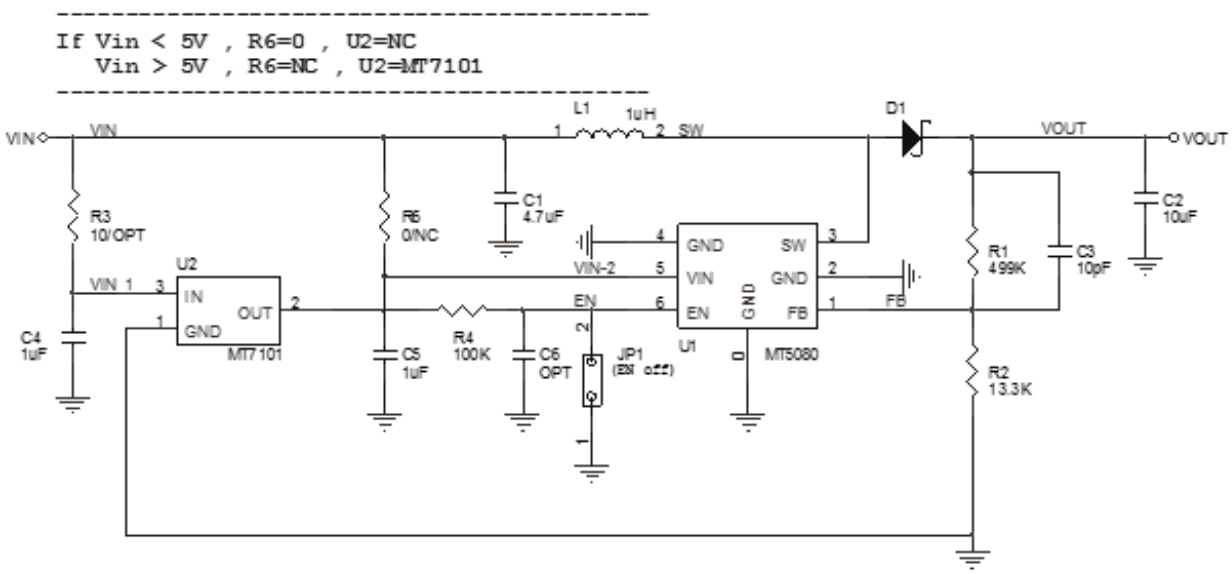
MT5080 EVB Schematic



EVB BOM List

Qty	Ref	Value		Description	Package
1	C1	4.7μF		Ceramic Capacitor, 50V, X7R	1206
1	C2	4.7or10μF		Ceramic Capacitor, 50V, X7R	1206
1	C3	Vin=3.3/5	NC	Ceramic Capacitor, 50V, X7R	0603
		Vin=12	10pF		
1	C4	0.1uF		Ceramic Capacitor, 50V, X5R	0603
1	C5	1μF		Ceramic Capacitor, 25V, X5R	0603
1	L1	Vin=3.3V,5V	1.5uH	Inductor, Irms 12A	Molding Power Choke
		Vin=12V	10uH	Inductor, Irms 4A	
1	R1	Vout=48V	499KΩ	Resistor, ±1%	0603
1	R2	Vout=48V	13.3KΩ	Resistor, ±1%	0603
1	R4	100KΩ		Resistor, ±1%	0603
1	R6	0Ω or NC		Resistor, ±1%	0603
1	D1	PD3S160		Schottky Diode	
1	U1	MT5080		Step-Up DC/DC LED Converter	DFN 6L 2x2

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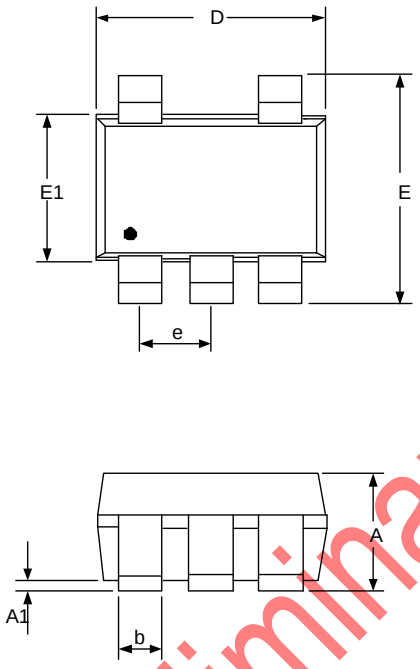
Package Information

SOT23_5L Outline Dimensions
Unit: inches/mm



SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.89	1.45	0.035	0.057
A1	0.00	0.15	0.000	0.006
b	0.30	0.50	0.012	0.020
D	2.70	3.10	0.106	0.122
E1	1.40	1.80	0.055	0.071
e	0.95		0.037	
E	2.60	3.00	0.102	0.118
L	0.30	0.60	0.012	0.024

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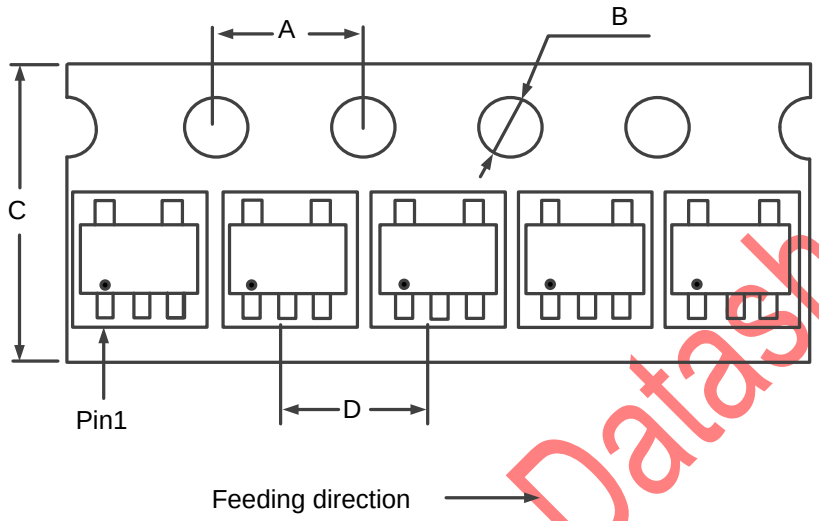
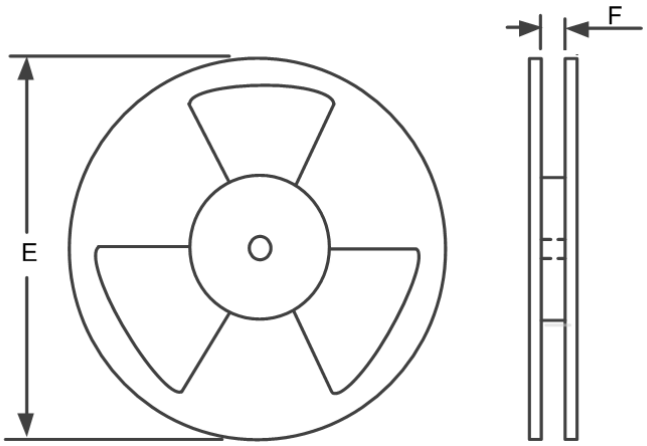
Tape & Reel Carrier Dimensions

1. Orientation / Carrier Tape Information :



2. Rokreel Information :



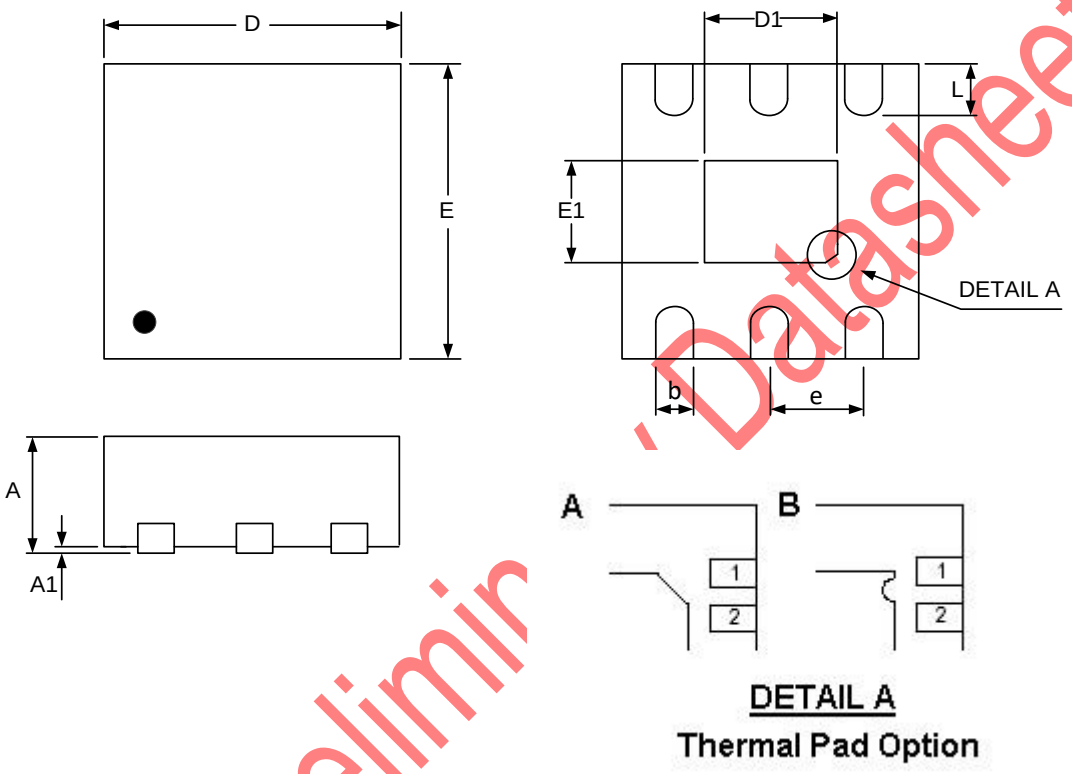
3. Dimension Details :

PKG Type	A	B	C	D	E	F	Q'ty/Reel
SOT23_5L	4.0 mm	1.5 mm	8.0 mm	4.0 mm	7 inches	9.0 mm	3,000

M3Tek Preliminary Datasheet

Package Information

DFN2x2_6L Outline Dimensions
Unit: inches/mm



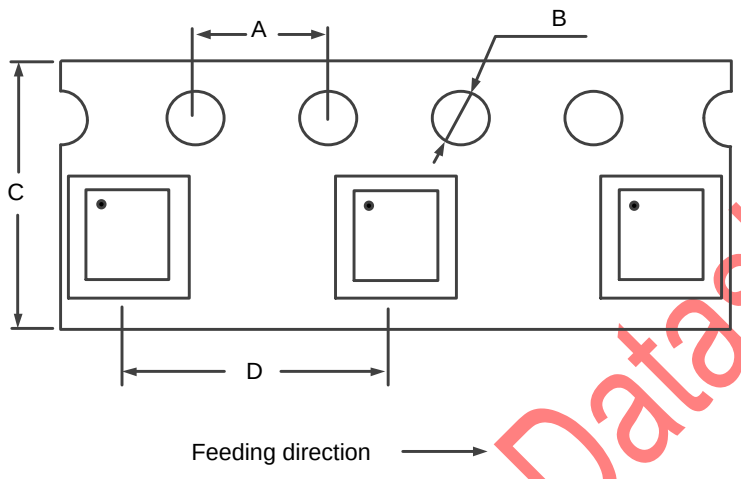
DETAIL A
Thermal Pad Option

SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
b	0.180	0.300	0.007	0.012
E	1.90	2.10	0.075	0.083
D	1.90	2.10	0.075	0.083
D1	1.00	1.70	0.040	0.067
E1	0.50	1.10	0.020	0.043
e	0.65		0.026	
L	0.20	0.45	0.008	0.018

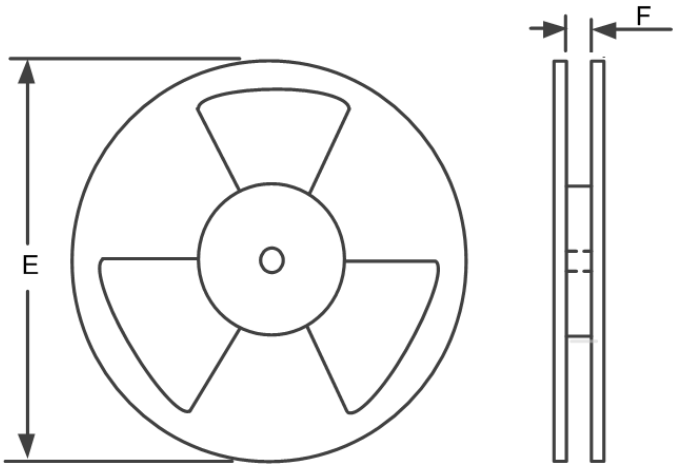
M3Tek Preliminary Datasheet

Tape & Reel Carrier Dimensions

1. Orientation / Carrier Tape Information:



2. Reel Information:



3. Dimension Details:

PKG Type	A	B	C	D	E	F	Q'ty/Reel
DFN2x2_6L	4.0 mm	1.5 mm	8.0 mm	4.0 mm	7 inches	9.0 mm	3,000

M3Tek ary Datasheet

Reflow Profile

Classification Of IR Reflow Profile

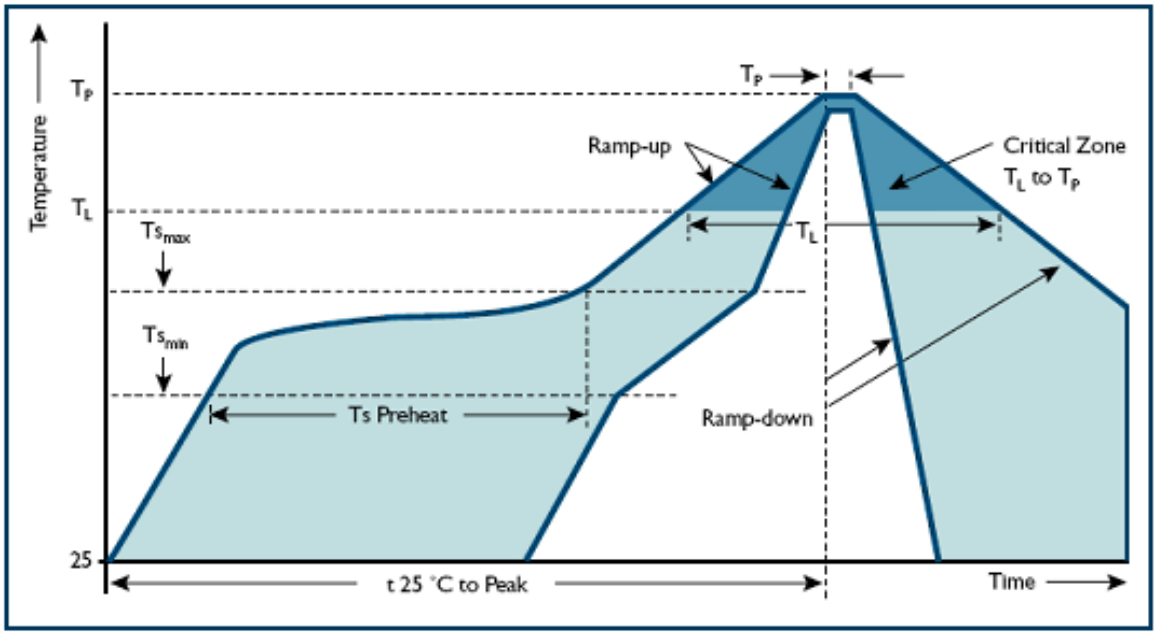
Reflow Profile	Green Assembly
Average Ramp-Up Rate (Ts_{min} to Tp)	1~2℃/second, 3℃/second max.
Preheat & Soak -Temperature Min(Ts_{min}) -Temperature Max(Ts_{max}) -Time(ts_{min} to ts ts_{max})	 150℃ 200℃ 60~120 seconds
Time maintained above: -Temperature(T_L) -Time(t_L)	 217℃ 60~150 seconds
Peak Temperature(Tp)	See Classification Temp in table 1
Time within 5℃ of actual Peak Temperature(tp)	30 seconds max.
Ramp-Down Rate	6℃/second max.
Time 25℃ to Peak Temperature	8 minutes max.

* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum.
** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.

Table 1. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 ℃	260 ℃	260 ℃
1.6 mm – 2.5 mm	260 ℃	250 ℃	245 ℃
≥2.5 mm	250 ℃	245 ℃	245 ℃

Note: For all temperature information, please refer to topside of the package, measured on the package body surface.



Preliminary Datasheet