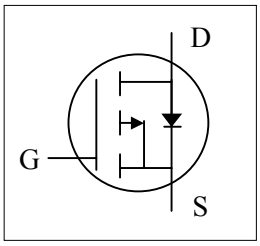
AP4P012MT

Halogen-Free Product

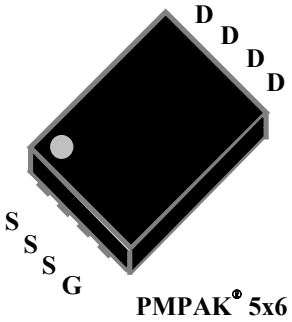
Advanced Power Electronics Corp.

P-CHANNEL ENHANCEMENT MODE POWER MOSFET

- ▼ **100% R_g & UIS Test**
- ▼ **Simple Drive Requirement**
- ▼ **Fast Switching Characteristic**
- ▼ **RoHS Compliant & Halogen-Free**



BV_{DSS}	-40V
$R_{DS(ON)}$	12mΩ
I_D	-52A



PMPAK® 5x6

Description

AP4P012 series are from Advanced Power innovated design and silicon process technology to achieve the lowest possible on-resistance and fast switching performance. It provides the designer with an extreme efficient device for use in a wide range of power applications.

The PMPAK® 5x6 package is special for voltage conversion application using standard infrared reflow technique with the backside heat sink to achieve the good thermal performance.

Absolute Maximum Ratings@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	-40	V
V_{GS}	Gate-Source Voltage	±20	V
I_D@T_C=25℃	Drain Current, V_{GS} @ 10V	-52	A
I_D@T_C=100℃	Drain Current, V_{GS} @ 10V	-33	A
I_D@T_A=25℃	Drain Current, V_{GS} @ 10V[3]	-16	A
I_D@T_A=70℃	Drain Current, V_{GS} @ 10V[3]	-13	A
I_{DM}	Pulsed Drain Current[1]	-208	A
P_D@T_C=25℃	Total Power Dissipation	52	W
P_D@T_A=25℃	Total Power Dissipation	5	W
E_{AS}	Single Pulse Avalanche Energy[4]	45	mJ
T_{STG}	Storage Temperature Range	-55 to 150	℃
T_J	Operating Junction Temperature Range	-55 to 150	℃

Thermal Data

Symbol	Parameter	Value	Unit
Rthj-c	Maximum Thermal Resistance, Junction-case	2.4	℃/W
Rthj-a	Maximum Thermal Resistance, Junction-ambient[3]	25	℃/W

Electrical Characteristics@T_j=25°C(unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250uA	-40	-	-	V
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	V_{GS}=-10V, I_D=-20A	-	-	12	mΩ
		V_{GS}=-4.5V, I_D=-10A	-	-	18	mΩ
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250uA	-1	-	-3	V
g_{fs}	Forward Transconductance	V_{DS}=-5V, I_D=-20A	-	46	-	S
I_{DSS}	Drain-Source Leakage Current	V_{DS}=-32V, V_{GS}=0V	-	-	-10	uA
I_{GSS}	Gate-Source Leakage	V_{GS}=±20V, V_{DS}=0V	-	-	±0.1	uA
Q_g(V_{GS}=-10V)	Total Gate Charge[5]	I_D=-20A	-	78	125	nC
Qg(V_{GS}=-4.5V)	Total Gate Charge[5]	V_{DS}=-32V		38	61	nC
Q_{gs}	Gate-Source Charge[5]		-	14	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge[5]		-	16	-	nC
$t_{d(on)}$	Turn-on Delay Time[5]	V_{DS}=-20V	-	16	-	ns
t_r	Rise Time[5]	I_D=-20A	-	58	-	ns
$t_{d(off)}$	Turn-off Delay Time[5]	R_G=3.3Ω	-	71	-	ns
t_f	Fall Time[5]	V_{GS}=-10V	-	104	-	ns
C_{iss}	Input Capacitance[5]	V_{GS}=0V	-	3800	6080	pF
C_{oss}	Output Capacitance[5]	V_{DS}=-25V	-	275	-	pF
C_{rss}	Reverse Transfer Capacitance[5]	f=1.0MHz	-	215	-	pF
R_g	Gate Resistance	f=1.0MHz	-	3	6	Ω

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage[2]	I_S=-20A, V_{GS}=0V	-	-	-1.2	V
t_{rr}	Reverse Recovery Time[5]	I_S=-20A, V_{GS}=0V,	-	19	-	ns
Q_{rr}	Reverse Recovery Charge[5]	dI/dt=-100A/μs	-	11	-	nC

Notes:

1.Pulse width limited by Max. junction temperature.

2.Pulse test

3.Surface mounted on 1 in^2 copper pad of FR4 board, t ≤10sec ; 60°C/W at steady state.

4.Starting T_j=25°C , V_{DD}=-30V , L=0.1mH , R_G=25Ω , I_{AS}=-30A

5.Guaranteed by design.

6.These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=150°C.

THIS PRODUCT IS SENSITIVE TO ELECTROSTATIC DISCHARGE, PLEASE HANDLE WITH CAUTION.

USE OF THIS PRODUCT AS A CRITICAL COMPONENT IN LIFE SUPPORT, AUTOMOTIVE OR OTHER SIMILAR SYSTEMS IS NOT AUTHORIZED.

APEC DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

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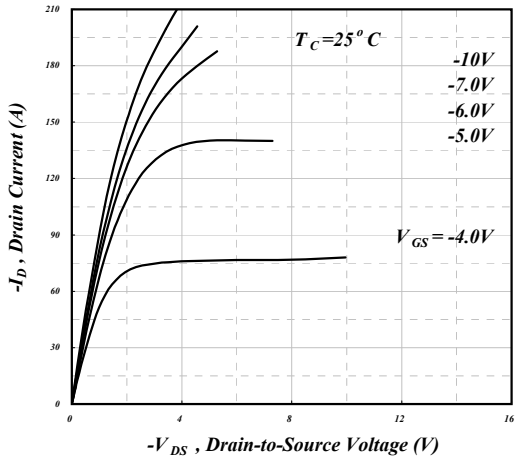


Fig 1. Typical Output Characteristics

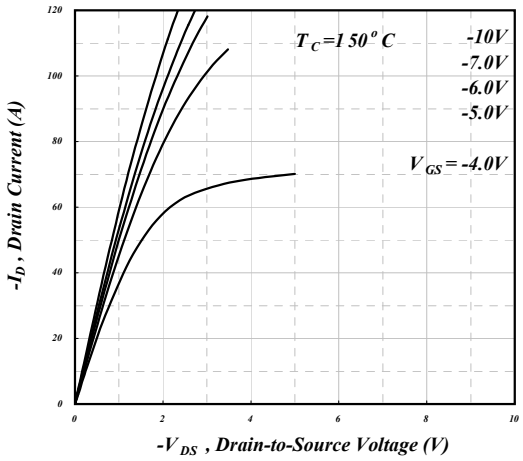


Fig 2. Typical Output Characteristics

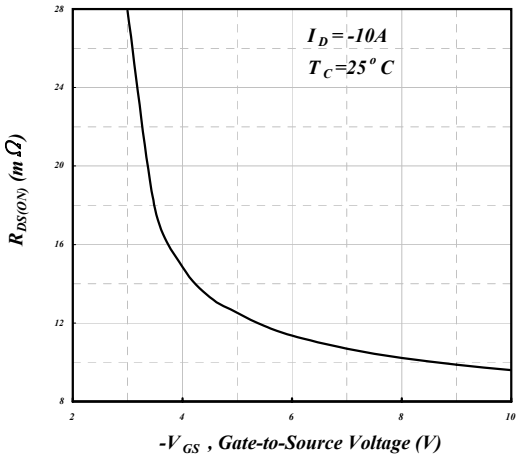


Fig 3. On-Resistance v.s. Gate Voltage

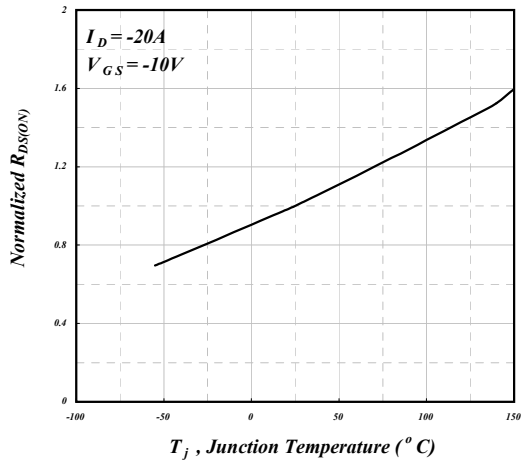


Fig 4. Normalized On-Resistance v.s. Junction Temperature

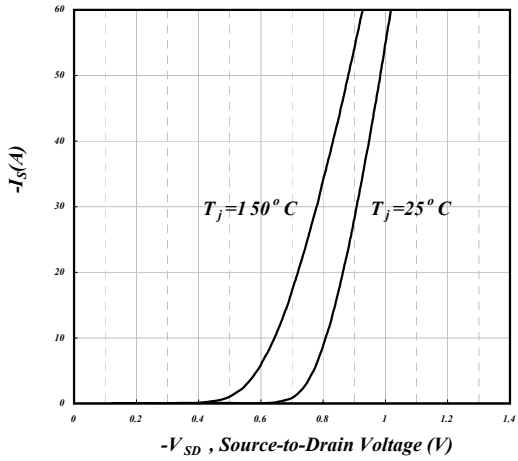


Fig 5. Forward Characteristic of Reverse Diode

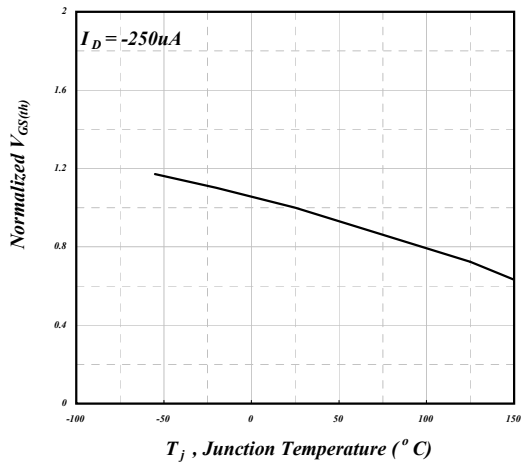


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

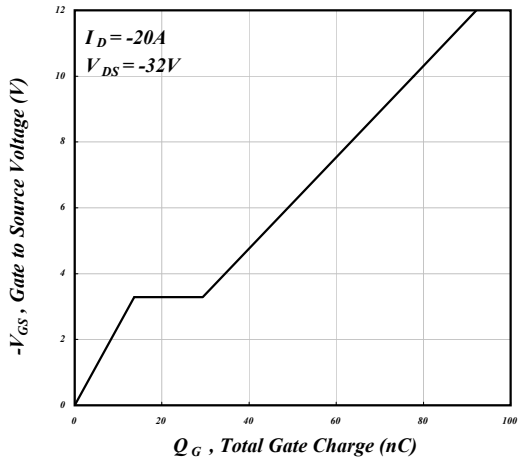


Fig 7. Gate Charge Characteristics

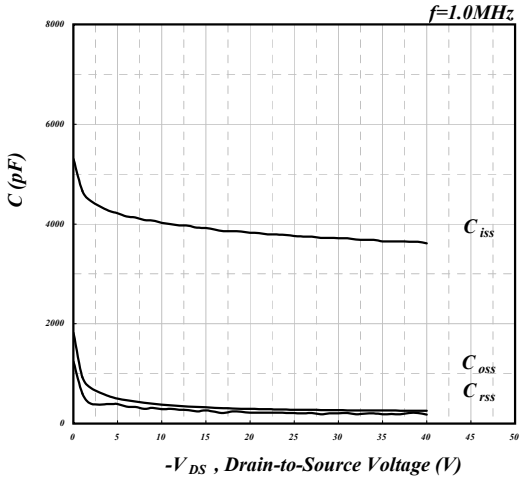


Fig 8. Typical Capacitance Characteristics

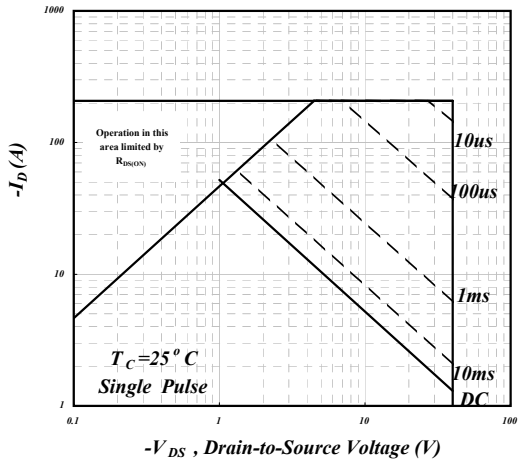


Fig 9. Maximum Safe Operating Area[6]

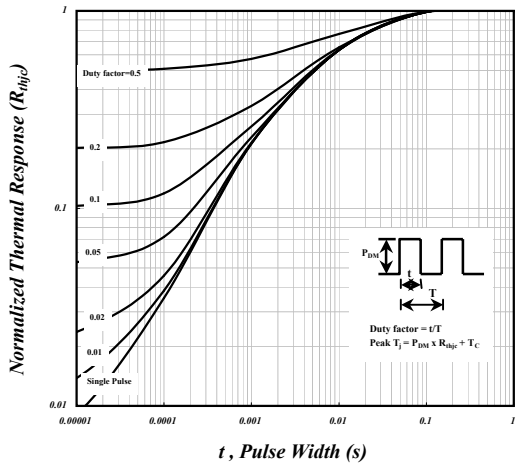


Fig 10. Effective Transient Thermal Impedance

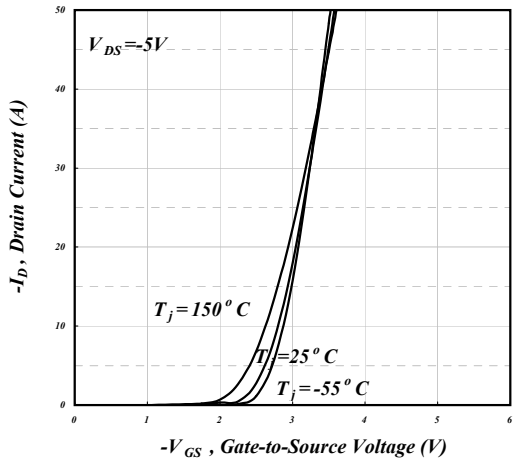


Fig 11. Transfer Characteristics

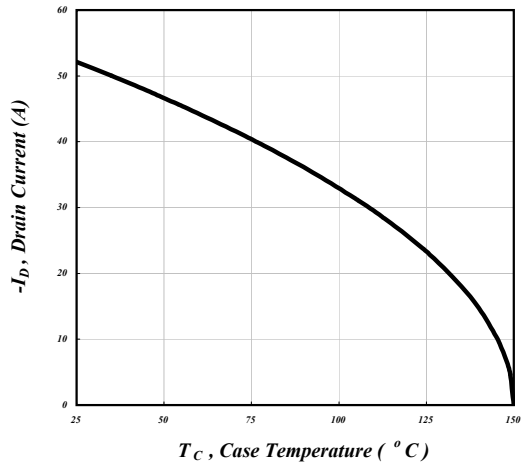


Fig 12. Drain Current v.s. Case Temperature

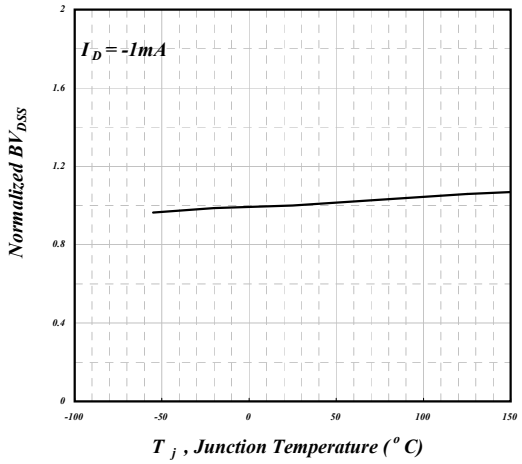


Fig 13. Normalized BV_{DSS} v.s. Junction Temperature

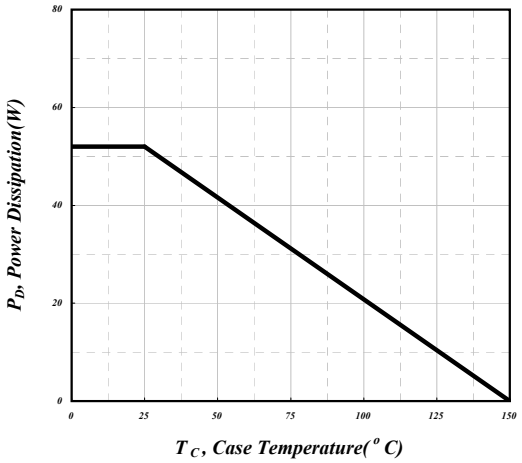


Fig 14. Total Power Dissipation

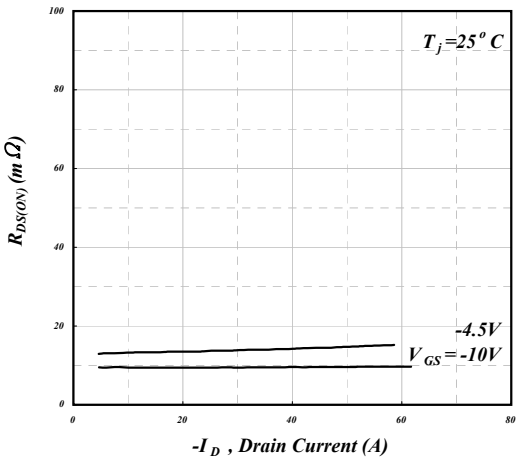


Fig 15. Typ. Drain-Source on State Resistance

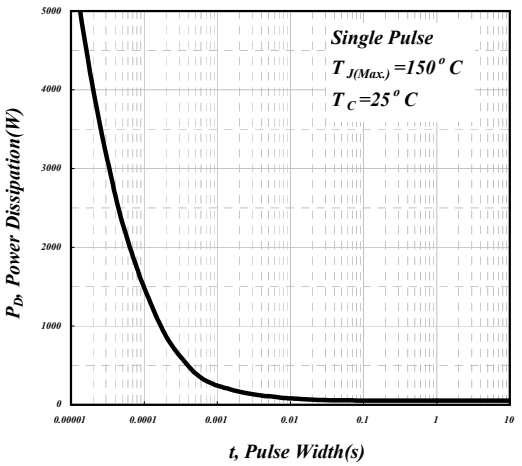
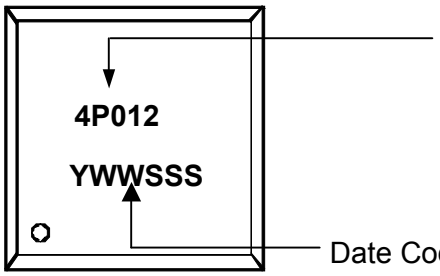


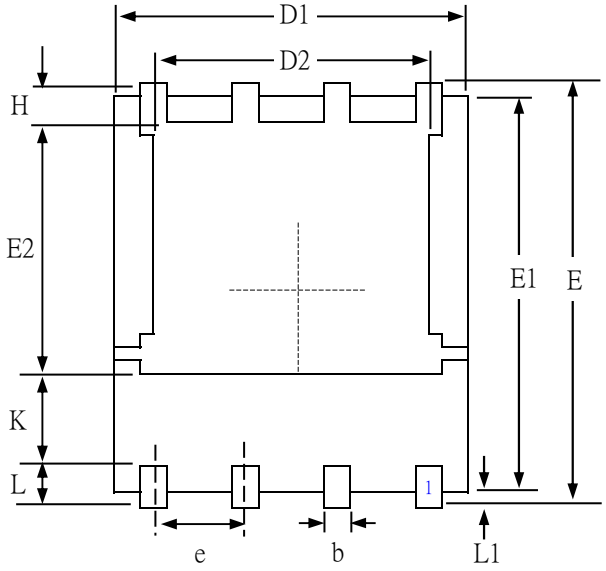
Fig 16. Single Pulse Power Dissipation

MARKING INFORMATION

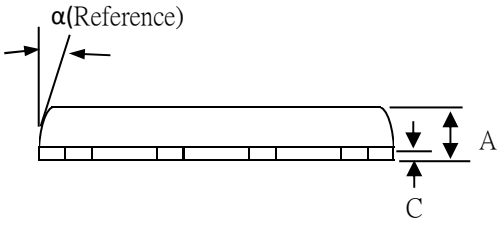


Y：Last Digit Of The Year
WW：Week
SSS：Sequence

Package Outline : PMPAK 5x6



BACKSIDE VIEW



SYMBOLS	Millimeters		
	MIN	NOM	MAX
A	0.90	1.10	1.30
b	0.33	0.41	0.51
C		0.254(Ref.)	
D1	4.80	4.90	5.10
D2	3.61	4.00	4.40
E	5.80	6.03	6.25
E1 (Ref.)	5.60	5.75	5.90
E2 (Ref.)	3.30	3.55	3.80
e		1.27 BSC	
H	0.35	—	0.90
K (Ref.)	1.00	1.275	—
L	0.35	0.55	0.75
L1	0.06	0.13	0.20
α(Ref.)	0°	—	12°

1.All dimension are in millimeters.

2.Dimension does not include burrs and mold flash/protrusions.

3.The outline schematic is not to scale and slightly different from the actual product appearance.

PMPAK 5X6(E-TYPE) FOOTPRINT：

