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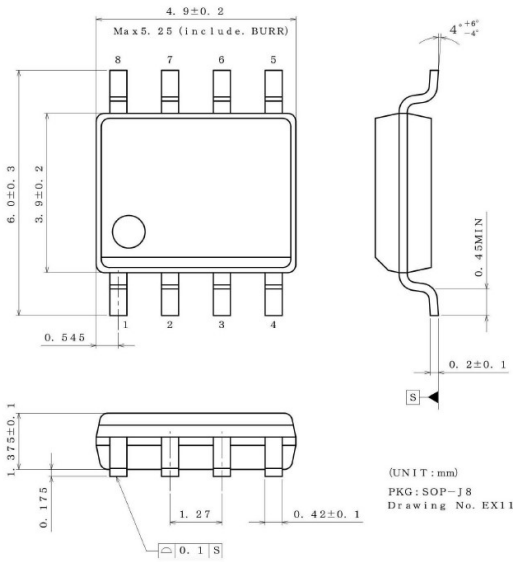
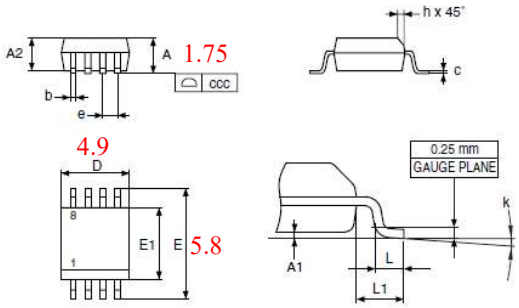
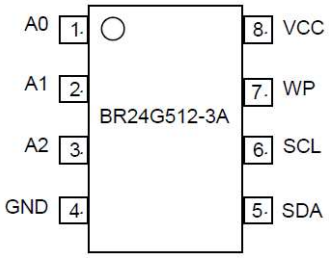
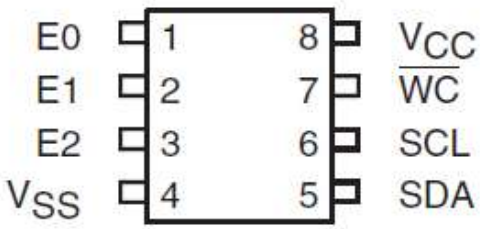
Comparison Report

1. Package Dimension

Item	Old	New
	BR24G512FJ-3AGTE2 (ROHM) **3A24G51201Y** **IC (BR24G512FJ-3AGTE2,SOP-J8,ROHM)**	M24512-WMN6TP (ST) 7B.24512.002 **3AM24512W1Y** IC (M24512-WMN6TP,SO8N,ST)
Outline	 **SOP-J8** 4.90mm x 6.00mm x 1.65mm  (UNIT : mm) PKG : SOP-J8 Drawing No. EX11	 SO8 (MN) 150 mils width  4.9 5.8 1.75
Pin Configuration	 A0 1. / A1 2. / A2 3. / GND 4. / 8. VCC / 7. WP / 6. SCL / 5. SDA BR24G512-3A	 E0 1 / E1 2 / E2 3 / VSS 4 / 8 VCC / 7 WC / 6 SCL / 5 SDA
Device select code	Type: BR24G512-3A Slave address: 1 0 1 0 A2 A1 A0 R/W Maximum number of Connected buses: 8	Device type identifier(1): b7 1, b6 0, b5 1, b4 0 Chip Enable address(2): b3 E2, b2 E1, b1 E0 RW: b0 Device select code: 1 0 1 0 E2 E1 E0 RW

Symbol	millimeters		
	Typ	Min	Max
A			1.75
A1		0.1	0.25
A2		1.25	
b		0.28	0.48
c		0.17	0.23
ccc			0.1
D	4.9	4.8	5
E	6	5.8	6.2
E1	3.9	3.8	4
e	1.27	-	-
h		0.25	0.5
k		0°	8°
L		0.4	1.27
L1	1.04		

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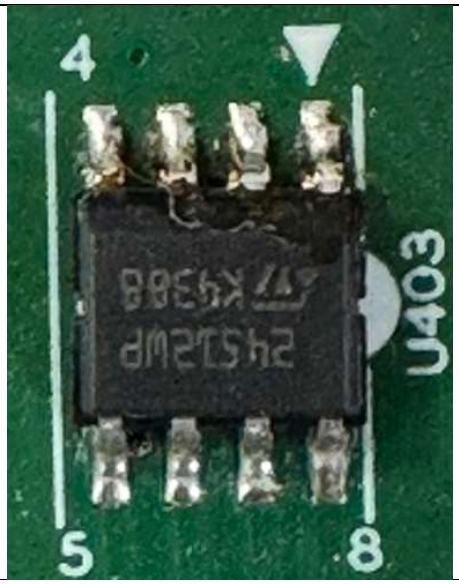
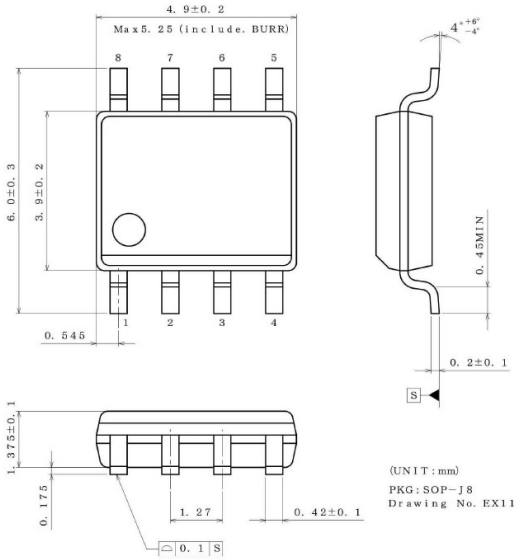
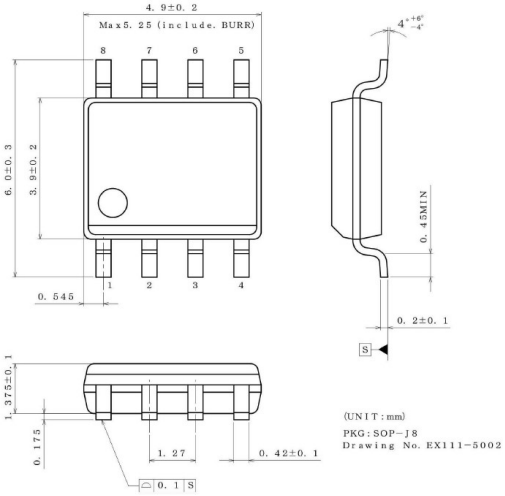
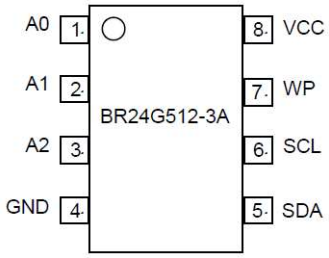
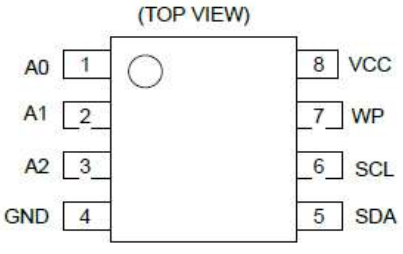
Pin 7	**Write Protect (WP) Terminal** Write Protect (WP) Function When WP terminal is set at Vcc(H level), data rewrite of all addresses is prohibited. When it is set GND (L level), data rewrite of all address is enabled. Be sure to connect this terminal to Vcc or GND, or control it to H level or L level. Do not leave it open. In case of using it as ROM, it is recommended to connect it to pull up or Vcc. At extremely low voltage at power ON/OFF, by setting the WP terminal 'H', write error can be prevented. 當 WP 端子設定為 Vcc（High，高電位）時，所有位址的資料重新寫入操作都會被禁止。 當 WP 端子設定為 GND（Low，低電位）時，所有位址都允許進行資料重新寫入。 請務必將此端子連接至 Vcc 或 GND，或者以控制訊號將其設定為 High 或 Low。請勿讓 WP 端子處於浮接（Open）狀態。 如果將此裝置當作 ROM（唯讀記憶體）使用，建議將 WP 端子連接至 Pull-up（上拉電阻）或 Vcc。 在電源開啟／關閉（Power ON/OFF）時，如果電源電壓處於極低電壓狀態，將 WP 端子設定為 High（H），可以防止發生寫入錯誤（Write Error）	**Write Control ($\overline{WC}$)** This input signal is useful for protecting the entire contents of the memory from inadvertent write operations. Write operations are disabled to the entire memory array when Write Control ($\overline{WC}$) is driven High. When unconnected, the signal is internally read as V_{IL}, and Write operations are allowed. When Write Control ($\overline{WC}$) is driven High, device select and address bytes are acknowledged, Data bytes are not acknowledged. 此輸入訊號可用於保護整個記憶體的內容，避免因意外而進行寫入操作。 當 Write Control（WC）被拉至 High（高電位）時，整個記憶體陣列的寫入操作都會被禁止。 當 WC 腳位未連接（浮接）時，晶片內部會將其判定為 VIL（低電位），因此允許進行寫入操作。 當 Write Control（WC）被拉至 High 時，Device Select（裝置選擇）與 Address（位址）位元組仍會回應 ACK（確認），但 Data（資料）位元組則不會回應 ACK。
		

Comparison Report

Item	Old	New
	BR24G512FJ-3AGTE2 (ROHM) **3A24G51201Y** **IC (BR24G512FJ-3AGTE2,SOP-J8,ROHM)**	BR24G512FJ-5AE2 (ROHM) **3A24G51211Y** **IC (BR24G512FJ-5AE2,SOP-J8,ROHM)**
	 **SOP-J8** 4.90mm x 6.00mm x 1.65mm 	 SOP-J8 4.9 mm x 6.0 mm x 1.65 mm 
Pin Configuration		

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Comparison Report

		

2. Electrical (Ta=25°C)

Parameter	Limits		
	Old	New	New
	(ROHM) BR24G512FJ-3AGTE2 DIVA:3A24G51201Y	(ST) M24512-WMN6TP DIVA: 3AM24512W1Y Qisda:7B.24512.002	(ROHM) BR24G512FJ-5AE2 DIVA: 3A24G51211Y
Memory Size	512 Kbit (64K×8)	512 Kbit (64K×8)	512 Kbit (64K×8)
Interface	I²C	I²C	I²C
Max Clock	1 MHz	1 MHz	1 MHz
Organization	64K × 8	64K × 8	64K × 8
Write Cycle	5ms Max	5ms Max	3.5ms Max
Operating Temp	-40 ~ +85°C	-40 ~ +85°C	-40 ~ +85°C
VCC	1.7 ~ 5.5V	2.5 ~ 5.5V	1.6 ~ 5.5V
Page Size	128 Bytes	128 Bytes	128 Bytes

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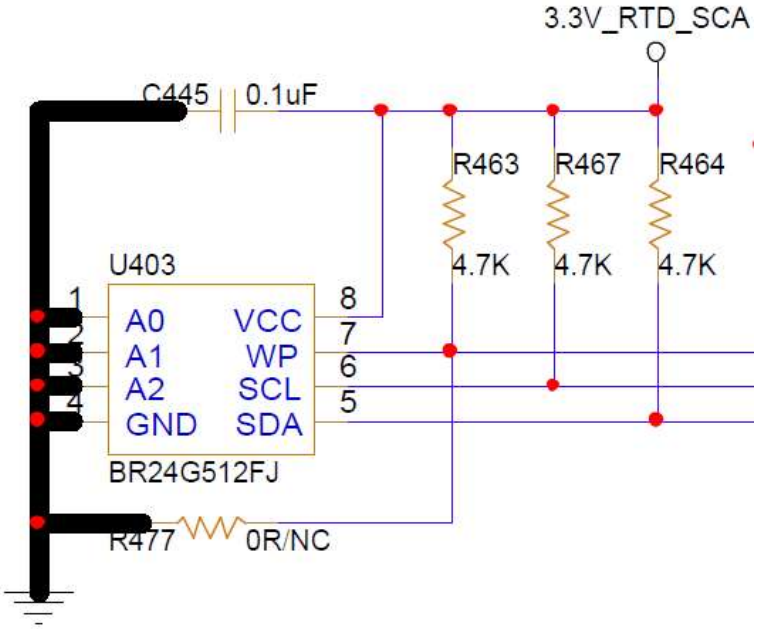
3. Circuit

The voltage supplied to the EEPROM is 3.3V.



4. Conclusion

This component change has been evaluated by DIVA; the initial successor evaluation showed the new successor is compatible with former model. None of the other components and program will be needed to recalibrate or implement. The ECN will be provided if you approve.