SY80082x

High Efficiency, 1.5MHz, 2A, 5.5V Input Synchronous Buck Converter

General Description

The SY80082x high efficiency 1.5MHz synchronous buck converter operates over a wide input voltage range of 2.5V to 5.5V, and can deliver an output current up to 2A. It integrates a top MOSFET and a bottom MOSFET with very low $R_{DS(ON)}$ to minimize conduction loss. The 1.5MHz pseudo-constant switching frequency enables using small external inductor and capacitor values.

The SY80082x uses constant-off time and peak current mode control strategy to achieve fast transient response, and high efficiency at light loads. It also provides cycle-by-cycle current limit protection, output under voltage protection and over temperature protection.

Only the input and output capacitors, inductor, feedback resistor divider and feedforward capacitor need to be selected for the targeted application specifications. The SY80082 is available in a compact SOT23-5 or SOT23-6 package.

Ordering Part Number	Details
SY80082AAT	SOT23-5, 50Ω Discharge, Hic-Cup Without Power Good (PG)
SY80082ABT	SOT23-6, 50Ω Discharge, Hic-Cup With Power Good (PG)
SY80082FABT	SOT23-6, 1.8kΩ Discharge, Latch off With Power Good (PG)
SY80082LABT	SOT23-6, 50Ω Discharge, Latch off With Power Good (PG)

Inductor and C_{OUT} Selection Table

V_{OUT}[V]	L[μH]	C_{OUT}[μF]			
		4.7	10	22	44
0.9	0.68		√	☆	√
1.8/2.5/3.3	1.0		☆	√	√
	2.2			√	√

Note: '☆' means recommended for most applications.

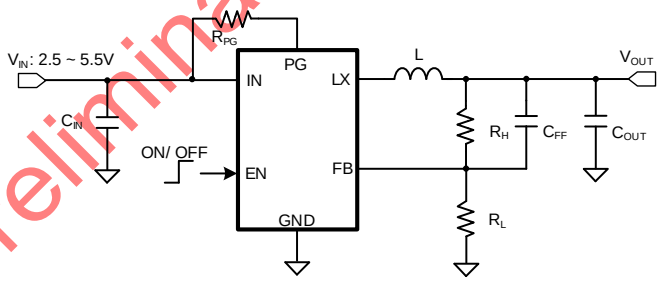
Features

- Low $R_{DS(ON)}$ for Internal MOSFETs: 130mΩ Top, 85mΩ Bottom
- Wide Input Voltage Range: 2.5V ~ 5.5V
- Up to 2A Output Current
- ±1.5% 0.6V Reference
- PFM Light Load Operation for High Efficiency
- Internal Soft-Start Limits the Inrush Current
- 1.5MHz Switching Frequency Minimizes the External Components
- Constant Off-time and Peak Current Mode Control to Achieve Fast Transient Responses
- 100% Dropout Operation
- Power Good Indicator for SY80082ABT,SY80082LABT,SY80082FABT
- Output Auto Discharge Function
- Cycle-by-Cycle Peak Current Limit Protection
- Hic-Cup Mode Output Under Voltage Protection for SY80082AAT, SY80082ABT
- Latch off Mode Output Under Voltage Pretection for SY80082FABT, SY80082LABT
- Auto-Recovery Mode Over Temperature Protection for SY80082AAT, SY80082ABT
- Latch off Mode Over Temperature Protection for SY80082FABT, SY80082LABT
- Input Under Voltage Lockout (UVLO)
- RoHS-Compliant and Halogen-Free
- Compact Package: SOT23-5/SOT23-6

Applications

- Set-Top Box
- USB Dongle
- Media Player
- Smart Phone

Typical Application



Note: PG pin only for SY80082ABT, SY80082FABT, SY80082LABT

Figure1. Schematic Diagram

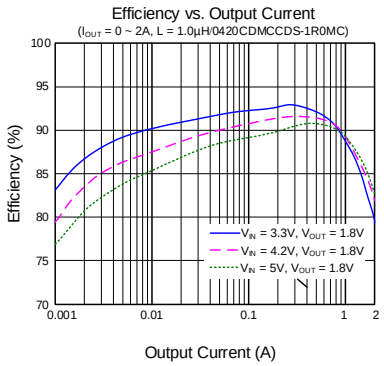


Figure2. Efficiency vs. Output Current

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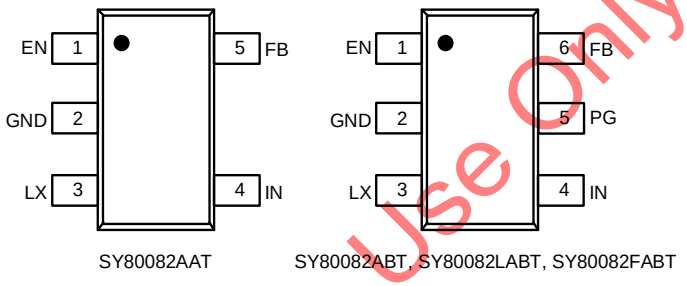
Ordering Information

Part Number	Top Mark	Package type
SY80082AAT	**HQQxyz**	SOT23-5 RoHS-Compliant, Halogen-Free
SY80082ABT	**KHQxyz**	SOT23-6 RoHS-Compliant, Halogen-Free
SY80082LABT	**LGMxyz**	
SY80082FABT	**LDJxyz**	

x = year code, y = week code, z = lot number code

Pinout (top view)



SY80082AAT

SY80082ABT, SY80082LABT, SY80082FABT

Pin Name	Pin No.		Pin Description
	SOT23-5	SOT23-6	
EN	1	1	Enable pin. Pull this pin high to turn on the device and pull this pin low to turn off the device. Do not leave this pin floating.
GND	2	2	Power ground pin.
LX	3	3	Inductor pin. Connect this pin to the switching node of inductor.
IN	4	4	Input pin. Decouple this pin from the GND pin with at least a 10μF ceramic capacitor.
PG	-	5	Power good indicator pin. PG pin should be connected to V_{IN} or another voltage source through a resistor (e.g., 10kΩ ~ 100kΩ). This pin becomes high when the output voltage is within 90% to 120% of regulated value under normal operation.
FB	5	6	Output feedback pin. Connect this pin to the center point of the output resistor divider as shown in Figure 1. $V_{OUT} = 0.6 \times (1 + R_H/R_L)$.

Pin Description

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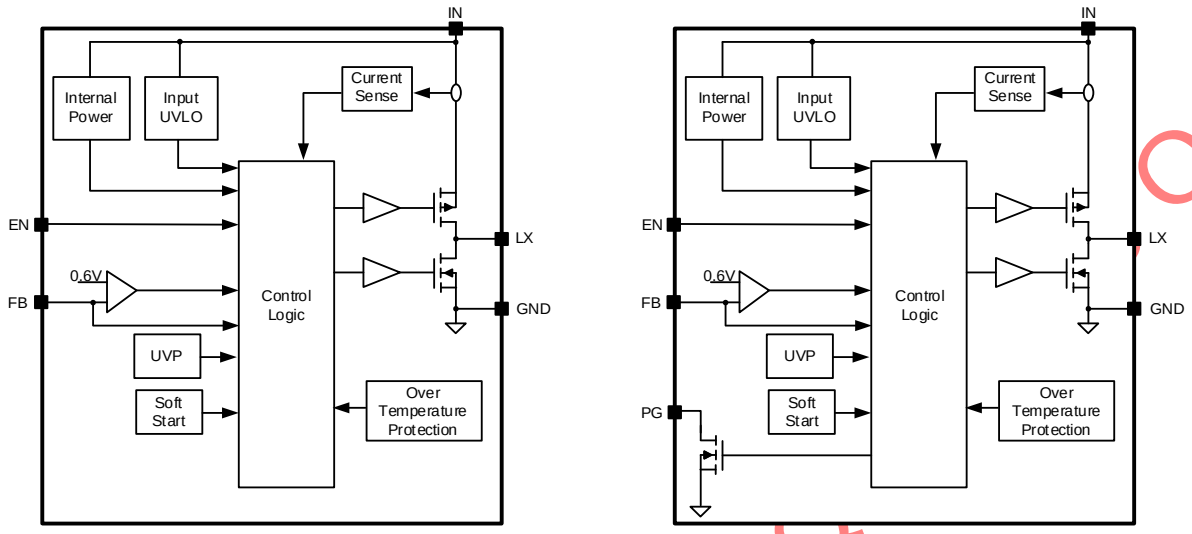
Block Diagram



SY80082AAT

SY80082ABT, SY80082LABT, SY80082FABT

Figure3. Block Diagram

Absolute Maximum Ratings

Parameter (Note 1)	Min	Max	Unit
IN, LX	-0.3	6.5	V
GND	-0.3	0.3	
EN, FB, PG	-0.3	IN + 0.6	
LX, 20ns duration	-3	7	
Junction Temperature, Operating	-40	150	°C
Lead Temperature (Soldering, 10s)		260	
Storage Temperature	-65	150	

Thermal Information

Parameter (Note 2)	Typ	Unit
θ_{JA} Junction-to-Ambient Thermal Resistance	120	°C/W
θ_{JC} Junction-to-Case Thermal Resistance	20	
P_D Power Dissipation T_A = 25°C	0.83	W

Recommended Operating Conditions

Parameter (Note 3)	Min	Max	Unit
Input Voltage	2.5	5.5	V
Output Voltage	0.6	5.5	
Continuous Output Current		2	A
Junction Temperature	-40	125	°C

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Electrical Characteristics

(V_{IN} = 5V, V_{OUT} = 1.8V, L = 1.0μH, C_{OUT} = 10μF, T_J = 25°C, I_{OUT} = 1A unless otherwise specified (note4))

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Input	Voltage Range	V_{IN}		2.5		5.5	V
	UVLO Rising Threshold	$V_{IN,UVLO}$	V_{IN} rising		2.4	2.49	
	UVLO Hysteresis	$V_{IN,HYS}$			0.15		
	Quiescent Current	I_Q	I_{OUT} = 0A, V_{FB} = V_{REF} × 105%		50	70	μA
	Shutdown Current	I_{SHDN}	V_{EN} = 0V		0.1	1	
Output	Voltage Range	V_{SET}		0.6		5.5	V
	FB Reference Voltage	V_{REF}		0.591	0.6	0.609	
	Turn On Delay Time	$t_{ON,DLY}$	From EN high to LX starts switching		0.5		ms
	Soft-Start Time	t_{SS}	V_{OUT} from 0% to 100% V_{SET}		1		
	UVP Threshold	V_{UVP}	(Note 5)		50		$\%V_{REF}$
	UVP Delay Time	$t_{UVP,DLY}$	(Note 5)		10		μs
	UVP Hiccup On-Time	$t_{HICCUP,ON}$	(Note 5)		2.5		ms
	UVP Hiccup Off-Time	$t_{HICCUP,OFF}$	(Note 5)		3		
	Discharge on Resistance	R_{DIS}	SY80082AAT, SY80082ABT SY80082LABT		50		Ω
			SY80082FABT		1.8		kΩ
Enable (EN)	Input Voltage High	$V_{EN,H}$		1			V
	Input Voltage Low	$V_{EN,L}$				0.4	
	Leakage Current	I_{EN}	V_{EN} = 5V		0	2	μA
Power Good (PG)	Thresholds (SY80082ABT, SY80082LABT, SY80082FABT)	$V_{PG,R}$	V_{FB} rising, PG from low to high		92		$\%V_{REF}$
		$V_{PG,F}$	V_{FB} falling, PG from high to low		90		
		$V_{PG,OVP}$	V_{FB} rising, PG from high to low		120		
		$V_{PG,HYS}$	V_{FB} falling, PG from low to high,		110		
	Delay Time (SY80082ABT, SY80082LABT, SY80082FABT)	$t_{PG,R}$	PG from low to high (Note 5)		1		μs
		$t_{PG,F}$	PG from high to low (Note 5)		20		
MOSFET	Top MOSFET $R_{DS(ON)}$	$R_{DS(ON),TOP}$			130		mΩ
	Bottom MOSFET $R_{DS(ON)}$	$R_{DS(ON),BOT}$			85		
	Top MOSFET Current Limit Threshold	$I_{LMT,TOP}$		3.5			A
Frequency	Switching Frequency	f_{SW}	I_{OUT} = 1A, CCM		1.5		MHz
	Minimum On-Time	$t_{ON,MIN}$	(Note 5)		50		ns
	Maximum Duty Cycle	D_{MAX}	(Note 5)	100			%
OTP	Temperature	T_{OTP}	(Note 5)		150		˚C
	Temperature Hysteresis	T_{HYS}	(Note 5)		15		

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a 6cm×6cm size, two-layer Silergy Evaluation Board with 2-oz copper. Paddle of SOT23-6 package is the case position for θ_{JC} measurement.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Unless otherwise stated, limits are 100% production tested under pulsed load conditions such that $T_A \cong T_J$ = 25°C. Limits over the operating temperature range (See recommended operating conditions) and relevant voltage range(s) are guaranteed by design, test, or statistical correlation.

Note 5: Guaranteed by design or statistical correlation and not production tested.

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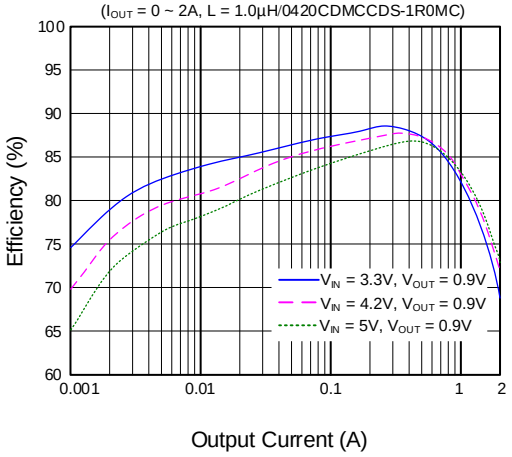
Typical Performance Characteristics

(SY80082ABT, T_A = 25°C, V_{IN} = 5V, V_{OUT} = 1.8V, L = 1µH, C_{OUT} = 10µF, unless otherwise noted)

Efficiency vs. Output Current

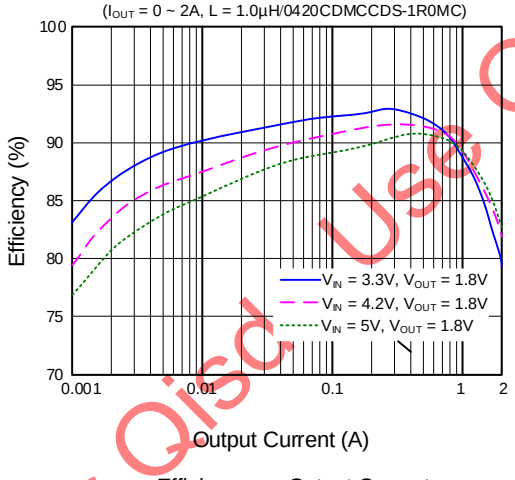
(I_{OUT} = 0 ~ 2A, L = 1.0µH/0420CDMCCDS-1R0MC)



Output Current (A)

Efficiency vs. Output Current

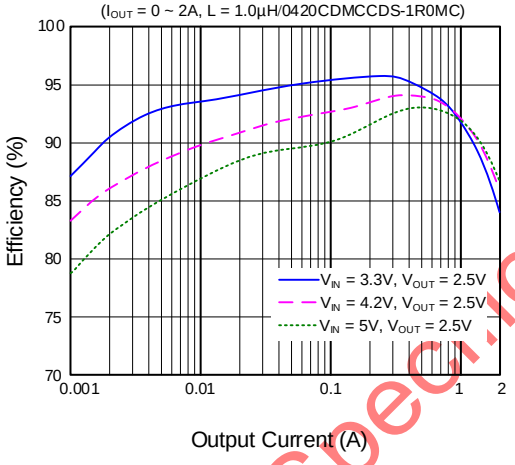
(I_{OUT} = 0 ~ 2A, L = 1.0µH/0420CDMCCDS-1R0MC)



Output Current (A)

Efficiency vs. Output Current

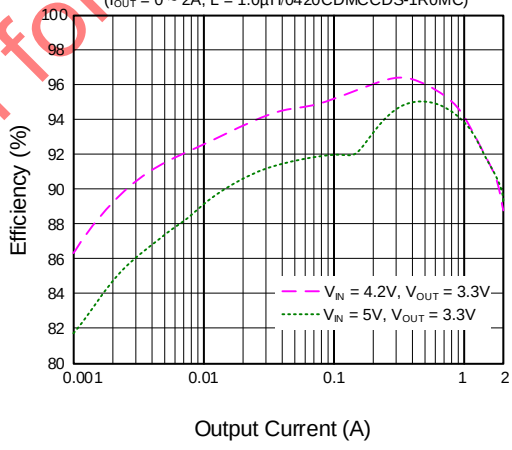
(I_{OUT} = 0 ~ 2A, L = 1.0µH/0420CDMCCDS-1R0MC)



Output Current (A)

Efficiency vs. Output Current

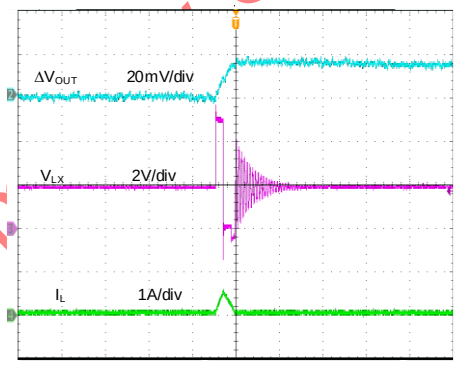
(I_{OUT} = 0 ~ 2A, L = 1.0µH/0420CDMCCDS-1R0MC)



Output Current (A)

Output Ripple

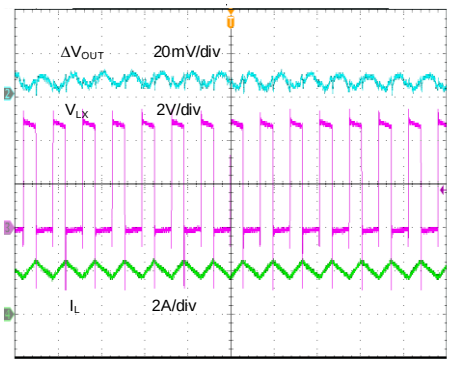
(V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 0A)



Time (1µs/div)

Output Ripple

(V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 2A)



Time (1µs/div)

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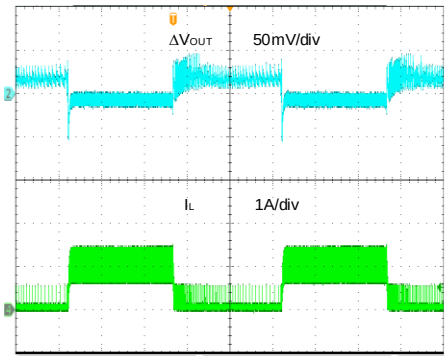
Load Transient

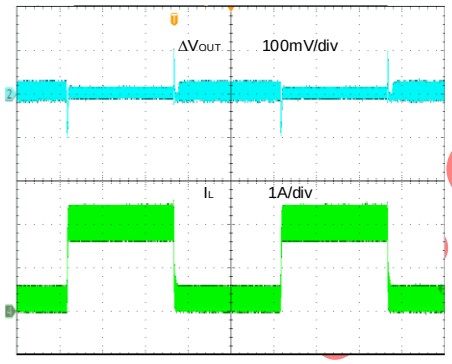
(V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 0A ~ 1A)



Time (400µs/div)

Load Transient

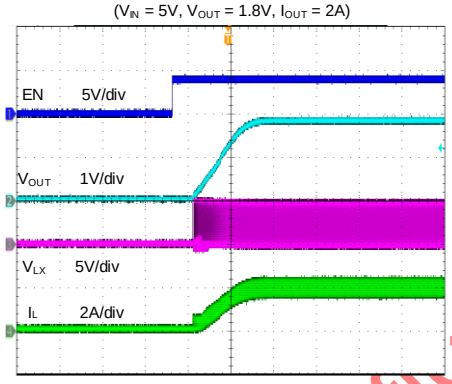
(V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 0.2A ~ 2A)



Time (400µs/div)

Startup from Enable

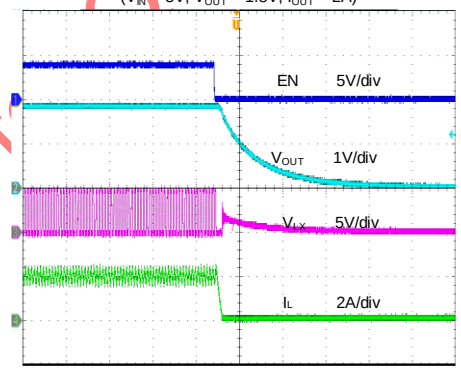
(V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 2A)



Time (800µs/div)

Shutdown from Enable

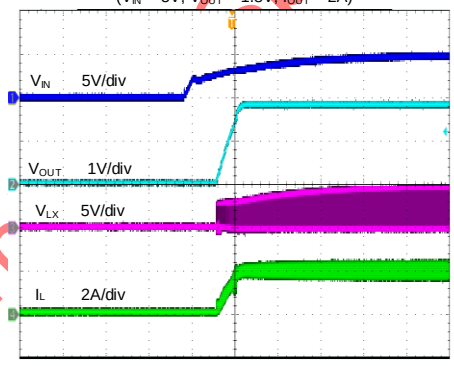
(V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 2A)



Time (10µs/div)

Startup from V_{IN}

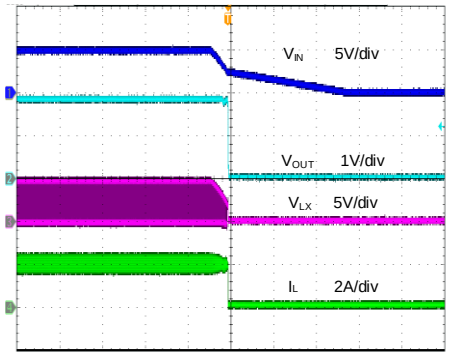
(V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 2A)



Time (2ms/div)

Shutdown from V_{IN}

(V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 2A)



Time (2ms/div)

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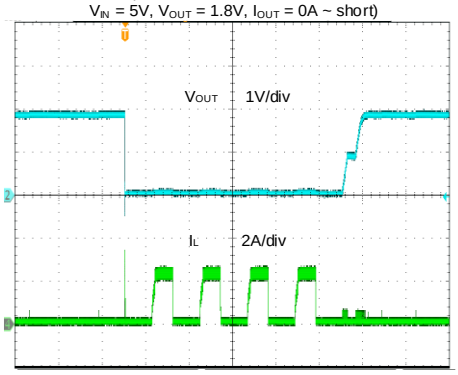
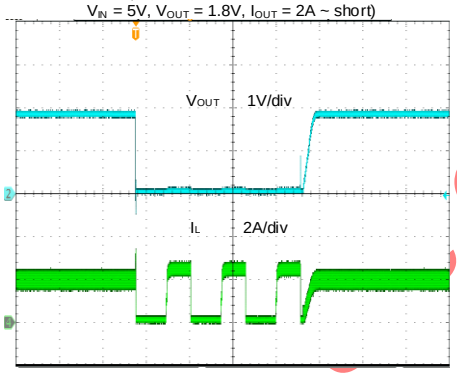
Short Circuit Protection
(SY80082AAT,SY80082ABT
V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 0A ~ short)



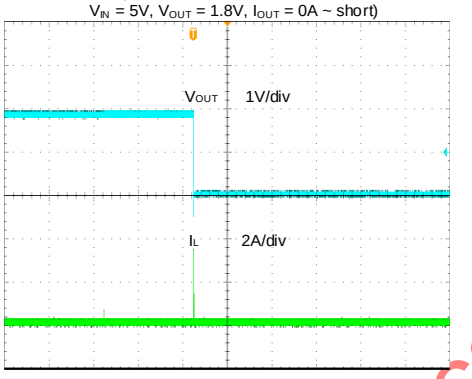
Time (4ms/div)

Short Circuit Protection
(SY80082AAT,SY80082ABT
V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 2A ~ short)



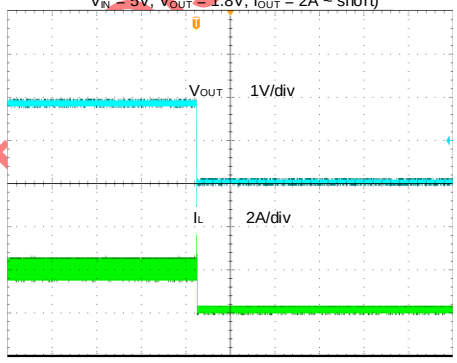
Time (4ms/div)

Short Circuit Protection
(SY80082FABT,SY80082LABT
V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 0A ~ short)



Time (800µs/div)

Short Circuit Protection
(SY80082FABT,SY80082LABT
V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 2A ~ short)



Time (800µs/div)

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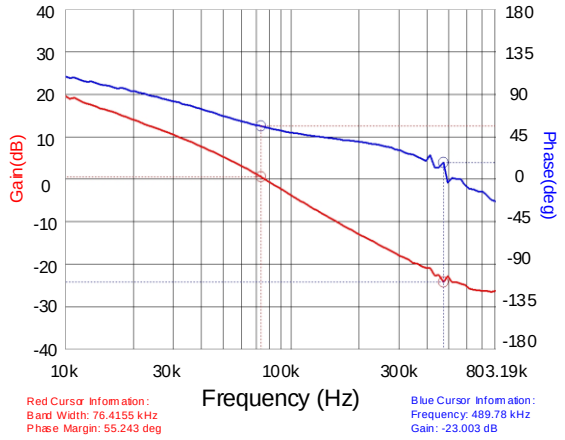
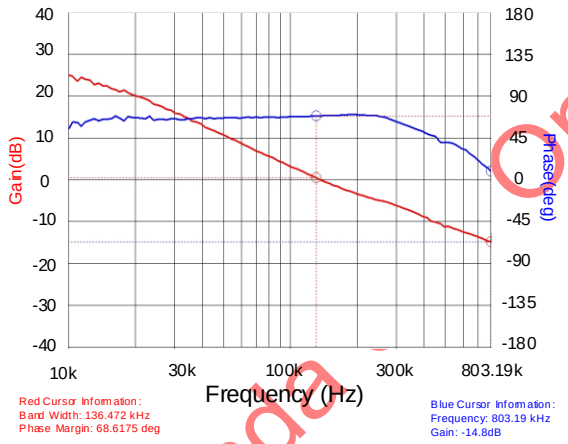
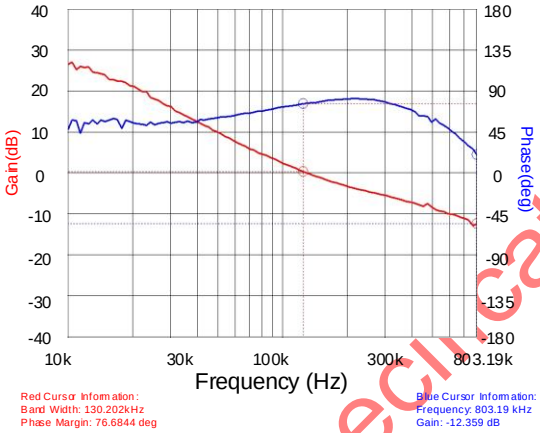
Bode Plot
(V_{IN} = 5V, V_{OUT} = 0.9V, I_{OUT} = 2A)



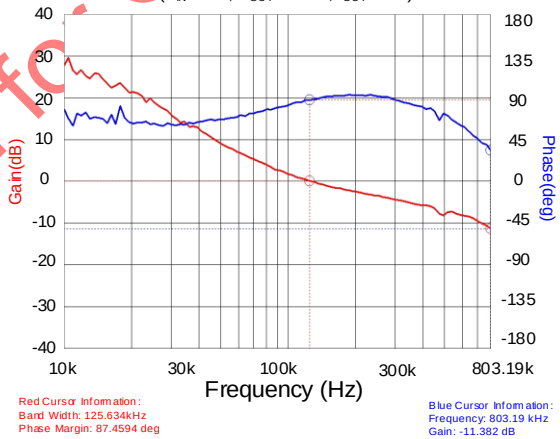
Bode Plot
(V_{IN} = 5V, V_{OUT} = 1.8V, I_{OUT} = 2A)



Bode Plot
(V_{IN} = 5V, V_{OUT} = 2.5V, I_{OUT} = 2A)



Bode Plot
(V_{IN} = 5V, V_{OUT} = 3.3V, I_{OUT} = 2A)



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Detailed Description

General Description

The SY80082x high efficiency 1.5MHz synchronous buck converter operates over a wide input voltage range of 2.5V to 5.5V, and can deliver an output current up to 2A. It integrates a top MOSFET and a bottom MOSFET with very low $R_{DS(ON)}$ to minimize conduction loss. The 1.5MHz pseudo-constant switching frequency allows small external inductor and capacitor values.

The SY80082x also provides cycle-by-cycle current limit protection output under voltage protection and over temperature protection.

Constant Off-Time and Peak Current Mode Control

The device uses instant PWM architecture to achieve fast transient response and high efficiency at light loads. It uses a constant off-time and peak current mode control strategy. When the top MOSFET's current-sense signal reaches internal V_{COMP}, the top MOSFET turns off and the bottom MOSFET turns on for a fixed period of time (constant t_{OFF}). t_{OFF} is internally calculated according to the input voltage, output voltage, and desired switching frequency (f_{SW}):

$$t_{OFF} = \frac{1 - V_{OUT}/V_{IN}}{f_{SW}}$$

The bottom MOSFET turns off after a period of t_{OFF}.

Minimum and Maximum Duty Cycle

There is minimum on-time limitation In the constant off-time architecture. The device supports low to 10% duty cycle application across the entire operating temperature range of -40˚C ~ 125˚C.

The device can support a maximum duty cycle of up to 100% across the entire operating temperature range of -40˚C ~ 125˚C.

PFM Light Load Operation

The device uses pulse-frequency modulation (PFM) operation mode under light load condition for high efficiency. Under light load conditions, typically when the load satisfies the following equation,

$$I_{OUT_CTL} = \frac{\Delta I_L}{2} = \frac{V_{OUT} \times (1 - D)}{2 \times f_{SW} \times L}$$

the current through the bottom MOSFET will ramp to near zero before the next t_{ON} time. When this occurs, the bottom MOSFET turns off, preventing recirculation current that can seriously reduce efficiency under these light load conditions. As load current is further reduced, the combined feedback and ramp signals remain much higher than the reference voltage, the instant-PWM control loop will not trigger another t_{ON} until needed, and the apparent operating switching frequency will correspondingly drop, improving efficiency. Continuous conduction mode (CCM) resumes smoothly as soon as the load current increases sufficiently for the inductor current to remain above zero at the time of the next t_{ON} cycle. The buck converter enters CCM once the load current exceeds the threshold shown in (1). Above the threshold, the switching frequency stays fairly constant over the output current range.

While in PFM mode, the output of the device doesn't require over voltage protection because the device stops switching as soon as the voltage at the FB node increases above V_{REF}, preventing the output voltage from increasing further.

Input Under Voltage Lockout (UVLO)

To prevent operation before the internal circuitry is ready and to ensure that the top and bottom MOSFETs can be properly driven, the device incorporates an input under voltage lockout protection. The device remains in a low current state and all LX node switching actions are inhibited until V_{IN} exceeds its rising threshold. At that time, if EN is enabled, the device will startup. If V_{IN} falls below $V_{IN,UVLO}$ less than the input UVLO hysteresis, the LX node switching actions will again be suppressed.

Enable Control

The EN input is a high-voltage input with logic-compatible threshold. When EN is driven above 1.0V, normal device operation is enabled. When EN is driven to less than 0.4V, the device will shut down, reducing the input current to less than 2μA.

It is not recommended to connect EN pin directly to V_{IN} or another voltage source. A resistor in a range of 1kΩ to 1MΩ should be used if EN pin is pulled high.

Soft-Start

The device incorporates an internal soft-start circuit to ramp the output to the desired voltage whenever the device is enabled. Internally, the soft-start circuit clamps the output at a low voltage and then allows the output to rise to the desired voltage over approximately 1ms, which avoids high current flow and transients during startup.

Power Good Indicator

For SY80082ABT, SY80082LABT and SY80082FABT, PG is an open drain output controlled by a window comparator connected to the feedback signal. If the voltage is higher than $V_{PG,R}$ and less than $V_{PG,OVP}$ for at least the power good delay time (low to high), PG will be set to high-impedance state.

PG should be connected to V_{IN} or another voltage source

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through a resistor (e.g., 100kΩ). After V_{IN} rises until the internal initial power is ready, the PG internal MOSFET is turned on so that PG is actively driven low before output voltage is ready. After the feedback voltage V_{FB} reaches $V_{PG,R}$, PG is set to high-impedance state after a delay time of 1μs (typ.). When V_{FB} drops to $V_{PG,F}$, or rises above $V_{PG,OVP}$, PG is driven low after a delay time of 20μs (typ.)

Fault Protection Modes

Cycle-by-Cycle Current Limit Protection
If the top MOSFET current exceeds the top current limit threshold, it will turn off and the bottom MOSFET will turn on. As a result, inductor peak current is limited.

Output Under Voltage Protection (UVP)
With output current increasing, the top MOSFET current will exceed its current limit threshold, and if the load current continues to increase, the output voltage will drop. When the output voltage falls below 50% of the regulated level, the output under voltage protection will be activated.

In this situation, SY80082AAT and SY80082ABT will operate in hiccup mode. The hiccup on-time is 2.5ms, and the hiccup off-time is 3ms. If the hard short condition is removed, the device will return to normal operation.

In this situation, SY80082LABT and SY80082FABT will enter latch off status.

Over Temperature Protection (OTP)
The device includes over temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. This will shut down the device when the junction temperature exceeds 160°C. When the junction temperature is reduced by approximately 20°C, SY80082AAT and SY80082ABT will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate thermal dissipation so that the junction temperature does not exceed the OTP threshold.

Application Information

The following paragraphs provide information on the selection of the external components needed to meet the targeted application specifications.

Feedback Resistor Divider R_H and R_L
Choose R_H and R_L to program the proper output voltage. A value between 1kΩ and 1MΩ is recommended for both resistors to minimize power consumption under light loads. As an example, if V_{OUT} = 1.8V and R_H selected value is 20kΩ, R_L can be calculated as follows:

$$R_L = \frac{0.6}{V_{OUT} - 0.6V} \times R_H$$

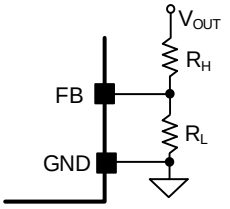

Figure4. Feedback Resistor Divider

With a calculated value of 10kΩ for R_L, a standard 1% 10kΩ resistor is selected. Recommended R_L resistance is no larger than 10kΩ.

Input Capacitor C_{IN}
For the best performance, select a typical X5R or better grade ceramic capacitor with a 10V rating, and at least 10μF capacitance. The capacitor should be placed as close as possible to the device, while also minimizing the loop area formed by C_{IN} and the IN/GND pins.

When selecting an input capacitor, ensure that its voltage rating is at least 20% greater than the maximum voltage of the input supply. X5R or X7R dielectric types are the most often selected due to their small size, low cost, surge current capability, and high RMS current rating over a wide temperature and voltage range.

In situations where the input rail is supplied through long wires, it is recommended to add some bulk capacitance like electrolytic, tantalum or polymer type capacitors to reduce the overshoot and ringing caused by the added parasitic inductance.

Consider the RMS current rating of the input capacitor, paralleling additional capacitors if required to meet the calculated RMS ripple current.

$$I_{CIN_RMS} = I_{OUT} \times \sqrt{D \times (1 - D)}$$

The worst-case condition occurs at D = 0.5, then

$$I_{CIN_RMS,MAX} = \frac{I_{OUT}}{2}$$

For simplicity, use an input capacitor with an RMS current rating greater than 50% of the maximum load current. The input capacitor value determines the input voltage ripple of the converter. If there is a voltage ripple requirement in the system, choose an appropriate input capacitor that meets the specification.

Given the very low ESR and ESL of ceramic capacitors, the input voltage ripple can be estimated using the formula:

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$$V_{CIN_RIPPLE,CAP} = \frac{I_{OUT}}{f_{SW} \times C_{IN}} \times D \times (1 - D)$$

The worst-case condition occurs at D = 0.5, then

$$V_{CIN_RIPPLE,CAP,MAX} = \frac{I_{OUT}}{4 \times f_{SW} \times C_{IN}}$$

The capacitance value is less important than the RMS current rating. A single 10µF X5R capacitor is sufficient for most applications.

Output Inductor L

Consider the following when choosing this inductor:

1) Choose the inductance to provide a ripple current that is approximately 40% of the maximum output current. The recommended inductance is calculated as:

$$L = \frac{V_{OUT}(1 - V_{OUT} / V_{IN,MAX})}{f_{sw} \times I_{OUT,MAX} \times 0.4}$$

where f_{SW} is the switching frequency and $I_{OUT,MAX}$ is the maximum load current.

The device has high tolerance for ripple current amplitude variation. As a result, the final choice of inductance can vary slightly from the calculated value with no significant performance impact.

2) The inductor's saturation current rating must be greater than the peak inductor current under full load:

$$I_{SAT,MIN} > I_{OUT,MAX} + \frac{V_{OUT}(1 - V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. Use an inductor with DCR less than 60mΩ to achieve good overall efficiency.

Output Capacitor C_{OUT}

Select the output capacitor C_{OUT} to handle the output ripple requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting C_{OUT}. For the best performance, use a X5R or better grade ceramic capacitor with a 6.3V rating, and capacitance of at least 10µF.

For applications where the design must meet stringent ripple requirements, the following considerations must be followed.

The output voltage ripple at the switching frequency is caused by the inductor current ripple (ΔI_L) on the output capacitor's ESR (ESR ripple), as well as the stored charge (capacitive ripple). When calculating total ripple, consider both.

$$V_{RIPPLE,ESR} = \Delta I_L \times ESR$$

$$V_{RIPPLE,CAP} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

The measured capacitive ripple might be higher than the theoretical value because the effective capacitance for ceramic capacitors decreases with the voltage across its terminals. The voltage derating is usually included as a chart in the capacitor datasheet, and the ripple can be recalculated after taking the target output voltage into account.

Feedforward Capacitor C_{FF}

The device integrates the compensation components to achieve good stability and fast transient responses. In some applications, adding a ceramic capacitor (feedforward capacitor C_{FF}) in parallel with R_H may further speed up the load transient response.

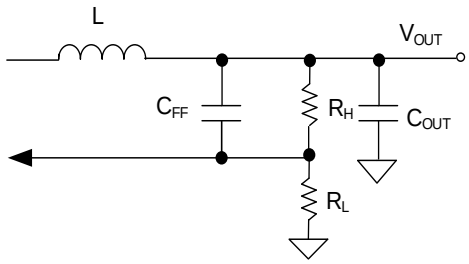

Figure5. Feedforward Network

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Application Schematic (V_{OUT} = 1.8V)

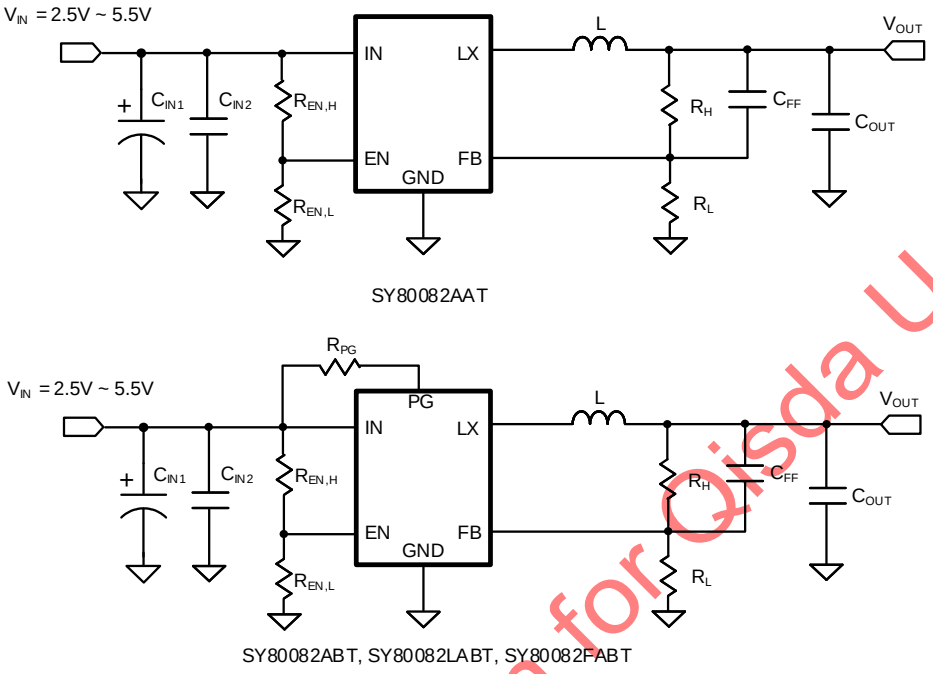

Figure6. Schematic Diagram

BOM List

Reference Designator	Description	Part Number	Manufacturer
C_{IN1}	47µF/50V Electrolytic Capacitor		
C_{IN2}	10µF/10V/X5R, 0805	GRM21BR71A106KA73L	mµRata
C_{OUT}	10µF/10V/X5R, 0805	GRM21BR71A106KA73L	mµRata
C_{FF}	22pF/50V/C0G, 0603	GRM1885C1H220JA01D	mµRata
L	1.0µH/inductor	0420CDMCCDS-1R0MC	Sumida
R_H	20kΩ, 1%, 0603		
R_L	10kΩ, 1%, 0603		
$R_{EN,H}$	10kΩ, 1%, 0603		
$R_{EN,L}$	1MΩ, 1%, 0603		
R_{PG}	100kΩ, 1%, 0603		

Recommend Component Values for Typical Applications

V_{OUT}(V)	R_H(kΩ)	R_L(kΩ)	C_{FF}(pF)	L/Part Number	C_{OUT}
0.9	5	10	22	0420CDMCCDS-R68MC	22µF/10V/X5R, 0805
1.8	20	10	22	0420CDMCCDS-1R0MC	10µF/10V/X5R, 0805
2.5	31.6	10	22	0420CDMCCDS-1R0MC	10µF/10V/X5R, 0805
3.3	45.3	10	22	0420CDMCCDS-1R0MC	10µF/10V/X5R, 0805

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Layout Design

Follow these PCB layout guidelines for optimal performance and thermal dissipation:

Input Capacitor: Place the input capacitor very close to IN and GND pins, minimizing the loop formed by these connections. The input capacitor should be connected to the IN and GND pins using a wide copper area.

Output Capacitor: Connect the C_{OUT} negative terminal to the GND pin using wide copper traces instead of vias, in order to achieve better accuracy and stability of the output voltage.

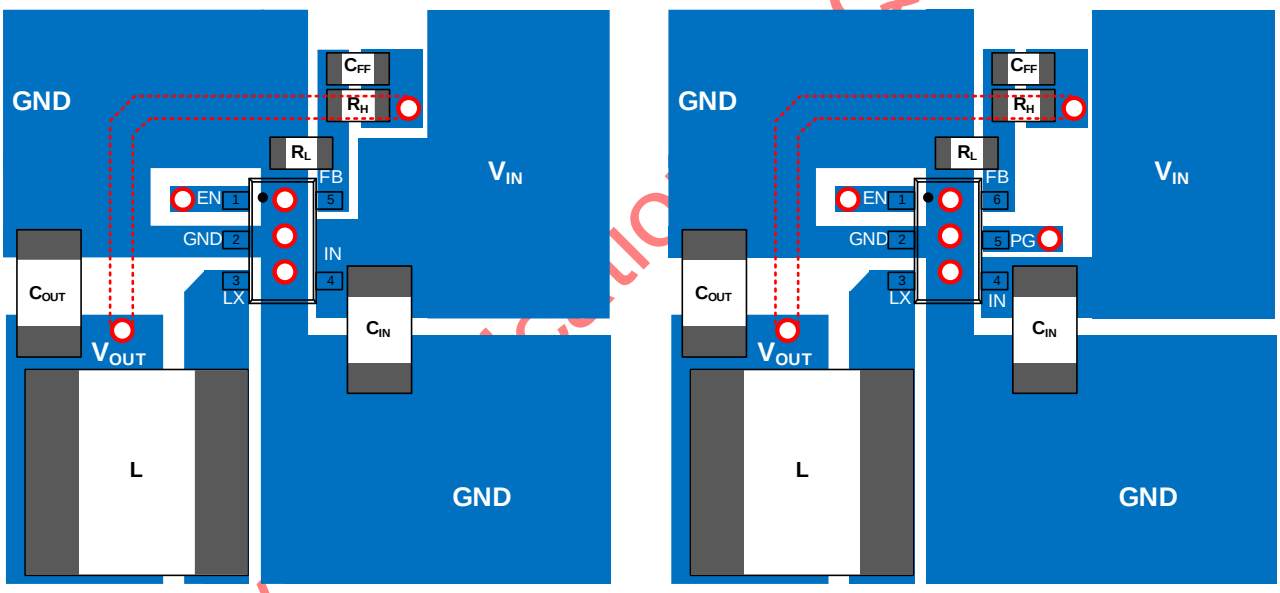
Feedback Network: Place the feedback components (R_H, R_L and C_{FF}) as close to the FB pin as possible. Avoid routing the feedback line near LX, or other high-frequency signals as it is noise-sensitive. Use a Kelvin connection to connect with C_{OUT} rather than the inductor output terminal.

LX Connection: Keep the LX area small to prevent excessive EMI, while providing a wide copper trace to minimize parasitic resistance and inductance.

EN Signal: It is **not** recommended to connect EN pin directly to V_{IN} or another voltage source. A resistor in a range of 1kΩ to 1MΩ should be used if EN pin is pulled high.

GND Vias: Place an adequate number of vias on the GND layer around the device for better thermal performance.

PCB Board: To achieve the best thermal and noise performance, maximize the PCB copper area connecting to the GND pin. A ground plane is highly recommended if possible. Connect the ground pad to a large copper area to enhance thermal performance.



SY80082AAT SY80082ABT, SY80082LABT, SY80082FABT

Figure7. Suggested PCB Layout

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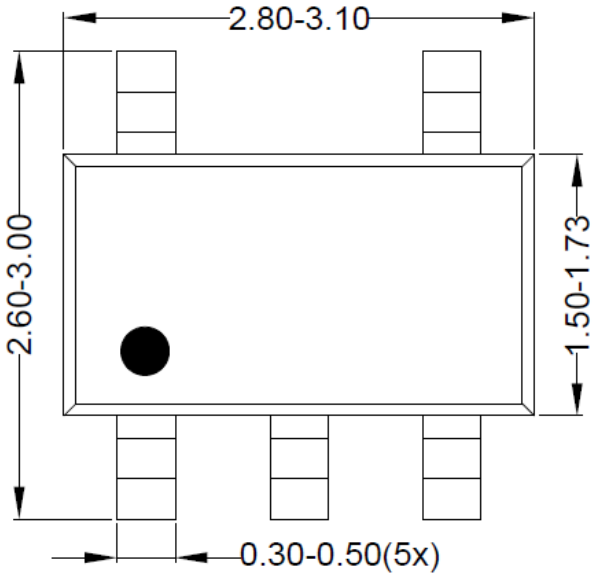
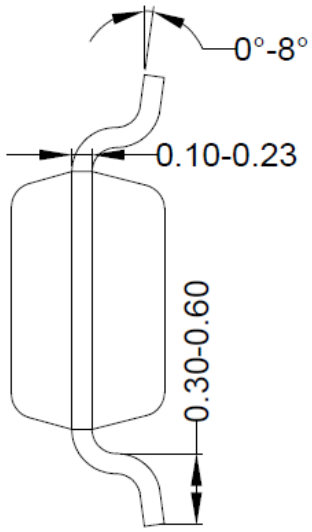
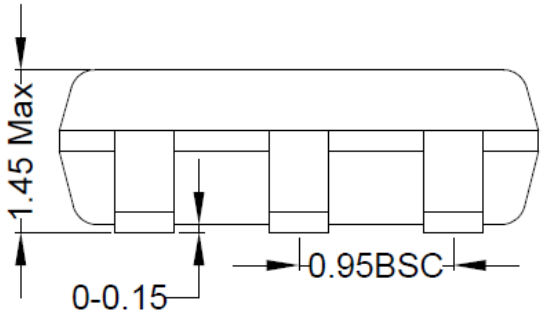
SOT23-5 Package Outline Drawing



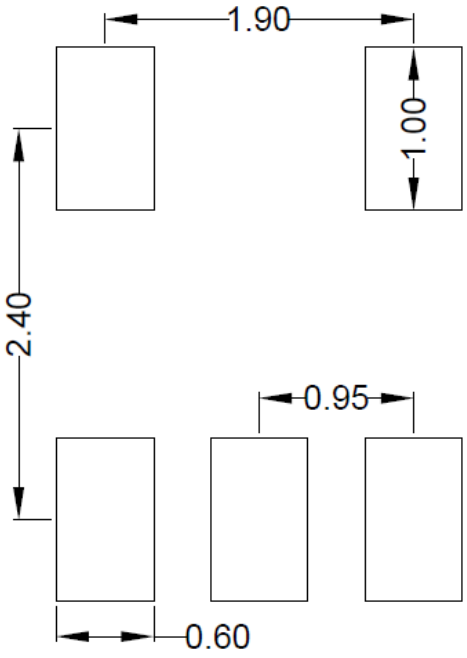
Top view



Side view



Front view



Recommended PCB pad Layout
(Reference only)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

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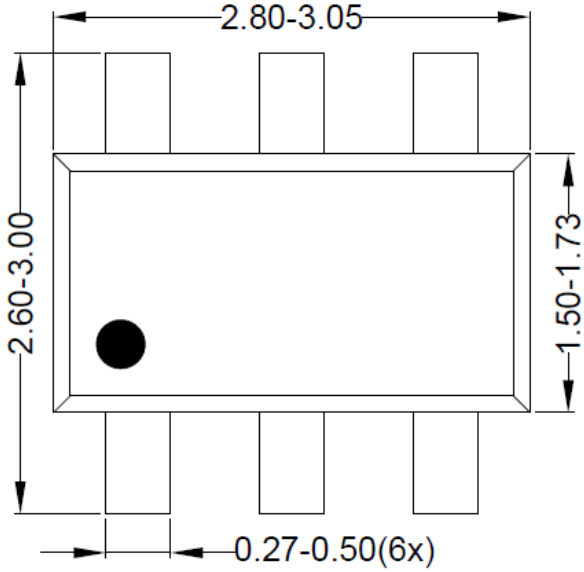
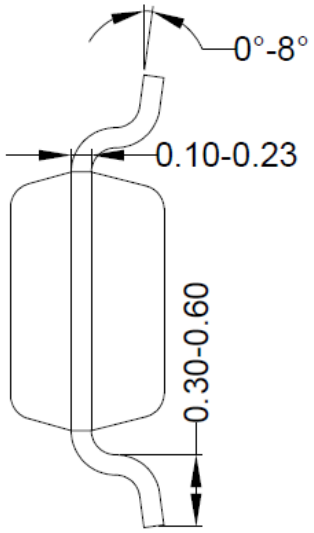
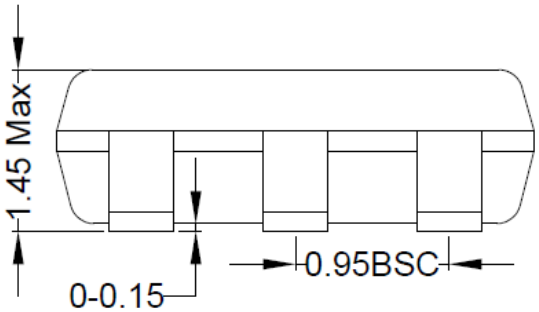
SOT23-6 Package Outline & PCB layout



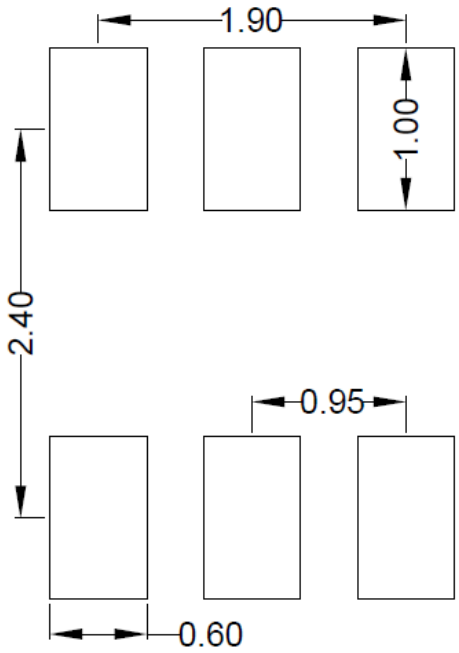
Top View



Side View



Front View



Recommended PCB Layout (Reference only)

Notes: All dimension in millimeter and exclude mold flash & metal burr.

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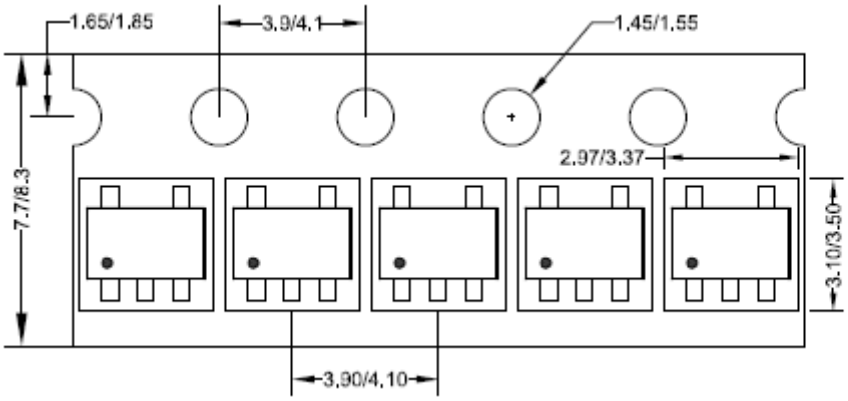
Taping & Reel Specification

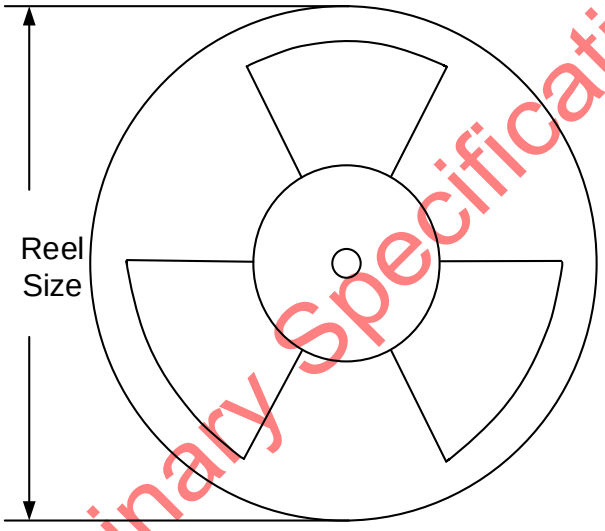
SOT23-5

1. Taping orientation



Feeding direction ⟶

2. Carrier Tape & Reel specification for packages



Package Type	Tape Width (mm)	Pocket Pitch (mm)	Reel Size (Inch)	Trailer Length (mm)	Leader Length (mm)	Qty per Reel
SOT23-5	8	4	7	280	160	3000

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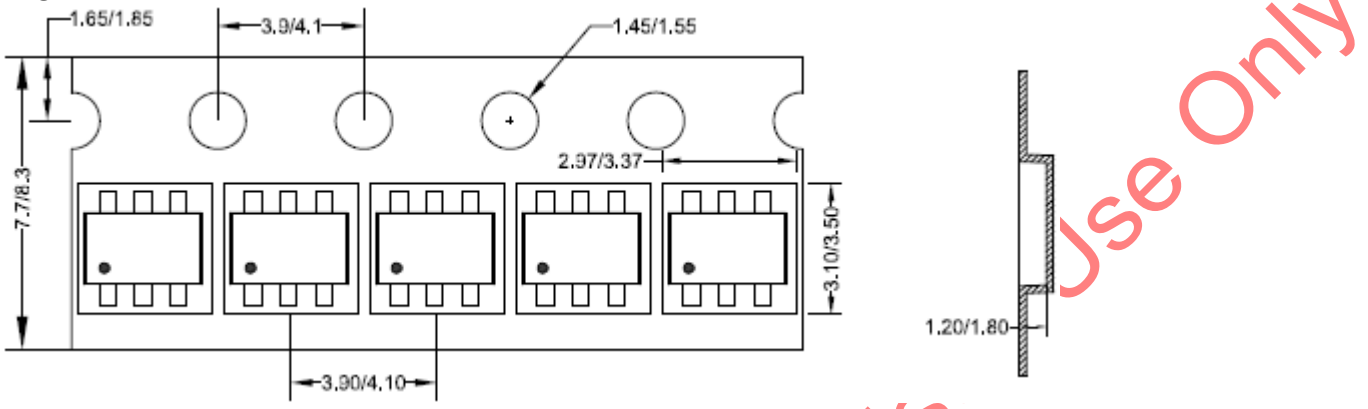
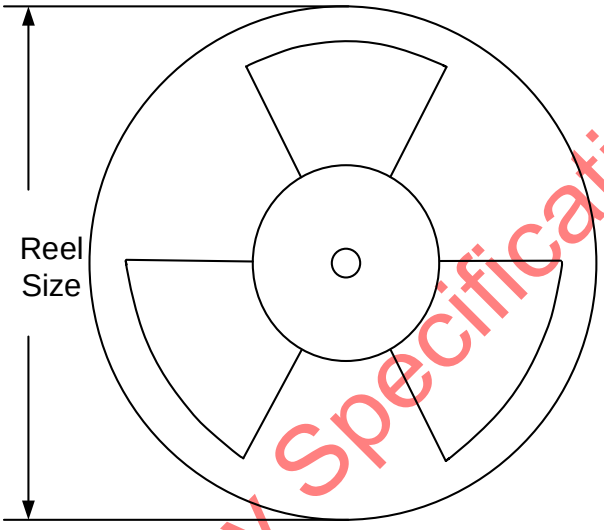
SOT23-6

1. Taping orientation



2. Carrier Tape & Reel specification for packages



Package Type	Tape Width (mm)	Pocket Pitch (mm)	Reel Size (Inch)	Trailer Length (mm)	Leader Length (mm)	Qty per Reel
SOT23-6	8	4	7	280	160	3000

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