SPECIFICATION
FOR
APPROVAL

( ) **Preliminary Specification**

(●) **Final Specification**

Title	27" QHD OLED

BUYER	General
MODEL	

SUPPLIER	LG Display Co., Ltd.
*MODEL	LW270AHQ
SUFFIX	ERG2

APPROVED BY	SIGNATURE DATE
/	
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/	

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▶ Module site : LG Display in VH (Lot E, Trang Due Industrial zone, Dinh Vu – Cat Hai EZ, Hong Phong commune, An Duong District, Hai Phong City, Vietnam)

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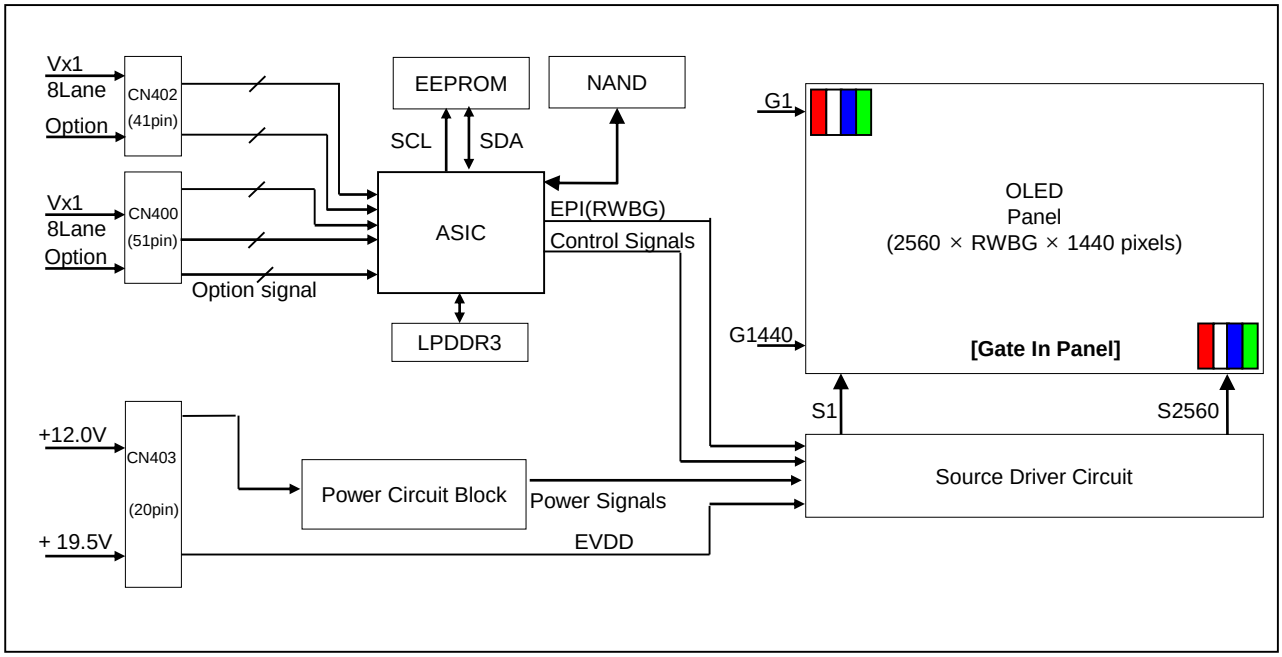
RECORD OF REVISIONS

Revision No.	Revision Date	Page	Description
0.1	Mar. 21. 2022	-	Preliminary Specification (First Draft)
0.2	Mar. 28. 2022	11	VRR Frequency Spec update
0.3	May. 09. 2022	6	Update Electric characteristic Specification
		-	Delete Timing Specification of 120Hz and 60Hz
0.4	June. 17. 2022	6	Add Power Consumption of CLASP standard
		7	Update Signal Pin Configuration
		16	Change T2 and T6 of Power sequence
		17	Add content of OFF-RS operation to Note
		18	Update content to Note
		21-22	Add Optical characteristic Specification
		33	Add Appropriate Condition for Commerical Display
0.5	July. 28. 2022	6	Update Power Consumption
		21	Delete min Specification of Color Gamut
		30, 34	Update Packing size and Pallet Ass'y
0.6	Oct. 06. 2022	16, 17, 20	Update Power Sequence
		21, 22, 46	Update Optical Specification and GtoG Spec and Measuring Method
		34	Update Pallet Assembly
		35	Update Serial Label
		38~41	Update APPENDIX - V. (Pull up/down value of option pins)
		45	Update PLC curve parameter
0.7	Oct. 22. 2022	16	Add Note. (T5 recommend for using power adapter)
		17	Add Note. (OFFRS recommend)
		-	Delete Contents of Appropriate Condition for Commercial Display
0.8	Nov. 22. 2022	19	Delete T6 of QSM sequence
		46	Update GtoG result
1.0	Dec. 27. 2022	-	Final Specification
1.1	Jun. 29. 2023	33	Change Box shape

1. General Description

The LW270AHQ is a Color Active Matrix Organic Light Emitting Diode Display (OLED).
The matrix employs Oxide Thin Film Transistor as the active element. It is a Bottom emission display type.
It has a 27 inch diagonally measured active display area with QHD resolution (1440 vertical by 2560 horizontal pixel array).
Each pixel is divided into Red, Green, Blue and White sub-pixels or dots which are arrayed in vertical stripes.
Gray scale or the luminance of the sub-pixel color is determined with a 10-bit gray scale signal for each dot.
Therefore, it can present a palette of more than 1.07B(true) colors.
It has been designed to apply the 10-bit 16-lane V by One interface.
It is intended to support Gaming Display where high brightness, super wide viewing angle,
high color gamut, high color depth and fast response time are important.



General Features

Active Screen Size	26.50 inch (673.2mm) diagonal
Outline Dimension (Typ.)	604.42(H) x 350.62 (V) × 5.4 (B)㎜
Pixel Pitch	0.2292 mm x 0.2292 mm
Pixel Format	2560 horiz. by 1440 vert. Pixels, RWBG stripe arrangement
Color Depth	10bit(R), 1.07Billion colors
Luminance, White	450 / 150 cd/m^2 (Center 1point ,Typ.)
Color Viewing Angle	R/L 120 (min.), U/D 120 (min.) (Δu'v' ≤ 0.025)
Power Consumption	25.15W (Typ.) [Logic: 11.65W, EVDD = 13.5W] @ IEC62087]
Weight	3.2Kg (Typ.)
Display Mode	Normally black
Surface Treatment	Anti-Glare Low-Reflection of the front polarizer (Reflectance 2%, Haze 35%)

2. Absolute Maximum Ratings

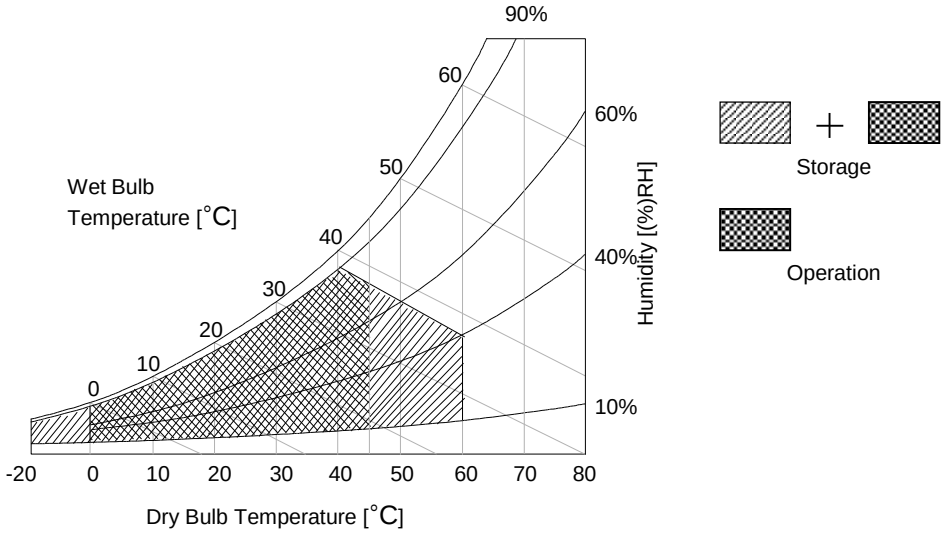
The following items are maximum values which, if exceeded, may cause faulty operation or damage to the OLED module.

Table 1. Absolute Maximum Ratings

Parameter		Symbol	Value		Unit	Note
			Min	Max		
Power Input Voltage	Logic	VDD	-0.3	+14.0	VDC	1
	EVDD	EVDD	-0.3	+ 26.0	VDC	
T-Con Option Selection Voltage		VLOGIC	-0.3	+3.7	VDC	
Operating Temperature		TOP	0	+45	˚C	2
Storage Temperature		TST	-20	+60	˚C	
Operating Ambient Humidity		HOP	10	90	%RH	2
Storage Humidity		HST	10	90	%RH	

Note:

1. Ambient temperature condition (Ta = 25 ± 2 ˚C)
2. Temperature and relative humidity range are shown in the figure below.
   Wet bulb temperature should be Max 39˚C, and no condensation of water.



3. Electrical Specifications

3-1. Electrical Characteristics

It requires two power inputs. One is employed to power for the circuit. The other is used for the EVDD.

Table 2. Electrical Characteristics

Parameter	Symbol		Values			Unit	Notes
			Min	Typ	Max		
Power Input Voltage	VDD		10.8	12.0	13.2	V	
	EVDD		18.5	19.5	20.5		
Power Input Current	I_{VDD}		-	0.97	1.07	A	1-1/1-2
			-	1.48	1.63		2
	I_{EVDD}		-	0.85	0.98		1-1
			-	0.83	0.95		1-2
			-	1.90	2.09		3
T-CON Option Voltage	V_{IL}		0	-	0.8	V	
	V_{IH}		2.7	-	3.6	V	
Power Consumption	P_{VDD}		-	11.65	12.82	Watt	1-1/1-2
			-	17.76	19.56		2
	P_{EVDD}		-	13.5	15.5		1-1
				13.1	15.1		1-2
			-	37.05	40.76		3
Rush current	I_{RUSH}	I_{RUSH_VDD}	-	-	7	A	
		I_{RUSH_EVDD}	-	-	15		
		T_{RUSH_VDD}	-	-	100	us	
		T_{RUSH_EVDD}	-	-	2	ms	

Note

1-1. The specified current and power consumption are under the VDD=12.0V, EVDD=19.5V Ta=25 ± 2°C, f_V=240Hz condition whereas standard moving picture(IEC62087) is displayed and f_V is the frame frequency.
1-2. The specified current and power consumption are under the VDD=12.0V, EVDD=19.5V Ta=25 ± 2°C, f_V=240Hz condition whereas standard moving picture(CLASP) is displayed and f_V is the frame frequency.
2. The current (I_{VDD}) is specified at the maximum current pattern (1by1 Horizontal Pattern) and under the VDD=12.0V, EVDD=19.5V Ta=25 ± 2°C condition.
3. The current (I_{EVDD}) is specified at the maximum current pattern (Secondary Color Pattern) and under the VDD=12.0V, EVDD=19.5V Ta=25 ± 2°C condition.

3-2. Interface Connections

This OLED module employs two kinds of interface connection, 51-pin connector and 41-pin connector are used for the module signals and 20-pin connectors are used for the module powers.

3-2-1. OLED Module (Signals)

- Module Connector(CN400): FI-RE51S-HF(JAE) or 05030WR-H51B (Yeonho) or GT05S-51S-H38(LSM)
- Mating Connector : FI-RE51HL(JAE) or compatible

Table 3. Module Connector(CN400) Pin Configuration

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	NC (Reserved)	No Connection (Reserved)	27	GND	Ground
2	NC (Reserved)	No Connection (Reserved)	28	Rx0n	V-by-One HS Data Lane 0
3	NC (Reserved)	No Connection (Reserved)	29	Rx0p	V-by-One HS Data Lane 0
4	NC (Reserved)	No Connection (Reserved)	30	GND	Ground
5	NC	No Connection	31	Rx1n	V-by-One HS Data Lane 1
6	NC (Reserved)	No Connection (Reserved)	32	Rx1p	V-by-One HS Data Lane 1
7	NC	No Connection	33	GND	Ground
8	NC	No Connection	34	Rx2n	V-by-One HS Data Lane 2
9	NC (Reserved)	No Connection (Reserved)	35	Rx2p	V-by-One HS Data Lane 2
10	JB&Off-RS Power_off done	JB&Off-RS&Power_off done (H), Set ← Module	36	GND	Ground
11	AC_DET	AC_DET (H= On), Set → Module	37	Rx3n	V-by-One HS Data Lane 3
12	Error Detection	H=Error, L=Normal (note 4)	38	Rx3p	V-by-One HS Data Lane 3
13	I2C-SDA1	I2C for Customer	39	GND	Ground
14	I2C-SCL1		40	Rx4n	V-by-One HS Data Lane 4
15	Data Format 0	Data Format[1:0] (note5, Default: 00) 00:1-div, 01:2-div, 10:4-div, 11:8-div	41	Rx4p	V-by-One HS Data Lane 4
16	Data Format 1		42	GND	Ground
17	NC	No Connection	43	Rx5n	V-by-One HS Data Lane 5
18	I2C-SDA	I2C for Customer	44	Rx5p	V-by-One HS Data Lane 5
19	I2C-SCL		45	GND	Ground
20	EVDD DET	EVDD reset, Set ← Module	46	Rx6n	V-by-One HS Data Lane 6
21	NC	No Connection	47	Rx6p	V-by-One HS Data Lane 6
22	GND	AGP0 (note 6)	48	GND	Ground
23	GND	AGP1 (note 6)	49	Rx7n	V-by-One HS Data Lane 7
24	GND	Ground	50	Rx7p	V-by-One HS Data Lane 7
25	HTPDN	Hot plug detect	51	GND	Ground
26	LOCKN	Lock detect	-	-	-

Notes :
1. All GND (ground) pins should be connected together.
2. All Input levels of V-by-One signals are based on the V-by-One HS Standard.
3. Specific pin No. **#10** is used for compensation when power turn off.
4. Specific pin No. **#12** is used for “Power Error detection” of the OLED module.
5. Specific pins No. **#15** and **#16** are Vx1 Input Format. This module can support 1~8 division mode (Please see the Appendix VI for more information.)
6. Specific pins No. **#22** and **#23** are used for “No signal detection” of system signal interface. It should be GND for NSB (No Signal Black) while the system interface signal is not. If this pin is “H”, OLED module displays AGP (Auto Generation Pattern).
7. **#5, #7, #8, #17, #21** NC (No Connection) : These pins are used only for LGD (Do not connect)

- Module Connector (CN402) : FI-RE41S-HF(JAE) or FI-RXE41S-HF(JAE) or 05030WR-H41B5(Yeonho)
- Mating Connector : FI-RE41HL(JAE) or compatible

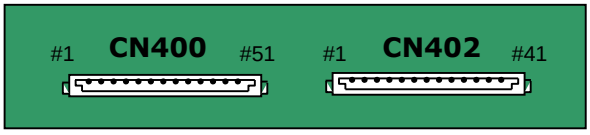
Table 4. Module Connector(CN402) Pin Configuration

No	Symbol	Description	No	Symbol	Description
1	GND	Ground	22	GND	Ground
2	Rx8n	V-by-One HS Data Lane 8	23	Rx15n	V-by-One HS Data Lane 15
3	Rx8p	V-by-One HS Data Lane 8	24	Rx15p	V-by-One HS Data Lane 15
4	GND	Ground	25	GND	Ground
5	Rx9n	V-by-One HS Data Lane 9	26	NC	No Connection
6	Rx9p	V-by-One HS Data Lane 9	27	NC	No Connection
7	GND	Ground	28	NC	No Connection
8	Rx10n	V-by-One HS Data Lane 10	29	NC	No Connection
9	Rx10p	V-by-One HS Data Lane 10	30	NC	No Connection
10	GND	Ground	31	NC	No Connection
11	Rx11n	V-by-One HS Data Lane 11	32	NC	No Connection
12	Rx11p	V-by-One HS Data Lane 11	33	NC	No Connection
13	GND	Ground	34	NC	No Connection
14	Rx12n	V-by-One HS Data Lane 12	35	NC	No Connection
15	Rx12p	V-by-One HS Data Lane 12	36	NC	No Connection
16	GND	Ground	37	NC	No Connection
17	Rx13n	V-by-One HS Data Lane 13	38	NC	No Connection
18	Rx13p	V-by-One HS Data Lane 13	39	QSMEN	QSMEN (Set→Module)
19	GND	Ground	40	ON_RF	ON_RF_DONE (Set ← Module)
20	Rx14n	V-by-One HS Data Lane 14	41	NC	No Connection
21	Rx14p	V-by-One HS Data Lane 14	-		

Notes :

1. All GND (ground) pins should be connected together.
2. **#26~#37, #41** NC (No Connection) : These pins are used only for LGD (Do not connect)

◆ **Rear view of OLED Module**



< Top view of PCB >

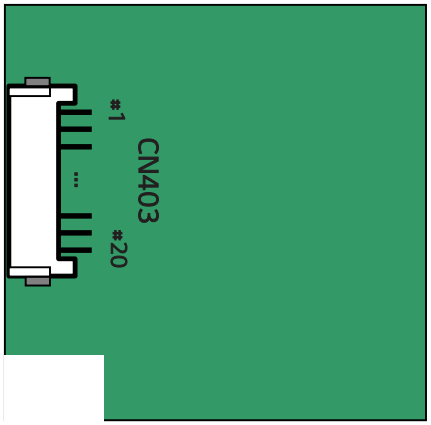
3-2-2. OLED Module (Powers)

- Power (EVDD & VDD) Connector(CN403): 12507WR-H20G (manufactured by Yeon Ho)
- Mating Connector : 12507HS-H20G1 (manufactured by Yeon Ho)

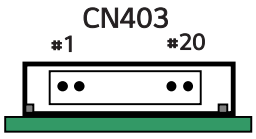
Table 5. EVDD / VDD Connector(CN403) Pin Configuration

No	Symbol	Description
1	Vin	Power Supply +12V
2	Vin	Power Supply +12V
3	Vin	Power Supply +12V
4	Vin	Power Supply +12V
5	Vin	Power Supply +12V
6	GND	Ground
7	GND	Ground
8	GND	Ground
9	GND	Ground
10	GND	Ground
11	EVSS	OLED Panel Ground
12	EVSS	OLED Panel Ground
13	EVSS	OLED Panel Ground
14	EVSS	OLED Panel Ground
15	EVSS	OLED Panel Ground
16	EVDD	OLED Panel Power Supply +19.5V
17	EVDD	OLED Panel Power Supply +19.5V
18	EVDD	OLED Panel Power Supply +19.5V
19	EVDD	OLED Panel Power Supply +19.5V
20	EVDD	OLED Panel Power Supply +19.5V

◆ **Rear view of OLED Module**



< Top view of PCB >



< Side view of PCB >

3-3. Signal Timing Specifications

Table 6 shows the signal timing required at the input of the V-by-One transmitter. All of the interface signal timings should be satisfied with the following specification for normal operation.

Table 6-1. Timing Table(DE Only Mode)

ITEM		Symbol	Min	Typ	Max	Unit	Note
Horizontal	Display Period	t_{HV}	160	160	160	tCLK	2560 / 16
	Blank	t_{HB}	12	13	14	tCLK	1
			0.179	0.195	0.212	us	3
	Total	t_{HP}	172	173	174	tCLK	
Vertical	Display Period	t_{VV}	1440	1440	1440	Lines	
	Blank	t_{VB}	162	163	164	Lines	1
			419.6	423.7	427.8	us	3
	Total	t_{VP}	1602	1603	1604	Lines	

ITEM		Symbol	Min	Typ	Max	Unit	Note
Frequency	DCLK	f_{CLK}	65.94	66.56	67.18	MHz	1064.9 / 16
	Horizontal	f_H	383.36	384.72	386.08	KHz	1
	Vertical	f_V	239	240	241	Hz	2

Note: 1. The input of HSYNC & VSYNC signal does not have an effect on normal operation (DE Only Mode). If you use spread spectrum of EMI, add some additional clock to minimum value for clock margin.
2. The performance of the electro-optical characteristics may be influenced by variance of the vertical refresh rate and the horizontal frequency.
3. If you change the DCLK, must satisfy the minimum horizontal & vertical blank time.

※ This OLED module supports Spread Spectrum Clocking tolerance with up to 30kHz/ ±0.5%
※ Timing should be set based on clock frequency.

Table 6-2. Timing Table(240Hz VRR Mode)

ITEM		Symbol	Min	Typ	Max	Unit	Note
Horizontal	Display Period	t_{HV}	160	160	160	tCLK	2560 / 16
	Blank	t_{HB}	13	13	13	tCLK	
	Total	t_{HP}	173	173	173	tCLK	
Vertical	Display Period	t_{VV}	1440	1440	1440	Lines	
	Blank	t_{VB}	163	163	8178	Lines	
	Total	t_{VP}	1602	1603	9618	Lines	

ITEM		Symbol	Min	Typ	Max	Unit	Note
Frequency	DCLK	f_{CLK}	66.56	66.56	66.56	MHz	1064.9 / 16
	Horizontal	f_H	384.72	384.72	384.72	KHz	
	Vertical	f_V	40	240	240	Hz	

Note:

1. Only applicable to Gaming mode with VRR operation
2. The device could not work properly in case it is operated by 240Hz VRR Mode
   1) This OLED module supports adaptive sync timing only under moving picture in room temperature(25±5℃)
   2) It would not work usually under still image & reliability test.
   3) Under those condition, the phenomenon such as image sticking, flickering, flashing and dither noise in low gray could be found on the screen.

3-4. V by One Signal Specifications

3-4-1. V by One Eye Mask Specification

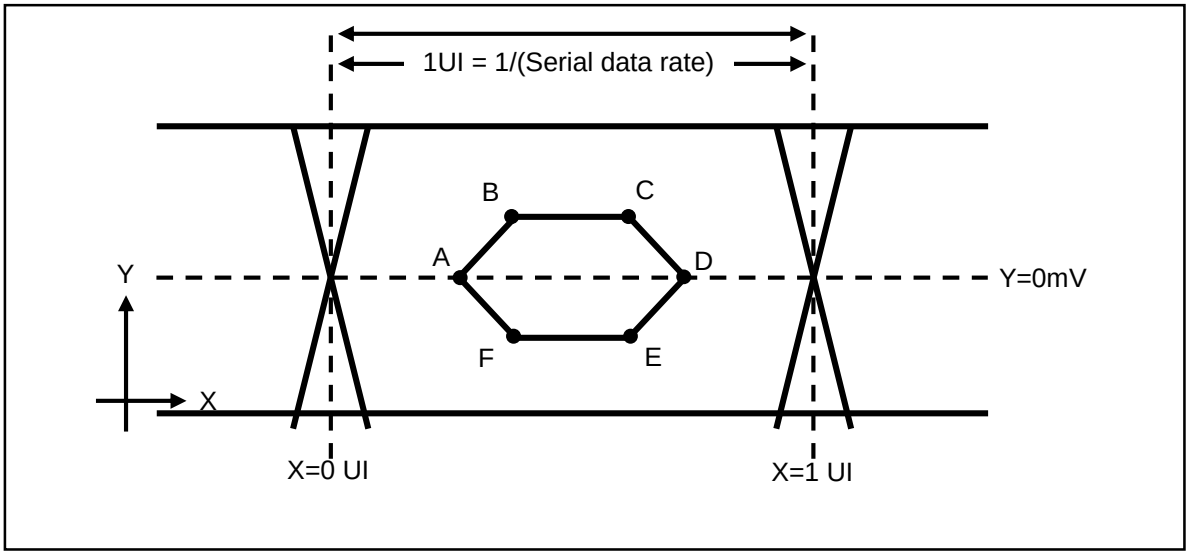


Table 7. Eye Mask Specification

	X [UI]	Note	Y [mV]	Note
A	0.25 (max)	2	0	-
B	0.30 (max)	2	50	3
C	0.70 (min)	3	50	3
D	0.75 (min)	3	0	-
E	0.70 (min)	3	|-50|	3
F	0.30 (max)	2	|-50|	3

Notes:

1.1 All Input levels of V by One signals are based on the V by One HS Standard.

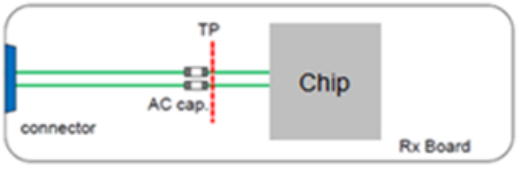
1.2 When using the Tx's Pre-Emphasis function to be set to a minimum value that meets the EYE mask spec.

2. This is allowable maximum value.

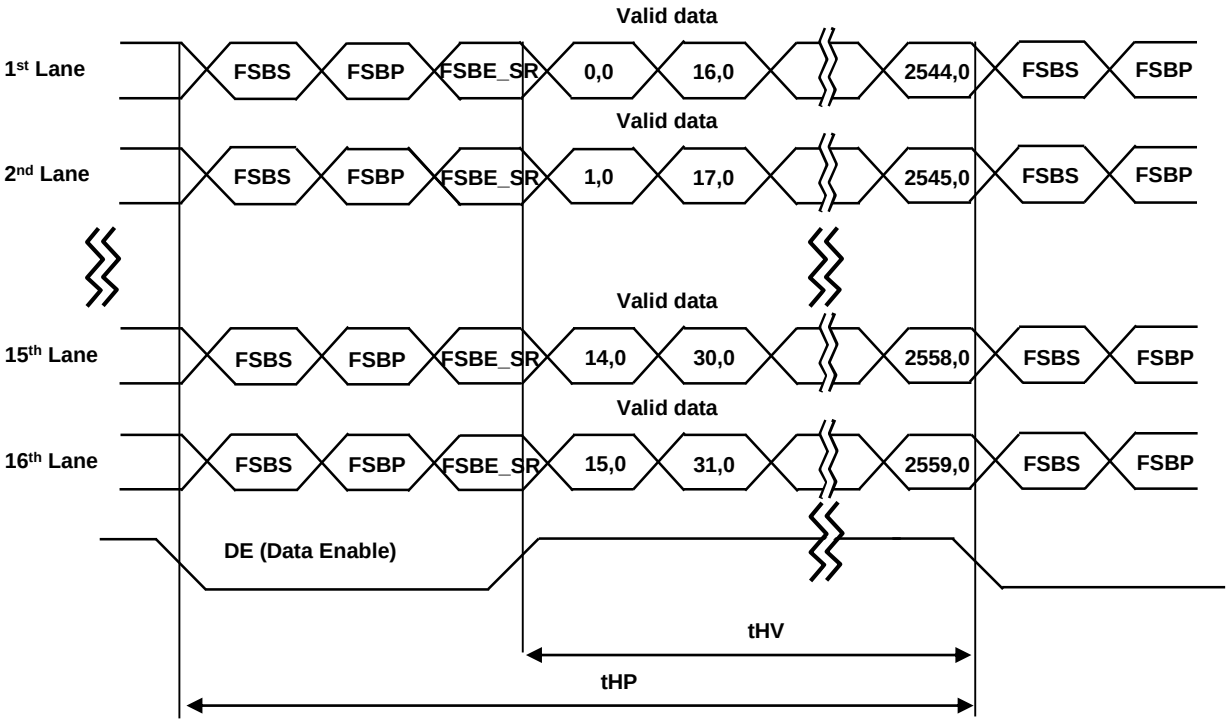
3. This is allowable minimum value.

4. The eye diagram is measured by the oscilloscope and receiver CDR characteristic must be emulated.
   - PLL type : 2nd Order
   - PLL bandwidth : 10Mhz
   - Damping Factor : 2

5. EYE mask measuring point

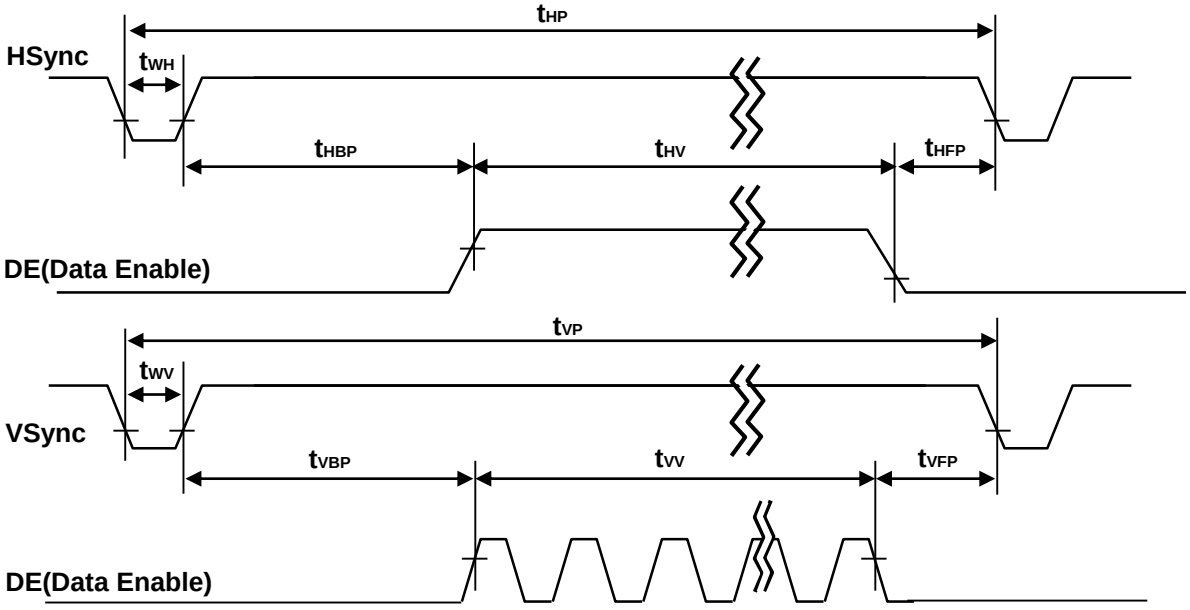


3-4-2. V by One Input Signal Timing Diagram



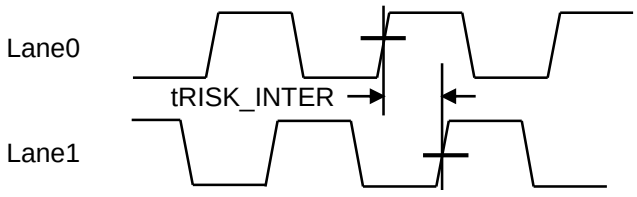
* Reference: Sync. Relation

* $t_{HB} = t_{HFP} + t_{WH} + t_{HBP}$
* $t_{VB} = t_{VFP} + t_{WV} + t_{VBP}$

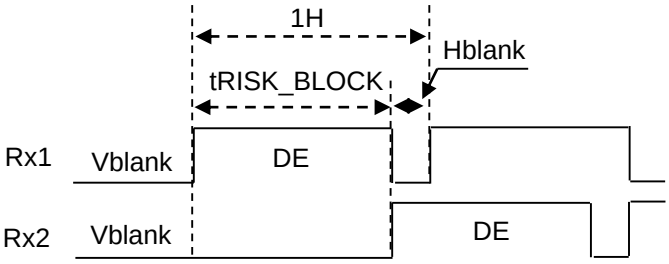


3-4-3. V by One Input Signal Characteristics

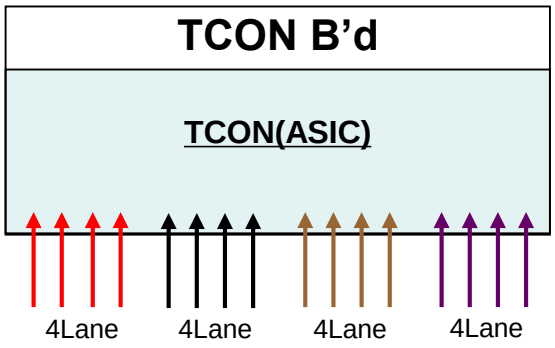
1) AC Specification



<Inter-pair skew between two lanes>



<Inter-pair skew between two sub-blocks>



<V by One Brief Diagram >

Description	Symbol	Min	Max	Unit	Note
Allowable inter-pair skew between lanes	tRISK_INTER	-	5	UI	1, 3
Allowable inter-pair skew between sub-blocks	tRISK_BLOCK	-	1	DE	1, 4

Notes: 1.1UI = 1/serial data rate

2. it is the time difference between the true and complementary single-ended signals.
3. it is the time difference of the differential voltage between any two lanes in one sub block.
4. it is the time difference of the differential voltage between any two blocks in one IP.

3-5. Color Data Reference

The brightness of each primary color (red, green, blue) is based on the 10bit gray scale data input for the color. The higher binary input, the brighter the color. Table 8 provides a reference for color versus data Input.

Table 8. Color Data Reference

Packer input & Unpacker output		30bpp RGB (10bit)
Byte0	D[0]	R[2]
	D[1]	R[3]
	D[2]	R[4]
	D[3]	R[5]
	D[4]	R[6]
	D[5]	R[7]
	D[6]	R[8]
	D[7]	R[9]
Byte1	D[8]	G[2]
	D[9]	G[3]
	D[10]	G[4]
	D[11]	G[5]
	D[12]	G[6]
	D[13]	G[7]
	D[14]	G[8]
	D[15]	G[9]
Byte2	D[16]	B[2]
	D[17]	B[3]
	D[18]	B[4]
	D[19]	B[5]
	D[20]	B[6]
	D[21]	B[7]
	D[22]	B[8]
	D[23]	B[9]
Byte3	D[24]	Don't care
	D[25]	Don't care
	D[26]	B[0]
	D[27]	B[1]
	D[28]	G[0]
	D[29]	G[1]
	D[30]	R[0]
	D[31]	R[1]

Notes 1. 30bpp RGB (10bit) is 4 byte mode

3-6. Power Sequence

3-6-1. OLED Driving Circuit

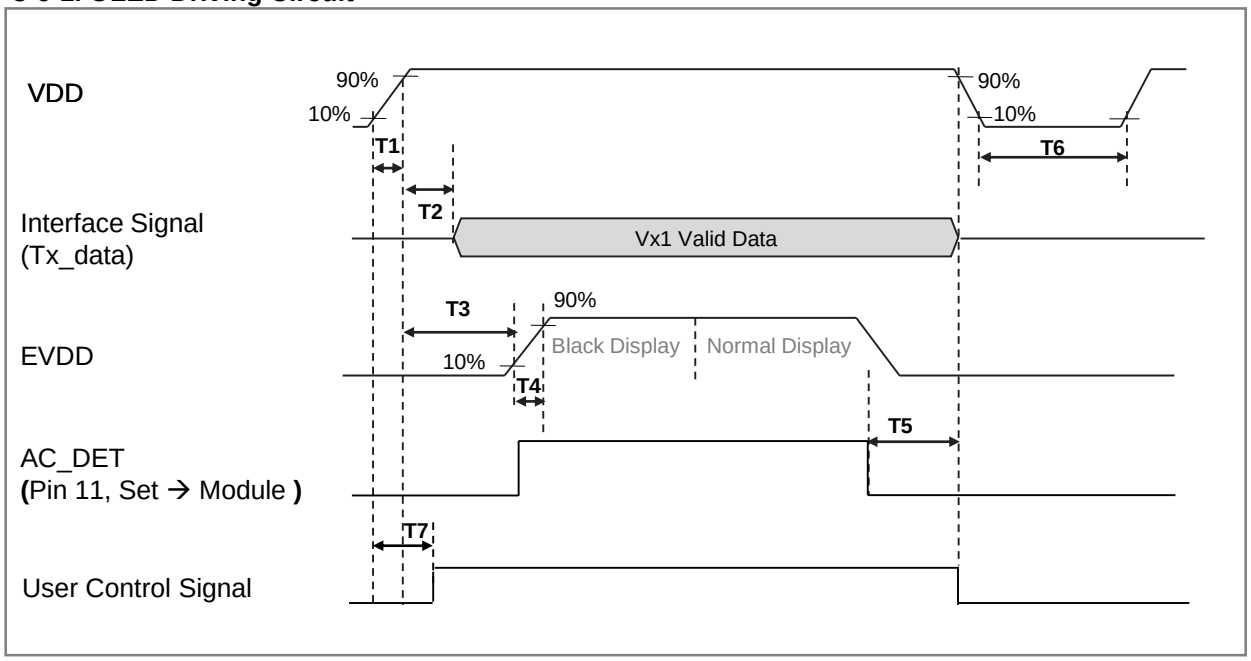


Table 9. Power Sequence

Parameter	Value			Unit	Notes
	Min	Typ	Max		
T1	1	-	35	ms	
T2	58	-	-	ms	
T3	0.7	-	-	sec	1
T4	5	-	50	ms	
T5	50	-	-	ms	
T6	1.5	-	-	sec	2
T7	0	-	T1+T2	ms	3

Note : 1. The T3 is recommended value, the case when failed to meet a minimum specification, abnormal display would be shown. There is no reliability problem. T3 should be larger than T2.

2. T6 should be measured after the module has been fully discharge between power off and on period.

3. If the on time of signals (Interface signal and user control signals) precedes the on time of Power(VDD) it will be happened abnormal display. When T7 is NC status, T7 doesn't need to be measured

4. I2C is able to be accessed from 700ms after VDD 90% rising

※ Black pattern is displayed during black display period before normal display. (ON RF Time 2.7s)

※ When the power for logic (VDD) turns on , EVDD should be less than 5V.
But, it does not matter if there is no garbage image.

※ T5 is recommendation value when using power Adapter. It causes abnormal display, Not reliability issue.

3-6-2. OFF RS Compensation Operation

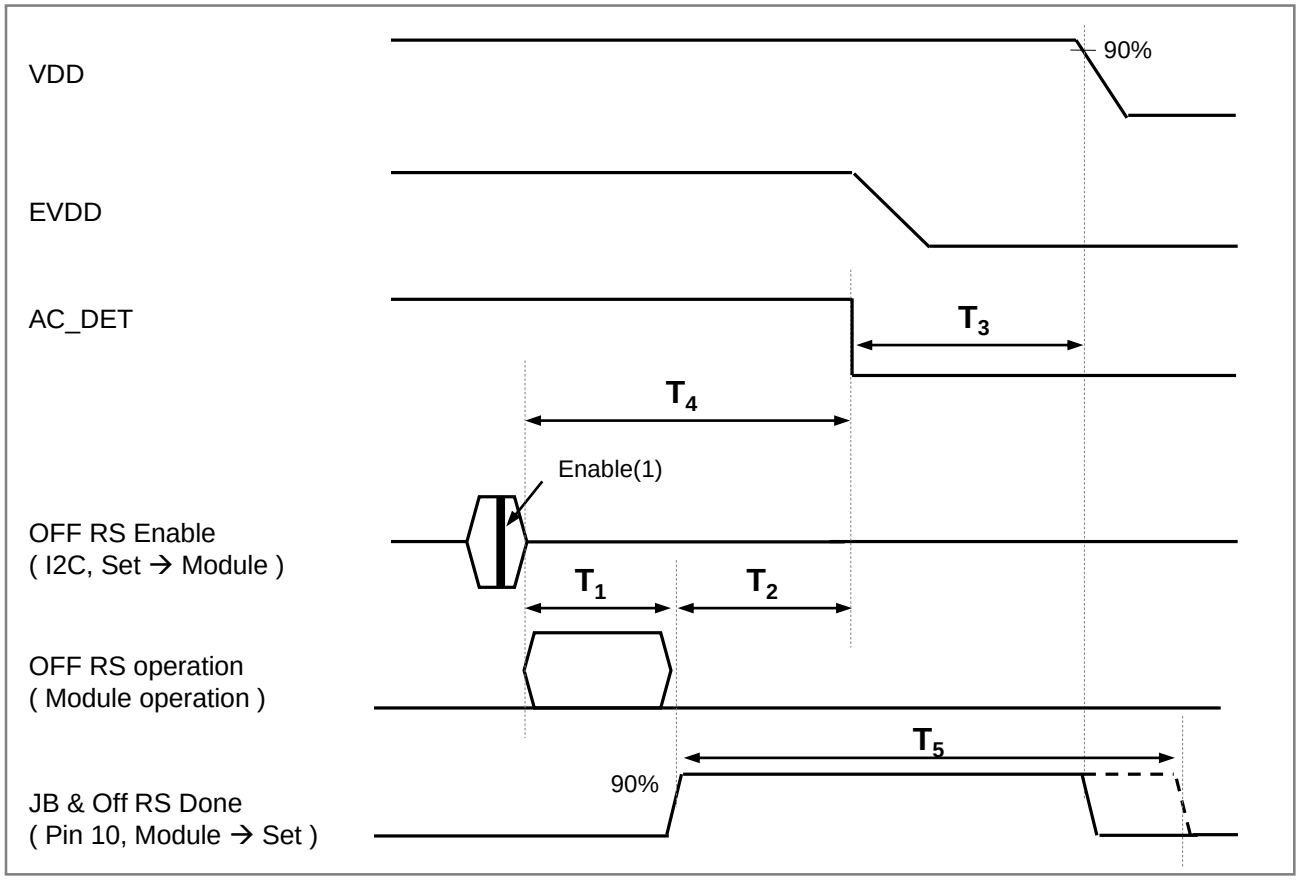


Table 10.Off-RS Power Sequence

Parameter	Value			Unit	Notes
	Min	Typ	Max		
T1	210	-	240	sec	**1**
T2	0	-	10	sec	
T3	50	-	-	ms	
T4	250	-	-	sec	2
T5	0.5	7	10	sec	

Note : 1. It is the actual RS sensing time. This timing is determined according to the characteristics of the panel. (LGD Internal timing)
2. Gaming Display system is recommended to be turned off **immediately** after T4 **min.** although Off-RS Done signal is not transferred.
3. Gaming Display system is recommended to JB and then OFFRS, sequentially.

※ When there is power on action before completing OFF RS operation, don't change OFF RS enable signal (1→0). Just do power off and power on.

※ Off RS Enable is only available during Normal Display period.
※ In order to prevent mura defects, it is recommended that customer do Off-RS in their lines.

3-6-3. JB Compensation Operation

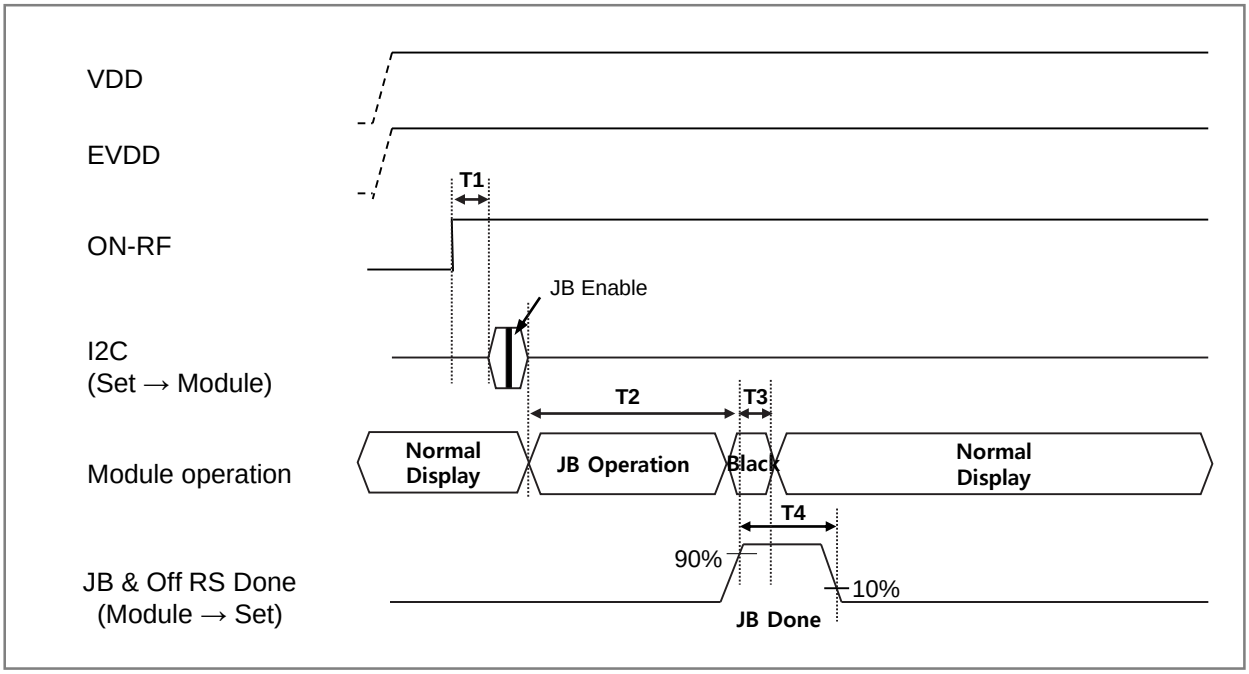


Table 11. JB Power Sequence

Parameter	Value			Unit	Notes
	Min	Typ	Max		
T1	200	-	-	ms	
T2	3	-	21	sec	
T3	415.6	-	508.0	ms	Black PTN
T4	0.5	7	10	sec	

Note : ※ T2 is the actual JB sensing time. This timing is determined according to the characteristics of the panel. (LGD Internal timing)
※ At VRR mode, T3 can change by adaptive sync timing(T3 need 19 frame) (VRR Only)
※ T3 can change by adaptive sync timing(T3 need 19 frame) (VRR only)

3-6-4. QSM Operation

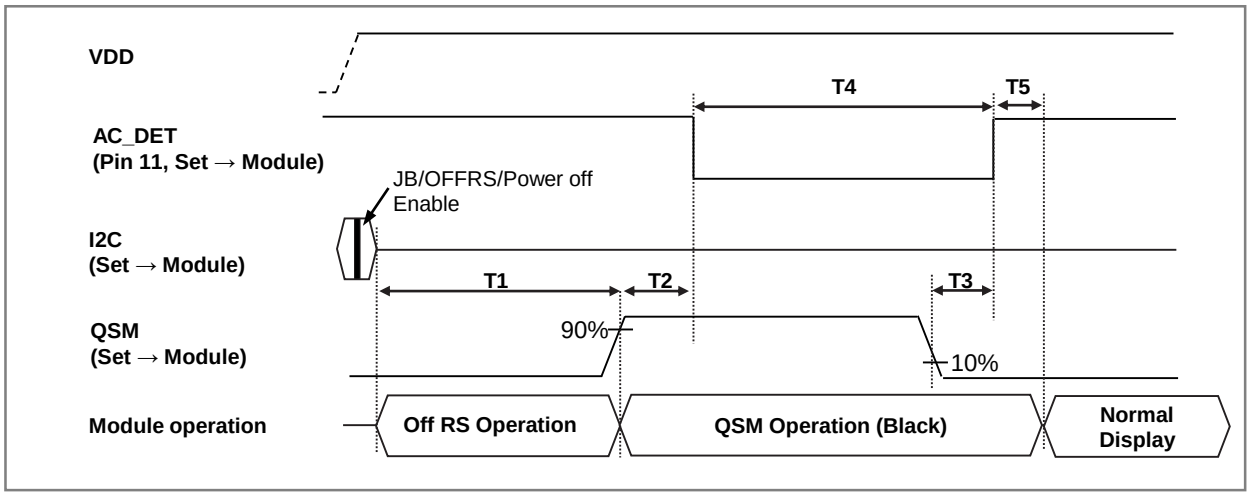


Table 12. QSM Sequence

Parameter	Value			Unit	Notes
	Min	Typ	Max		
T1	3	-	-	sec	JB/OFFRS
T2	75	-	-	ms	
T3	10	-	-	ms	
T4	1	-	-	sec	
T5	200	-	500	ms	

3-6-5. Power off sequence

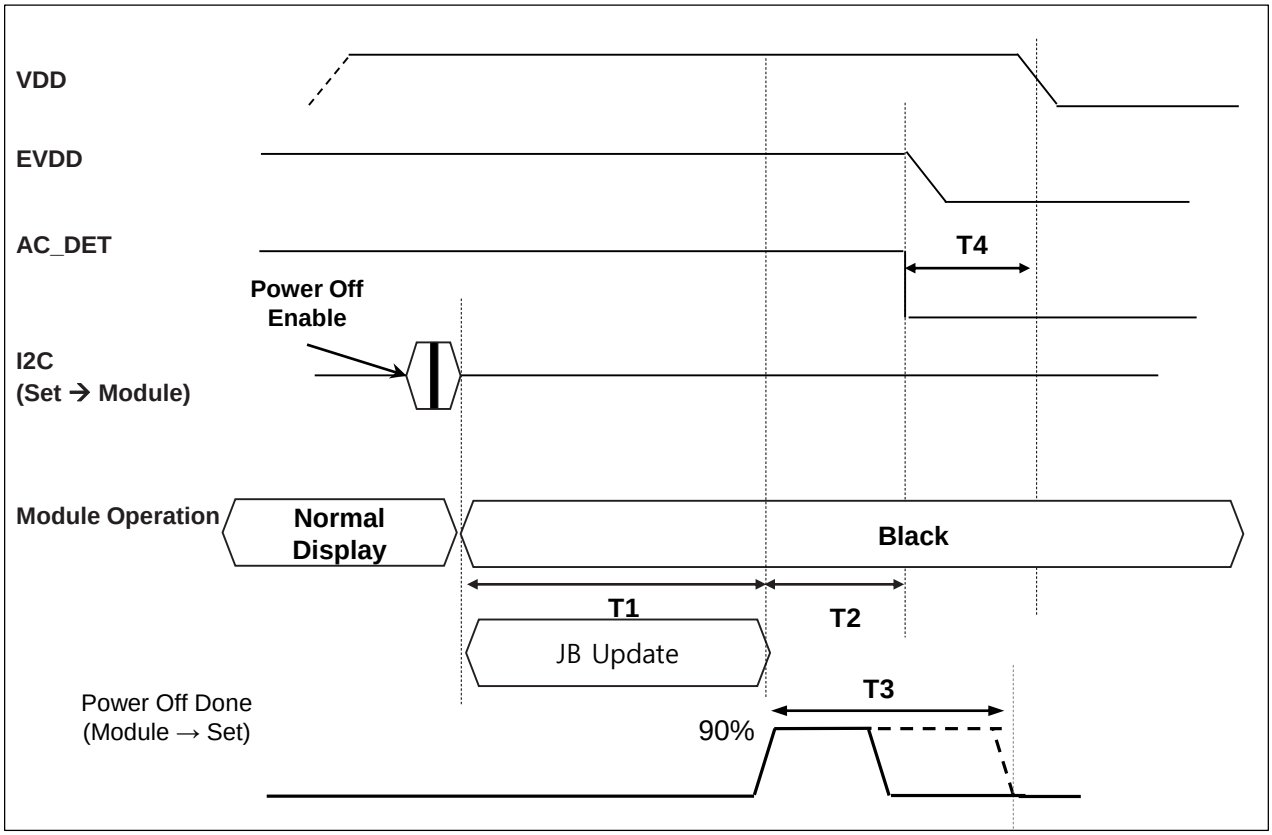


Table 13. POWER SEQUENCE

Parameter	Value			Unit	Notes
	Min	Typ	Max		
T1	-	-	16.5	sec	
T2	30	-	-	ms	
T3	5	7	10	sec	
T4	50	-	-	ms	

4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable in a dark environment at 25±2°C. The values are specified at distance 50cm from the OLED surface at a viewing angle of Φ and θ equal to 0 °. FIG. 1 shows additional information concerning the measurement equipment and method.

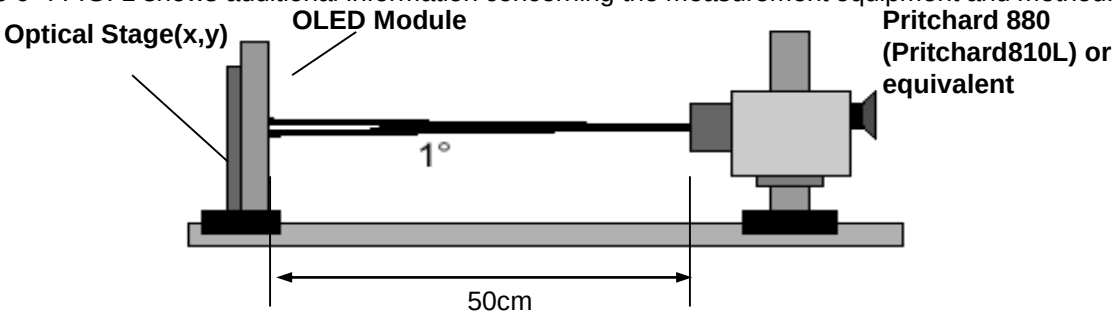


FIG. 1 Optical Characteristic Measurement Equipment and Method

Table 14. Optical Characteristics Ta= 25±2°C, VDD=12V, EVDD=19.5V, fv=240Hz, Dclk=66.56MHz,

Parameter		Symbol		Value			Unit	Note
				Min	Typ	Max		
Contrast Ratio		CR @ Pritchard 880		120,000	150,000	-		1
		CR @ Pritchard 810L @ 25% APL		1,200,000	1,500,000			
Surface Luminance, white		L_{WH}	Normal	120	150	-	cd/m²	2
			Peak	360	450	-		
			HDR 10%	640	800	-		
			HDR 3%	800	1000	-		
Luminance Uniformity		δ_{WHITE}	9P	75	80	-	%	3
Response Time		G to G		-	0.03	0.5	ms	4
Color Coordinates [CIE1931]	RED	Rx		Typ -0.02	0.677	Typ +0.02		
		Ry			0.321			
	GREEN	Gx			0.249			
		Gy			0.685			
	BLUE	Bx			0.146			
		By			0.057			
	WHITE	Wx			0.291			
		Wy			0.300			
Color Temperature					8,500		K	
Color Gamut (CIE1976)		DCI		90	98.5		%	
Color Viewing Angle								
(Δu'v'≤0.025)	x axis, right(ϕ=0°)	θr		60	-	-	degree	5
	x axis, left (ϕ=180°)	θl		60	-	-		
	y axis, up (ϕ=90°)	θu		60	-	-		
	y axis, down (ϕ=270°)	θd		60	-	-		
Life Time (B10)		Hrs		-	30,000	-		6
Gray Scale				-	2.2	-		7

Note : 1. Contrast Ratio(CR) is defined mathematically as :

$$\text{Contrast Ratio} = \frac{\text{Surface Luminance with all white pixels}}{\text{Surface Luminance with all black pixels}}$$

It is measured at center 1-point.

2. . Normal full white luminance is determined with 100% APL after 30 minutes 'ON' with APL 100%(Full white) pattern in a dark environment at 25±2°C . It is the luminance value at center 1-point across the OLED surface 50cm from the surface with all pixels displaying white. For additional measurement, OLED module need to power-off for 2 minutes(min). Peak luminance is determined with 25% APL after 1.5 minutes at least 'ON' with 25% white window box. HDR luminance is determined with 10% APL after 60 seconds at least 'ON' with 10% white window box. For more information, see FIG 2.

※ Normal : APL 100% (Full white) / Peak : APL 25% / HDR : APL 10% / HDR : APL 3%

※ HDR Luminance should only be applied when entering HDR Contents

3. The variation in surface luminance , δ WHITE is defined as :

δ WHITE(9P) = Minimum(L_{on1},,…. L_{on9}) / Maximum(L_{on1}….. L_{on9})

Where L_{on1} to L_{on9} are the luminance with all pixels displaying white at 9 locations .

For more information, see the FIG. 2.

4. Response time is the time required for the display to transit from G(N) to G(M) (Rise Time, Tr_R) and from G(M) to G(N) (Decay Time, Tr_D). For additional information, see the FIG. 3. (N<M)

※ G to G Spec stands for average value of all measured points.

※ Test equipment : PR-810, Test Distance : Display Height * 0.35

※ Measuring Field : 1˚, Test Pattern : APL10% Window Box

5. Viewing Angle Color Shift (VACS) is defined as follows after measuring color coordinates at each angle.; VACS = sqrt(du2+dv2) (@ CIE (u', v') color space) For more information, see the FIG. 4.

6. Test Condition : IEC62087 standard video with OFF-RS every 4 hours at room temperature 25℃ (If the cumulative time of usage is over 4 hours, OFF-RS compensation should be performed.)

7. Gray scale specification.

Gamma Value is approximately 2.2. For more information, see the Table 15.

Table 15. Gray Scale Specification

Gray Level	Luminance [%] (Typ)
L0	0.001
L63	0.20
L127	0.97
L191	2.42
L255	4.61
L319	7.59
L383	11.4
L447	16.0
L511	21.6
L575	28.0
L639	35.4
L703	43.7
L767	53.0
L831	63.2
L895	74.5
L959	86.7
L1023	100

Measuring point for surface luminance & measuring point for luminance variation.

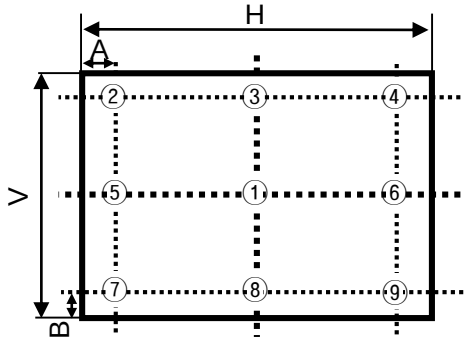


FIG. 2-1 9 Points for Luminance Measure with 100% APL

A: H/9 B: V/9 @ H,V: Active Area

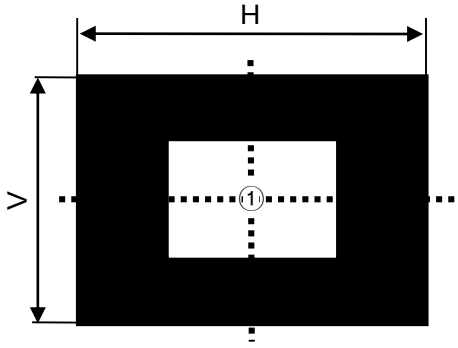


FIG. 2-2. 1 Point for peak luminance measure with 25% APL

@ H,V: Active Area

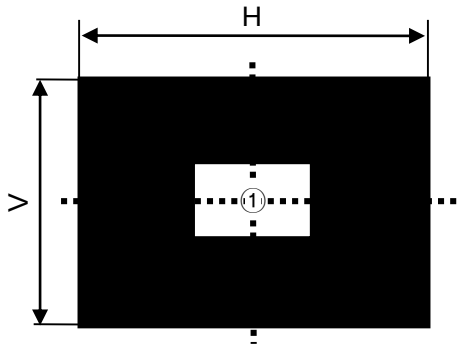


FIG. 2-3. 1 Point for peak luminance measure with 10% APL

@ H,V: Active Area

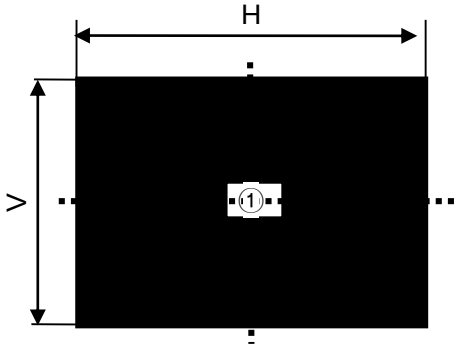
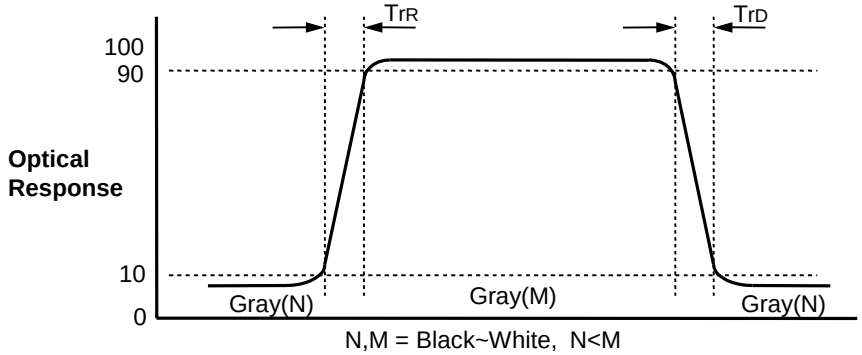


FIG. 2-4. 1 Point for peak luminance measure with 3% APL

@ H,V: Active Area

Response time is defined as the following figure and shall be measured by switching the input signal for "Gray(N)" and "Gray(M)".



N,M = Black~White, N<M

FIG. 3 Response Time

Dimension of viewing angle range

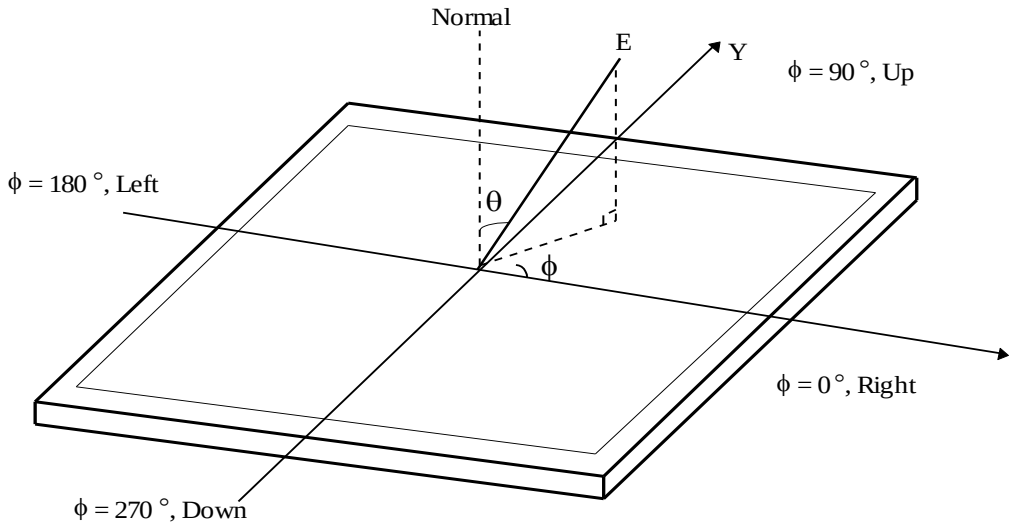


FIG. 4 Viewing Angle

5. Mechanical Characteristics

Table 16 provides general mechanical characteristics.

Table 16. Mechanical Characteristics

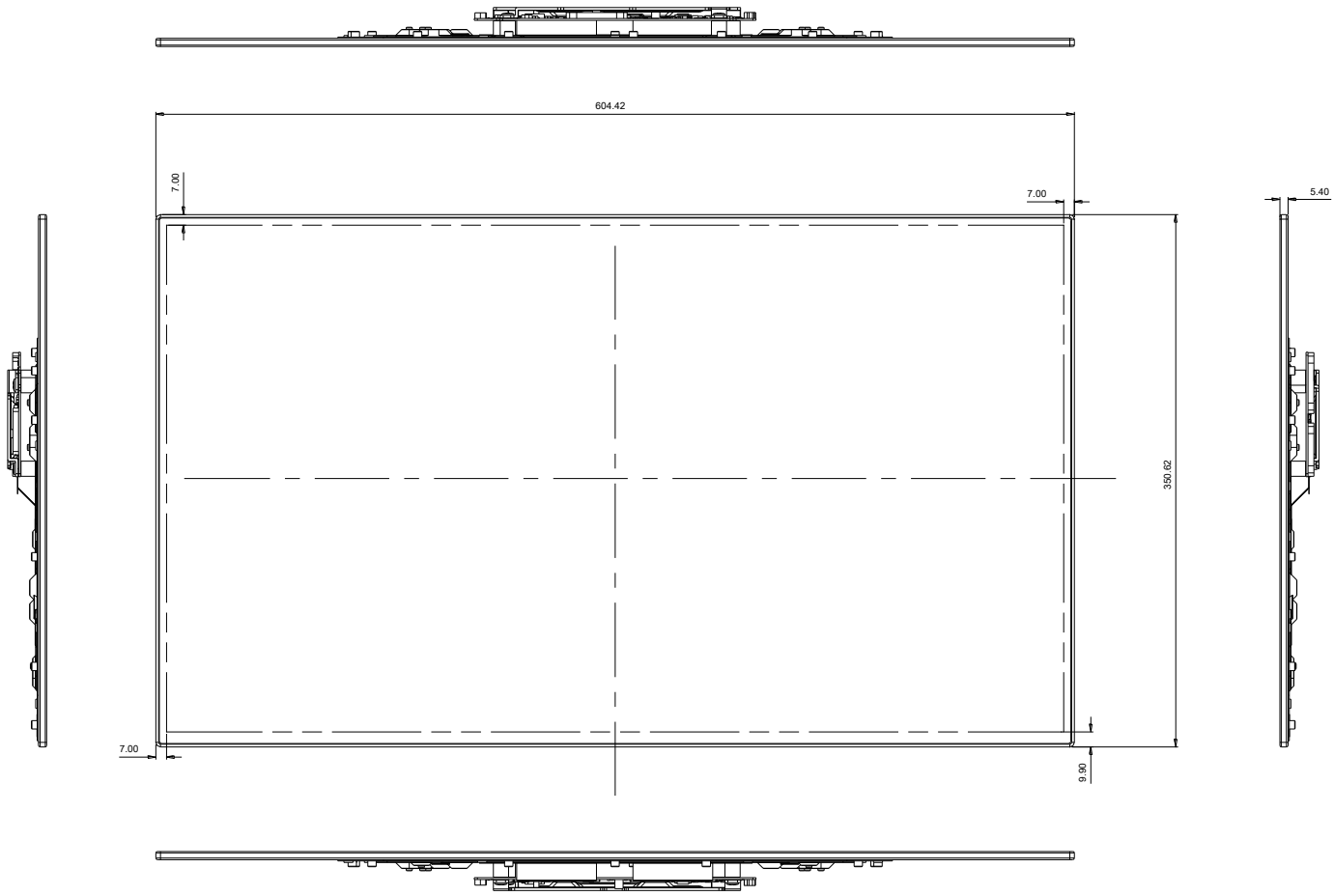
Item	Value	
Outline Dimension (Base on Flat Module)	Horizontal	604.42 mm
	Vertical	350.62 mm
	Thickness(at slimmest part)	5.4 mm
Active Display Area (Base on Flat Panel)	Horizontal	586.75 mm (Display area) 590.42 mm (Include Real Orbit area)
	Vertical	330.05 mm (Display area) 333.72 mm (Include Real Orbit area)
Weight	3.2 kg (Typ.), 3.4 kg (Max)	

Note : Please refer to a mechanical drawing in terms of tolerance at the next page.

Table 17. On Bezel Mechanical Characteristics

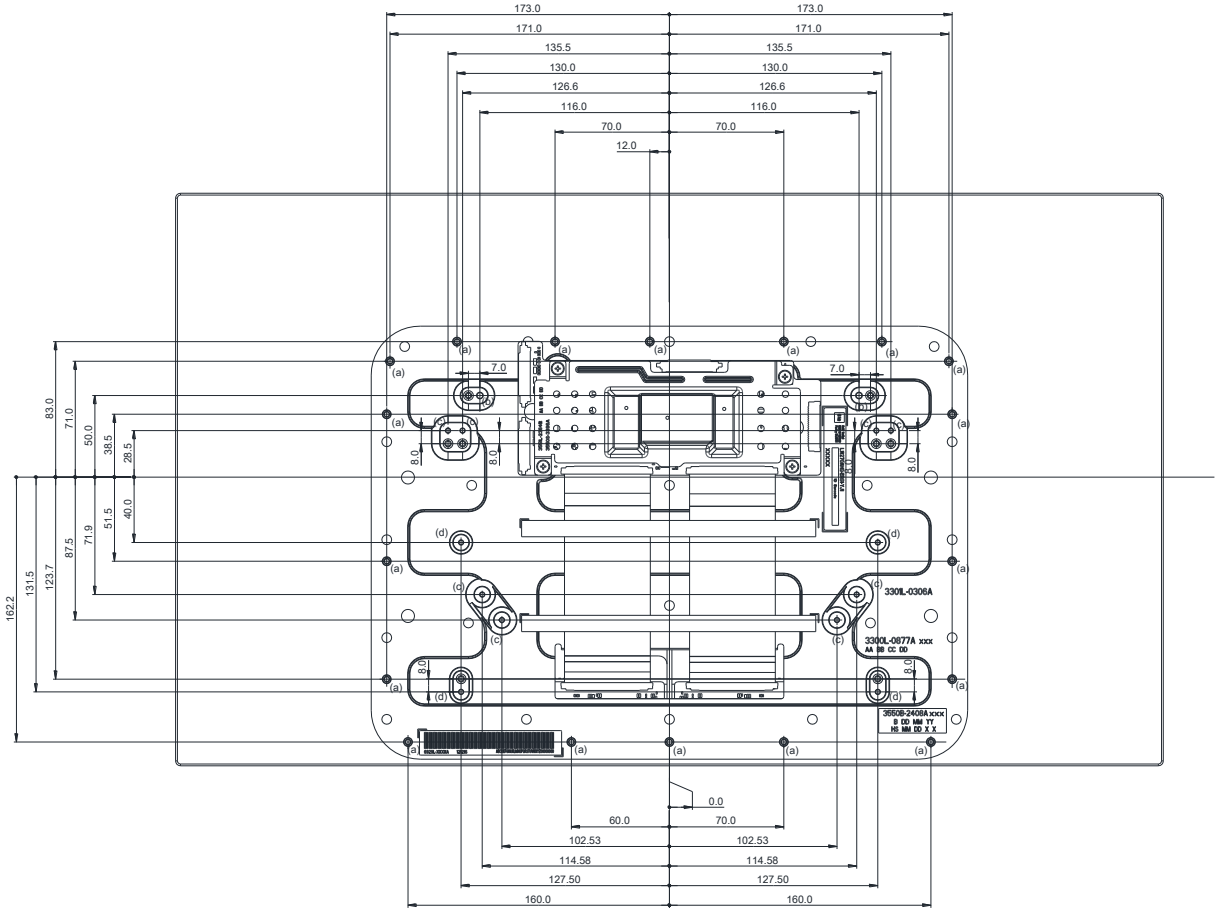
Item	Value	
On Bezel (Active Area ~ Edge of Module)	Horizontal	7.0mm (Left) / 7.0mm (Right)
	Vertical	7.0mm (Top) / 9.9mm (Bottom)

[FRONT VIEW]



NOTE
1. Unspecified tolerance is ±1.0㎜
2. Border Gap 0.0~1.2mm @ Power off, Room Temp.

[REAR VIEW]



Item	Tap	Diameter		Height		Max Depth	Notes
		d1	d2	h1	h2		
(a)	M3	Ø5.5	-	3.8	-	3.8	18ea

Item	Tap	Max Depth (mm)	Max Torque (Kgf*cm)	Notes
(b)	M4	4.8	Max 6.0	2ea
(c)	M3	4.8	Max 6.0	8ea
(d)	M3	2.8	Max 6.0	4ea

Note
1. Unspecified tolerance is ± 1.0mm
2. The tapping type and max. depth for each mounting hole comply with above table “Pem-nut information”
3. Border Gap : 0≤X≤1.2mm, (@Power off) Room Temperature.

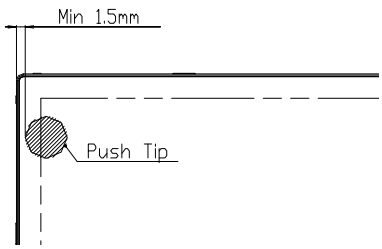
6. Reliability

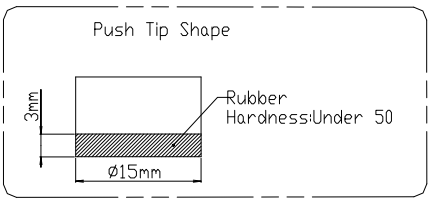
Table 18. Environment Test Condition

No.	Test Item	Condition
1	High temperature storage test	Ta= 60°C 240h
2	Low temperature storage test	Ta= -20°C 240h
3	High temperature operation test	Ta= 50°C 50%RH 240h
4	Low temperature operation test	Ta= 0°C 240h
5	Humidity condition Operation	Ta= 40 °C, 90%RH
6	Altitude operating storage / shipment	0 - 15,000 ft 0 - 40,000 ft
7	Panel Push Test (Module Condition)	6kgf (Note 2.)

Note : 1. Before and after Reliability test, OLED Module should be operated with normal function.
(After Reliability test, some OLED Module need to do OFF-RS before function check)
2. Guarantee panel crack less than 6kgf

Panel Push Test Method





7. International Standards

7-1. Safety

(1)IEC 62368-1, The International Electro-technical Commission(IEC).
Audio/video, Information and Communication Technology Equipment - Safety - Safety Requirements.

(2)EN 62368-1, European Committee for Electro-technical Standardization (CENELEC)
Audio/video, Information and Communication Technology Equipment - Safety Requirements

(3)UL 62368-1, UL LLC.
Audio/video, Information and Communication Technology Equipment - Safety Requirements.

(4)CAN/CSA C22.2 No.62368-1, Canadian Standards Association (CSA).
Audio/video, Information and Communication Technology Equipment - Safety Requirements

(5)IEC 60065, The International Electro-technical Commission (IEC).
Audio, Video and Similar Electronic Apparatus - Safety Requirements

7-2. Environment

(1) RoHS, Commission Delegated Directive (EU) 2015/863 of 31 March 2015 amending Annex II to Directive 2011/65/EU of the European Parliament and of the Council

8. Packing

8-1. Information of OLED Module Label

(1) Lot Mark

A	B	C	D	E	F	G	H	I	J	K	L	M

A,B,C : SIZE(INCH)
D : YEAR
E : MONTH
F ~ M : SERIAL NO.

Note

1. YEAR

Year	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030
Mark	K	L	M	N	P	Q	R	S	T	U	V

2. MONTH

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Spe	Oct	Nov	Dec
Mark	1	2	3	4	5	6	7	8	9	A	B	C

(2) Location of Lot Mark

Serial NO. is printed on the label. The label is attached to the backside of the OLED module.
This is subject to change without prior notice.

8-2. Packing Form

a) Package quantity in one Box : 7 pcs
Package quantity in one Pallet : 42 pcs

b) Box Size : 365 mm(W) X 710 mm(D) X 493 mm(H)
Pallet Size : 1140 mm(W) X 740 mm(D) X 1125 mm(H)

9. Precautions

Please pay attention to the followings when you use this OLED module.

9.1 Operating Precautions

(1) The spike noise causes the mis-operation of circuits. It should be lower than following voltage :
V=±200mV(Over and under shoot voltage)
(2) Response time depends on the temperature.(In lower temperature, it becomes longer.)
(3) Be careful for condensation at sudden temperature change.Condensation makes damage to polarizer or electrical contacted parts. And after fading condensation, smear or spot will occur.
(4) When fixed patterns are displayed for a long time, Image Retention is likely to occur.
(5) Module has high frequency circuits. Sufficient suppression to the electromagnetic interference shall be done by system manufacturers. Grounding and shielding methods may be important to minimized the interference.
(6) Please do not give any mechanical and/or acoustical impact to Module. Otherwise, Module can't be operated its full characteristics perfectly.
(7) A screw which is fastened up the steels should be a machine screw.
(if not, it can causes conductive particles and deal Module a fatal blow)
(8) Please do not set OLED on its edge.
(9) If system antenna (Wifi) is overlapped with source PCB and FFC, It might be cause the noise.

9-2. Electrostatic Discharge Control

Since a module is composed of electronic circuits, it is not strong to electrostatic discharge. Make certain that treatment persons are connected to ground through wrist band etc. And don't touch interface pin directly.

9-3. Precautions for Strong Light Exposure

Strong light exposure causes degradation of polarizer and color filter.

9-4. Storage

When storing modules as spares for a long time, the following precautions are necessary.

Storage conditions for packing

Item	Temperature	Humidity	Period
Storage Standard	5~35℃	35~75%	12months

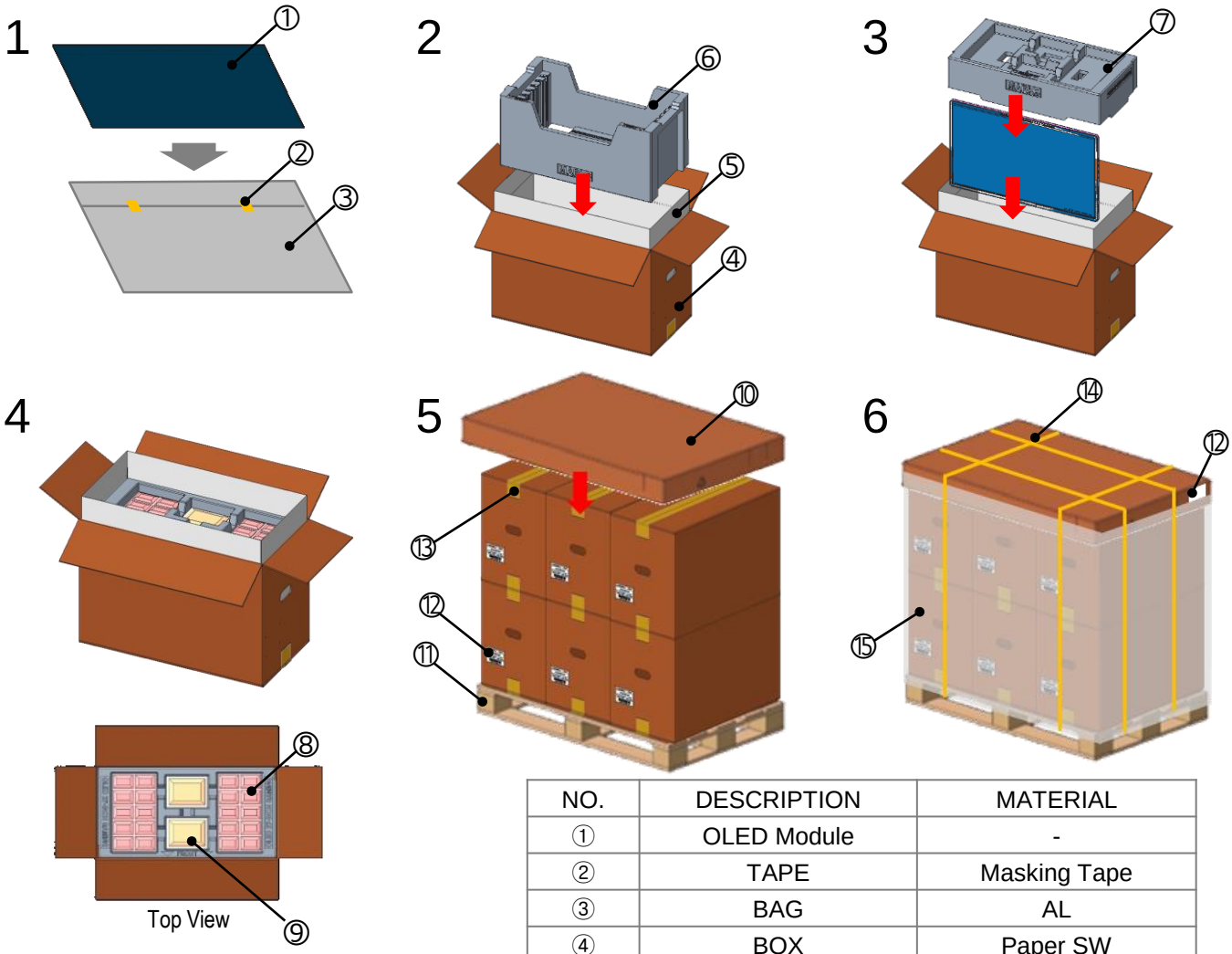
(1) It must be stored in an environment equipped with a dark and air conditioning / ventilation system and a room in controlling specific condition.
(2) It must be stored in a space composed of general air atmosphere.
(3) Do not expose the module to sunlight or fluorescent light.
(4) Contact with humid spaces, rainy environments, high humid atmosphere, moisture and condensation within package is prohibited.
(5) Storing products in outside environment and out door is prohibited.
(6) If products are stored in specified conditions over more than 3 months, it is recommended to check the product packaging condition.

9-5. Handling Precautions for Protection Film

(1) The protection film is attached to the bezel with a small masking tape.
When the protection film is peeled off, static electricity is generated between the film and polarizer.
This should be peeled off slowly and carefully by people who are electrically grounded and with well ion-blown equipment or in such a condition, etc.
(2) When the module with protection film attached is stored for a long time, sometimes there remains a very small amount of glue still on the bezel after the protection film is peeled off.
(3) You can remove the glue easily. When the glue remains on the bezel surface or its vestige is recognized, please wipe them off with absorbent cotton waste or other soft material like chamois soaked with normal-hexane.

APPENDIX - I

■ Pallet Ass'y

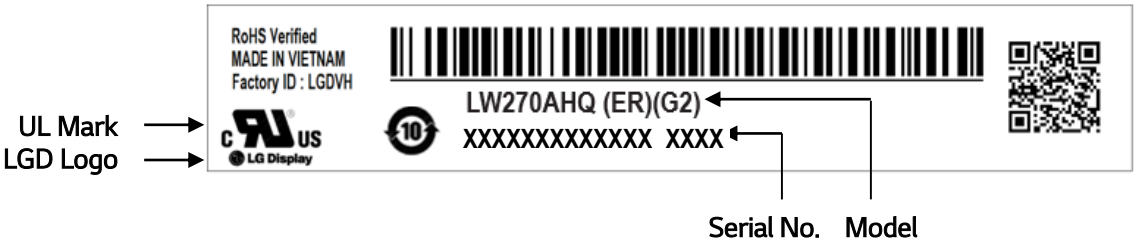


* The position and quantity of Oxygen Absorber & desiccant can be changed

NO.	DESCRIPTION	MATERIAL
①	OLED Module	-
②	TAPE	Masking Tape
③	BAG	AL
④	BOX	Paper SW
⑤	BAG	AL
⑥	PACKING, BOTTOM	EPS
⑦	PACKING, TOP	EPS
⑧	OXYGEN ABSORBER	-
⑨	DESICCANT	-
⑩	ANGLE COVER	Paper SW
⑪	PALLET	Plywood
⑫	LABEL	Yupo Paper
⑬	SINGLE SIDE TAPE	OPP
⑭	BAND	PP
⑮	WRAP	LLDPE

APPENDIX - II

■ Serial Label



 # APPENDIX - III

■ Box Label

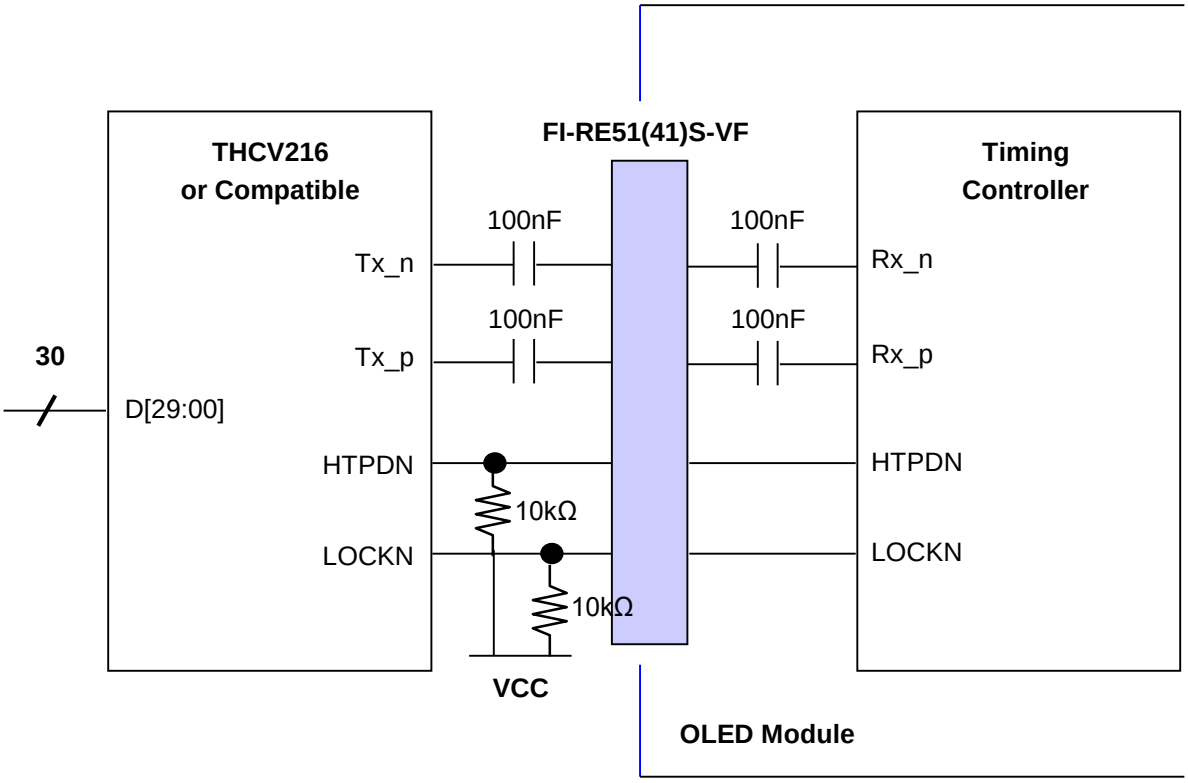


■ Pallet Label



APPENDIX - IV

■ Required Signal Assignment for Flat Link (Thine : THCV215) Transmitter

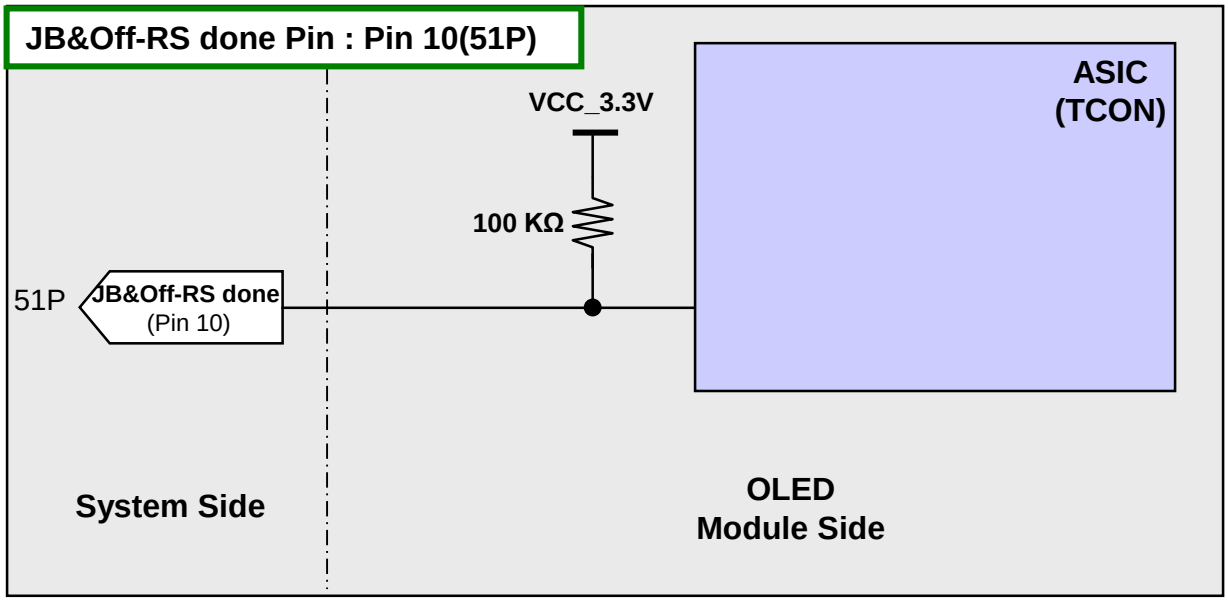


Note: 1. The OLED module uses a 100 nF capacitor on positive and negative lines of each receiver input.
2. Refer to VbyOne Transmitter Data Sheet for detail descriptions. (THCV216 or Compatible)
3. About Module connector pin configuration, Please refer to the Page 7~8.

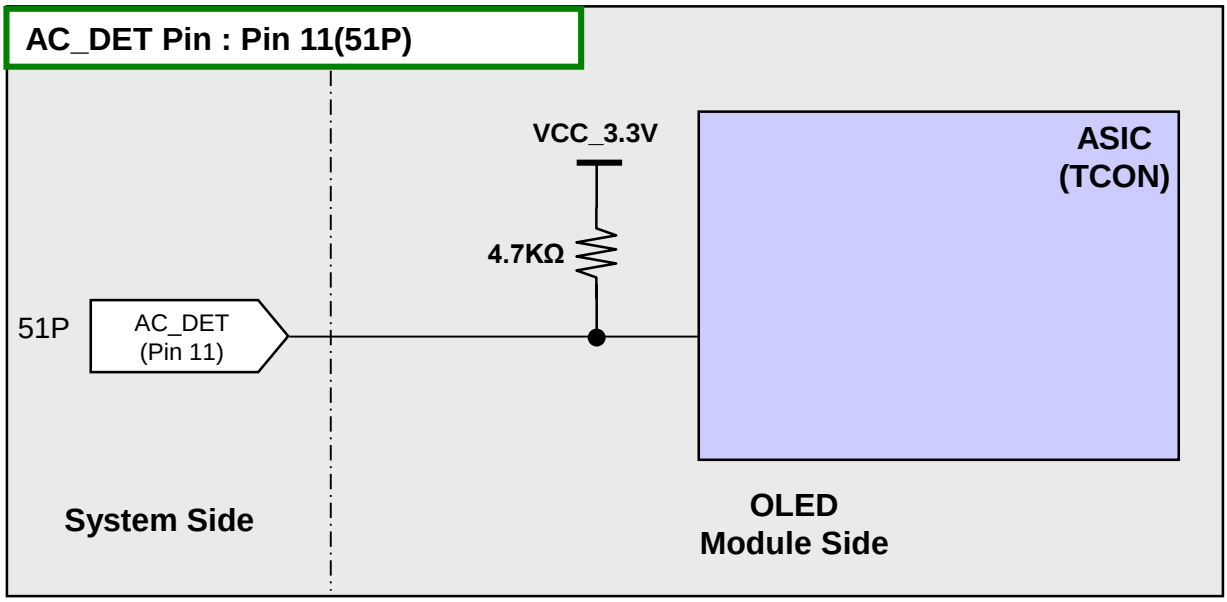
APPENDIX - V - 1

■ Circuit Block Diagram for Option Pin

(1) Circuit Block Diagram of **JB&Off-RS done** pin



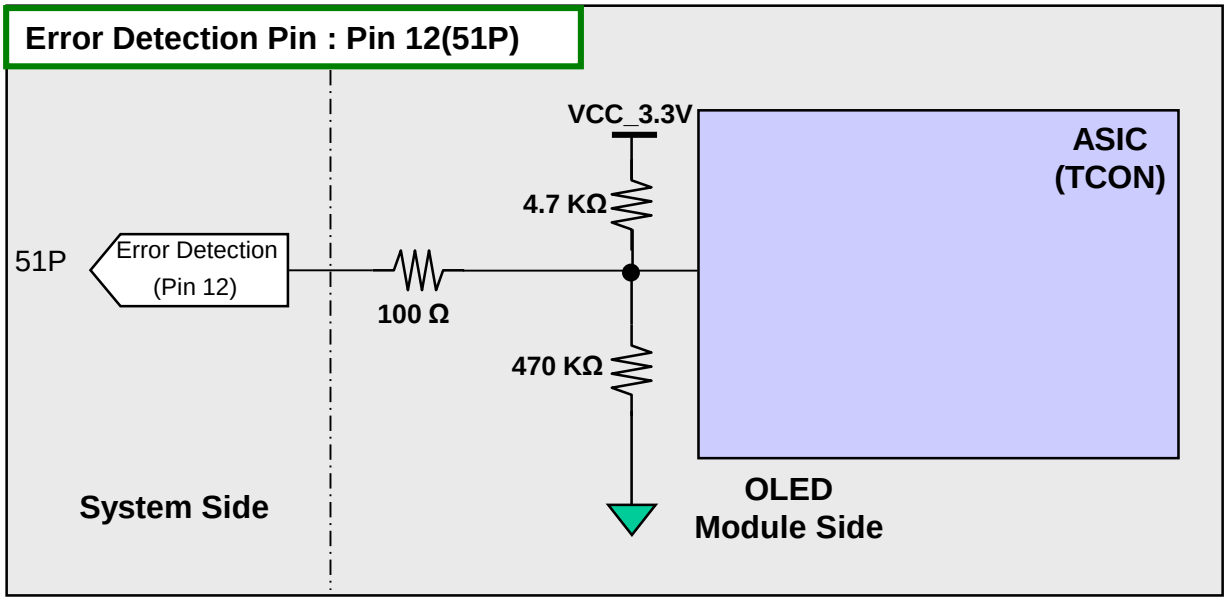
(2) Circuit Block Diagram of **AC_DET** pin



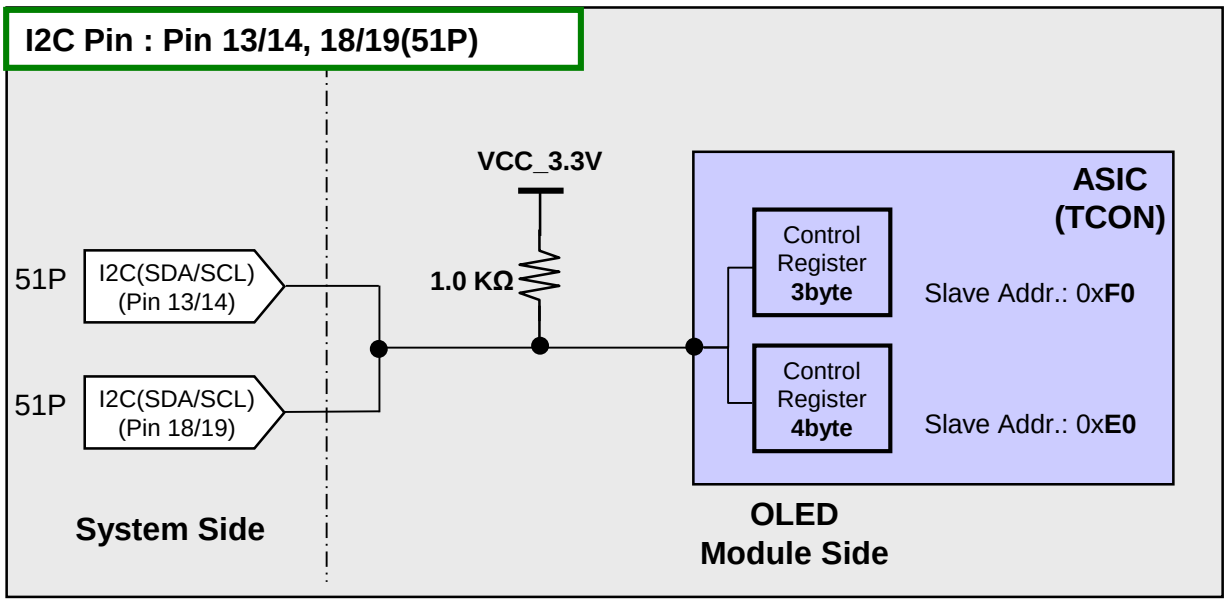
APPENDIX - V - 2

■ Circuit Block Diagram for Option Pin

(3) Circuit Block Diagram of **Error Detection** pin



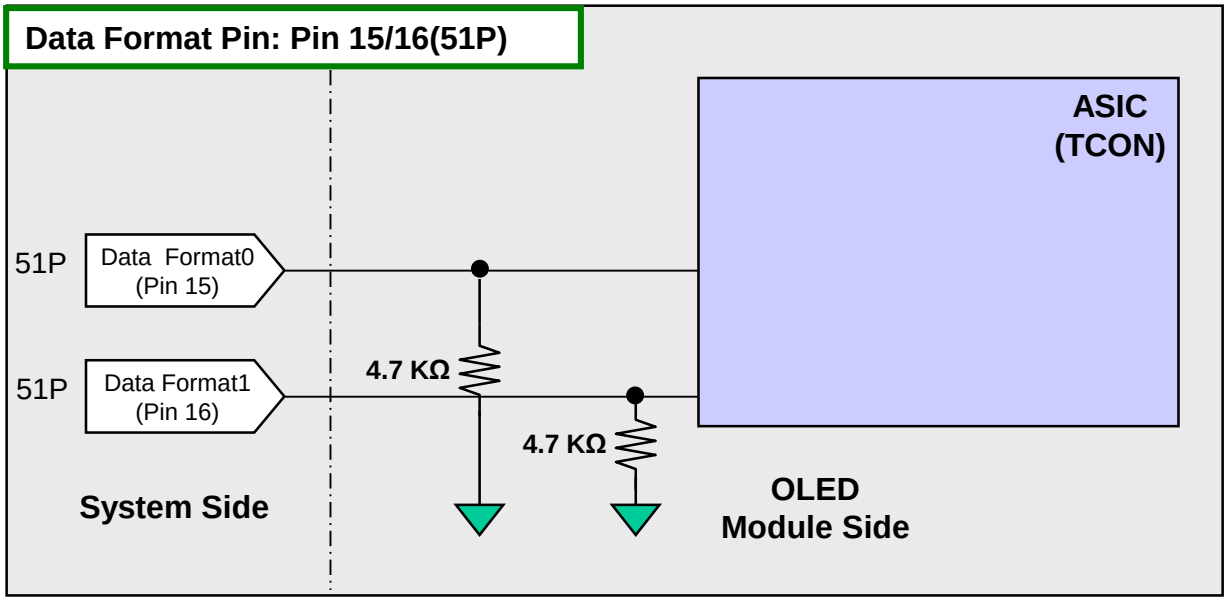
(4) Circuit Block Diagram of **I2C(SDA/SCL)** pin



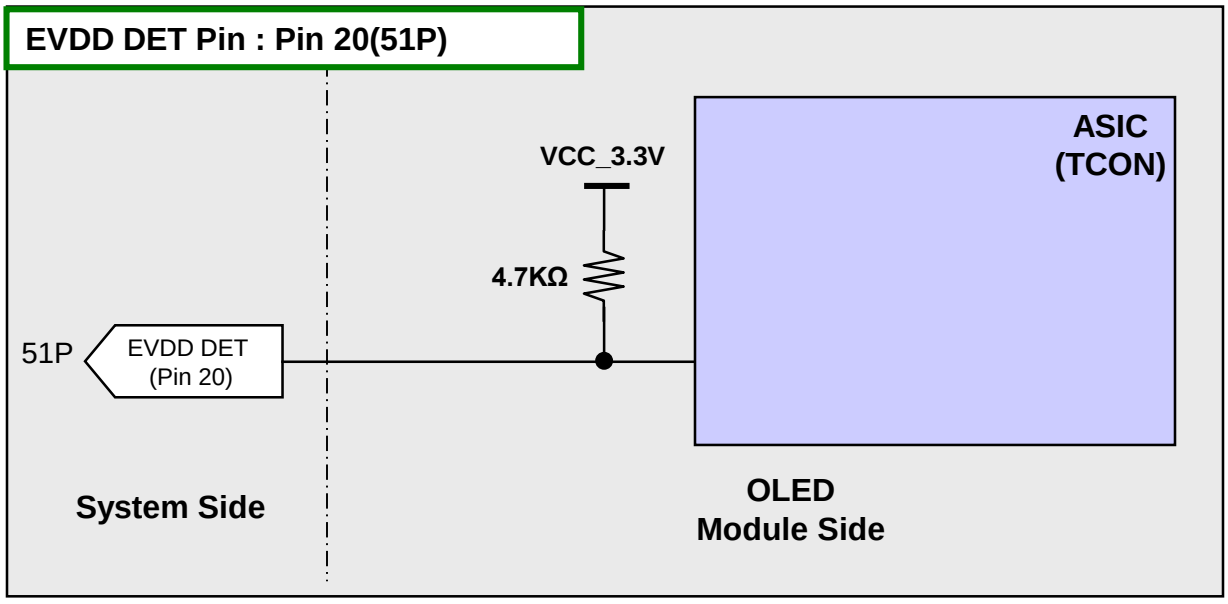
APPENDIX - V - 3

■ Circuit Block Diagram for Option Pin

(5) Circuit Block Diagram of Data Format pin



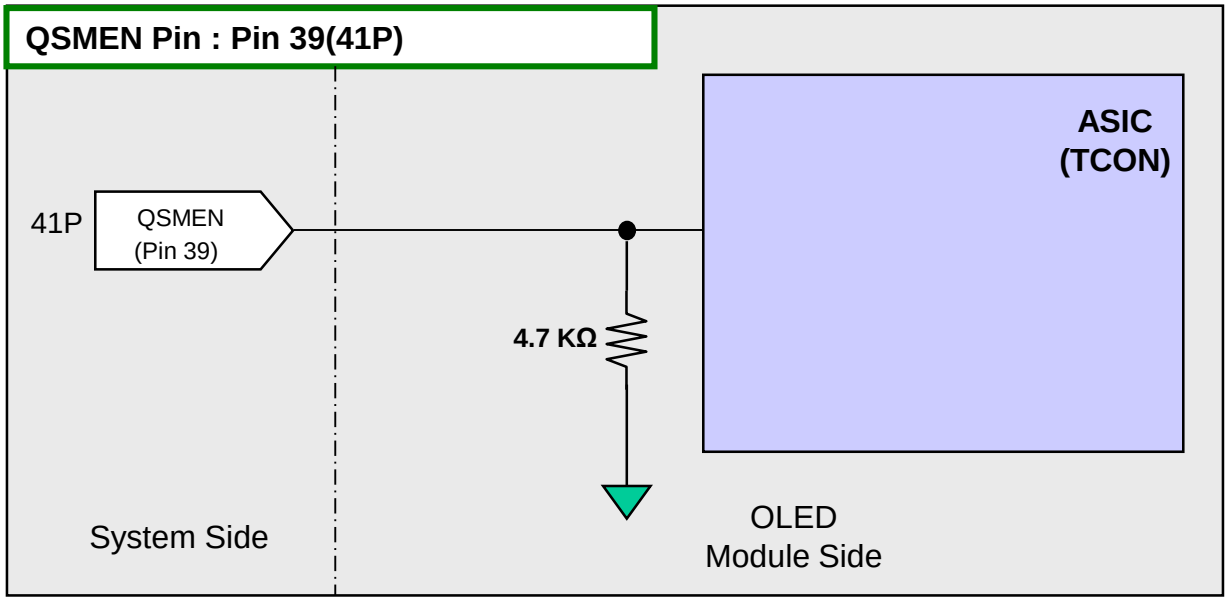
(6) Circuit Block Diagram of EVDD DET pin



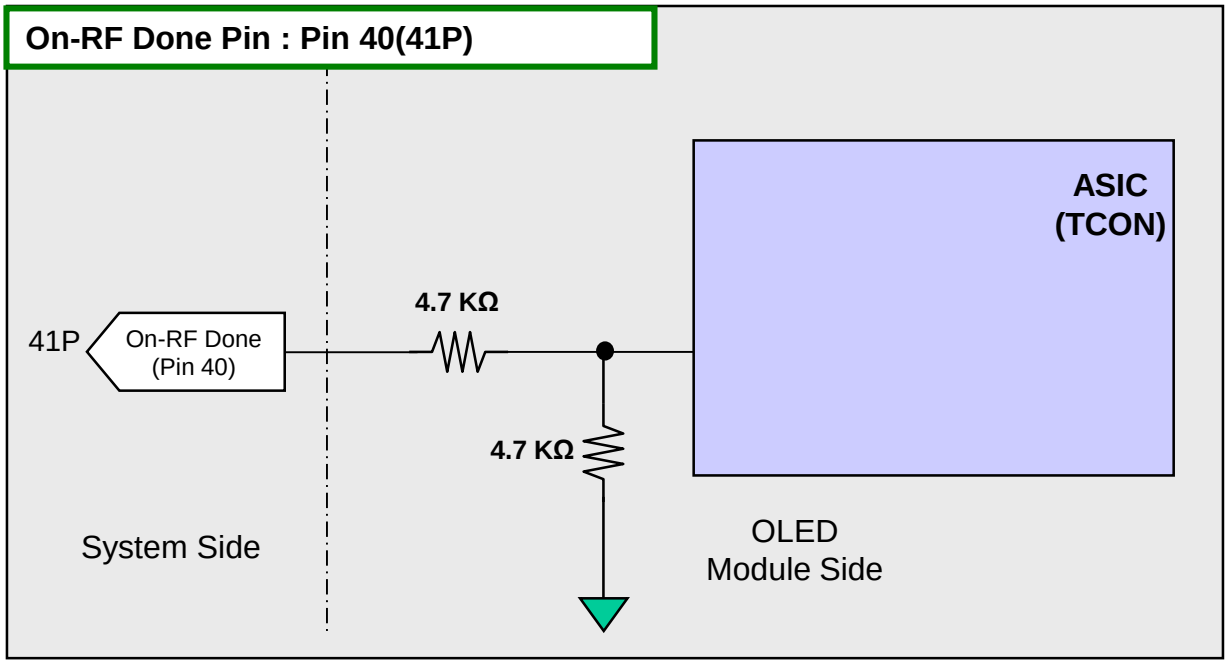
APPENDIX - V - 4

■ Circuit Block Diagram for Option Pin

(5) Circuit Block Diagram of **QSMEN** pin



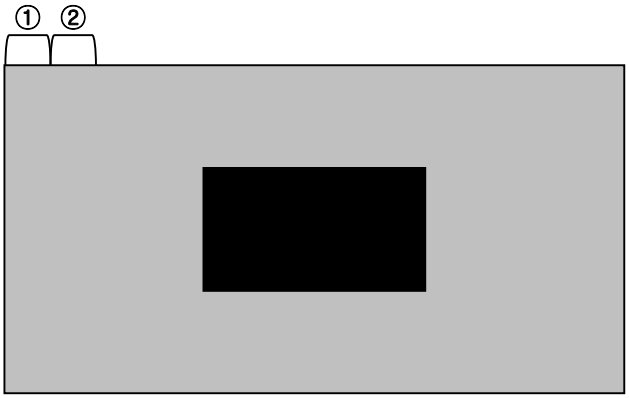
(6) Circuit Block Diagram of **On-RF Done** pin



APPENDIX - VI - 1

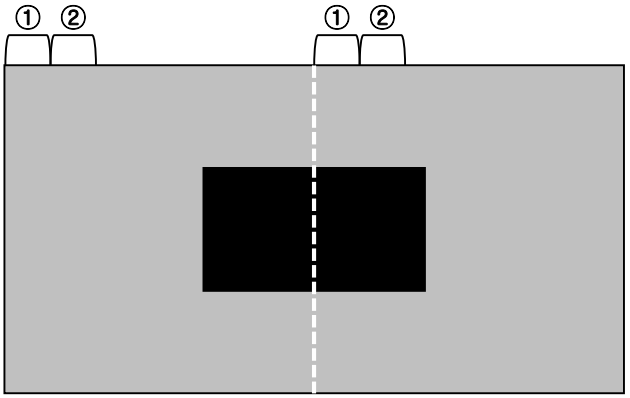
■ Input Mode of Pixel Data

Mode 1 : Non Division Mode



	1'st Data	2'nd Data	…	Data #
Lane00	1	17	…	2545
Lane01	2	18	…	2546
Lane02	3	19	…	2547
Lane03	4	20	…	2548
Lane04	5	21	…	2549
Lane05	6	22	…	2550
Lane06	7	23	…	2551
Lane07	8	24	…	2552
Lane08	9	25	…	2553
Lane09	10	26	…	2554
Lane10	11	27	…	2555
Lane11	12	28	…	2556
Lane12	13	29	…	2557
Lane13	14	30	…	2558
Lane14	15	31	…	2559
Lane15	16	32	…	2560

Mode 2 : 2 Division Mode

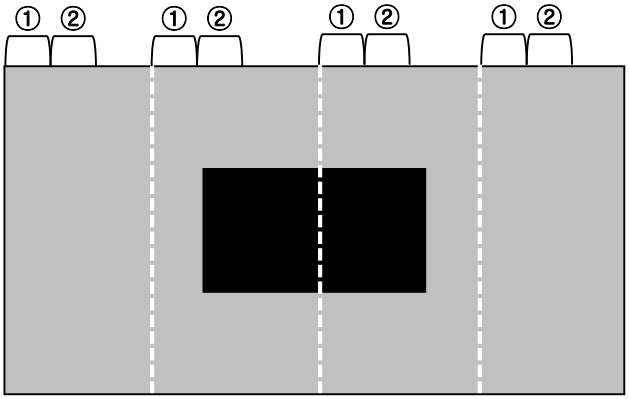


	1'st Data	2'nd Data	…	Data #
Lane00	1	9	…	1273
Lane01	2	10	…	1274
Lane02	3	11	…	1275
Lane03	4	12	…	1276
Lane04	5	13	…	1277
Lane05	6	14	…	1278
Lane06	7	15	…	1279
Lane07	8	16	…	1280
Lane08	1281	1289	…	2553
Lane09	1282	1290	…	2554
Lane10	1283	1291	…	2555
Lane11	1284	1292	…	2556
Lane12	1285	1293	…	2557
Lane13	1286	1294	…	2558
Lane14	1287	1295	…	2559
Lane15	1288	1296	…	2560

APPENDIX – VI - 2

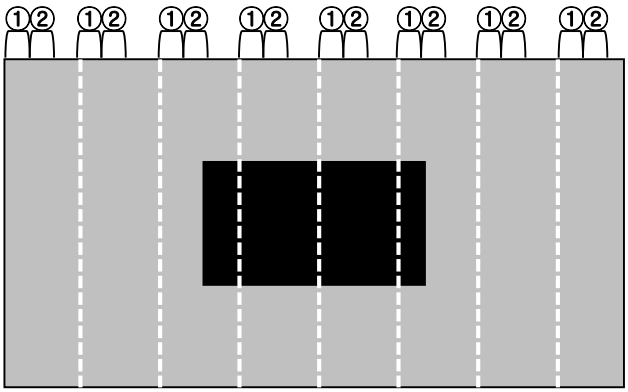
■ Input Mode of Pixel Data

Mode 3 : 4 Division Mode



	1'st Data	2'nd Data	…	Data #
Lane00	1	5	…	637
Lane01	2	6	…	638
Lane02	3	7	…	639
Lane03	4	8	…	640
Lane04	641	645	…	1277
Lane05	642	646	…	1278
Lane06	643	647	…	1279
Lane07	644	648	…	1280
Lane08	1281	1285	…	1917
Lane09	1282	1286	…	1918
Lane10	1283	1287	…	1919
Lane11	1284	1288	…	1920
Lane12	1921	1925	…	2557
Lane13	1922	1926	…	2558
Lane14	1923	1927	…	2559
Lane15	1924	1928	…	2560

Mode 4 : 8 Division Mode



	1'st Data	2'nd Data	…	Data #
Lane00	1	3	…	319
Lane01	2	4	…	320
Lane02	321	323	…	639
Lane03	322	324	…	640
Lane04	641	643	…	959
Lane05	642	644	…	960
Lane06	961	963	…	1279
Lane07	962	964	…	1280
Lane08	1281	1283	…	1599
Lane09	1282	1284	…	1600
Lane10	1601	1603	…	1919
Lane11	1602	1604	…	1920
Lane12	1921	1923	…	2239
Lane13	1922	1924	…	2240
Lane14	2241	2243	…	2559
Lane15	2242	2244	…	2560

APPENDIX - VII

■ Register Map

The following register is controlled by I2C Interface.

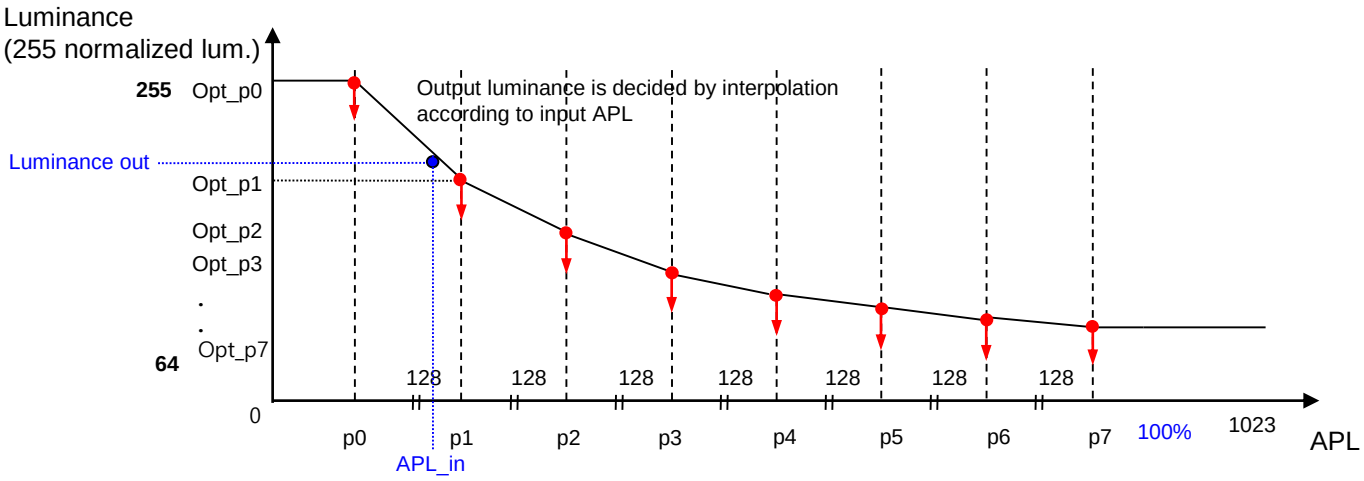
	Bit[7]: MSB	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]: LSB
Addr : 0x001	CPC EN	TPC EN	Not Use	OFF RS EN	Not Use	Not Use	Not Use	Not Use

Device Address: 0xE0

Address [Hex]	Register Name	Description	Remark
0x000	Valid	Read only register (LGD use)	
0x001	[7] : CPC enable	1: enable (default), 0: disable	
	[6] : TPC enable	1: enable (default), 0: disable	
	[5] : Not used	Must Be : 1	
	[4] : Off RS enable	1: enable, 0: disable	
	[3] : Not used	Must Be : 0	
	[2] : Not used	Must Be : 0	
	[1:0] Not used	LGD reserved	
0x003	Opt_p0	APL P0 point corresponds to the 255 normalized luminance	
0x004	Opt_p1	APL P1 point corresponds to the 255 normalized luminance	
0x005	Opt_p2	APL P2 point corresponds to the 255 normalized luminance	
0x006	Opt_p3	APL P3 point corresponds to the 255 normalized luminance	
0x007	Opt_p4	APL P4 point corresponds to the 255 normalized luminance	
0x008	Opt_p5	APL P5 point corresponds to the 255 normalized luminance	
0x009	Opt_p6	APL P6 point corresponds to the 255 normalized luminance	
0x00A	Opt_p7	APL P7 point corresponds to the 255 normalized luminance	

Address [Hex]	Register Name	Description	Remark
0x00B	[7] : Not used	LGD reserved	
	[6:5] : Not used	LGD reserved	
	[4] : LEA refresh mode en	1: LEA disable, 0: LEA enable (default)	
	[3] : HDR_en	1: Enable, 0: Disable (default)	
	[2] : Not used	LGD reserved	
	[1:0]:Not used	LGD reserved	

❑ PLC curve parameter

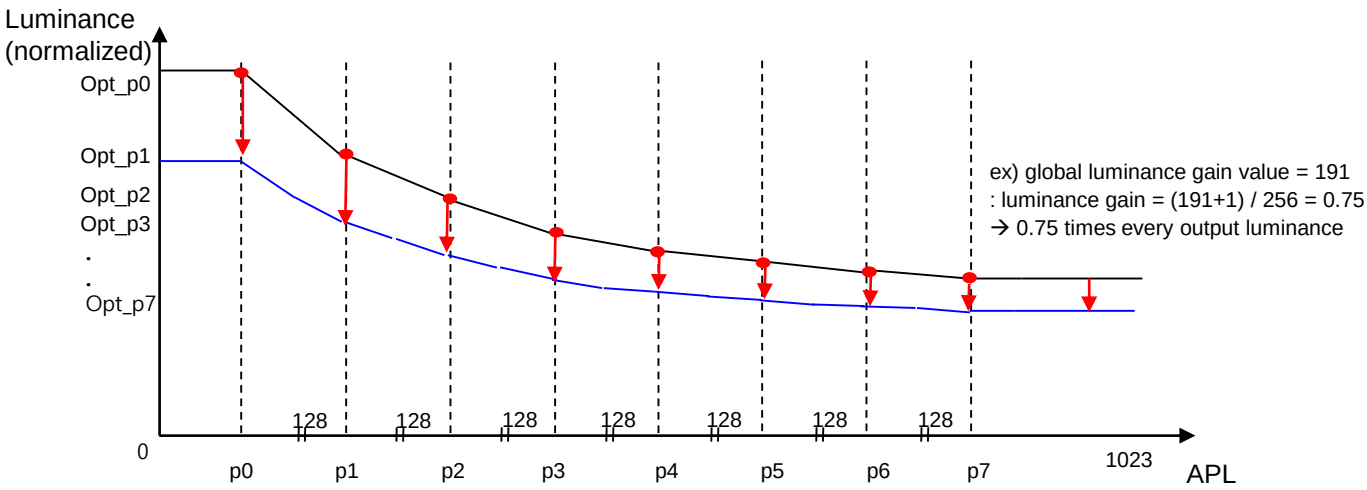


Every interval between each points except P0 is fixed to 128

- Luminance of p7~1023 interval are Opt_p7
- The point over 1023 is discarded

Address [Hex]	Register Name	Description	Remark
0x016	Opt_global_luminance_gain	Adjust global luminance gain 0~1 luminance gain according to 0~255 value (Same luminance gain is applied to every P0~P7 points)	Value Range: 0~255
0x054	[7] Power Off Enable	1: Enable, 0 : Disable (JB Update)	
	[6:0] Not Used	LGD reserved	
0x05D	[7] JB_en	1: Enable, 0: Disable	
	[6:0] Not used	LGD reserved	
0x05E	Test_temp1[15:8]	1st temperature sensor	Read only
0x05F	Test_temp1[7:0]		

❑ Global luminance gain



APPENDIX – VIII-1

■ Gray to Gray Response Time Uniformity

This is only the reference data of G to G and uniformity for LW270AHQ-ERG2 model.

(1) G to G Response Time :
Response time is defined as FIG. 3 and shall be measured by switching the input signal for "Gray (N) " and "Gray(M)".(64Gray Step at 8bit)

(2) G to G Uniformity
The variation of G to G Uniformity , $\delta_{G\ to\ G}$ is defined as :

$$\text{G to G Uniformity} = \frac{Maximum(GtoG) - Typical(GtoG)}{Typical(GtoG)} \leq 1$$

*Maximum (GtoG) means maximum value of measured time (N, M = 0 (Black) ~ 1023(White), 256 gray step).

	0Gray	255Gray	…	767Gray	1023Gray
0Gray		TrR:0G→255G	…	TrR:0G→767G	TrR:0G→1023G
255Gray	TrD:255G→0G		…	TrR:255G→767G	TrR:255G→1023G
…	…	…		…	…
767Gray	TrD:767G→0G	TrD:767G→255G	…		TrR:767G→1023G
1023Gray	TrD:1023G→0G	TrD:1023G→255G	…	TrD:1023G→767G	

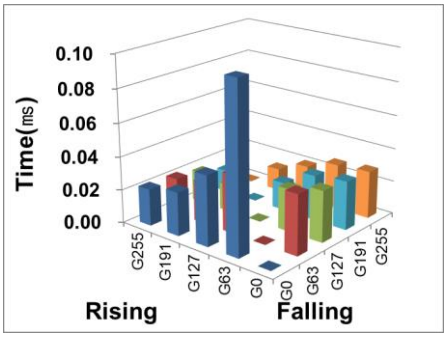
(3) Sampling Size : 2 pcs

(4) Measurement Method : Follow the same rule as optical characteristics measurement.

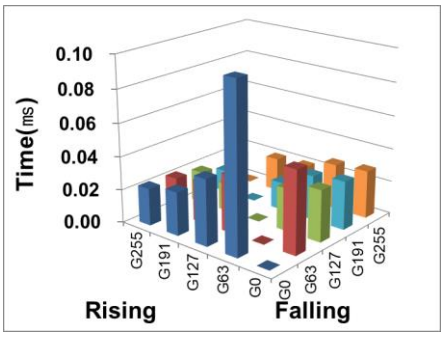
(5) Current Status

Below table is actual data of production on Nov. 22. 2022 (LGD PRV Event Sample)

	G to G Response Time [ms]		Average
	Min.	Max.	
# 1	0.01	0.13	0.03
# 2	0.01	0.12	0.03



< # 1 >



< # 2 >

APPENDIX - IX

■ PLC Curve

(1) It is recommended to the set the Gaming Display Set Peak Luminance to 50% of the Module Peak Luminance at P0 point in Default display mode for considering power savings and prevention of Image retention. (Fig. 1. Set PLC Curve)

- If End users watch videos with fixed images such as broadcast logos for a long time at the level of Module Peak luminance, there is a risk of image retention defects.
  Therefore, the shipping mode luminance control can proactively prevent the risk of image retention defects.
- If customer need to promote the Picture Quality, It is recommended to user store mode.
- It is recommended that the HDR function be applied to the module shipment condition, 'HDR Off'.

(2) It is recommended to automatically operate the light sensor 'On' in Set shipping mode.
- It is recommended to prevent the risk of eye fatigue and image retention defects through the user of appropriate illumination depending on the user's environment.

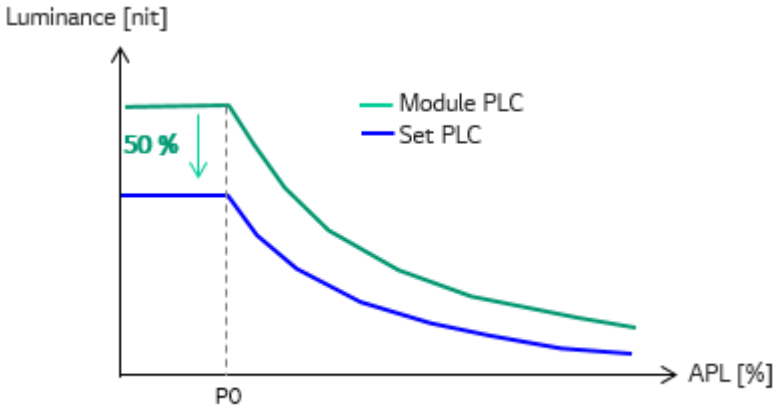


Fig. 1. Set PLC Curve

※ Default Display mode(End-user) : Set Peak Luminance ≤ 50% of Module Peak Luminance
※ Shipment mode : Picture mode first used by end-users after factory shipments
ex) Standard mode