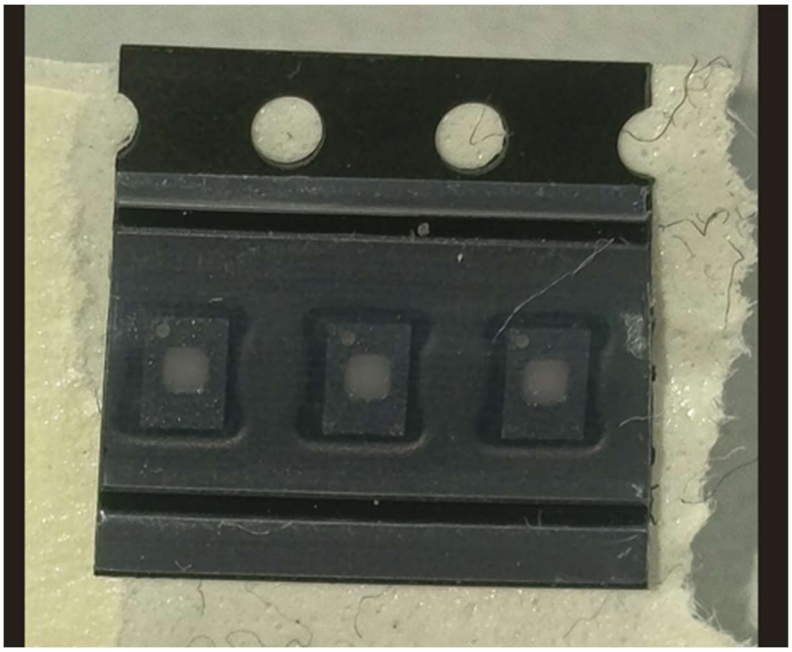

設計驗證
工程課
2026 -04- 02
發行

承　認　書

(Approval Sheet)

客戶名稱: 鈺緯科技開發股份有限公司　DIVA Laboratories. Ltd.

客戶料號: 3ATCS35301Y (A0574)

品名: IC (TCS3530,OLGA,AMS)

設計驗證
工程課
2026 -04- 02
發行
鈺緯科技開發股份有限公司

廠商名稱: 世平興業股份有限公司

產品型號: ams TCS3530

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Product Document

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TCS3530

Fully Embedded, True Color Ambient Light Sensor with Selective Flicker Detection

General Description

The TCS3530 features true color XYZ ambient light detection, as well as flicker detection up to 7kHz. The device comes in a small footprint 8-pin optical module with a dimension of L2.50mm x W1.80mm x H1.50mm. The optical module is fully embedded offering an integrated aperture and integrated diffuser. This unparalleled scale of integration, containing the photodiodes, aperture and diffuser, as well as precise distances between these key optical elements, allows accurate pre-calibration in final optical device test.

The ambient light detection function provides eight concurrent ambient light sensing channels with independent gain configuration. These channels can be arbitrarily connected to the 27 photodiodes. A built-in sequencer enables automated measurements without the need to reprogram the device after every measurement cycle. All photodiodes are covered with an UV/IR blocking filter. This architecture accurately measures ambient light and calculates illuminance, chromaticity, and correlated color temperature (CCT) to manage display appearance.

The device also integrates direct detection of ambient light flicker up to 7kHz. This extended sampling range enables flicker detection from either conventional mains powered 50Hz/60Hz AC light sources as well as modern PDM controlled LED lighting systems. Flicker detection is executed in parallel with ambient light sensing and has independent gain configuration. The flicker detection engine will sample and buffer data for calculating flicker frequencies externally on a host CPU.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits & Features

The benefits and features of TCS3530 are listed below:

Figure 1:
Added Value of Using TCS3530

Benefits	Features

• Invisible ambient light and color sensing under glass	• Configurable, high sensitivity
	  • Programmable gain and integration time
	  • 8192x dynamic range by gain adjustment only
	  • 1mlux minimum detectable illuminance (100ms)
	• Tailored ALS and color response
	  • UV/IR blocking filter for all channels
	  • Clear reference channel
	• ALS/color interrupt with thresholds

• Unique fast ALS integration mode	• Flicker-immune ambient light sensing with programmable integration time
• Integrated ambient light flicker detection on chip	• Independently configurable timing and gain • Concurrent flicker and ALS measurement with new simplified readout methodology • Up to 7kHz flicker detection (14kHz sampling) • FIFO buffer interrupt
• Low power consumption and minimum I^2C traffic (optional I3C mode)	• $1.8V_{BUS}$ and $1.2V_{BUS}$ operation • Configurable sleep mode • Interrupt-driven device • I^2C interface up to 1 MHz (Fast-Mode Plus) • On-chip data compression decreases serial bus traffic
• Integrated status checking for all functions	• Digital and analog ALS saturation flags

Applications

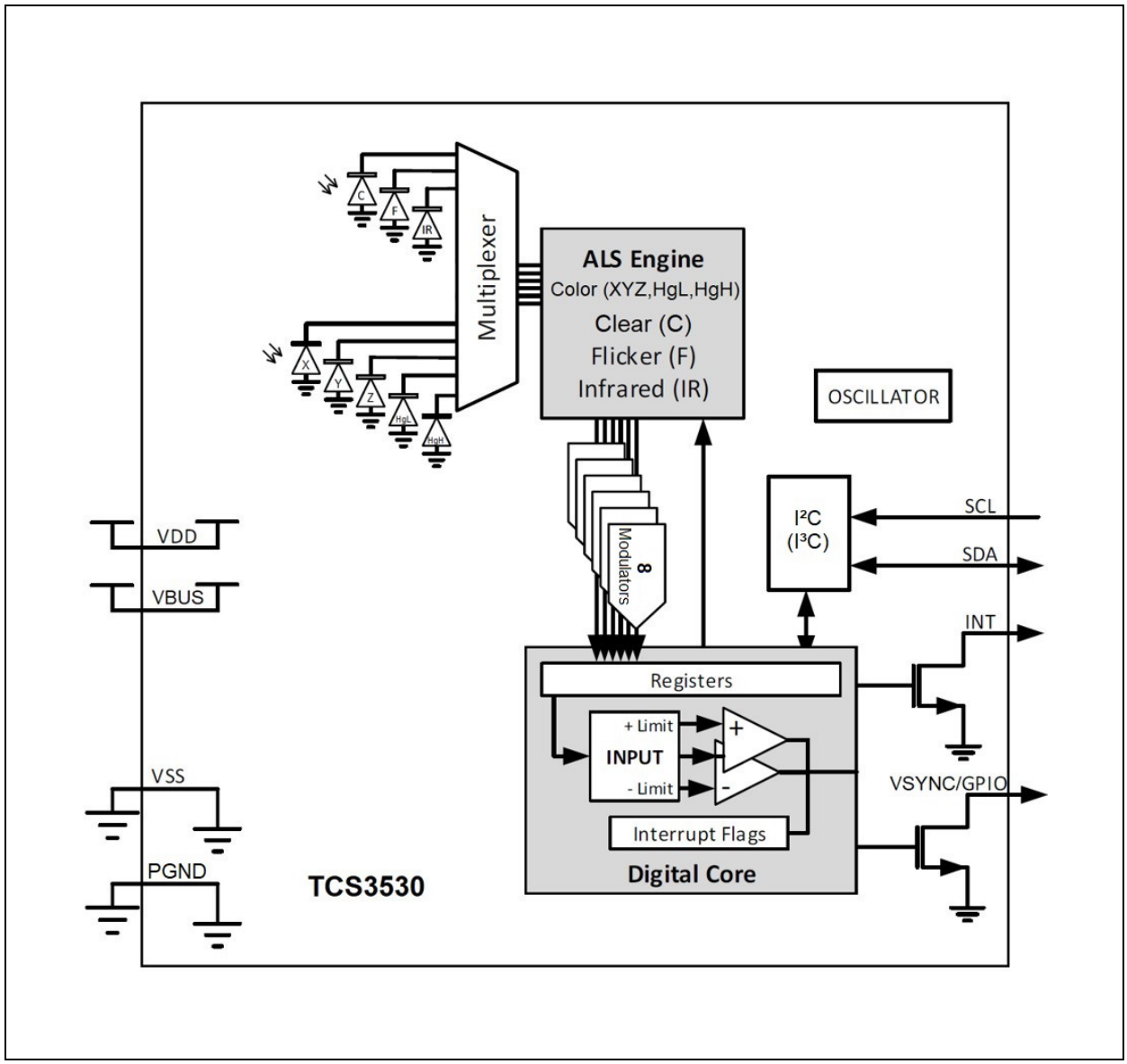
TCS3530 integrates multiple applications within one device. The applications for TCS3530 include:

- CCT and chromaticity calculation
- Auxiliary auto white balancing
- Light type identification
- Flicker-immune camera operation

Block Diagram

The functional blocks of this device are shown below:

Figure 2:
Functional Blocks of TCS3530



Pin Assignments

Figure 3:
Pin Diagram of TCS3530

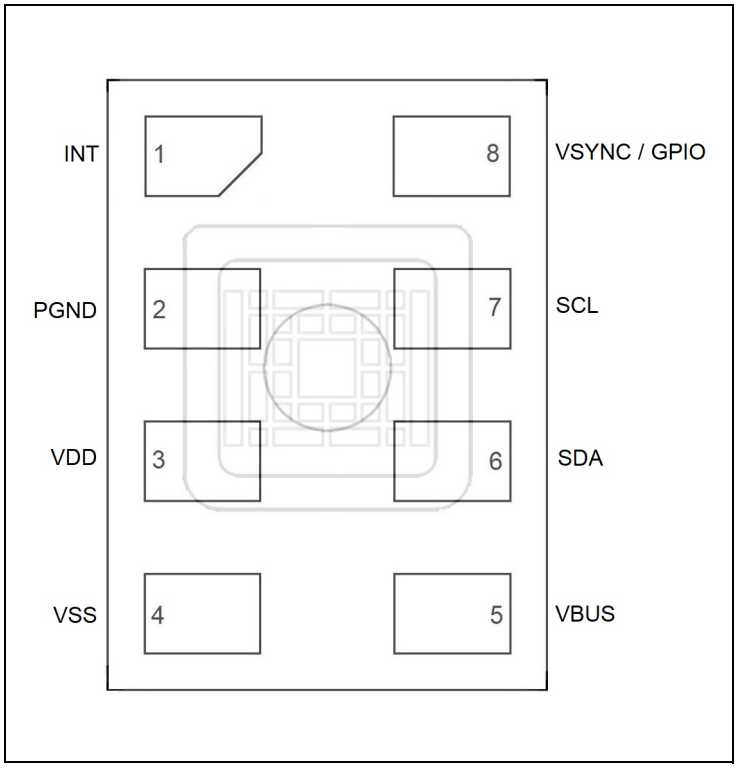


Figure 4:
Pin Description of TCS3530

Pin Number	Pin Name	Description
1	INT	Interrupt. Open-drain output.
2	PGND	Ground. All voltages are referenced to VSS/PGND, and both ground pins must be connected to ground.
3	VDD	Supply voltage (1.8V)
4	VSS	Ground. All voltages are referenced to VSS/PGND, and both ground pins must be connected to ground.
5	VBUS	I^2C (I3C) bus supply voltage
6	SDA	I^2C (I3C) serial data I/O terminal
7	SCL	I^2C (I3C) serial bus clock terminal
8	VSYNC/GPIO	Synchronization input or General Purpose open-drain Input/Output

Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

All voltages with respect to VSS/PGND. Device parameters are guaranteed at V_{DD} = 1.8 V and T_A = 25°C unless otherwise noted.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
V_{DD}	Supply Voltage	-0.3	1.98	V	
V_{BUS}	I²C (I3C) Bus Supply Voltage	-0.3	1.98		
V_{IO}	$V_{SYNC/GPIO}$, V_{INT} Terminal Voltage	-0.3	3.6		
I_{IO}	Output Terminal Current	-3	20	mA	
Stress Parameters					
ESD_{HBM}	HBM Electrostatic Discharge	± 2000		V	JEDEC JS-001-2017
ESD_{CDM}	CDM Electrostatic Discharge	± 500		V	JEDEC JS-002-2018
I_{SCR}	Input Current (latch-up immunity)	± 100		mA	Class II JEDEC JESD78E
Temperature Ranges and Storage Conditions					
T_{STRG}	Storage Temperature Range	-40	85	°C	

Figure 6:
Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Supply voltage		1.7	1.8	1.98	V
V_{IO}	I/O supply voltage		1.62	1.8	3.3	V
$V_{BUS1.2}$	VBUS I/O voltage	V_{BUS}=1.2V	1.08	1.2	1.32	V
$V_{BUS1.8}$	VBUS I/O voltage	V_{BUS}=1.8V	1.62	1.8	1.98	V
$V_{IL-INT/GPIO}$	INT, GPIO input low voltage				0.54	V
$V_{IH-INT/GPIO}$	INT, GPIO input high voltage		0.84			V
$V_{IL-SCL/SDA}$	SCL, SDA		-0.1*V_{BUS}		0.3*V_{BUS}	V
$V_{IH1.2-SCL/SDA}$	SCL, SDA	V_{BUS}=1.2V	0.7*V_{BUS}		1.1*V_{BUS}	V
$V_{IH1.8-SCL/SDA}$	SCL, SDA	V_{BUS}=1.8V	0.7*V_{BUS}		1.98	V
I^2C Bus Operation						
$V_{OL-SDA-I2C}$	SDA output low voltage	V_{BUS}=1.2V/1.8V@ 20mA			0.4	V
I3C Bus Operation						
$V_{OL-SDA1.2-I3C}$	SDA output low voltage	V_{BUS}=1.2V@2mA		0.18		V
$V_{OL-SDA1.8-I3C}$	SDA output low voltage	V_{BUS}=1.8V@3mA		0.27		V
$V_{OH-SDA1.2-I3C}$	SDA output high voltage	V_{BUS}=1.2V@-2mA	V_{BUS}-0.18			V
$V_{OH-SDA1.8-I3C}$	SDA output high voltage	V_{BUS}=1.8V@-3mA	V_{BUS}-0.27			V
Temperature Ranges and Storage Conditions						
T_A	Operating free-air temperature (1)		-30	25	85	°C
Other Conditions						
C_I	Input pin capacitance			4		pF

1. While the device is operational across the temperature range, functionality will vary with temperature.

Optical Characteristics

Parameters listed under Test Level 4 are guaranteed with production tests and SQC (Statistical Quality Control). Parameters listed under Test Level 3 are measured in-line with transparent monitor glasses. Parameters listed under Test Level 2 are measured in lab bench characterization. Parameters listed under Test Level 1 are guaranteed by design. All Test Levels are measured with V_{DD} = 1.8V and T_A = 25°C unless otherwise noted.

Figure 7:
ALS/Color Characteristics of TCS3530, ALS Gain = 128x, Integration Time = 11ms (unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Unit	Test Level
Dark ADC count value (1)	E_e = 0µW/cm^2 ALS gain: 512x Integration time: 100ms	0	0	3	counts	4
ALS gain ratios (2)	0.5x		1/261.10			4
	1x		1/126.90			
	2x		1/63.69			
	4x		1/31.85			
	8x		1/15.53			
	16x		1/8			
	32x		1/4			
	64x		1/2			
	256x		1.92			
	512x		3.79			
	1024x		7.44			
	2048x		14.40			
	4096x		27.90			
ADC noise (4)	White LED, 2700K (3) Integration time: 100ms		0.05			2

Note(s):

1. The typical 3-sigma distribution shows less than 1 count for an ATIME setting of less than 98ms. Residual counts are not considered for dark count measurement.
2. The gain ratios are calculated relative to the response with ALS gain = 128x.
3. The White LED is an InGaN light-emitting diode with integrated phosphor and the following characteristic: correlated color temperature = 2700K.
4. ADC noise is calculated as the standard deviation relative to full scale.

Figure 8:
Channel Irradiance Responsivity

Parameter	Conditions	Min	Typ	Max	Unit	Test Level
X (MOD0)	Optical channel irradiance responsivity of uncalibrated module: 20ms integration time, 128x gain, 2700K White LED light source with an irradiance of 150 µW/cm^2 (approx. 450 lux). Measured with residual counts enabled which corresponds to an effective gain of 2048x.	174	205	230	counts/ (µW/cm^2)	4
Y (MOD1)		170	190	210		
Z (MOD2)		23	30	36		
IR (MOD3)		7	11	16		
HgL (MOD4)		12	17	21		
HgH (MOD5)		18	23	28		
Clear (MOD6)		123	144	163		
Flicker (MOD7)		450	532	607		

Color and Lux Measurement Accuracy

Typical achievable accuracy for color and lux measurements with a calibrated TCS3530. The delta is calculated versus results from reference spectrometer Instrument Systems CAS140 and illuminated with lights sources in XRITE Box (Test Level 2, lab bench, not guaranteed by production testing)

Figure 9:
Color and Lux Measurement Accuracy

Parameter	Conditions	Min	Typ	Max	Unit	Test Level
dE00	LED 2800K (1)		0.2			2
	LED 4000K		0.5			
	Fluorescent (CFL) 6500K (1)		1.1			
	Fluorescent (CWF) 4000K		0.7			
	D65		1.2			
	Halogen (A) 2900K		0.8			
	Halogen (HZ) 2300K		1.7			
	Incandescent (A) 2600K (1)		1.1			

Parameter	Conditions	Min	Typ	Max	Unit	Test Level
dLUX	LED 2800K (1)		1.6		%	2
	LED 4000K		0.1			
	Fluorescent (CFL) 6500K (1)		-1.3			
	Fluorescent (CWF) 4000K		0.1			
	D65		1.3			
	Halogen (A) 2900K		0.4			
	Halogen (HZ) 2300K		2.0			
	Incandescent (A) 2600K(1)		-0.9			
dCCT	LED 2800K (1)		0.2		%	2
	LED 4000K		-0.6			
	Fluorescent (CFL) 6500K (1)		-1.7			
	Fluorescent (CWF) 4000K		-1.9			
	D65		-0.9			
	Halogen (A) 2900K		0.6			
	Halogen (HZ) 2300K		1.6			
	Incandescent (A) 2600K (1)		0.6			

Note(s):

1. Light source not native in XRITE light box.

Wavelength Accuracy

The Channel Center Wavelength and Full-Width-Half-Max Wavelength is measured in-line during filter deposition by means of monitor glasses placed next to the wafers (Test Level 3).

Figure 10:
Channel Center Wavelength

Parameter	Conditions	Min	Typ	Max	Unit	Test Level
X1	Measured in-line with calibrated monochromator using transparent monitor glasses and placed behind a diffuser.	426	436	446	nm	3
X2		584	594	604		
Y		545	555	565		
Z		435	445	455		
HgL		509	519	529		
HgH		535	545	555		

Figure 11:
Channel Full Width Half Max Wavelength (FWHM)

Parameter	Conditions	Min	Typ	Max	Unit	Test Level
X1_low	Measured in-line with calibrated monochromator using transparent monitor glasses and placed behind a diffuser.	410	420	430	nm	3
X2_low		538	548	558		
Y_low		498	508	518		
Z_low		411	421	431		
HgL_low		498	508	518		
HgH_low		525	535	545		
X1_high		455	465	475		
X2_high		622	632	642		
Y_high		603	613	623		
Z_high		466	476	486		
HgL_high		521	531	541		
HgH_high		547	557	567		

Electrical Characteristics

Parameters listed under Test Level 4 are guaranteed with production tests and SQC (Statistical Quality Control). Parameters listed under Test Level 3 are measured in-line with transparent monitor glasses. Parameters listed under Test Level 2 are measured in lab bench characterization. Parameters listed under Test Level 1 are guaranteed by design. All Test Levels are measured with V_{DD} = 1.8V and T_A = 25°C unless otherwise noted.

Figure 12:
Electrical Characteristics of TCS3530, V_{DD} = 1.8 V, T_A = 25°C (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Test Level
$I_{DD;ALS}$	ALS supply current	Active ALS state (1) (PON=AEN=1)		485	560	µA	4
$I_{DD;IDLE}$	Idle current	Idle state (2) (PON=1, AEN=0)		98	130		
$I_{DD;SLEEP}$	Sleep current	Sleep state (3)		0.7	5.0		
I_{LEAK}	Leakage current	Measured on SDA, SCL, INT, GPIO	-5		5		

Note(s):

1. This parameter indicates the supply current during periods of ALS integration. The ALS gain setting will have an effect on the active supply current. The ALS gain setting used for this parameter is 128x.
2. Idle state occurs when PON=1 and all functions are disabled.
3. Sleep state occurs when PON = 0 and I^2C/I3C bus is idle. If Sleep state has been entered as the result of operational flow, SAI = 1, PON will remain high.

Timing Characteristics

Parameters listed under Test Level 4 are guaranteed with production tests and SQC (Statistical Quality Control). Parameters listed under Test Level 3 are measured in-line with transparent monitor glasses. Parameters listed under Test Level 2 are measured in lab bench characterization. Parameters listed under Test Level 1 are guaranteed by design. All Test Levels are measured with V_{DD} = 1.8V and T_A = 25°C unless otherwise noted.

Figure 13:
I²C Timing Characteristics of TCS3530

Symbol	Parameter	Min	Typ	Max	Unit	Test Level
f_{SCL}	I²C clock frequency	0		400	kHz	1
t_{BUF}	Bus free time between start and stop condition	1.3			µs	1
$t_{HD;STA}$	Hold time after (repeated) start condition. After this period, the first clock is generated	0.6				
$t_{SU;STA}$	Repeated start condition setup time	0.6				
$t_{SU;STO}$	Stop condition setup time	0.6				
t_{LOW}	SCL clock low period	1.3				
t_{HIGH}	SCL clock high period	0.6				
$t_{HD;DAT}$	Data hold time	0			ns	1
$t_{SU;DAT}$	Data setup time	100				
t_F	Clock/data fall time			300		
t_R	Clock/data rise time			300		

Figure 14:
Timing Diagram for TCS3530

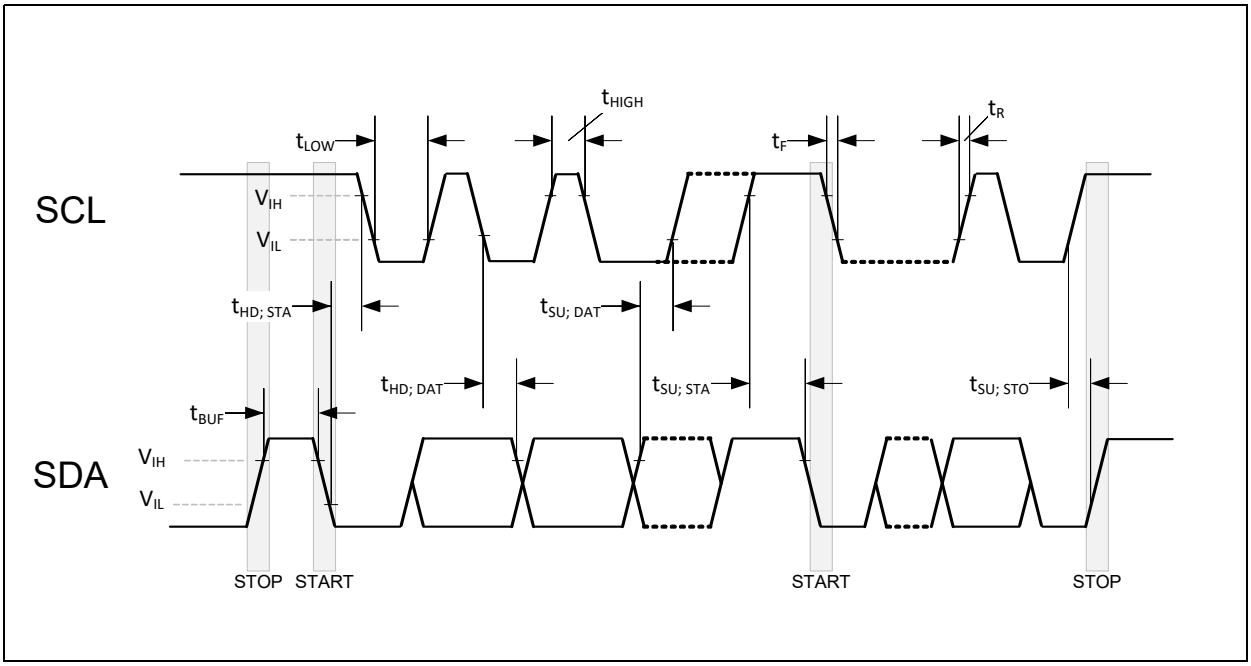
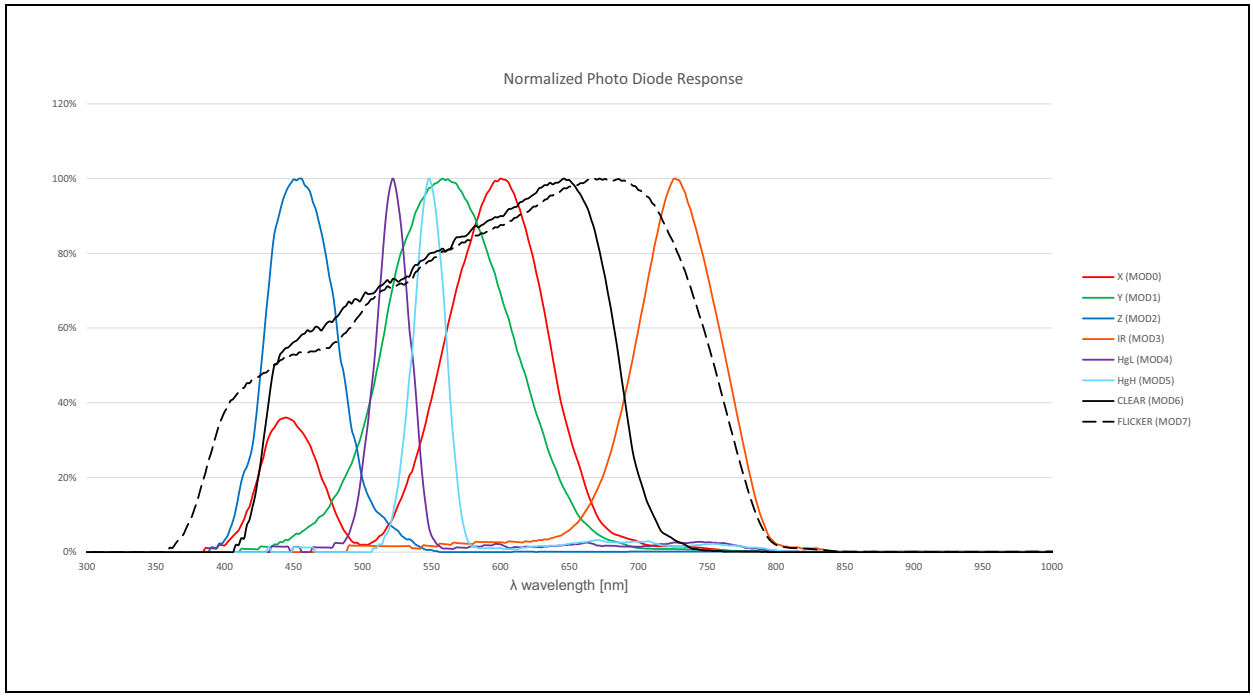


Figure 15:
Functional Timing Characteristics of TCS3530

Symbol	Parameter	Min	Typ	Max	Unit	Test Level
f_{OSC}	Oscillator clock frequency	700	720	740	kHz	4

Typical Operating Characteristics

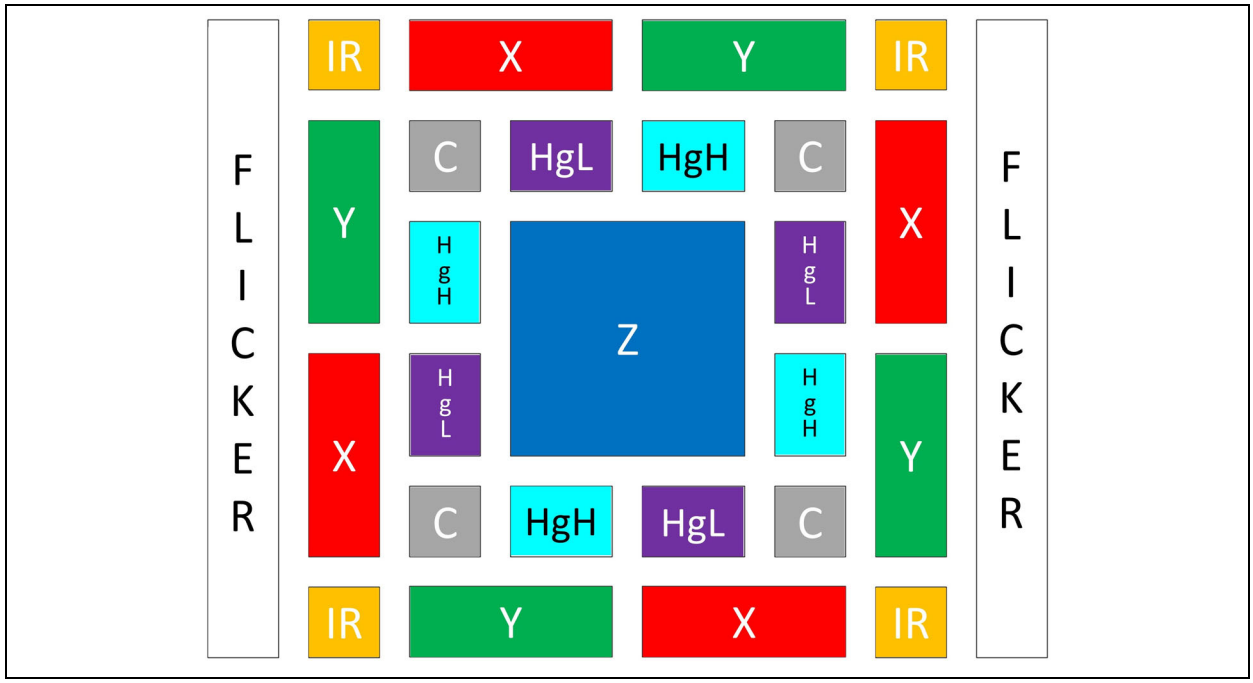
Figure 16:
Normalized Spectral Responsivity



Note(s):

1. The spectral responsivities shown in the figure are measured under a diffuser and normalized.

Figure 17:
Sensor Field Array



Detailed Description

Upon power-up, POR, the device initializes. During initialization (typically 200µs), the device will deterministically send NAK on I^2C and cannot accept I^2C transactions. All communication with the device must be delayed, and all outputs from the device must be ignored including interrupts. After initialization, the device enters the SLEEP state. In this operational state the internal oscillator and other circuitry are not active, resulting in ultra-low power consumption. If an I^2C transaction occurs during this state, the I^2C core wakes up temporarily to service the communication. Once the Power ON bit, PON, is enabled, the device enters the IDLE state in which the internal oscillator and attendant circuitry are active, but power consumption remains low. Whenever a function is enabled (AEN = 1), the device exits the IDLE state. If all functions are disabled (AEN = 0), the device returns to the IDLE state.

As depicted in Figure 18 and Figure 19, the color sensing functions operate in parallel when enabled. Each function is individually configured (e.g. gain, ADC integration time, wait time, persistence, thresholds, etc.).

If Sleep after Interrupt is enabled the state machine will enter SLEEP when an interrupt occurs. Entering SLEEP does not automatically change any of the register settings (e.g. PON bit is still high, but the normal operational state is over-ridden by SLEEP state). SLEEP state is terminated when the SAI_ACTIVE bit is cleared (the status bit is in register 0xA7 and the clear status bit is in register 0xFA).

State Machine Diagrams

Figure 18:
Simplified State Diagram

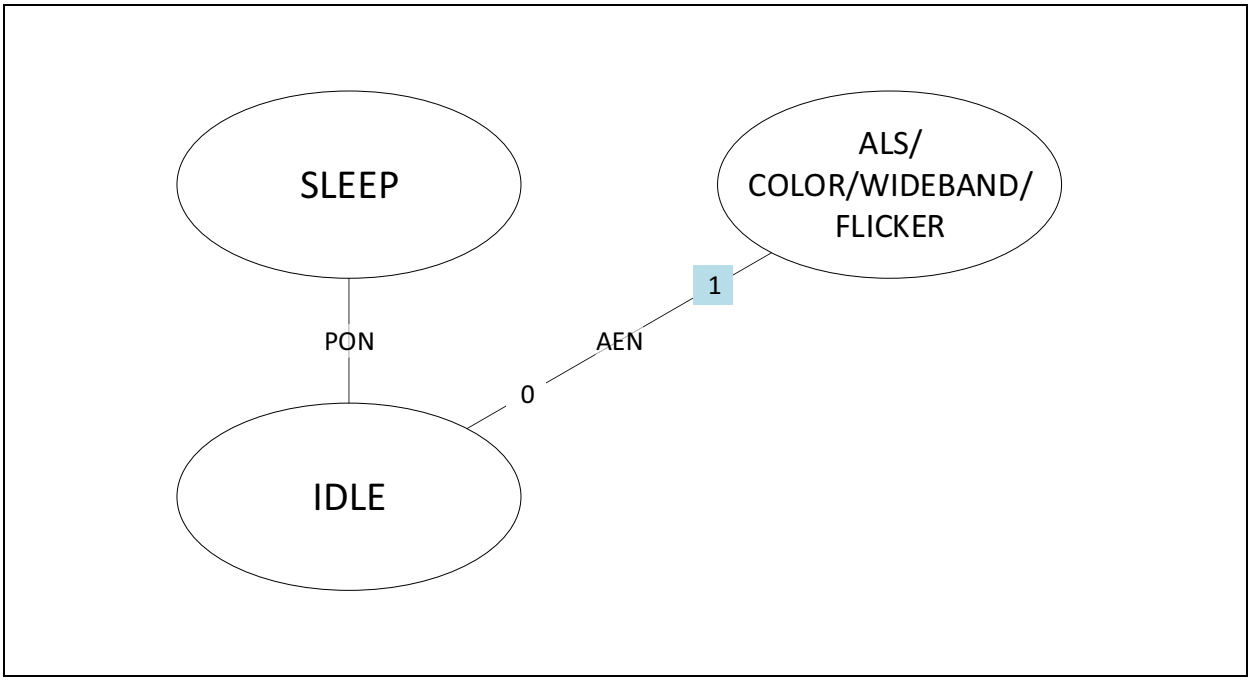
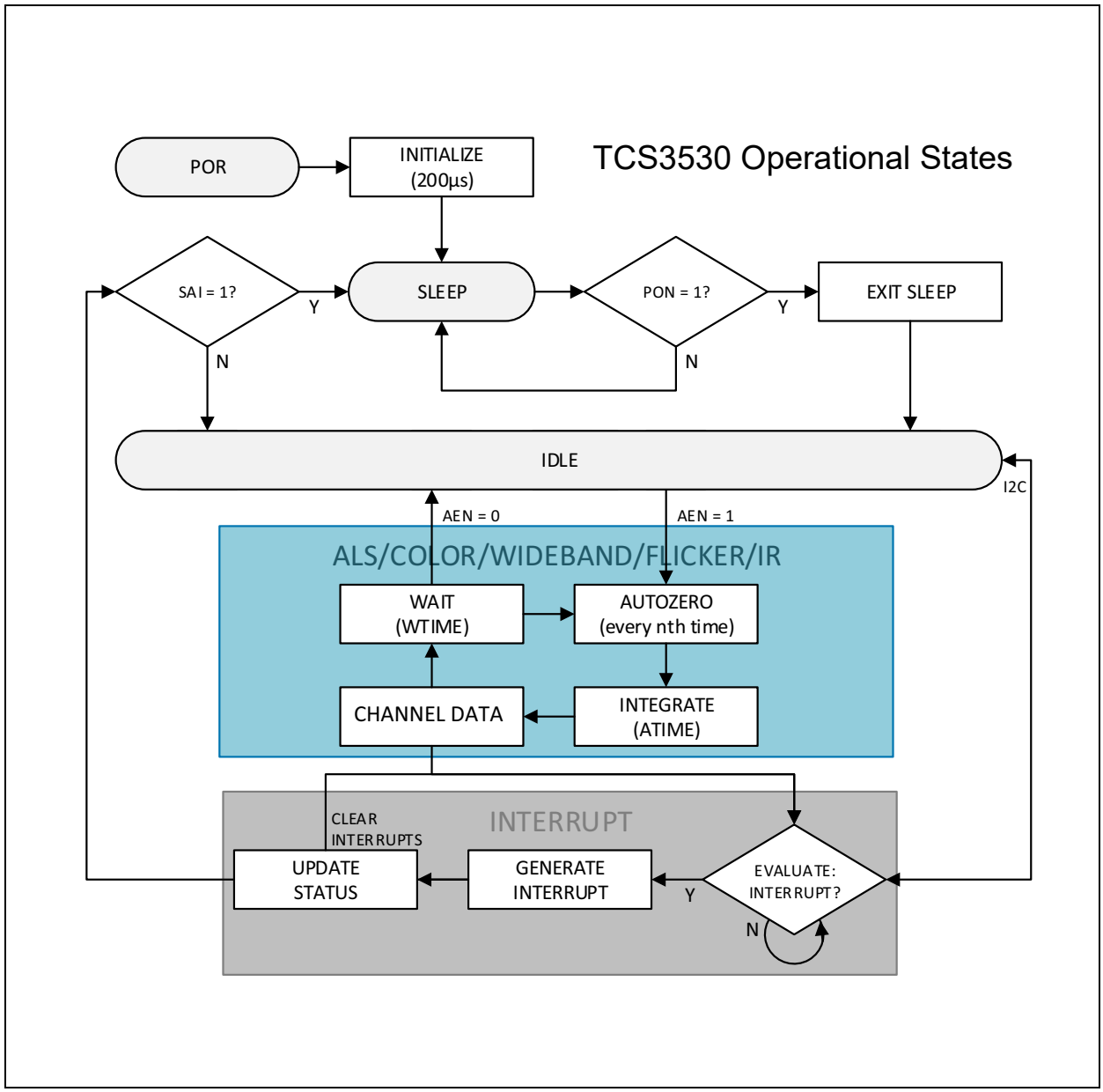


Figure 19:
Detailed State Diagram



I²C Protocol

The device uses I²C serial communication protocol for communication. The device supports 7-bit chip addressing and both standard and full-speed clock frequency modes. Read and Write transactions comply with the standard set by Philips (now NXP). For a complete description of the I²C protocol, please review the NXP I²C design specification.

Internal to the device, an 8-bit buffer stores the register address location of the desired byte to read or write. This buffer auto-increments upon each byte transfer and is retained between transaction events (i.e. valid even after the master issues a STOP command and the I²C bus is released). During consecutive Read transactions, the future/repeated I²C Read transaction may omit the memory address byte normally following the chip address byte; the buffer retains the last register address +1.

All 16-bit fields have a latching scheme for reading and writing. In general it is recommended to use I²C bursts whenever possible, especially in this case when accessing two bytes of one logical entity. When reading these fields, the low byte must be read first, and it triggers a 16-bit latch that stores the 16-bit field. The high byte must be read immediately afterwards. When writing to these fields, the low byte must be written first, immediately followed by the high byte. Reading or writing to these registers without following these requirements will cause errors.

A Write transaction consists of a START, CHIP-ADDRESSWRITE, REGISTER-ADDRESS WRITE, DATA BYTE(S), and STOP. Following each byte (9TH clock pulse) the slave places an ACKNOWLEDGE/NOT- ACKNOWLEDGE (ACK/NACK) on the bus. If NACK is transmitted by the slave, the master may issue a STOP.

A Read transaction consists of a START, CHIP-ADDRESSWRITE, REGISTER-ADDRESS, RESTART, CHIP-ADDRESSREAD, DATA BYTE(S), and STOP. Following all but the final byte the master places an ACK on the bus (9TH clock pulse). Termination of the Read transaction is indicated by a NACK being placed on the bus by the master, followed by STOP.

Register Overview

The device is controlled and monitored by registers accessed through the I²C serial interface. These registers provide device control functions and are read to determine device status and acquire device data.

Register Map

The register set is summarized in Figure 20. The values of all registers and fields that are listed as reserved or are not listed must not be changed at any time. The power-on reset values of each bit are indicated in these columns. Two-byte fields are always latched with the low byte followed by the high byte.

Figure 20:
Register Map

Addr	Name	Description	Reset
0x24	CONTROL_SCL	Initialize the device	0x00
0x40	MOD_OFFSET0[7:0]	Modulator Offset Register	0x00
0x41	MOD_OFFSET0[9:8]	Modulator Offset Register	0x00
0x42	MOD_OFFSET1[7:0]	Modulator Offset Register	0x00
0x43	MOD_OFFSET1[9:8]	Modulator Offset Register	0x00
0x44	MOD_OFFSET2[7:0]	Modulator Offset Register	0x00
0x45	MOD_OFFSET2[9:8]	Modulator Offset Register	0x00
0x46	MOD_OFFSET3[7:0]	Modulator Offset Register	0x00
0x47	MOD_OFFSET4[9:8]	Modulator Offset Register	0x00
0x48	MOD_OFFSET4[7:0]	Modulator Offset Register	0x00
0x49	MOD_OFFSET4[9:8]	Modulator Offset Register	0x00
0x4A	MOD_OFFSET5[7:0]	Modulator Offset Register	0x00
0x4B	MOD_OFFSET5[9:8]	Modulator Offset Register	0x00
0x4C	MOD_OFFSET6[7:0]	Modulator Offset Register	0x00
0x4D	MOD_OFFSET6[9:8]	Modulator Offset Register	0x00
0x4E	MOD_OFFSET7[7:0]	Modulator Offset Register	0x00
0x4F	MOD_OFFSET7[9:8]	Modulator Offset Register	0x00
0x7F	OSCEN	Power on polling	0x00
0x80	ENABLE	Enables device states	0x00
0x81	MEAS_MODE0	Measurement mode settings 0	0x04
0x82	MEAS_MODE1	Measurement mode settings 1	0x0C

Addr	Name	Description	Reset
0x83	SAMPLE_TIME0	Flicker and ALS sample time settings 0	0x60
0x84	SAMPLE_TIME1	Flicker and ALS sample time settings 1	0x16
0x85	SAMPLE_TIME_ ALTERNATIVE0	Alternative sample time setting 0	0x60
0x86	SAMPLE_TIME_ ALTERNATIVE1	Alternative sample time setting 1	0x16
0x87	ALS_NR_SAMPLES0	ALS number of samples setting 0	0x00
0x88	ALS_NR_SAMPLES1	ALS number of samples setting 1	0x00
0x89	ALS_NR_SAMPLES_ ALTERNATIVE0	Alternative ALS number of samples setting 0	0x00
0x8A	ALS_NR_SAMPLES_ ALTERNATIVE1	Alternative ALS number of samples setting 1	0x00
0x8B	FD_NR_SAMPLES0	ALS Interrupt Low Threshold [15:8]	0x00
0x8C	FD_NR_SAMPLES1	ALS Interrupt Low Threshold [23:16]	0x00
0x8D	FD_NR_SAMPLES_ ALTERNATIVE0	ALS Interrupt High Threshold [7:0]	0x00
0x8E	FD_NR_SAMPLES_ ALTERNATIVE1	ALS Interrupt High Threshold [15:8]	0x00
0x8F	WTIME	Wait Time	0x00
0x90	AUX_ID	Auxiliary Identification	0x00
0x91	REV_ID	Revision Identification	0x14
0x92	ID	Device Identification	0x68
0x93	AILT0	ALS Interrupt Low Threshold 0	0x00
0x94	AILT1	ALS Interrupt Low Threshold 1	0x00
0x95	AILT2	ALS Interrupt Low Threshold 2	0x00
0x96	AIHT0	ALS Interrupt High Threshold 0	0x00
0x97	AIHT1	ALS Interrupt High Threshold 1	0x00
0x98	AIHT2	ALS Interrupt High Threshold 2	0x00
0x99	AGC_NR_ SAMPLES[7:0]	AGC Number of Samples	0x00
0x9A	AGC_NR_ SAMPLES[10:8]	AGC Number of Samples	0x00
0x9B	STATUS	Device Status Information	0x00
0x9C	STATUS2	Device Status Information 2	0x00

Addr	Name	Description	Reset
0x9D	STATUS3	Device Status Information 3	0x08
0x9E	STATUS4	Device Status Information 4	0x00
0x9F	STATUS5	Device Status Information 5	0x00
0xA0	STATUS6	Device Status Information 6	0x00
0xA1	CFG0	Configuration 0	0x00
0xA2	CFG1	Configuration 1	0x00
0xA3	CFG2	Configuration 2	0x00
0xA4	CFG3	Configuration 3	0x00
0xA5	CFG4	Configuration 4	0x00
0xA6	CFG5	Configuration 5	0x00
0xA7	CFG6	Configuration 6	0x03
0xA8	CFG7	Configuration 7	0x01
0xA9	CFG8	Configuration 8	0xC3
0xAA	CFG9	Configuration 9	0x00
0xAB	MOD_CHANNEL_CTRL	Modulator Channel Control	0x00
0xAD	TRIGGER_MODE	Repetition time of modulator or sequencer measurement	0x00
0xAE	OSC_TUNE	Oscillator tuning settings	0x00
0xB0	VSYNC_GPIO_INT	Control of VSYNC/GPIO pin	0x02
0xBA	INTENAB	Enable interrupts	0x00
0xBB	SIEN	Enable saturation interrupts	0x00
0xBC	CONTROL	Device control settings	0x00
0xBD	ALS_DATA_STATUS	ALS measurement data status	0x00
0xBE	ALS_DATA_FIRST	ALS data read and update control	0x00
0xBF	ALS_DATA	ALS data read and update control	0x00
0xC0	MEAS_SEQR_STEP0_MOD_GAINX_0	Defines the gain of modulator for the measurement sequencer step	0x88
0xC1	MEAS_SEQR_STEP0_MOD_GAINX_1	Defines the gain of modulator for the measurement sequencer step	0x88
0xC2	MEAS_SEQR_STEP0_MOD_GAINX_2	Defines the gain of modulator for the measurement sequencer step	0x88

Addr	Name	Description	Reset
0xC3	MEAS_SEQR_STEP0_MOD_GAINX_3	Defines the gain of modulator for the measurement sequencer step	0x88
0xC4	MEAS_SEQR_STEP1_MOD_GAINX_0	Defines the gain of modulator for the measurement sequencer step	0x88
0xC5	MEAS_SEQR_STEP1_MOD_GAINX_1	Defines the gain of modulator for the measurement sequencer step	0x88
0xC6	MEAS_SEQR_STEP1_MOD_GAINX_2	Defines the gain of modulator for the measurement sequencer step	0x88
0xC7	MEAS_SEQR_STEP1_MOD_GAINX_3	Defines the gain of modulator for the measurement sequencer step	0x88
0xC8	MEAS_SEQR_STEP2_MOD_GAINX_0	Defines the gain of modulator for the measurement sequencer step	0x88
0xC9	MEAS_SEQR_STEP2_MOD_GAINX_1	Defines the gain of modulator for the measurement sequencer step	0x88
0xCA	MEAS_SEQR_STEP2_MOD_GAINX_2	Defines the gain of modulator for the measurement sequencer step	0x88
0xCB	MEAS_SEQR_STEP2_MOD_GAINX_3	Defines the gain of modulator for the measurement sequencer step	0x88
0xCC	MEAS_SEQR_STEP3_MOD_GAINX_0	Defines the gain of modulator for the measurement sequencer step	0x88
0xCD	MEAS_SEQR_STEP3_MOD_GAINX_1	Defines the gain of modulator for the measurement sequencer step	0x88
0xCE	MEAS_SEQR_STEP3_MOD_GAINX_2	Defines the gain of modulator for the measurement sequencer step	0x88
0xCF	MEAS_SEQR_STEP3_MOD_GAINX_3	Defines the gain of modulator for the measurement sequencer step	0x88
0xD0	MEAS_SEQR_STEP0_FD	Defines whether or not a flicker measurement shall be executed with respective modulator	0x00
0xD1	MEAS_SEQR_STEP1_FD	Defines whether or not a flicker measurement shall be executed with respective modulator	0x00
0xD2	MEAS_SEQR_STEP2_FD	Defines whether or not a flicker measurement shall be executed with respective modulator	0x00
0xD3	MEAS_SEQR_STEP3_FD	Defines whether or not a flicker measurement shall be executed with respective modulator	0x00
0xD4	MEAS_SEQR_STEP0_RESIDUAL	Defines whether or not a residual measurement shall be executed with respective modulator	0xFF
0xD5	MEAS_SEQR_STEP1_RESIDUAL	Defines whether or not a residual measurement shall be executed with respective modulator	0xFF

Addr	Name	Description	Reset
0xD6	MEAS_SEQR_STEP2_RESIDUAL	Defines whether or not a residual measurement shall be executed with respective modulator	0xFF
0xD7	MEAS_SEQR_STEP3_RESIDUAL	Defines whether or not a residual measurement shall be executed with respective modulator	0xFF
0xD8	MEAS_SEQR_STEP0_ALS	Defines whether or not an ALS measurement shall be executed with respective modulator	0xFF
0xD9	MEAS_SEQR_STEP1_ALS	Defines whether or not an ALS measurement shall be executed with respective modulator	0x00
0xDA	MEAS_SEQR_STEP2_ALS	Defines whether or not an ALS measurement shall be executed with respective modulator	0x00
0xDB	MEAS_SEQR_STEP3_ALS	Defines whether or not an ALS measurement shall be executed with respective modulator	0x00
0xDC	MEAS_SEQR_APERS_AND_VSYNC_WAIT	Defines the measurement sequencer pattern	0x01
0xDD	MEAS_SEQR_AGC	Defines the measurement sequencer pattern	0xFF
0xDE	MEAS_SEQR_SMUX_AND_SAMPLE_TIME	Defines the measurement sequencer pattern	0x00
0xDF	MEAS_SEQR_WAIT_AND_TS_ENABLE	Defines the measurement sequencer pattern	0x01
0xE0	MOD_CALIB_CFG0	Defines the modulator calibration repetition rate	0xFF
0xE2	MOD_CALIB_CFG2	Defines the modulator calibration settings	0x69
0xE3	MOD_CALIB_CFG3	Defines the modulator autozero settings	0x6A
0xE7	MOD_COMP_CFG2	Allows to change the modulator IDAC range	0xBF
0xE8	MOD_RESIDUAL_CFG0	Defines modulator clock cycles for residual measurements	0x00
0xE9	MOD_RESIDUAL_CFG1	Defines relative steps for residual measurements	0x00
0xEA	MOD_RESIDUAL_CFG2	Defines relative steps for residual measurements	0x00
0xEB	VSYNC_DELAY_CFG0	Defines the delay time relative to VSYNC	0x00
0xEC	VSYNC_DELAY_CFG1	Defines the delay time relative to VSYNC	0x00
0xED	VSYNC_PERIOD0	Allows to measure the period of a VSYNC input signal	0x00
0xEE	VSYNC_PERIOD1	Allows to measure the period of a VSYNC input signal	0x00
0xEF	VSYNC_PERIOD_TARGET0	Allows to set a target period depending on the VSYNC input signal	0x00

Addr	Name	Description	Reset
0xF0	VSYNC_PERIOD_TARGET1	Allows to set a target period depending on the VSYNC input signal	0x00
0xF1	VSYNC_CONTROL	Allows to sets various oscillator synchronization modes	0x00
0xF2	VSYNC_CFG	Defines the oscillator calibration and synchronization mode	0x00
0xF3	FIFO_THR	Configuration of FIFO threshold interrupt	0x7F
0xF4	MOD_FIFO_DATA_CFG0	Defines conditions and data format for corresponding modulator to write to FIFO	0x8F
0xF5	MOD_FIFO_DATA_CFG1	Defines conditions and data format for corresponding modulator to write to FIFO	0x8F
0xF6	MOD_FIFO_DATA_CFG2	Defines conditions and data format for corresponding modulator to write to FIFO	0x8F
0xF7	MOD_FIFO_DATA_CFG3	Defines conditions and data format for corresponding modulator to write to FIFO	0x8F
0xF8	MOD_FIFO_DATA_CFG4	Defines conditions and data format for corresponding modulator to write to FIFO	0x8F
0xF9	MOD_FIFO_DATA_CFG5	Defines conditions and data format for corresponding modulator to write to FIFO	0x8F
0xFA	MOD_FIFO_DATA_CFG6	Defines conditions and data format for corresponding modulator to write to FIFO	0x8F
0xFB	MOD_FIFO_DATA_CFG7	Defines conditions and data format for corresponding modulator to write to FIFO	0x8F
0xFC	FIFO_STATUS0	Contains number of FIFO entries	0x00
0xFD	FIFO_STATUS0	Contains number of FIFO entries	0x00
0xFD	FIFO_STATUS1	Contains FIFO overflow and underflow status	0x00
0xFE	FIFO_DATA_PROTOCOL	Register to read out FIFO with FIFO protocol mechanism	0x00
0xFF	FIFO_DATA	Register contains FIFO data for read-out	0x00

Register Description

CONTROL_SCL Register

Figure 21:
CONTROL_SCL

Addr: 0x24		CONTROL_SCL		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:1	Reserved	0		
0	SOFT_RESET	0	R/W	**Software Reset.** If set and executable, the software Reset will initialize the device in the same way as hardware reset.

Note(s):

1. Return to the Register Map (0x24).

Modulator Offset Register

Figure 22:
Modulator Offset Register

Addr	Bit	Field	Reset	Type	Description
0x40	7:0	MOD_ OFFSET0[7:0]	0	R/W	**Modulator Offset Registers** These registers hold the 8 LSB or the 2 MSB bits of the modulator offset value for the related modulator channel. It can be overwritten, and it gets overwritten by the auto-zero mechanism. The value is 10-bit wide and 2's complement encoded. -512 gets saturated to -511, thus the range is from ±511. Do not write -512.
0x41	7:2	Reserved	0		
0x41	1:0	MOD_ OFFSET0[9:8]	0	R/W	
0x42	7:0	MOD_ OFFSET1[7:0]	0	R/W	
0x43	7:2	Reserved	0		
0x43	1:0	MOD_ OFFSET1[9:8]	0	R/W	
0x44	7:0	MOD_ OFFSET2[7:0]	0	R/W	

Addr	Bit	Field	Reset	Type	Description
0x45	7:2	Reserved	0		**Modulator Offset Registers** These registers hold the 8 LSB or the 2 MSB bits of the modulator offset value for the related modulator channel. It can be overwritten, and it gets overwritten by the auto-zero mechanism. The value is 10-bit wide and 2's complement encoded. -512 gets saturated to -511, thus the range is from ±511. Do not write -512.
0x45	1:0	MOD_ OFFSET2[9:8]	0	R/W	
0x46	7:0	MOD_ OFFSET3[7:0]	0	R/W	
0x47	7:2	Reserved	0		
0x47	1:0	MOD_ OFFSET4[9:8]	0	R/W	
0x48	7:0	MOD_ OFFSET4[7:0]	0	R/W	
0x49	7:2	Reserved	0		
0x49	1:0	MOD_ OFFSET4[9:8]	0	R/W	
0x4A	7:2	MOD_ OFFSET5[7:0]	0	R/W	
0x4B	1:0	Reserved	0		
0x4B	7:0	MOD_ OFFSET5[9:8]	0	R/W	
0x4C	7:2	MOD_ OFFSET6[7:0]	0	R/W	
0x4D	1:0	Reserved	0		
0x4D	7:0	MOD_ OFFSET6[9:8]	0	R/W	
0x4E	7:2	MOD_ OFFSET7[7:0]	0	R/W	
0x4F	1:0	Reserved	0		
0x4F	7:0	MOD_ OFFSET7[9:8]	0	R/W	

Note(s):

1. Return to the Register Map (0x40, 0x41, 0x42, 0x43, 0x44, 0x45, 0x46, 0x47, 0x48, 0x49, 0x4A, 0x4B, 0x4C, 0x4D, 0x4E, 0x4F).

OSCEN Register

Figure 23:
OSCEN

Addr: 0x7F		OSCEN		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:3	Reserved	0		
2	PON_INIT	0	R	This bit is "1" after power on for about 300µs. The device will not respond to any I²C/I3C bus traffic. It can be used for power on polling.
1	OSCEN_STATUS	0	R	**Oscillator Enable.** The I²C/I3C access to all clocked registers is disabled, if the oscillator is turned off.
0	OSCEN	0	R/W	**Oscillator Enable.** Writing a "1" activates the oscillator. Writing a "0" disables the oscillator. Note, that "PON" in register 0x80 also indicates when the oscillator is on and the internal state-machine is enabled and operating. This operation is temporarily disabled by "SAI" in register 0xA1 while the oscillator keeps running (e.g. for single-shot measurements).

Note(s):

1. Return to the Register Map (0x7F).

ENABLE Register

Figure 24:
ENABLE

Addr: 0x80		ENABLE		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	Reserved	0		
6	FDEN	0	R/W	**Flicker Detection Enable.** Writing a "1" activates flicker detection. Writing a "0" disables flicker detection.
5:2	Reserved	0		
1	AEN	0	R/W	**ALS Enable.** Writing a "1" enables ALS/Color. Writing a **"0"** disables ALS/Color.
0	PON	0	R/W	**Power ON**. When asserted, the internal oscillator is activated, allowing timers and ADC channels to operate. Writing a "0" disables the oscillator and clears PEN, and AEN. Only set this bit after all other registers have been initialized by the host.

Note(s):

1. Return to the Register Map (0x80).

MEAS_MODE0 Register

Figure 25:
MEAS_MODE0

Addr: 0x81		MEAS_MODE0		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	STOP_AFTER_NTH_ ITERATION	0	R/W	Stops a manual calibration after n^{th} iterations by setting FDEN and AEN to "0". PON will stay at "1". Per default it stops after one calibration.
6	ENABLE_AGC_ ASAT_DOUBLE_ STEP_DOWN	0	R/W	Enables two gain steps down at once in case of an analogue AGC saturation and at a gain step still >0. This will allow a faster reach of 25% full-scale range and a more prompt reaction if analogue saturations occurs.
5	MEASUREMENT_ SEQUENCER_ SINGLE_SHOT_ MODE	0	R/W	Start one measurement cycle with sequencer settings and stop it by asserting Sleep After Interrupt (SAI)
4	MOD_FIFO_ALS_ STATUS_WRITE_ ENABLE	0	R/W	Enables writing of ALS status to the FIFO RAM in case ALS data scaling is used as well as 16-bit ALS data writing. It is needed to be able to correctly interpret the ALS data.
3:0	ALS_SCALE	4	R/W	ALS_SCALE is used to avoid that redundant ALS MSBs are transmitted and are reducing possible resolution, since the ALS data register is only 16 bits wide (internally the result can be 26 bits wide = 11 bits samples + 11 bits sampling time + 4 bits residuals - ALS_MSB_POSITION). The ALS_ SCALE register defines the number of MSBs which must be "0" so that the scaled representation is used in the ALS data registers instead of the unscaled representation.

Note(s):

1. Return to the Register Map (0x81).

MEAS_MODE1 Register

Figure 26:
MEAS_MODE1

Addr: 0x82		MEAS_MODE1		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	MOD_FIFO_FD_END_MARKER_WRITE_ENABLE	0	R/W	Enables writing of end marker to FIFO after each complete flicker measurement.
6	MOD_FIFO_FD_CHECKSUM_WRITE_ENABLE	0	R/W	Enables writing of flicker checksum to FIFO after each complete flicker measurement.
5	MOD_FIFO_FD_GAIN_WRITE_ENABLE	0	R/W	Enables writing of gain to FIFO after each complete flicker measurement. This is required in case AGC is enabled.
4:0	ALS_MSB_POSITION	12	R/W	Internally the result can be 26 bits wide = 11-bit samples + 11-bit sampling time + 4-bit residuals and is stored in a 32-bit register. ALS_MSB_POSITION defines the MSB in this 32-bit register.

Note(s):

1. Return to the Register Map (0x82).

SAMPLE_TIME0 Register

Figure 27:
SAMPLE_TIME0

Addr: 0x83		SAMPLE_TIME0		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:5	SAMPLE_TIME[2:0]	011b	R/W	Flicker sampling time and ALS measurement time step. Sets the time in steps of 1.388889µs modulator clock. Please observe that SAMPLE_TIME needs to be set in register 0x83 and 0x84 (11-bit wide). It counts from 0-2047 (2048 counts). SAMPLE_TIME+1 = 1/FlickerSamplingFreq/1.388889µs Default: 179+1 = 1/4000Hz / 1.388889µs (180 counts as counted 0-179) ALSMeasurementTimeStep = (SAMPLE_TIME+1) x 1.388889µs Default: 250µs = (179+1) x 1.388889µs
4	Reserved	0		
3:0	MEASUREMENT_ SEQUENCER_ FD_NR_SAMPLES_ PATTERN	0	R/W	Sets the number of flicker samples for each sequencer step. If set to 0001b the number is FD_NR_SAMPLES else it is FD_ NR_SAMPLES_ALTERNATIVE.

Note(s):

1. Return to the Register Map (0x83).

SAMPLE_TIME1 Register

Figure 28:
SAMPLE_TIME1

Addr: 0x84		SAMPLE_TIME1		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	SAMPLE_ TIME[10:3]	0x16	R/W	Please see SAMPLE_TIME0.

Note(s):

1. Return to the Register Map (0x84).

SAMPLE_TIME_ALTERNATIVE0 Register

Figure 29:
SAMPLE_TIME_ALTERNATIVE0

Addr: 0x85		SAMPLE_TIME_ALTERNATIVE0		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:5	SAMPLE_TIME_ ALTERNATIVE[2:0]	011b	R/W	**Alternative SAMPLE_TIME.** Can be selected with MEASUREMENT_SEQUENCER_SMUX_PATTERN, per measurement sequencer step.
4	Reserved	0		
3:0	MEASUREMENT_ SEQUENCER_ALS_ NR_SAMPLES_ PATTERN	0	R/W	Sets the number of ALS samples for each sequencer step. If set to 0001b, the number is ALS_ NR_SAMPLES, else it is ALS_NR_SAMPLES_ ALTERNATIVE.

Note(s):

1. Return to the Register Map (0x85).

SAMPLE_TIME_ALTERNATIVE1 Register

Figure 30:
SAMPLE_TIME_ALTERNATIVE1

Addr: 0x86		SAMPLE_TIME_ALTERNATIVE1		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	SAMPLE_TIME_ ALTERNATIVE[10:3]	0x16	R/W	Please see SAMPLE_TIME_ALTERNATIVE0.

Note(s):

1. Return to the Register Map (0x86).

ALS_NR_SAMPLES0 Register

Figure 31:
ALS_NR_SAMPLES0

Addr: 0x87		ALS_NR_SAMPLES0		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	ALS_NR_ SAMPLES[7:0]	0	R/W	ALS_NR_OF_SAMPLES defines the total measurement time for ALS together with SAMPLE_TIME in steps of 1.388889µs modulator clock. Please observe that ALS_ NR_OF_SAMPLES needs to be set in register 0x87 and 0x88 (11-bit wide). It counts from 0-2047 (2048 counts). ALSMeasurementTime = (ALS_NR_SAMPLES+1) x (SAMPLE_TIME+1) x 1.388889µs Default: 250µs = (0+1) x (179+1) x 1.388889µs Example: 100ms = (399+1) x (179+1) x 1.388889µs In case residual measurement is enabled, SAMPLE_TIME is reduced which also reduces ALSMeasurementTime.

Note(s):

1. Return to the Register Map (0x87).

ALS_NR_SAMPLES1 Register

Figure 32:
ALS_NR_SAMPLES1

Addr: 0x88		ALS_NR_SAMPLES1		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:3	Reserved	0	0	
2:0	ALS_NR_ SAMPLES[10:8]	0	R/W	Please see ALS_NR_SAMPLES0.

Note(s):

1. Return to the Register Map (0x88).

ALS_NR_SAMPLES_ALTERNATIVE0 Register

Figure 33:
ALS_NR_SAMPLES_ALTERNATIVE0

Addr: 0x89		ALS_NR_SAMPLES_ALTERNATIVE0		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	ALS_NR_ SAMPLES_ ALTERNATIVE[7:0]	0	R/W	ALS_NR_OF_SAMPLES_ALTERNATIVE defines the total measurement time for ALS together with SAMPLE_TIME in steps of 1.388889µs modulator clock. Please observe that ALS_NR_OF_SAMPLES_ALTERNATIVE needs to be set in register 0x89 and 0x8A (11-bit wide). It counts from 0-2047 (2048 counts). ALSMeasurementTime = (ALS_NR_SAMPLES_ ALTERNATIVE+1) x (SAMPLE_TIME+1) x 1.388889µs Default: 250µs = (0+1) x (179+1) x 1.388889µs Example: 100ms = (399+1) x (179+1) x 1.388889µs Attention: In case residual measurement is enabled, SAMPLE_TIME is reduced, which also reduces ALSMeasurementTime.

Note(s):

1. Return to the Register Map (0x89).

ALS_NR_SAMPLES_ALTERNATIVE1 Register

Figure 34:
ALS_NR_SAMPLES_ALTERNATIVE1

Addr: 0x8A		ALS_NR_SAMPLES_ALTERNATIVE1		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:3	Reserved	0		
2:0	ALS_NR_ SAMPLES_ ALTERNATIVE[10:8]	0	R/W	Please see ALS_NR_SAMPLES_ALTERNATIVE0.

Note(s):

1. Return to the Register Map (0x8A).

FD_NR_SAMPLES0 Register

Figure 35:
FD_NR_SAMPLES0

Addr: 0x8B		FD_NR_SAMPLES0		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	FD_NR_ SAMPLES[7:0]	0	R/W	FD_NR_OF_SAMPLES defines the total measurement time for Flicker together with SAMPLE_TIME in steps of 1.388889µs modulator clock. Please observe that FD_NR_ OF_SAMPLES needs to be set in register 0x8B and 0x8C (11-bit wide). It counts from 0-2047 (2048 counts). FDMeasurementTime = (FD_NR_SAMPLES+1) x (SAMPLE_ TIME+1) x 1.388889µs Default: 250µs = (0+1) x (179+1) x 1.388889µs Example: 100ms = (399+1) x (179+1) x 1.388889µs In case residual measurement is enabled, SAMPLE_TIME is reduced which also reduces FDMeasurementTime.

Note(s):

1. Return to the Register Map (0x8B).

FD_NR_SAMPLES1 Register

Figure 36:
FD_NR_SAMPLES1

Addr: 0x8C		FD_NR_SAMPLES1		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	FD_NR_ SAMPLES_ INFINITE	0	R/W	When asserted flicker measurement sequences will be infinitely repeated. In this mode, no end markers are inserted but results are continuously written into the FIFO.
6:3	Reserved	0		
2:0	FD_NR_ SAMPLES[10:8]	0	R/W	Please see FD_NR_SAMPLES0.

Note(s):

1. Return to the Register Map (0x8C).

FD_NR_SAMPLES_ALTERNATIVE0 Register

Figure 37:
FD_NR_SAMPLES_ALTERNATIVE0

Addr: 0x8D		FD_NR_SAMPLES_ALTERNATIVE0		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	FD_NR_SAMPLES_ ALTERNATIVE [7:0]	0	R/W	FD_NR_OF_SAMPLES_ALTERNATIVE defines the total measurement time for Flicker together with SAMPLE_ TIME in steps of 1.388889µs modulator clock. Please observe that FD_NR_OF_SAMPLES_ALTERNATIVE needs to be set in register 0x8D and 0x8E (11-bit wide). It counts from 0-2047 (2048 counts). FDMeasurementTime = (FD_NR_SAMPLES_ ALTERNATIVE+1) x (SAMPLE_TIME+1) x 1.388889µs Default: 250µs = (0+1) x (179+1) x 1.388889µs Example: 100ms = (399+1) x (179+1) x 1.388889µs In case residual measurement is enabled, SAMPLE_TIME is reduced which also reduces FDMeasurementTime.

Note(s):

1. Return to the Register Map (0x8D).

FD_NR_SAMPLES_ALTERNATIVE1 Register

Figure 38:
FD_NR_SAMPLES_ALTERNATIVE1

Addr: 0x8E		FD_NR_SAMPLES_ALTERNATIVE1		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:3	Reserved	0		
2:0	FD_NR_SAMPLES_ ALTERNATIVE[10:8]	0	R/W	Please see FD_NR_SAMPLES_ALTERNATIVE0.

Note(s):

1. Return to the Register Map (0x8E)

WTIME Register

Figure 39:
WTIME

Addr: 0x8F		WTIME		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	WTIME	0	R/W	Sets the WaitTime between 2 measurements of the modulator or sequencer. WTIME together with TRIGGER_MODE_TIMING (in register 0xAD, TRIGGER_MODE) define the actual time between measurements. WaitTime = TRIGGER_MODE_TIMING x WTIME Default: 0 = 0 x (0+1) no WaitTime.

Note(s):

1. Return to the Register Map (0x8F)

Identification Registers

Figure 40:
Identification Registers

Bits	Addr	Field	Reset	Type	Description
7:0	0x90	AUX_ID	0x00	R	**AUX_ID**: Identifies package and wafer factory
7:0	0x91	REV_ID	0x14	R	**REV_ID:** Identifies revision number of CMOS die
7:0	0x92	ID	0x68	R	**ID**: Device Identification

Note(s):

1. Return to the Register Map (0x90, 0x91, 0x92).

ALS Interrupt Low Threshold Register

Figure 41:
ALS Interrupt Low Threshold

Bits	Addr	Field	Reset	Type	Description
7:0	0x93	AILT0	0	R/W	**ALS Interrupt Low Threshold:** The ALS interrupt threshold registers are 24-bit wide. ALS interrupt level detection compares the threshold registers with the data accumulated by the selected modulator. The modulator can be selected via ALS_THRESHOLD_CHANNEL. If AIEN is asserted and the accumulated data is below AILT for the number of consecutive samples specified in APERS, an interrupt is asserted on the interrupt pin (internally AINT_AILT and AINT are asserted).
15:8	0x94	AILT1	0	R/W	
23:16	0x95	AILT2	0	R/W	

Note(s):

1. Return to the Register Map (0x93, 0x94, 0x95).

ALS Interrupt High Threshold Register

Figure 42:
ALS Interrupt High Threshold

Bits	Addr	Field	Reset	Type	Description
7:0	0x96	AIHT0	0	R/W	**ALS Interrupt High Threshold**: The ALS interrupt threshold registers are 24-bit wide. ALS interrupt level detection compares the threshold registers with the data accumulated by the selected modulator. The modulator can be selected via ALS_THRESHOLD_CHANNEL. If AIEN is asserted and the accumulated data is above AIHT for the number of consecutive samples specified in APERS, an interrupt is asserted on the interrupt pin (internally AINT_AIHT and AINT are asserted).
15:8	0x97	AIHT1	0	R/W	
23:16	0x98	AIHT2	0	R/W	

Note(s):

1. Return to the Register Map (0x96, 0x97, 0x98).

AGC Number of Samples Register

Figure 43:
AGC Number of Samples

Bits	Addr	Field	Reset	Type	Description
7:0	0x99	AGC_NR_ SAMPLES[7:0]	0	R/W	**AGC Number of Samples**: Sets the number of samples for every AGC measurement.
7:3	0x9A	Reserved	0		
2:0	0x9A	AGC_NR_ SAMPLES[10:8]	0	R/W	

Note(s):

1. Return to the Register Map (0x99, 0x9A).

STATUS Register

Figure 44:
STATUS

Addr: 0x9B		STATUS		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	MINT	0	R/W	**Modulator Interrupt:** Indicates that a modulator interrupt has occurred because of saturation. Check the STATUS2 register to differentiate between analog or digital saturation. Writing 1 to this bit clear MINT and all subsequent interrupts.
6:4	Reserved	0		
3	AINT	0	R/W	**ALS Interrupt:** If AIEN is set, this interrupt indicates that an ALS event that met the programmed ALS thresholds (AILT or AIHT) and persistence (APERS) occurred. Check the STATUS3 register to differentiate. Writing 1 to this bit clear AINT and all subsequent interrupts.
2	FINT	0	R/W	**FIFO Interrupt.** Indicates that the data level in the FIFO met the programmed FIFO thresholds (FIFO_LVL and FIFO_THR). This interrupt is automatically asserted/removed depending on the programmed FIFO thresholds. Writing 1 to this bit clears FINT. The interrupt, however, will be promptly asserted again in case the FIFO has not been read out or cleared.

Addr: 0x9B		STATUS		
Bit	Field	Reset	Type	Bit Description
1	Reserved	0		
0	SINT	0	0	**System Interrupt.** If SIEN is set, indicates that one or more of several events has occurred or is complete. The events related to this interrupt are indicated in the STATUS5 register.

Note(s):

1. Return to the Register Map (0x9B).

STATUS2 Register

Figure 45:
STATUS2

Addr: 0x9C		STATUS2		
Bit	Field	Reset	Type	Bit Description
7:5	Reserved	0	R	
4	ALS_DIGITAL_ SATURATION	0	R	**ALS Digital Saturation**. Indicates that a counter value has been reached that cannot be expressed with the selected data format defined with ALS_MSB_POSITION. Maximum counter value also depends on integration time set in the ATIME register.
3	FD_DIGITAL_ SATURATION	0	R	**Flicker Detect Digital Saturation.** Indicates that the maximum counter value has been reached during flicker detection.
2:1	Reserved	0	R	
0	MOD_ANALOG_ SATURATION_ANY	0	R	**ALS Analog Saturation of any Modulator.** Indicates that the intensity of ambient light has exceeded the maximum integration level for the ALS analog circuit.

Note(s):

1. Return to the Register Map (0x9C).

STATUS3 Register

Figure 46:
STATUS3

Addr: 0x9D		STATUS3		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:6	Reserved	0		
5	AINT_AIHT	0	R/W	**ALS Interrupt High.** Indicates that an ALS interrupt occurred because the ALS data exceeded the high threshold. Writing "1" to this bit clears this interrupt.
4	AINT_AILT	0	R/W	**ALS Interrupt Low.** Indicates that an ALS interrupt occurred because the ALS data is below the low threshold. Writing "1" to this bit clears this interrupt.
3	VSYNC_LOST	1	R	Indicates that synchronization is out of sync with clock provided at vsync pin. Default value is "1" since device always starts unsynchronized. The detected vsync clock is not within the expected range. Please see VSYNC_PERIOD_TARGET for more details.
2	Reserved	0		
1	OSC_CALIB_ SATURATION	0	R	Indicates that oscillator calibration with the current values of TRIM_OSC and OSC_TUNE is out of range abs(TRIM_ OSC+OSC_TUNE) > 32 .
0	OSC_CALIB_ FINISHED	0	R	Indicates that oscillator calibration is finished.

Note(s):

1. Return to the Register Map (0x9D).

STATUS4 Register

Figure 47:
STATUS4

Addr: 0x9E		STATUS4		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	Reserved	0		
3	MOD_SAMPLE_ TRIGGER_ERROR	0	R	**Indicates that Measured Data is Corrupted.** For a valid measurement, this bit must not be asserted. This error condition does not trigger an interrupt, however AEN and FDEN will be cleared and SINT_MEASURMENT_ SEQUENCER will be set. Writing "1" clears this bit.
2	MOD_TRIGGER_ ERROR	0	R	Indicates that WTIME is too short for the programmed configuration (SAMPLE_TIME, ALS_NR_SAMPLES, FD_NR_ SMAPLES). This error condition does not trigger an interrupt. Writing "1" clears this bit.
1	SAI_ACTIVE	0	R	**Sleep After Interrupt Active**. Indicates that the device is in sleep due to an interrupt. To exit sleep mode, clear this bit by writing "1" to CLEAR_SAI_ACTIVE.
0	INIT_BUSY	0	R	**Initialization Busy.** Indicates that the device is initializing. This bit will remain 1 for about 300µs after power on. Do not interact with the device until initialization is complete (e.g. via I^2C/I3C).

Note(s):

1. Return to the Register Map (0x9E).

STATUS5 Register

Figure 48:
STATUS5

Addr: 0x9F		STATUS5		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:3	Reserved	0		
2	SINT_AUX	0	R/W	**Auxiliary System Interrupt Enable.** Setting this bit will allow a system interrupt SINT as soon as an auxiliary interrupt occurs.
1	SINT_ MEASUREMENT_ SEQUENCER	0	R/W	**Measurement Sequencer Interrupt Enable.** Setting this bit will allow a system interrupt SINT as soon as invoked by a measurement sequencer event.
0	SINT_VSYNC	0	R/W	**Vsync Interrupt Enable.** Setting this bit will allow a system interrupt SINT as soon as soon as a vysnc interrupt occurs.

Note(s):

1. Return to the Register Map (0x9F).

STATUS6 Register

Figure 49:
STATUS6

Addr: 0xA0		STATUS6		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	MOD_ANALOG_SATURATION7	0	R	**ALS Analog Saturation of Modulator7.** Indicates that the intensity of ambient light has exceeded the maximum integration level for the ALS analog circuit.
6	MOD_ANALOG_SATURATION6	0	R	**ALS Analog Saturation of Modulator6.** Indicates that the intensity of ambient light has exceeded the maximum integration level for the ALS analog circuit.
5	MOD_ANALOG_SATURATION5	0	R	**ALS Analog Saturation of Modulator5.** Indicates that the intensity of ambient light has exceeded the maximum integration level for the ALS analog circuit.
4	MOD_ANALOG_SATURATION4	0	R	**ALS Analog Saturation of Modulator4.** Indicates that the intensity of ambient light has exceeded the maximum integration level for the ALS analog circuit.
3	MOD_ANALOG_SATURATION3	0	R	**ALS Analog Saturation of Modulator3.** Indicates that the intensity of ambient light has exceeded the maximum integration level for the ALS analog circuit.
2	MOD_ANALOG_SATURATION2	0	R	**ALS Analog Saturation of Modulator2.** Indicates that the intensity of ambient light has exceeded the maximum integration level for the ALS analog circuit.
1	MOD_ANALOG_SATURATION1	0	R	**ALS Analog Saturation of Modulator1.** Indicates that the intensity of ambient light has exceeded the maximum integration level for the ALS analog circuit.
0	MOD_ANALOG_SATURATION0	0	R	**ALS Analog Saturation of Modulator0.** Indicates that the intensity of ambient light has exceeded the maximum integration level for the ALS analog circuit.

Note(s):

1. Return to the Register Map (0xA0).

CFG0 Register

Figure 50:
CFG0

Addr: 0xA1		CFG0		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	Reserved	0		
6	SAI	0	R/W	**Sleep After Interrupt.** If asserted, the oscillator is turned off whenever interrupt is active (low). SAI_ ACTIVE is set in this event. To activate the oscillator again, service and clear all interrupts plus clear the SAI_ACTIVE bit by writing "1" to CLEAR_SAI_ACTIVE. Sleep after interrupt is asserted only in combination with MEASUREMENT_ SEQUENCER_SINT_PER_STEP or SIEN or SIEN_ MEASUREMENT_SEQUENCER.
5:0	Reserved	0		Do not overwrite default.

Note(s):

1. Return to the Register Map (0xA1).

CFG1 Register

Figure 51:
CFG1

Addr: 0xA2		CFG1		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:3	Reserved	0		
2	DO_ALS_FINAL_ PROCESSING	0	R/W	If this bit is set to "1" and flicker measurement takes longer than ALS measurement, ALS measurement writings are postponed until flicker measurement is finished. Otherwise ALS data is not written to FIFO.
1:0	Reserved	0		Do not overwrite default.

Note(s):

1. Return to the Register Map (0xA2).

CFG2 Register

Figure 52:
CFG2

Addr: 0xA3		CFG2		
Bit	Field	Reset	Type	Bit Description
7:3	Reserved	0		
2:0	FIFO_THR[2:0]	1	R/W	**FIFO Threshold LSB.** Please see FIFO_THR for information.

Note(s):

1. Return to the Register Map (0xA3).

CFG3 Register

Figure 53:
CFG3

Addr: 0xA4		CFG3		
Bit	Field	Reset	Type	Bit Description
7:6	Reserved	0		
5:4	INT_PINMAP	0	R/W	**Interrupt Pin Mapping.** Defines internal signal which is routed to the external INT pin. 00b: Default, INTERRUPT 01b: Reserved, do not use 10b: Reserved, do not use 11b: Reserved, do not use
3:2	Reserved	0		
1:0	VSYNC_GPIO_ PINMAP	0	R/W	**Vsync/GPIO Pin Mapping.** Defines internal signal which is routed to the external VSYNC/GPIO pin. 00b: Default, VSYNC_GPIO_OUT 01b: Reserved, do not use 10b: Reserved, do not use 11b: Reserved, do not use

Note(s):

1. Return to the Register Map (0xA4).

CFG4 Register

Figure 54:
CFG4

Addr: 0xA5		CFG4		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	Reserved	0		
6	MOD_ CALIBRATION_ NTH_ITERATION_ STEP_ENABLE	0	R/W	Enable a modulator calibration with n^{th} iterations per sequencer step instead of waiting for a full round for all sequencers to be finished. In case of AGC enabled (MOD_ CALIB_NTH_ITERATION_AGC_ENABLE) this bit must be set "0", otherwise AGC will not properly work.
5	MEASUREMENT_ SEQUENCER_AGC_ PREDICT_TARGET_ LEVEL	0	R/W	Sets the target measurement levels for AGC prediction. 0b: 50% of max value 1b: 25% of max value
4	MEASURMENT_ SEQUENCER_ SINT_PER_STEP	0	R/W	Invokes the system interrupt SINT_MEASUREMENT_ SEQUENCER per sequencer step instead of after a full sequencer round.
3	OSC_TUNE_NO_ RESET	0	R	If set to 0, OSC_TUNE gets reset to 0 if PON is set to 1. If set to 1, OSC_TUNE keeps its value if PON is set to 1.
2	Reserved	0		
1:0	MOD_ALS_FIFO_ DATA_FORMAT	0	R/W	Sets the format for ALS data written to FIFO. Please observe readout pattern if digital or analog saturation has occurred. 00b: 16-bit (FFFF analog sat, FFFE digital sat) 01b: 24-bit (FFFFFF analog sat, FFFFFE digital sat) 10b: Reserved 11b: 32-bit (FFFFFFFF analog sat)

Note(s):

1. Return to the Register Map (0xA5).

CFG5 Register

Figure 55:
CFG5

Addr: 0xA6		CFG5		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	Reserved	0		
6:4	ALS_THRESHOLD_ CHANNEL	0	R/W	Selects the modulator channel used for the ALS threshold metering and subsequent interrupt. 000b default, Modulator 0 001b: Modulator 1 010b: Modulator 2 011b: Modulator 3 …. 111b: Modulator7
3:0	APERS	0	R/W	**ALS Interrupt Persistence.** Defines a filter for the number of consecutive occurrences that ALS measurement data must remain outside the threshold range between AILT and AIHT before an interrupt is generated. The ALS data channel used for the persistence filter is set by ALS_THRESHOLD_CHANNEL. Any sample that is inside the threshold range resets the counter to 0. Interrupts are generated at 0x0: Every ALS cycle 0x1: Any ALS value outside the threshold range 0x2: 2 consecutive ALS values outside the range 0x3: 3 consecutive ALS values outside the range 0x4: 5 … 0x5: 10 … …… continued in increments of 5 values 0xE: 55 … 0xF: 60 consecutive ALS values outside the range

Note(s):

1. Return to the Register Map (0xA6).

CFG6 Register

Figure 56:
CFG6

Addr: 0xA7		CFG6		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:6	Reserved	0		
5	MOD_ MEASUREMENT_ COMPLETE_ STARTUP	0	R/W	Activated complete start procedure in for each measurement sample. This reduces measurement time per sample by 9 modulator clock cycles.
4	Reserved	0		
3:2	MOD_MINIMUM_ RESIDUAL_BITS	0	R/W	Limits the number of residual bits to a minimum within this value. ATTENTION: When this function is used, the default settings for the gains are not correct anymore. Thus a residual calibration is mandatory (use MOD_CALIB_ RESIDUAL_ENABLE_AUTO_CALIB_ON_GAIN_ CHANGE or MOD_CALIB_NTH_ITERATION_RC_ ENABLE to enforce residual calibration) 00b: 0 residual bits at minimum (default, turned off) 01b: 1 residual bits at minimum 10b: 2 residual bits at minimum 11b: 3 residual bits at minimum
1:0	MOD_MAXIMUM_ RESIDUAL_BITS	10b	R/W	Limits the number of residual bits to a maximum within this value. ATTENTION: When this function is used, the default settings for the gains are not correct anymore. Thus a residual calibration is mandatory (use MOD_CALIB_ RESIDUAL_ENABLE_AUTO_CALIB_ON_GAIN_ CHANGE or MOD_CALIB_NTH_ITERATION_RC_ ENABLE to enforce residual calibration). 00b: 1 residual bits at maximum 01b: 2 residual bits at maximum 10b: 3 residual bits at maximum (default) 11b: 4 residual bits at maximum

Note(s):

1. Return to the Register Map (0xA7).

CFG7 Register

Figure 57:
CFG7

Addr: 0xA8		CFG7		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	ALS_CB_ENABLE	0x00	R/W	**Enable coherence buffering.** PON must be 0 when this bit is written, otherwise buffer data will be corrupted.
6:0	Reserved	0x01		

Note(s):

1. Return to the Register Map (0xA8).

CFG8 Register

Figure 58:
CFG8

Addr: 0xA9		CFG8		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	MEASUREMENT_ SEQUENCER_ MAX_MOD_GAIN	0xC	R/W	Sets the maximum gain for all channels in all sequencer steps.
3:0	MEASUREMENT_ SEQUENCER_AGC_ PREDICT_MOD_ GAIN_REDUCTION	0x4	R/W	Sets the modulator gain reduction in AGC predict mode. All channels in the actual measurement sequence are reduced by the programmed gain reduction before gain prediction starts.

Note(s):

1. Return to the Register Map (0xA9).

CFG9 Register

Figure 59:
CFG9

Addr: 0xAA		CFG9		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:2	Reserved	0		
1:0	MOD_RESIDUAL_ BITS_IGNORE	0	R/W	Sets the number of residual bits ignored and shifted in flicker data. Please observe to set MOD_FD_FIFO_DATAx_ WIDTH accordingly.

Note(s):

1. Return to the Register Map (0xAA).

MOD_CHANNEL_CTRL Register

Figure 60:
MOD_CHANNEL_CTRL

Addr: 0xAB		MOD_CHANNEL_CTRL		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	MOD7_DISABLE	0	R/W	When asserted modulator 7 is disabled
6	MOD6_DISABLE	0	R/W	When asserted modulator 6 is disabled
5	MOD5_DISABLE	0	R/W	When asserted modulator 5 is disabled
4	MOD4_DISABLE	0	R/W	When asserted modulator 4 is disabled
3	MOD3_DISABLE	0	R/W	When asserted modulator 3 is disabled
2	MOD2_DISABLE	0	R/W	When asserted modulator 2 is disabled
1	MOD1_DISABLE	0	R/W	When asserted modulator 1 is disabled
0	MOD0_DISABLE	0	R/W	When asserted modulator 0 is disabled

Note(s):

1. Return to the Register Map (0xAB).

TRIGGER_MODE Register

Figure 61:
TRIGGER_MODE

Addr: 0xAD		TRIGGER_MODE		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:3	Reserved	0		
2:0	MOD_TRIGGER_ TIMING	0	R/W	Sets the repetition rate of a modulator or sequencer measurement. Counting will immediately start or will wait for the first vsync pulse. 000: OFF 001: Normal = 2.844ms * WTIME 010: Long = 45.511ms * WTIME 011: Fast = 88.889µs * WTIME 100: Fastlong = 1.422ms * WTIME 101: vsync = One vsync per WTIME step 110: Reserved 111: Reserved

Note(s):

1. Return to the Register Map (0xAD).

OSC_TUNE Register

Figure 62:
OSC_TUNE

Addr: 0xAE		OSC_TUNE		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	Reserved	0		Do not overwrite default. It will artificially detune the oscillator.

Note(s):

1. Return to the Register Map (0xAE).

VSYNC_GPIO_INT Register

Figure 63:
VSYNC_GPIO_INT

Addr: 0xB0		VSYNC_GPIO_INT		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	Reserved	0		
6	INT_INVERT	0	R/W	If set to "1" the INT pin output is inverted. This applies to all output signals as selected in INT_PINMAP.
5	INT_IN_EN	0	R/W	If programmed to "1" the INT pin is set as input. Please observe that the connected net must not be floating since INT is an open drain input.
4	INT_IN	0	R	External HIGH or LO value applied to INT pin.
3	VSYNC_GPIO_ INVERT	0	R/W	If set to "1" the VSYNC/GPIO pin output is inverted. This applies to all output signals as selected in VSYNC_GPIO_ PINMAP.
2	VSYNC_GPIO_ IN_EN	0	R/W	If programmed to "1" the VSYNC/GPIO pin is set as in-put. Please observe that the connected net must not be floating since VSYNC/GPIO is an open drain input.
1	VSYNC_GPIO_OUT	1	R/W	Programs the VSYNC/GPIO pin HI or LOW. Since the pin is an open drain I/O pin, the default value is HIGH to avoid any unintended power consumption through pull-up resistor. The routed internal signal is selected in VSYNC_ GPIO_PINMAP.
0	VSYNC_GPIO_IN	0	R	External HIGH or LO value applied to VSYNC/GPIO pin.

Note(s):

1. Return to the Register Map (0xB0).

INTENAB Register

Figure 64:
INTENAB

Addr: 0xBA		INTENAB		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	MIEN	0	R/W	**Modulator Interrupt Enable.** Setting this bit will allow a modulator interrupt on the external INT pin. Please check in STATUS2 for the reason of the interrupt.
6:4	Reserved	0		
3	AIEN	0	R/W	**ALS Interrupt Enable.** Setting this bit will allow an ALS interrupt on the external INT pin. Please check in STATUS3 for the reason of the interrupt.
2	FIEN	0	R/W	**FIFO Interrupt Enable.** Setting this bit will allow a fifo interrupt on the external INT pin. Please observe that this interrupt indicates that data in the FIFO is available for readout. Check FINT for further information.
1	Reserved	0		
0	SIEN	0	R/W	**System Interrupt Enable.** Setting this bit will allow a system interrupt on the external INT pin. Please check in STATUS5 for the reason of the interrupt.

Note(s):

1. Return to the Register Map (0xBA).

SIEN Register

Figure 65:
SIEN

Addr: 0xBB		SIEN		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:3	Reserved	0		
2	SIEN_AUX	0	R/W	**Auxiliary System Interrupt Enable.** Setting this bit will allow a system interrupt SINT as soon as an auxiliary interrupt occurs. Please see SINT_AUX for further information.
1	SIEN_ MEASUREMENT_ SEQUENCER	0	R/W	**Measurement Sequencer Interrupt Enable.** Setting this bit will allow a system interrupt SINT as soon as invoked by a measurement sequencer event. Please see SINT_ MEASUREMENT_SEQUENCER for further information
0	SIEN_VSYNC	0	R/W	**Vsync Interrupt Enable.** Setting this bit will allow a system interrupt SINT as soon as soon as a vysnc interrupt occurs. Please see SINT_VSYNC for further information.

Note(s):

1. Return to the Register Map (0xBB).

CONTROL Register

Figure 66:
CONTROL

Addr: 0xBC		CONTROL		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:2	Reserved	0		
1	FIFO_CLR	0	R/W	Setting this bit will clear the FIFO, as well as FINT, FIFO_ FULL, FIFO_OVERFLOW, FIFO_UNDERFLOW and FIFO_LVL.
0	CLEAR_SAI_ ACTIVE	0	R/W	Setting this bit will clear the Sleep After Interrupt Active SAI_ACTIVE and start measurements if enabled.

Note(s):

1. Return to the Register Map (0xBC).

ALS_DATA_STATUS Register

Figure 67:
ALS_DATA_STATUS

Addr: 0xBD		ALS_DATA_STATUS		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	ALS_DATA_VALID	0	R	**ALS Data Valid.** Indicates that the ALS state has completed a cycle since either an assertion of AEN or the last readout of the ALS_DATA_FIRST register.
6:0	Reserved	0		

Note(s):

1. Return to the Register Map (0xBD).

ALS_DATA_FIRST Register

Figure 68:
ALS_DATA_FIRST

Addr: 0xBE		ALS_DATA_FIRST		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	ALS_DATA_FIRST	0	R	**ALS Data First.** ALS_CB_ENABLE needs to be set in order to read and update to the latest ALS data. A part of the FIFO is used for this function. In such case the FIFO size will be reduced from 1280 to 896 bytes.
6:0	Reserved	0		

Note(s):

1. Return to the Register Map (0xBE).

ALS_DATA Register

Figure 69:
ALS_DATA

Addr: 0xBF		ALS_DATA		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	ALS_DATA	0	R	**Continue Reading ALS data.** ALS_CB_ENABLE needs to be set in order to read and update to the latest ALS data. A part of the FIFO is used for this function. In such case the FIFO size will be reduced from 1280 to 896 bytes. ATTENTION: Automatic address wrap from to this address. In this case the wrap is done from ALS_DATA_H to ALS_DATA_H.

Note(s):

1. Return to the Register Map (0xBF).

MEAS_SEQR_STEP0_MOD_GAINX_0 Register

Figure 70:
MEAS_SEQR_STEP0_MOD_GAINX_0

Addr: 0xC0		MEAS_SEQR_STEP0_MOD_GAINX_0		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	MEASUREMENT_ SEQUENCER_ STEP0_ MOD_GAIN1	1000b	R/W	Defines the gain of modulator 1 for the measurement sequencer step 0.
3:0	MEASUREMENT_ SEQUENCER_ STEP0_ MOD_GAIN0	1000b	R/W	Defines the gain of modulator 0 for the measurement sequencer step 0.

Note(s):

1. Return to the Register Map (0xC0).

MEAS_SEQR_STEP0_MOD_GAINX_1 Register

Figure 71:
MEAS_SEQR_STEP0_MOD_GAINX_1

Addr: 0xC1		MEAS_SEQR_STEP0_MOD_GAINX_1		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	MEASUREMENT_ SEQUENCER_ STEP0_ MOD_GAIN3	1000b	R/W	Defines the gain of modulator 3 for the measurement sequencer step 0.
3:0	MEASUREMENT_ SEQUENCER_ STEP0_ MOD_GAIN2	1000b	R/W	Defines the gain of modulator 2 for the measurement sequencer step 0.

Note(s):

1. Return to the Register Map (0xC1).

MEAS_SEQR_STEP0_MOD_GAINX_2 Register

Figure 72:
MEAS_SEQR_STEP0_MOD_GAINX_2

Addr: 0xC2		MEAS_SEQR_STEP0_MOD_GAINX_2		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	MEASUREMENT_ SEQUENCER_ STEP0_ MOD_GAIN5	1000b	R/W	Defines the gain of modulator 5 for the measurement sequencer step 0.
3:0	MEASUREMENT_ SEQUENCER_ STEP0_ MOD_GAIN4	1000b	R/W	Defines the gain of modulator 4 for the measurement sequencer step 0.

Note(s):

1. Return to the Register Map (0xC2).

MEAS_SEQR_STEP0_MOD_GAINX_3 Register

Figure 73:
MEAS_SEQR_STEP0_MOD_GAINX_3

Addr: 0xC3		MEAS_SEQR_STEP0_MOD_GAINX_3		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	MEASUREMENT_ SEQUENCER_ STEP0_ MOD_GAIN7	1000b	R/W	Defines the gain of modulator 7 for the measurement sequencer step 0.
3:0	MEASUREMENT_ SEQUENCER_ STEP0_ MOD_GAIN6	1000b	R/W	Defines the gain of modulator 6 for the measurement sequencer step 0.

Note(s):

1. Return to the Register Map (0xC3).

MEAS_SEQR_STEP1_MOD_GAINX_0 Register

Figure 74:
MEAS_SEQR_STEP1_MOD_GAINX_0

Addr: 0xC4		MEAS_SEQR_STEP1_MOD_GAINX_0		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	MEASUREMENT_ SEQUENCER_ STEP1_ MOD_GAIN1	1000b	R/W	Defines the gain of modulator 1 for the measurement sequencer step 1.
3:0	MEASUREMENT_ SEQUENCER_ STEP1_ MOD_GAIN0	1000b	R/W	Defines the gain of modulator 0 for the measurement sequencer step 1.

Note(s):

1. Return to the Register Map (0xC4).

MEAS_SEQR_STEP1_MOD_GAINX_1 Register

Figure 75:
MEAS_SEQR_STEP1_MOD_GAINX_1

Addr: 0xC5		MEAS_SEQR_STEP1_MOD_GAINX_1		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	MEASUREMENT_ SEQUENCER_ STEP1_ MOD_GAIN3	1000b	R/W	Defines the gain of modulator 3 for the measurement sequencer step 1.
3:0	MEASUREMENT_ SEQUENCER_ STEP1_ MOD_GAIN2	1000b	R/W	Defines the gain of modulator 2 for the measurement sequencer step 1.

Note(s):

1. Return to the Register Map (0xC5).

MEAS_SEQR_STEP1_MOD_GAINX_2 Register

Figure 76:
MEAS_SEQR_STEP1_MOD_GAINX_2

Addr: 0xC6		MEAS_SEQR_STEP1_MOD_GAINX_2		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	MEASUREMENT_ SEQUENCER_ STEP1_ MOD_GAIN5	1000b	R/W	Defines the gain of modulator 5 for the measurement sequencer step 1.
3:0	MEASUREMENT_ SEQUENCER_ STEP1_ MOD_GAIN4	1000b	R/W	Defines the gain of modulator 4 for the measurement sequencer step 1.

Note(s):

1. Return to the Register Map (0xC6).

MEAS_SEQR_STEP1_MOD_GAINX_3 Register

Figure 77:
MEAS_SEQR_STEP1_MOD_GAINX_3

Addr: 0xC7		MEAS_SEQR_STEP1_MOD_GAINX_3		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	MEASUREMENT_ SEQUENCER_ STEP1_ MOD_GAIN7	1000b	R/W	Defines the gain of modulator 7 for the measurement sequencer step 1.
3:0	MEASUREMENT_ SEQUENCER_ STEP1_ MOD_GAIN6	1000b	R/W	Defines the gain of modulator 6 for the measurement sequencer step 1.

Note(s):

1. Return to the Register Map (0xC7).

MEAS_SEQR_STEP2_MOD_GAINX_0 Register

Figure 78:
MEAS_SEQR_STEP2_MOD_GAINX_0

Addr: 0xC8		MEAS_SEQR_STEP2_MOD_GAINX_0		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	MEASUREMENT_ SEQUENCER_ STEP2_ MOD_GAIN1	1000b	R/W	Defines the gain of modulator 1 for the measurement sequencer step 2.
3:0	MEASUREMENT_ SEQUENCER_ STEP2_ MOD_GAIN0	1000b	R/W	Defines the gain of modulator 0 for the measurement sequencer step 2.

Note(s):

1. Return to the Register Map (0xC8).

MEAS_SEQR_STEP2_MOD_GAINX_1 Register

Figure 79:
MEAS_SEQR_STEP2_MOD_GAINX_1

Addr: 0xC9		MEAS_SEQR_STEP2_MOD_GAINX_1		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	MEASUREMENT_ SEQUENCER_ STEP2_ MOD_GAIN3	1000b	R/W	Defines the gain of modulator 3 for the measurement sequencer step 2.
3:0	MEASUREMENT_ SEQUENCER_ STEP2_ MOD_GAIN2	1000b	R/W	Defines the gain of modulator 2 for the measurement sequencer step 2.

Note(s):

1. Return to the Register Map (0xC9).

MEAS_SEQR_STEP2_MOD_GAINX_2 Register

Figure 80:
MEAS_SEQR_STEP2_MOD_GAINX_2

Addr: 0xCA		MEAS_SEQR_STEP2_MOD_GAINX_2		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	MEASUREMENT_ SEQUENCER_ STEP2_ MOD_GAIN5	1000b	R/W	Defines the gain of modulator 5 for the measurement sequencer step 2.
3:0	MEASUREMENT_ SEQUENCER_ STEP2_ MOD_GAIN4	1000b	R/W	Defines the gain of modulator 4 for the measurement sequencer step 2.

Note(s):

1. Return to the Register Map (0xCA).

MEAS_SEQR_STEP2_MOD_GAINX_3 Register

Figure 81:
MEAS_SEQR_STEP2_MOD_GAINX_3

Addr: 0xCB		MEAS_SEQR_STEP2_MOD_GAINX_3		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	MEASUREMENT_ SEQUENCER_ STEP2_ MOD_GAIN7	1000b	R/W	Defines the gain of modulator 7 for the measurement sequencer step 2.
3:0	MEASUREMENT_ SEQUENCER_ STEP2_ MOD_GAIN6	1000b	R/W	Defines the gain of modulator 6 for the measurement sequencer step 2.

Note(s):

1. Return to the Register Map (0xCB).

MEAS_SEQR_STEP3_MOD_GAINX_0 Register

Figure 82:
MEAS_SEQR_STEP3_MOD_GAINX_0

Addr: 0xCC		MEAS_SEQR_STEP3_MOD_GAINX_0		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	MEASUREMENT_ SEQUENCER_ STEP3_ MOD_GAIN1	1000b	R/W	Defines the gain of modulator 1 for the measurement sequencer step 3.
3:0	MEASUREMENT_ SEQUENCER_ STEP3_ MOD_GAIN0	1000b	R/W	Defines the gain of modulator 0 for the measurement sequencer step 3.

Note(s):

1. Return to the Register Map (0xCC).

MEAS_SEQR_STEP3_MOD_GAINX_1 Register

Figure 83:
MEAS_SEQR_STEP3_MOD_GAINX_1

Addr: 0xCD		MEAS_SEQR_STEP3_MOD_GAINX_1		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	MEASUREMENT_ SEQUENCER_ STEP3_ MOD_GAIN3	1000b	R/W	Defines the gain of modulator 3 for the measurement sequencer step 3.
3:0	MEASUREMENT_ SEQUENCER_ STEP3_ MOD_GAIN2	1000b	R/W	Defines the gain of modulator 2 for the measurement sequencer step 3.

Note(s):

1. Return to the Register Map (0xCD).

MEAS_SEQR_STEP3_MOD_GAINX_2 Register

Figure 84:
MEAS_SEQR_STEP3_MOD_GAINX_2

Addr: 0xCE		MEAS_SEQR_STEP3_MOD_GAINX_2		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	MEASUREMENT_ SEQUENCER_ STEP3_ MOD_GAIN5	1000b	R/W	Defines the gain of modulator 5 for the measurement sequencer step 3.
3:0	MEASUREMENT_ SEQUENCER_ STEP3_ MOD_GAIN4	1000b	R/W	Defines the gain of modulator 4 for the measurement sequencer step 3.

Note(s):

1. Return to the Register Map (0xCE).

MEAS_SEQR_STEP3_MOD_GAINX_3 Register

Figure 85:
MEAS_SEQR_STEP3_MOD_GAINX_3

Addr: 0xCF		MEAS_SEQR_STEP3_MOD_GAINX_3		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	MEASUREMENT_ SEQUENCER_ STEP3_ MOD_GAIN7	1000b	R/W	Defines the gain of modulator 7 for the measurement sequencer step 3.
3:0	MEASUREMENT_ SEQUENCER_ STEP3_ MOD_GAIN6	1000b	R/W	Defines the gain of modulator 6 for the measurement sequencer step 3.

Note(s):

1. Return to the Register Map (0xCF).

MEAS_SEQR_STEP0_FD Register

Figure 86:
MEAS_SEQR_STEP0_FD

Addr: 0xD0		MEAS_SEQR_STEP0_FD		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	MEASUREMENT_ SEQUENCER_ STEP0_ MOD_FD_ PATTERN	0x01	R/W	This register contains one bit for each modulator channel (LSB = modulator 0, MSB = modulator 7) which defines if a flicker measurement shall be executed with the respective modulator during measurement sequencer step 0.

Note(s):

1. Return to the Register Map (0xD0).

MEAS_SEQR_STEP1_FD Register

Figure 87:
MEAS_SEQR_STEP1_FD

Addr: 0xD1		MEAS_SEQR_STEP1_FD		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	MEASUREMENT_ SEQUENCER_ STEP1_ MOD_FD_ PATTERN	0	R/W	This register contains one bit for each modulator channel (LSB = modulator 0, MSB = modulator 7) which defines if a flicker measurement shall be executed with the respective modulator during measurement sequencer step 1.

Note(s):

1. Return to the Register Map (0xD1).

MEAS_SEQR_STEP2_FD Register

Figure 88:
MEAS_SEQR_STEP2_FD

Addr: 0xD2		MEAS_SEQR_STEP2_FD		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	MEASUREMENT_ SEQUENCER_ STEP2_ MOD_FD_ PATTERN	0	R/W	This register contains one bit for each modulator channel (LSB = modulator 0, MSB = modulator 7) which defines if a flicker measurement shall be executed with the respective modulator during measurement sequencer step 2.

Note(s):

1. Return to the Register Map (0xD2).

MEAS_SEQR_STEP3_FD Register

Figure 89:
MEAS_SEQR_STEP3_FD

Addr: 0xD3		MEAS_SEQR_STEP3_FD		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	MEASUREMENT_ SEQUENCER_ STEP3_ MOD_FD_ PATTERN	0	R/W	This register contains one bit for each modulator channel (LSB = modulator 0, MSB = modulator 7) which defines if a flicker measurement shall be executed with the respective modulator during measurement sequencer step 3.

Note(s):

1. Return to the Register Map (0xD3).

MEAS_SEQR_STEP0_RESIDUAL Register

Figure 90:
MEAS_SEQR_STEP0_RESIDUAL

Addr: 0xD4		MEAS_SEQR_STEP0_RESIDUAL		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	MEASUREMENT_ SEQUENCER_ STEP0_ MOD_RESIDUAL_ ENABLE_PATTERN	0xFF	R/W	This register contains one bit for each modulator channel (LSB = modulator 0, MSB = modulator 7) which defines if a residual measurement shall be executed with the respective modulator during measurement sequencer step 0.

Note(s):

1. Return to the Register Map (0xD4).

MEAS_SEQR_STEP1_RESIDUAL Register

Figure 91:
MEAS_SEQR_STEP1_RESIDUAL

Addr: 0xD5		MEAS_SEQR_STEP1_RESIDUAL		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	MEASUREMENT_ SEQUENCER_ STEP1_ MOD_RESIDUAL_ ENABLE_PATTERN	0xFF	R/W	This register contains one bit for each modulator channel (LSB = modulator 0, MSB = modulator 7) which defines if a residual measurement shall be executed with the respective modulator during measurement sequencer step 1.

Note(s):

1. Return to the Register Map (0xD5).

MEAS_SEQR_STEP2_RESIDUAL Register

Figure 92:
MEAS_SEQR_STEP2_RESIDUAL

Addr: 0xD6		MEAS_SEQR_STEP2_RESIDUAL		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	MEASUREMENT_ SEQUENCER_ STEP2_ MOD_RESIDUAL_ ENABLE_PATTERN	0xFF	R/W	This register contains one bit for each modulator channel (LSB = modulator 0, MSB = modulator 7) which defines if a residual measurement shall be executed with the respective modulator during measurement sequencer step 2.

Note(s):

1. Return to the Register Map (0xD6).

MEAS_SEQR_STEP3_RESIDUAL Register

Figure 93:
MEAS_SEQR_STEP3_RESIDUAL

Addr: 0xD7		MEAS_SEQR_STEP3_RESIDUAL		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	MEASUREMENT_ SEQUENCER_ STEP3_ MOD_RESIDUAL_ ENABLE_PATTERN	0xFF	R/W	This register contains one bit for each modulator channel (LSB = modulator 0, MSB = modulator 7) which defines if a residual measurement shall be executed with the respective modulator during measurement sequencer step 3.

Note(s):

1. Return to the Register Map (0xD7).

MEAS_SEQR_STEP0_ALS Register

Figure 94:
MEAS_SEQR_STEP0_ALS

Addr: 0xD8		MEAS_SEQR_STEP0_ALS		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	MEASUREMENT_ SEQUENCER_ STEP0_ MOD_ALS_ PATTERN	0xFF	R/W	This register contains one bit for each modulator channel (LSB = modulator 0, MSB = modulator 7) which defines if an ALS measurement shall be executed with the respective modulator during measurement sequencer step 0.

Note(s):

1. Return to the Register Map (0xD8).

MEAS_SEQR_STEP1_ALS Register

Figure 95:
MEAS_SEQR_STEP1_ALS

Addr: 0xD9		MEAS_SEQR_STEP1_ALS		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	MEASUREMENT_ SEQUENCER_ STEP1_ MOD_ALS_ PATTERN	0	R/W	This register contains one bit for each modulator channel (LSB = modulator 0, MSB = modulator 7) which defines if an ALS measurement shall be executed with the respective modulator during measurement sequencer step 1.

Note(s):

1. Return to the Register Map (0xD9).

MEAS_SEQR_STEP2_ALS Register

Figure 96:
MEAS_SEQR_STEP2_ALS

Addr: 0xDA		MEAS_SEQR_STEP2_ALS		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	MEASUREMENT_ SEQUENCER_ STEP2_MOD_ALS_ PATTERN	0	R/W	This register contains one bit for each modulator channel (LSB = modulator 0, MSB = modulator 7) which defines if an ALS measurement shall be executed with the respective modulator during measurement sequencer step 2.

Note(s):

1. Return to the Register Map (0xDA).

MEAS_SEQR_STEP3_ALS Register

Figure 97:
MEAS_SEQR_STEP3_ALS

Addr: 0xDB		MEAS_SEQR_STEP3_ALS		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	MEASUREMENT_ SEQUENCER_ STEP3_MOD_ALS_ PATTERN	0	R/W	This register contains one bit for each modulator channel (LSB = modulator 0, MSB = modulator 7) which defines if an ALS measurement shall be executed with the respective modulator during measurement sequencer step 3.

Note(s):

1. Return to the Register Map (0xDB).

MEAS_SEQR_APERS_AND_VSYNC_WAIT Register

Figure 98:
MEAS_SEQR_APERS_AND_VSYNC_WAIT

Addr: 0xDC		MEAS_SEQR_APERS_AND_VSYNC_WAIT		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	MEASUREMENT_ SEQUENCER_ VSYNC_WAIT_ PATTERN	0000b	R/W	Defines if a measurement sequence shall wait for a vsync before starting the measurement. The bit pattern does not represent a value but controls bitwise which sequencer step shall be used. The leftmost position of "0000" refers to sequencer step 3, the rightmost refers to sequencer step 0.
3:0	MEASUREMENT_ SEQUENCER_ APERS_ PATTERN	0001b	R/W	Defines the sequencer steps where an ALS persistence evaluation shall be performed on modulator data selected by ALS_THRESHOLD_CHANNEL. The bit pattern does not represent a value but controls bitwise which sequencer step shall be used. The leftmost position of "0000" refers to sequencer step 3, the rightmost refers to sequencer step 0. By default step 0 is used on all modulators.

Note(s):

1. Return to the Register Map (0xDC).

MEAS_SEQR_AGC Register

Figure 99:
MEAS_SEQR_AGC

Addr: 0xDD		MEAS_SEQR_AGC		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	MEASUREMENT_ SEQUENCER_AGC_ PREDICT_PATTERN	1111b	R/W	Defines the sequencer steps where predict AGC is enabled for the corresponding measurement. The bit pattern does not represent a value but controls bitwise which sequencer step shall be used. The leftmost position of "0000" refers to sequencer step 3, the rightmost refers to sequencer step 0. By default this feature is enabled for all sequencer steps.
3:0	MEASUREMENT_ SEQUENCER_AGC_ ASAT_PATTERN	1111b	R/W	Defines the sequencer steps where analog saturation AGC is enabled for the corresponding measurement. The bit pattern does not represent a value but controls bitwise which sequencer step shall be used. The leftmost position of "0000" refers to sequencer step 3, the rightmost refers to sequencer step 0. By default this feature is enabled for all sequencer steps.

Note(s):

1. Return to the Register Map (0xDD).

MEAS_SEQR_SMUX_AND_SAMPLE_TIME Register

Figure 100:
MEAS_SEQR_SMUX_AND_SAMPLE_TIME

Addr: 0xDE		MEAS_SEQR_SMUX_AND_SAMPLE_TIME		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	MEASUREMENT_ SEQUENCER_ SAMPLE_ TIME_ PATTERN	0	R/W	This register contains one bit for each sequencer step (LSB = step 0, MSB = step 3) which selects the smux configuration from the two available variants for the corresponding sequencer step.
3:0	MEASUREMENT_ SEQUENCER_ SMUX_ PATTERN	0	R/W	This register contains one bit for each sequencer step (LSB = step 0, MSB = step 3) which selects the sample time configuration from the two available variants for the corresponding sequencer step.

Note(s):

1. Return to the Register Map (0xDE).

MEAS_SEQR_WAIT_AND_TS_ENABLE Register

Figure 101:
MEAS_SEQR_WAIT_AND_TS_ENABLE

Addr: 0xDF		MEAS_SEQR_WAIT_AND_TS_ENABLE		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:4	Reserved	0		
3:0	MEASUREMENT_ SEQUENCER_ WAIT_ PATTERN	0001b	R/W	Defines if a sequencer step will wait for the modulator trigger timer to finish as programmed in MOD_TRIGGER_ TIMING and WTIME. At the same time the timer is restarted. In case this bit is not set, the next sequencer step will start as soon as all measurements in the prior step are completed. Please observe that MOD_TRIGGER_TIMIMG is "0" by default. In this case the programmed wait pattern is ignored since measurement time has always priority over wait time. The bit pattern does not represent a value but controls bitwise which sequencer step shall be used. The leftmost position of "0000" refers to sequencer step 3, the rightmost refers to sequencer step 0. By default the wait is executed for sequencer step 3 (last sequencer step).

Note(s):

1. Return to the Register Map (0xDF).

MOD_CALIB_CFG0 Register

Figure 102:
MOD_CALIB_CFG0

Addr: 0xE0		MOD_CALIB_CFG0		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	MODE_CALIB_ NTH_ITERATION	0xFF	R/W	Defines the repetition rate of calibrations in sequencer rounds or steps depending on MOD_CALIB_NTH_ ITERATION_STEP_ENABLE. 0x00: Never 0x01-0xFE: Every n^{th} time 0xFF: Only once at start

Note(s):

1. Return to the Register Map (0xE0).

MOD_CALIB_CFG2 Register

Figure 103:
MOD_CALIB_CFG2

Addr: 0xE2		MOD_CALIB_CFG2		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	MOD_CALIB_NTH_ ITERATION_RC_ ENABLE	1	R/W	Enables a residual calibration during the nth iteration. Please observe that this residual calibration feature only makes sense for modulators which are enabled in the first sequences step, since a gain calibration only happens in the first sequencer step.
6	MOD_CALIB_NTH_ ITERATION_AZ_ ENABLE	1	R/W	Enables auto-zero calibration during the nth iteration.
5	MOD_CALIB_NTH_ ITERATION_AGC_ ENABLE	0	R/W	Enables AGC calibration during the nth iteration. Please observe in this case, that MOD_CALIB_NTH_ ITERATION_STEP_ENABLE must be “0” otherwise AGC will not be properly executed.
4	MOD_CALIB_ RESIDUAL_ENABLE_ AUTO_CALIB_ON_ GAIN_CHANGE	1	R/W	Enables an automatic re-calibration in case of a change in gain. This recalibration is executed at the beginning of each sequencer step.
3:0	MOD_CALIB_ RESIDUAL_AVERAGE_ ROUNDS	0011	R/W	Defines the number of averaging rounds during residual calibrations. 0000b: No averaging 0001b: 2 averaging rounds 0010b: 3 averaging rounds …. 1111b: 16 averaging rounds

Note(s):

1. Return to the Register Map (0xE2).

MOD_CALIB_CFG3 Register

Figure 104:
MOD_CALIB_CFG3

Addr: 0xE3		MOD_CALIB_CFG3		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:6	MOD_AZ_SETTLING_ FACTOR	01b	R/W	**Modulator Autozero Settling Factor**: Defines the settling time factor during modulator autozero iterations 00b: 1x 01b: 2x 10b: 3x 11b: 4x
5:3	MOD_AZ_ ITERATIONS	101b	R/W	**Modulator Autozero Iterations:** Defines the number of modulator autozero iterations 000b: 0 001b: 1 010b: 2 011b: 4 100b: 8 101b:16 110b: 32 111b: 64
2:0	MOD_AZ_ SETTLING	101b	R/W	**Defines the Modulator Autozero Settling Time:** (MOD_AZ_SETTLING*(4µs*k) + (8µs*k)) * scale (k = 0.925925925925926), where scale = 1 in SAR phase and (MOD_AZ_SETTLING_FACTOR + 1) in averaging phase.

Note(s):

1. Return to the Register Map (0xE3).

MOD_COMP_CFG2 Register

Figure 105:
MOD_COMP_CFG2

Addr: 0xE7		MOD_COMP_CFG2		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:6	MOD_IDAC_ RANGE	10	R/W	Sets the auto zero range of the current digital-to-analog converter. 00: 58µV 01: 38µV 10: 18µV 11: 9µV

Addr: 0xE7		MOD_COMP_CFG2		
Bit	Field	Reset	Type	Bit Description
5:0	Reserved	0xF		Do not overwrite

Note(s):

1. Return to the Register Map (0xE7).

MOD_RESIDUAL_CFG0 Register

Figure 106:
MOD_RESIDUAL_CFG0

Addr: 0xE8		MOD_RESIDUAL_CFG0		
Bit	Field	Reset	Type	Bit Description
7:6	Reserved	0		
5:0	MOD_RESIDUAL_ MINIMUM_STEPS	0	R/W	Defines the minimum number of modulator clock cycles for residual measurements, hence the minimum measurement time for residual measurements. This can be used during e.g. AGC to receive equidistant measurements throughout all gain steps. mod_clock_cycles = MOD_RESIDUAL_MINIMUM_STEPS + 1

Note(s):

1. Return to the Register Map (0xE8).

MOD_RESIDUAL_CFG1 Register

Figure 107:
MOD_RESIDUAL_CFG1

Addr: 0xE9		MOD_RESIDUAL_CFG1		
Bit	Field	Reset	Type	Bit Description
7:4	MOD_RESIDUAL_ RELATIVE_ STEPS_3	0	R/W	Relative number of steps to add to 8 steps in case of number of residual bits 3.
3:0	MOD_RESIDUAL_ RELATIVE_ STEPS_2	0	R/W	Relative number of steps to add to 4 steps in case of number of residual bits 2.

Note(s):

1. Return to the Register Map (0xE9).

MOD_RESIDUAL_CFG2 Register

Figure 108:
MOD_RESIDUAL_CFG2

Addr: 0xEA		MOD_RESIDUAL_CFG2		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:3	MOD_RESIDUAL_RELATIVE_STEPS_3	0	R/W	Relative number of steps to add to 16 steps in case of number of residual bits 4.
2:0	MOD_RESIDUAL_RELATIVE_STEPS_2	0	R/W	Relative number of steps to add to 2 steps in case of number of residual bits 1.

Note(s):

1. Return to the Register Map (0xEA).

VSYNC_DELAY_CFG0 Register

Figure 109:
VSYNC_DELAY_CFG0

Addr: 0xEB		VSYNC_DELAY_CFG0		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	VSYNC_DELAY[7:0]	0	R/W	Sets the time to delay an input from the VSYNC pin in multiples of 1.3888µs. The selectable range is 1.3888µs to 2^14*1.3888µs=22.754ms. ATTENTION: Reset value must be 0 so that RAM initialization works.

Note(s):

1. Return to the Register Map (0xEB).

VSYNC_DELAY_CFG1 Register

Figure 110:
VSYNC_DELAY_CFG1

Addr: 0xEC		VSYNC_DELAY_CFG1		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:6	Reserved	0		
5:0	VSYNC_DELAY[13:8]	0	R/W	See VSYNC_DELAY_CFG0.

Note(s):

1. Return to the Register Map (0xEC).

VSYNC_PERIOD0 Register

Figure 111:
VSYNC_PERIOD0

Addr: 0xED		VSYNC_PERIOD0		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	VSYNC_PERIOD[7:0]	0	R	The measured vsync period in multiples of 1.3888µs. This can be used to correct the internal RC oscillator with an input signal at the VSYNC pin derived from a crystal oscillator.

Note(s):

1. Return to the Register Map (0xED).

VSYNC_PERIOD1 Register

Figure 112:
VSYNC_PERIOD1

Addr: 0xEE		VSYNC_PERIOD1		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	VSYNC_PERIOD[15:8]	0	R	The measured vsync period in multiples of 1.3888µs. This can be used to correct the internal RC oscillator with an input signal at the VSYNC pin derived from a crystal oscillator.

Note(s):

1. Return to the Register Map (0xEE).

VSYNC_PERIOD_TARGET0 Register

Figure 113:
VSYNC_PERIOD_TARGET0

Addr: 0xEF		VSYNC_PERIOD_TARGET0		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	VSYNC_PERIOD_TARGET[7:0]	0	R/W	It sets the target vsync period. The value can be calculated as VSYNC_PERIOD_TARGET = ((1/target_frequency_in_Hz) * 1.3888888 * 10^{-6}).

Note(s):

1. Return to the Register Map (0xEF).

VSYNC_PERIOD_TARGET1 Register

Figure 114:
VSYNC_PERIOD_TARGET1

Addr: 0xF0		VSYNC_PERIOD_TARGET1		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	VSYNC_PERIOD_USE_FAST_TIMING_EVAL	0	R/W	If set to “0” it selects VSYNC_PERIOD[15:1] (range 15Hz to 500Hz) and if set to “1” it selects VSYNC_PERIOD[14:0] (range 30Hz to 1kHz).
6:0	VSYNC_PERIOD_TARGET[14:8]	0	R/W	See VSYNC_PERIOD_TARGET0.

Note(s):

1. Return to the Register Map (0xF0).

VSYNC_CONTROL Register

Figure 115:
VSYNC_CONTROL

Addr: 0xF1		VSYNC_CONTROL		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:1	Reserved	0		
0	SW_VSYNC_TRIGGER	0	R/W	**Trigger Software vsync Pulse.** In case if vsync_mode is 1, this register can be written to 1 to trigger a vsync from I²C/I3C side. If one knows the exact time between two such I²C/I3C writings, the oscillator offset can be calculated by using the resulting value in vsync_ trigger.

Note(s):

1. Return to the Register Map (0xF1).

VSYNC_CFG Register

Figure 116:
VSYNC_CFG

Addr: 0xF2		VSYNC_CFG				
Bit	**Field**	**Default**	**Access**	**Bit Description**		
7:6	OSC_CALIB_MODE	0	R/W	Oscillator calibration mode register		
				Value	**ID**	**Meaning**
				0	osccal_ disable	no autmatic oscillator calibration is done
				1	osccal_ after_pon	if pon goes to 1 or after each vsync_lost goes 0 an oscillator calibration is done once not during measurement
				2	osccal_ always_on	oscillator calibration is done always if possible, not during measurement and not if vsync_lost is detected
				3	osccal_ reserved	if set to 3, osccal is also not starting

Addr: 0xF2		VSYNC_CFG				
Bit	**Field**	**Default**	**Access**	**Bit Description**		
2	VSYNC_MODE	0	R/W	Select which input to use for vsync		
				Value	**ID**	**Meaning**
				0	pad_ vsync_ trigger	Use VSYNC/GPIO/INT input as vsync start trigger
				1	sw_vsync_ trigger	Use VSYNC_ CONTROL.sw_vsync_ trigger as vsync trigger
1	VSYNC_SELECT	0	R/W	Select which input to use for vsync		
				Value	**ID**	**Meaning**
				0	vsync_gpio	Use VSYNC/GPIO input
				1	int	Use INT input
0	VSYNC_INVERT	0	R/W	If enabled then the selected vsync input is inverted.		
				Value	**ID**	**Meaning**
				0	do_not_ invert	Do not invert
				1	invert	Do invert

Note(s):

1. Return to the Register Map (0xF2).

FIFO_THR Register

Figure 117:
FIFO_THR

Addr: 0xF3		FIFO_THR		
Bit	**Field**	**Default**	**Access**	**Bit Description**
7:0	FIFO_THR[10:3]	127	R/W	If FIFO_LVL > FIFO_THR, an FIFO interrupt FINT is raised. See CFG2 and FIFO_LVL[2:0] for lsbs.

Note(s):

1. Return to the Register Map (0xF3).

MOD_FIFO_DATA_CFG0 Register

Figure 118:
MOD_FIFO_DATA_CFG0

Addr: 0xF4		MOD_FIFO_DATA_CFG0		
Bit	**Field**	**Default**	**Access**	**Bit Description**
7	MOD_ALS_FIFO_DATA0_WRITE_ENABLE	1	RAM=0x10L	Enable ALS data write to fifo of modulator 0, if flicker measurement is not enabled in this sequencer step or ficker measurement has already finished (select als_nr_samples >= fd_nr_samples) or in case of do_als_final_processing_after_flicker.
5	MOD_FD_FIFO_DATA0_COMPRESSION_ENABLE	0	RAM=0x10L	Enables data compression in case of flicker detection mode.
4	MOD_FD_FIFO_DATA0_DIFFERENCE_ENABLE	0	RAM=0x10L	Enables that only the difference between previous and actual data is used for data writing instead of actual data value. This makes only sense in case of MOD_FD_FIFO_DATA0_COMPRESSION_ENABLE=1.
3:0	MOD_FD_FIFO_DATA0_WIDTH	15	RAM=0x10L	Select data width to use for FIFO writing of flicker data0. Or in case of compression select the width of the data parts. See MOD_ALS_FIFO_DATA0_WRITE_ENABLE for more details. In case of no compression the user must specify the mod_fd_fifo_dataX_width's so that the full possible data is written to the fifo (log2(sample_time)+4). ATTENTION: There is no digital saturation implemented that show's a range overflow. There was not enough resources left to implement this.

Note(s):

1. Return to the Register Map (0xF4).

MOD_FIFO_DATA_CFG1 Register

Figure 119:
MOD_FIFO_DATA_CFG1

Addr: 0xF5		MOD_FIFO_DATA_CFG1		
Bit	**Field**	**Default**	**Access**	**Bit Description**
7	MOD_ALS_FIFO_DATA1_WRITE_ENABLE	1	RAM=0x11L	See MOD_ALS_FIFO_DATA0_WRITE_ENABLE.
5	MOD_FD_FIFO_DATA1_COMPRESSION_ENABLE	0	RAM=0x11L	See MOD_FD_FIFO_DATA0_COMPRESSION_ENABLE and MOD_FD_FIFO_DATA0_WIDTH for more details.
4	MOD_FD_FIFO_DATA1_DIFFERENCE_ENABLE	0	RAM=0x11L	See MOD_FD_FIFO_DATA0_DIFFERENCE_ENABLE.
3:0	MOD_FD_FIFO_DATA1_WIDTH	15	RAM=0x11L	See MOD_FD_FIFO_DATA0_WIDTH.

Note(s):

1. Return to the Register Map (0xF5).

MOD_FIFO_DATA_CFG2 Register

Figure 120:
MOD_FIFO_DATA_CFG2

Addr: 0xF6		MOD_FIFO_DATA_CFG2		
Bit	**Field**	**Default**	**Access**	**Bit Description**
7	MOD_ALS_FIFO_DATA2_WRITE_ENABLE	1	RAM=0x12L	See MOD_ALS_FIFO_DATA0_WRITE_ENABLE.
5	MOD_FD_FIFO_DATA2_COMPRESSION_ENABLE	0	RAM=0x12L	See MOD_FD_FIFO_DATA0_COMPRESSION_ENABLE and MOD_FD_FIFO_DATA0_WIDTH for more details.
4	MOD_FD_FIFO_DATA2_DIFFERENCE_ENABLE	0	RAM=0x12L	See MOD_FD_FIFO_DATA0_DIFFERENCE_ENABLE.
3:0	MOD_FD_FIFO_DATA2_WIDTH	15	RAM=0x12L	See MOD_FD_FIFO_DATA0_WIDTH.

Note(s):

1. Return to the Register Map (0xF6).

MOD_FIFO_DATA_CFG3 Register

Figure 121:
MOD_FIFO_DATA_CFG3

Addr: 0xF7		MOD_FIFO_DATA_CFG3		
Bit	**Field**	**Default**	**Access**	**Bit Description**
7	MOD_ALS_FIFO_DATA3_WRITE_ENABLE	1	RAM=0x13L	See MOD_ALS_FIFO_DATA0_WRITE_ENABLE.
5	MOD_FD_FIFO_DATA3_COMPRESSION_ENABLE	0	RAM=0x13L	See MOD_FD_FIFO_DATA0_COMPRESSION_ENABLE and MOD_FD_FIFO_DATA0_WIDTH for more details.
4	MOD_FD_FIFO_DATA3_DIFFERENCE_ENABLE	0	RAM=0x13L	See MOD_FD_FIFO_DATA0_DIFFERENCE_ENABLE
3:0	MOD_FD_FIFO_DATA3_WIDTH	15	RAM=0x13L	See MOD_FD_FIFO_DATA0_WIDTH.

Note(s):

1. Return to the Register Map (0xF7).

MOD_FIFO_DATA_CFG4 Register

Figure 122:
MOD_FIFO_DATA_CFG4

Addr: 0xF8		MOD_FIFO_DATA_CFG4		
Bit	**Field**	**Default**	**Access**	**Bit Description**
7	MOD_ALS_FIFO_DATA4_WRITE_ENABLE	1	RAM=0x14L	See MOD_ALS_FIFO_DATA0_WRITE_ENABLE.
5	MOD_FD_FIFO_DATA4_COMPRESSION_ENABLE	0	RAM=0x14L	See MOD_FD_FIFO_DATA0_COMPRESSION_ENABLE and MOD_FD_FIFO_DATA0_WIDTH for more details.
4	MOD_FD_FIFO_DATA4_DIFFERENCE_ENABLE	0	RAM=0x14L	See MOD_FD_FIFO_DATA0_DIFFERENCE_ENABLE.
3:0	MOD_FD_FIFO_DATA4_WIDTH	15	RAM=0x14L	See MOD_FD_FIFO_DATA0_WIDTH.

Note(s):

1. Return to the Register Map (0xF8).

MOD_FIFO_DATA_CFG5 Register

Figure 123:
MOD_FIFO_DATA_CFG5

Addr: 0xF9		MOD_FIFO_DATA_CFG5		
Bit	**Field**	**Default**	**Access**	**Bit Description**
7	MOD_ALS_FIFO_DATA5_WRITE_ENABLE	1	RAM=0x15L	See MOD_ALS_FIFO_DATA0_WRITE_ENABLE.
5	MOD_FD_FIFO_DATA5_COMPRESSION_ENABLE	0	RAM=0x15L	See MOD_FD_FIFO_DATA0_COMPRESSION_ENABLE and MOD_FD_FIFO_DATA0_WIDTH for more details.
4	MOD_FD_FIFO_DATA5_DIFFERENCE_ENABLE	0	RAM=0x15L	See MOD_FD_FIFO_DATA0_DIFFERENCE_ENABLE.
3:0	MOD_FD_FIFO_DATA5_WIDTH	15	RAM=0x15L	See MOD_FD_FIFO_DATA0_WIDTH.

Note(s):

1. Return to the Register Map (0xF9).

MOD_FIFO_DATA_CFG6 Register

Figure 124:
MOD_FIFO_DATA_CFG6

Addr: 0xFA		MOD_FIFO_DATA_CFG6		
Bit	**Field**	**Default**	**Access**	**Bit Description**
7	MOD_ALS_FIFO_DATA6_WRITE_ENABLE	1	RAM=0x16L	See MOD_ALS_FIFO_DATA0_WRITE_ENABLE.
5	MOD_FD_FIFO_DATA6_COMPRESSION_ENABLE	0	RAM=0x16L	See MOD_FD_FIFO_DATA0_COMPRESSION_ENABLE and MOD_FD_FIFO_DATA0_WIDTH for more details.
4	MOD_FD_FIFO_DATA6_DIFFERENCE_ENABLE	0	RAM=0x16L	See MOD_FD_FIFO_DATA0_DIFFERENCE_ENABLE.
3:0	MOD_FD_FIFO_DATA6_WIDTH	15	RAM=0x16L	See MOD_FD_FIFO_DATA0_WIDTH.

Note(s):

1. Return to the Register Map (0xFA).

MOD_FIFO_DATA_CFG7 Register

Figure 125:
MOD_FIFO_DATA_CFG7

Addr: 0xFB		MOD_FIFO_DATA_CFG7		
Bit	**Field**	**Default**	**Access**	**Bit Description**
7	MOD_ALS_FIFO_DATA7_WRITE_ENABLE	1	RAM=0x17L	See MOD_ALS_FIFO_DATA0_WRITE_ENABLE.
5	MOD_FD_FIFO_DATA7_COMPRESSION_ENABLE	0	RAM=0x17L	See MOD_FD_FIFO_DATA0_COMPRESSION_ENABLE and MOD_FD_FIFO_DATA0_WIDTH for more details.
4	MOD_FD_FIFO_DATA7_DIFFERENCE_ENABLE	0	RAM=0x17L	See MOD_FD_FIFO_DATA0_DIFFERENCE_ENABLE
3:0	MOD_FD_FIFO_DATA7_WIDTH	15	RAM=0x17L	See MOD_FD_FIFO_DATA0_WIDTH.

Note(s):

1. Return to the Register Map (0xFB).

FIFO_STATUS0 Register

Figure 126:
FIFO_STATUS0

Bits	Addr	Field	Reset	Type	Description
7:0	0xFC	FIFO_LVL[10:3]	0	R	**FIFO Status 0** Contains the number of 1-byte FIFO entries. The size of the FIFO is 1280x8 (5x128x16). Thus FIFO_LVL ranges between 0 (empty) and 1280 (full). Always read FIFO_STATUS0 and then FIFO_STATUS1 one after the other to receive correct FIFO status information.
2:0	0xFD	FIFO_LVL[2:0]	0	R	

Note(s):

1. Return to the Register Map (0xFC, 0xFD).

FIFO_STATUS1 Register

Figure 127:
FIFO_STATUS1

Addr: 0xFD		FIFO_STATUS1		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7	FIFO_OVERFLOW	0	R	If set to "1" a FIFO overflow has occurred and data for the FIFO was lost (e.g. reading from FIFO was too slow). This flag is cleared by PON and FIFO_CLR. Always check this flag before and after reading the FIFO. Read FIFO_STATUS0 and then FIFO_STATUS1 to get consistent values for both registers.
6	FIFO_UNDERFLOW	0	R	If set to "1" the FIFO was read out too often and has returned 0 at least once. In such case the read-out data may not consistent anymore. This flag is cleared by PON and FIFO_CLR. Always check this flag before and after reading the FIFO. Read FIFO_STATUS0 and then FIFO_STATUS1 to get consistent values for both registers.
5:3	Reserved	0		
2:0	FIFO_LVL[2:0]	0	R	See FIFO Status 0 for description. Read FIFO_STATUS0 and then FIFO_STATUS1 to get consistent values for both registers.

Note(s):

1. Return to the Register Map (0xFD).

FIFO_DATA_PROTOCOL Register

Figure 128:
FIFO_DATA_PROTOCOL

Addr: 0xFE		FIFO_DATA_PROTOCOL		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	FIFO_DATA_ PROTOCOL	0	R	The register FIFO_DATA_PROTOCOL can used to read-out FIFO data using the protocol mechanism. It can be read out with single reads or with a block-read.

Note(s):

1. Return to the Register Map (0xFE).

FIFO_DATA Registers

Figure 129:
FIFO_DATA

Addr: 0xFF		FIFO_DATA		
Bit	**Field**	**Reset**	**Type**	**Bit Description**
7:0	FIFO_DATA	0	R	The register FIFO_DATA can be read-out with single reads or with a block-read. Upon reading out FIFO_DATA, the internal FIFO read pointer is advanced and FIFO_LVL is decreased. A false reading upon the FIFO_LVL will return 0 and set the FIFO_UNDERFLOW flag.

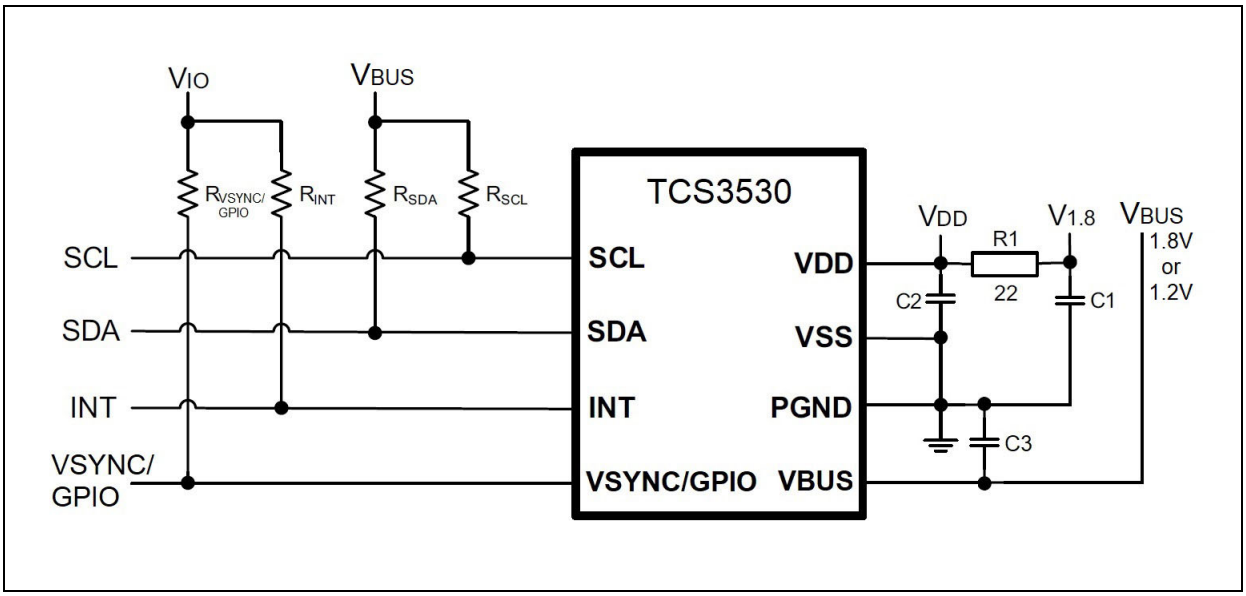
Note(s):

1. Return to the Register Map (0xFF).

Application Information

It is highly recommended to consult the ams OSRAM application team for circuit diagram and layout review at design-in.

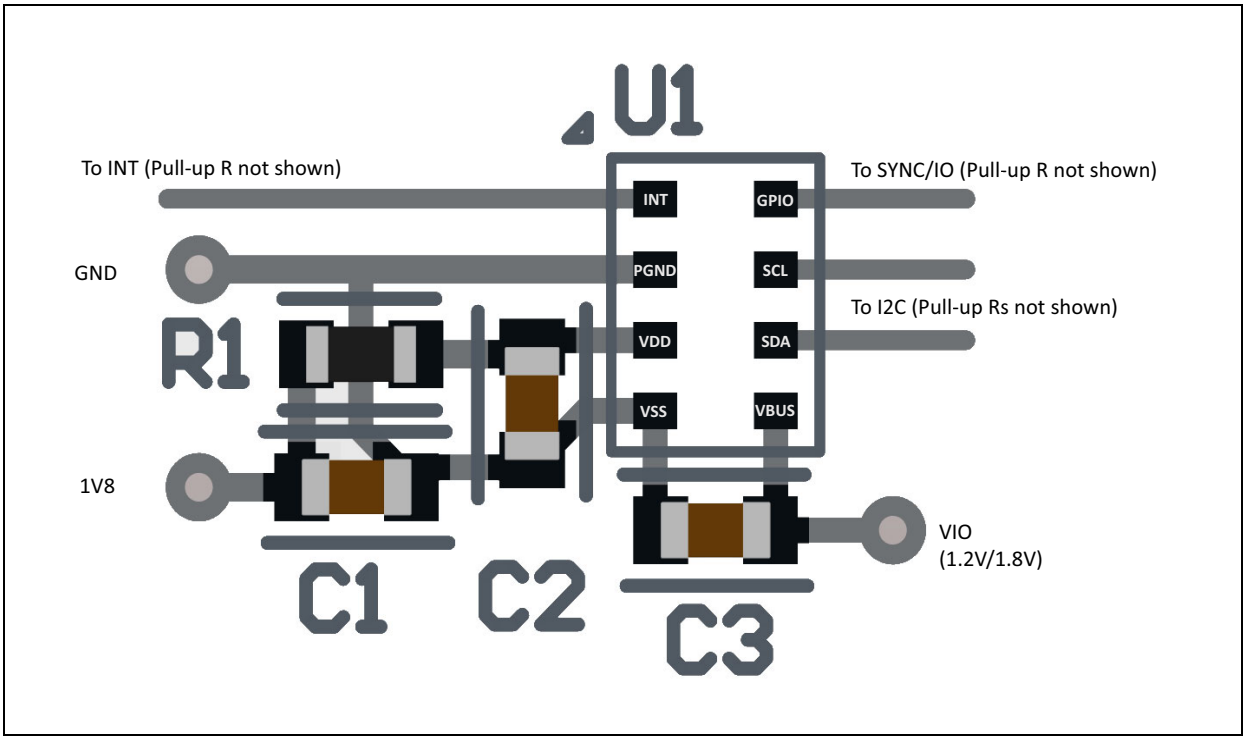
Figure 130:
TCS3530 Typical Application Circuit



Note(s):

1. C1 in the graphic above shall be 4.7µF, 6.3V, 10% and C2 in the graphic above shall be 1µF, 6.3V, 20%. All ground vias shall connected to a solid ground plane.

Figure 131:
TCS3530 Recommended Part Placement

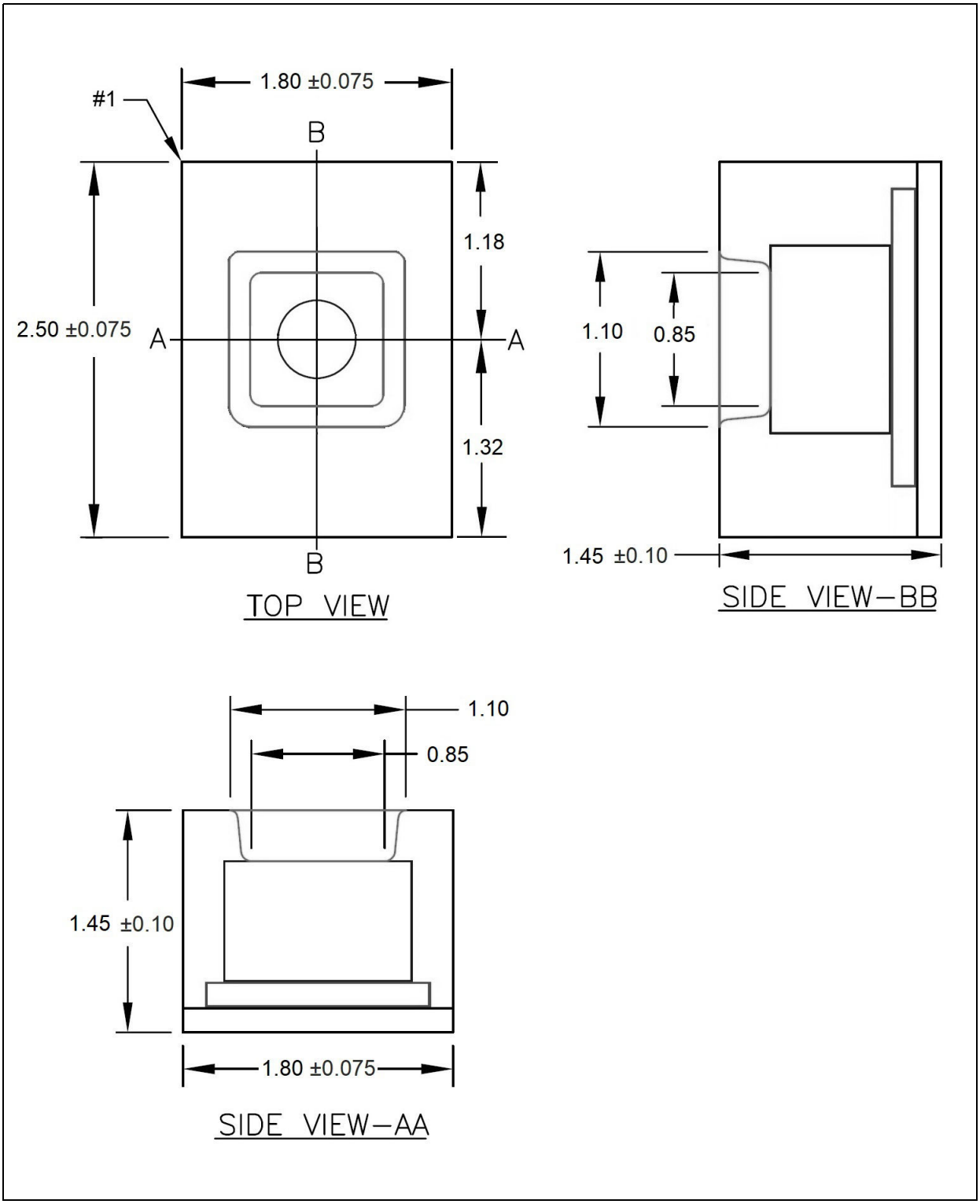


Note(s):

1. NC pins do not have an internal electrical connection. For device ESD protection, it is recommended to connect it to ground.

Package Drawings & Markings

Figure 132:
TCS3530 Module Dimensions



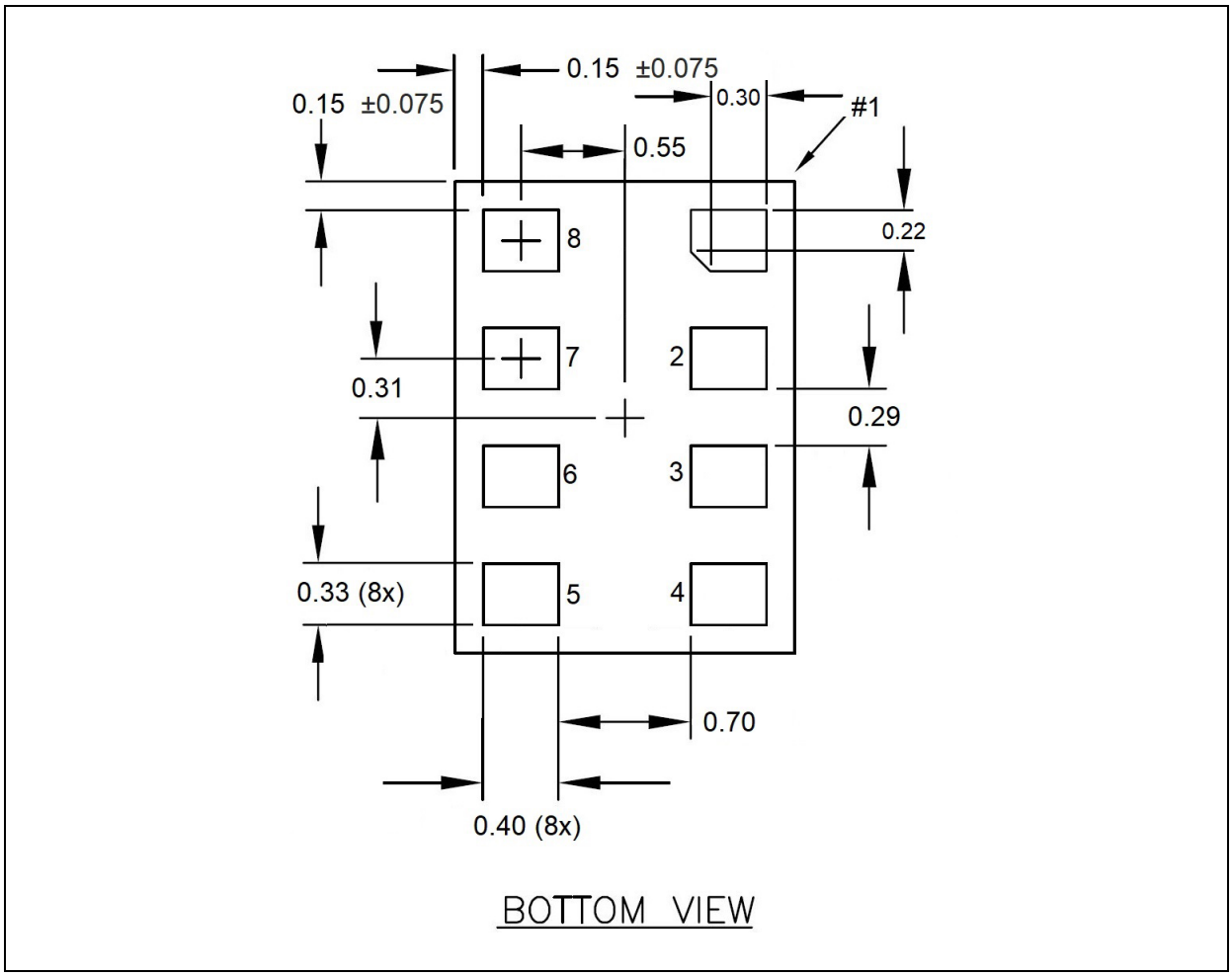
Note(s):

1. All linear dimensions are in millimeters.
2. Contacts are copper with NiPdAu plating (ENEPIG).
3. This package contains no lead (Pb).
4. This drawing is subject to change without notice.

PCB Pad Layout

Suggested PCB pad layout guidelines for the surface mount module are shown. Flash Gold is recommended as a surface finish for the landing pads.

Figure 133:
TCS3530 PCB Pad Layout

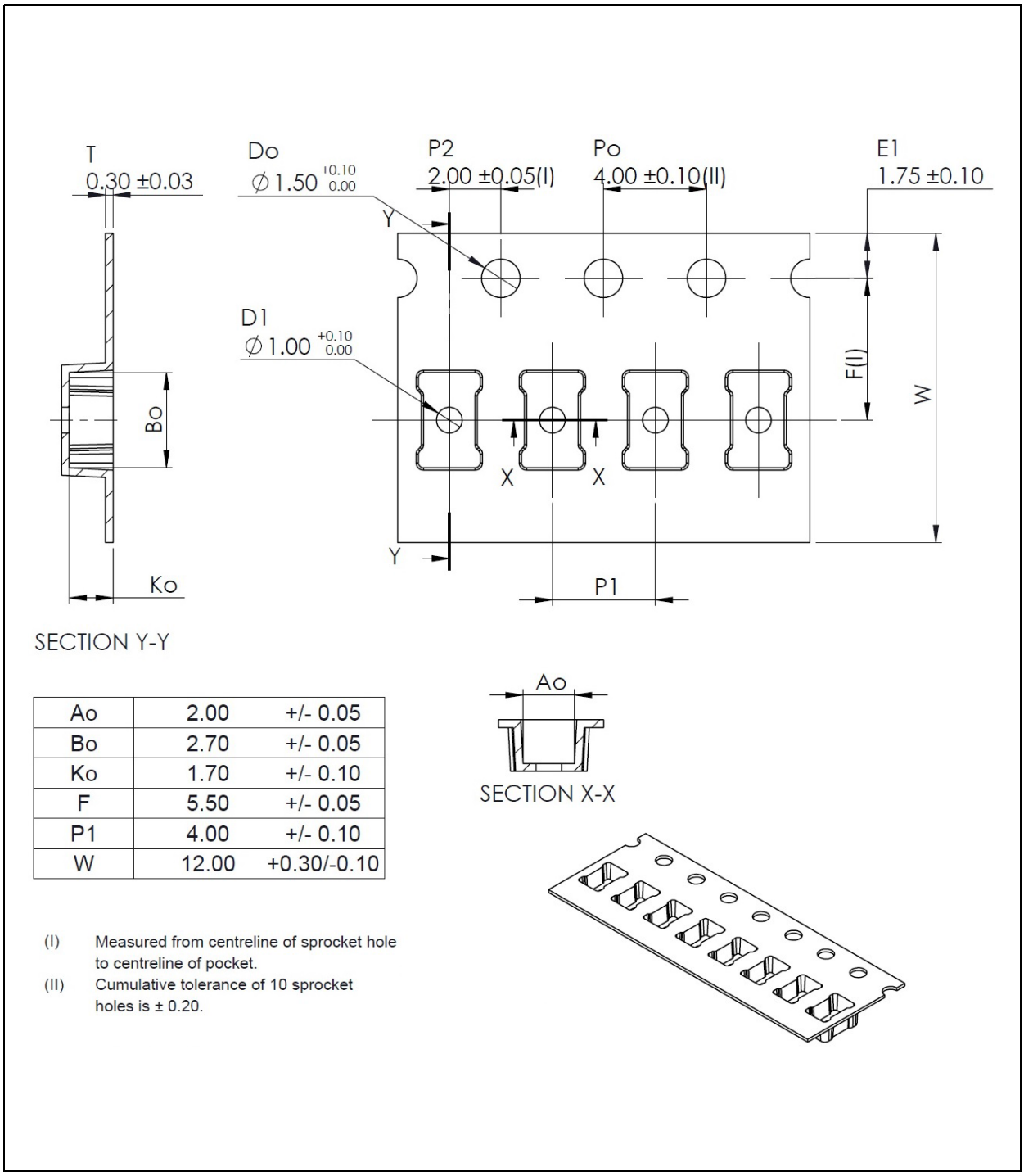


Note(s):

1. All linear dimensions are in millimeters.
2. This drawing is subject to change without notice.

Tape & Reel Information

Figure 134:
Tape and Reel Mechanical Drawing



Ao	2.00	+/- 0.05
Bo	2.70	+/- 0.05
Ko	1.70	+/- 0.10
F	5.50	+/- 0.05
P1	4.00	+/- 0.10
W	12.00	+0.30/-0.10

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20.

Note(s):

1. All linear dimensions are in millimeters. Dimension tolerance is ± 0.10 mm unless otherwise noted.
2. The dimensions on this drawing are for illustrative purposes only. Dimensions of an actual carrier may vary slightly.
3. Symbols on drawing Ao, Bo, and Ko are defined in ANSI EIA Standard 481−B 2001.
4. Each reel is generally 330 millimeters in diameter and contains 5000 parts. Please reconfirm for actual orders.
5. ams OSRAM packaging tape and reel conform to the requirements of EIA Standard 481−B.
6. In accordance with EIA standard, device pin 1 is located next to the sprocket holes in the tape.
7. This drawing is subject to change without notice.

Soldering & Storage Information

Soldering Information

The module has been tested and has demonstrated an ability to be reflow soldered to a PCB substrate. The solder reflow profile describes the expected maximum heat exposure of components during the solder reflow process of product on a PCB. Temperature is measured on top of component. The components should be limited to a maximum of three passes through this solder reflow profile.

Please observe that re-soldering the module will influence color measurement accuracy. Please consult with application team in such case.

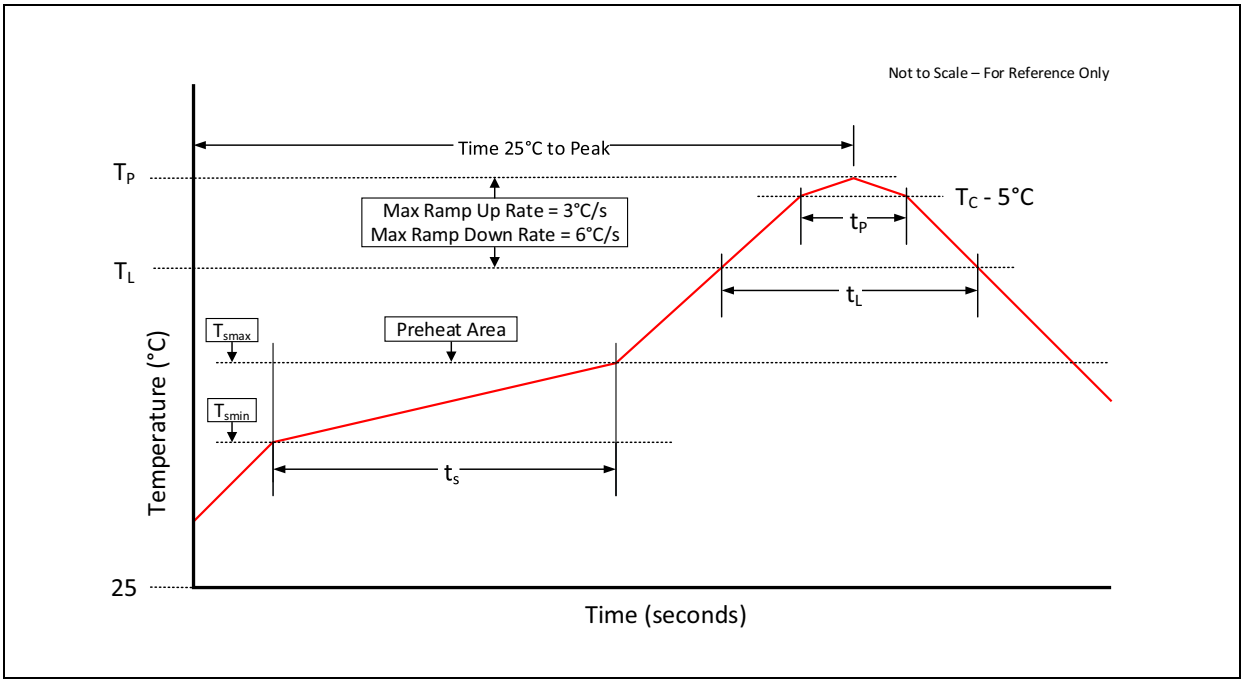
Figure 135:
Solder Reflow Profile

Profile Feature Preheat/Soak	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Temperature Min (T_{smin})	100°C	150°C
Temperature Max (T_{smax})	150°C	200°C
Time (t_s) from (T_{smin} to T_{smax})	60-120 s	60-120 s
Ramp-up rate (T_L to T_P)	3°C/s max.	3°C/s max.
Liquidous temperature (T_L) Time (t_L) maintained above T_L	183°C 60-150 s	217°C 60-150 s
Peak package body temperature (T_P)	For users T_P must not exceed the Classification temp of 235°C For suppliers T_P must equal or exceed the Classification temp of 235°C	For users T_P must not exceed the Classification temp of 260°C For suppliers T_P must equal or exceed the Classification temp of 260°C
Time (t_P)[(1)] within 5°C of the specified classification temperature (T_c)	20[(1)]s	30[(1)]s
Ramp-down rate (T_P to T_L)	6°C/s max.	6°C/s max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.

Note(s):

1. Tolerance for peak profile temperature (TP) is defined as a supplier minimum and a user maximum.

Figure 136:
Solder Reflow Profile Graph



Storage Information

Moisture Sensitivity

Optical characteristics of the device can be adversely affected during the soldering process by the release and vaporization of moisture that has been previously absorbed into the package. To ensure the package contains the smallest amount of absorbed moisture possible, each device is baked prior to being dry packed for shipping. Devices are dry packed in a sealed aluminized envelope called a moisture-barrier bag with silica gel to protect them from ambient moisture during shipping, handling, and storage before use.

Shelf Life

The calculated shelf life of the device in an unopened moisture barrier bag is 24 months from the date code on the bag when stored under the following conditions:

- Shelf Life: 24 months
- Ambient Temperature: <40°C
- Relative Humidity: <90%

Rebaking of the devices will be required if the devices exceed the 24 months shelf life or the Humidity Indicator Card shows that the devices were exposed to conditions beyond the allowable moisture region.

Floor Life

The module has been assigned a moisture sensitivity level of MSL 3. As a result, the floor life of devices removed from the moisture barrier bag is 168 hours from the time the bag was opened, provided that the devices are stored under the following conditions:

- Floor Life: 168 hours
- Ambient Temperature: <30°C
- Relative Humidity: <60%

If the floor life or the temperature/humidity conditions have been exceeded, the devices must be rebaked prior to solder reflow or dry packing.

Rebaking Instructions

When the shelf life or floor life limits have been exceeded, rebake at 50°C for 12 hours.

Ordering & Contact Information

Figure 137:
Ordering Information

Ordering Code	Address	Interface	Delivery Form	Delivery Quantity
TCS35303-2	0x39	1.8V/1.2V I^2C	Tape & Reel	5000 pcs/reel
TCS35303-2M	0x39	1.8V/1.2V I^2C	Tape & Reel	500 pcs/reel

Note(s):

1. TCS35303-3 on request with I3C mode enabled.

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Document Status

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
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Revision Information

Changes from 2-00 (2022-Jun-24) to current revision 3-00 (2023-Jun-23)	Page
Updated document security class from “Confidential” to “Public”	
Updated Shelf Life from 12 months to 24 months	96

Note(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

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72 MOD_CALIB_CFG0 Register
73 MOD_CALIB_CFG2 Register
74 MOD_CALIB_CFG3 Register
74 MOD_COMP_CFG2 Register

75 MOD_RESIDUAL_CFG0 Register
75 MOD_RESIDUAL_CFG1 Register
76 MOD_RESIDUAL_CFG2 Register
76 VSYNC_DELAY_CFG0 Register
77 VSYNC_DELAY_CFG1 Register
77 VSYNC_PERIOD0 Register
77 VSYNC_PERIOD1 Register
78 VSYNC_PERIOD_TARGET0 Register
78 VSYNC_PERIOD_TARGET1 Register
79 VSYNC_CONTROL Register
79 VSYNC_CFG Register
80 FIFO_THR Register
81 MOD_FIFO_DATA_CFG0 Register
82 MOD_FIFO_DATA_CFG1 Register
83 MOD_FIFO_DATA_CFG2 Register
84 MOD_FIFO_DATA_CFG3 Register
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86 MOD_FIFO_DATA_CFG5 Register
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Compliance Statement to RoHS Directive (2011/65/EU including amendment (EU) 2015/863) for Semiconductor Products in brand ams and OSRAM

ams OSRAM declares that:

- the company has installed an internal management system which ensures compliance of our semiconductor products with the applicable legal requirements. This system includes products, parts and materials procured from suppliers,
- all ams and OSRAM branded semiconductor products conform to the substance requirements of EU Directive 2011/65/EU - RoHS (including amendment (EU) 2015/863), quantity limit of 0.1% by mass (1000 ppm) in homogeneous material for: Lead (Pb), Mercury (Hg), Hexavalent Chromium (Cr^{+6}), Polybrominated Biphenyls (PBB), Polybrominated Diphenyl Ethers (PBDE) Bis(2-Ethylhexyl) Phthalate (DEHP), Benzyl Butyl Phthalate (BBP), Dibutyl Phthalate (DBP), and Diisobutyl Phthalate (DIBP) and quantity limit of 0.01% by mass (100 ppm) of homogeneous material for Cadmium are not exceeded unless in an application exempted by Annex III of the Directive.
- products' full material declaration can be referred to for RoHS compliance status of a product.

We continue to monitor our semiconductor products and the supply chain for the requirements posed by this and other regulations, e.g.:

- Directive 2000/53/EC (End-of-life vehicles – ELV)
- Non-EU RoHS regulations similar to above Directive

For other inquiries, please visit our webpage (Product stewardship - Semiconductor | ams OSRAM (ams-osram.com)) or contact your respective sales representative for the material declarations of specific semiconductor products.

The information provided in this statement represents our knowledge and belief as of the date that it is provided. We base our knowledge and belief on information provided by third parties and make no representation or warranty as to the accuracy and shall have no liability for the consequences of use of such information. We have taken and continue to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. We and our suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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Release Date: 2022-08-09

ams OSRAM Compliance Statement to REACh Regulation (EC) No. 1907/2006 for its Semiconductor Products

Entered into force on 1 June 2007, Regulation (EC) No 1907/2006 concerning the Registration, Evaluation, Authorization and Restriction of Chemicals (REACh) aims to improve the protection of human health and the environment from the risks posed by chemicals, while enhancing the competitiveness of the business industries.

The Candidate List of Substances has been updated on **4th February 2026** (253 substances of very high concern - SVHC). We, based on best available information provided by our suppliers, declare:

- None of the Candidate List substances is exceeding 0.1% (weight) in a semiconductor article
- Our semiconductor products do not contain substances as listed in REACh Annex XVII exceeding the relevant limits
- ams OSRAM semiconductor products are “articles”, not chemicals; Safety Data Sheets are not applicable

More information on the regulation and related directives to which our semiconductor products comply can be viewed here:

- REACh – SVHC candidate List (https://echa.europa.eu/candidate-list-table)
- REACh Annex XVII Substances (https://echa.europa.eu/substances-restricted-under-reach)

We continue to monitor our semiconductor products and the supply chain for the requirements posed by the regulations. For other inquiries, please visit our webpage (Product stewardship - semiconductor | ams OSRAM (ams-osram.com)) or contact your respective sales representative for the material declarations of specific semiconductor products.

The information provided in this statement represents our knowledge and belief as of the date that it is provided. We base our knowledge and belief on information provided by third parties and make no representation or warranty as to the accuracy and shall have no liability for the consequences of use of such information. We have taken and continue to take reasonable steps to provide representative and accurate information, but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. We and our suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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