SA22307

High Efficiency, 36V Input Single Inductor Synchronous Step Up/Down Regulator

General Description

The SA22307 is a high voltage synchronous Buck-Boost converter. The device operates over a wide input voltage range from 4V to 36V. The SA22307 offers two operational modes, PSM and FCCM, under light load condition. The four-integrated low $R_{DS(ON)}$ switches minimize the conduction loss.

The SA22307 features external soft-start, enable control, open drain power good indicator and 1uA shutdown current. The SA22307 also includes full protection features, such as output over current limit protection, short circuit protection, over voltage protection and thermal shutdown for reliable operating.

The device is available in compact QFN5×5-30 package.

Features

- 4V to 36V Input Voltage Range
- 3V to 20V Output Voltage Range
- Low $R_{DS(ON)}$ for Internal Switches: 35mΩ
- External Soft-start Limits the Inrush Current
- 1μA shutdown current
- 7A Internal Switch Peak Current Capability
- Programmable Frequency 200kHz~600kHz
- 1.0V±2% Reference over -40°C to 125°C
- Light Load Operating Mode Selection: PSM or FCCM
- Power Good Indicator
- Hic-cup Mode for Output Short-circuit Protection
- Output Over Current Protection
- Thermal Shutdown with Auto Recovery
- Compact Package: QFN5×5-30
- Automotive AEC- Q100 Grade 1 Qualified

Ordering Information

SA22307 □(□□)□
- Temperature Code
- Package Code
- Optional Spec Code

Ordering Number	Package type	Note
SA22307TVA	QFN5×5-30	

Applications

- Automotive
- Infotainment
- High-Voltage DC-DC Converters

Typical Application

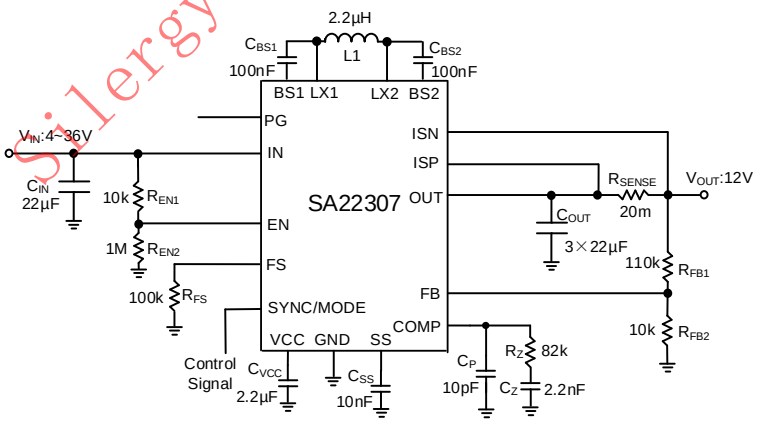


Figure1. Typical Schematic Diagram

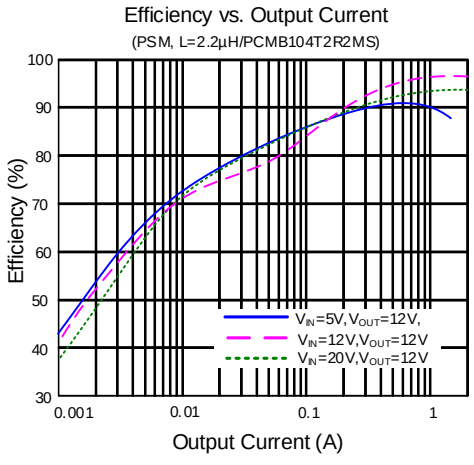
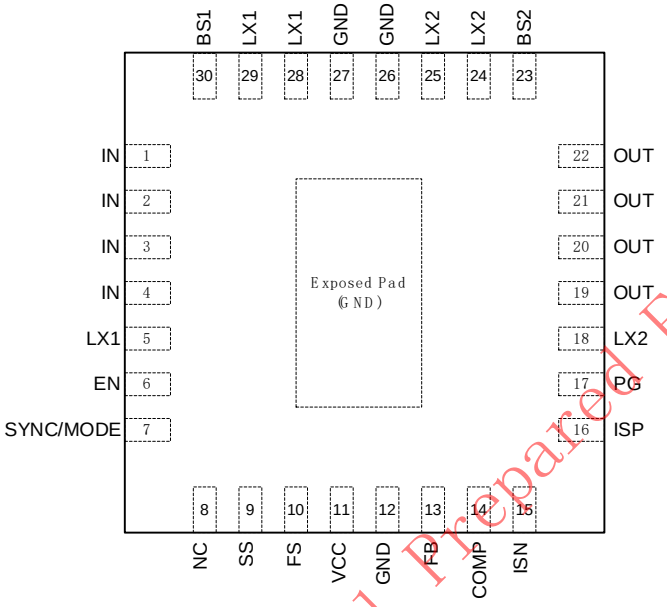


Figure2. Efficiency vs. Output Current

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Pinout (Top View)



Top Mark: CBK*xyz* (Device code: CBK, ***x=year code, y=week code, z= lot number code***)

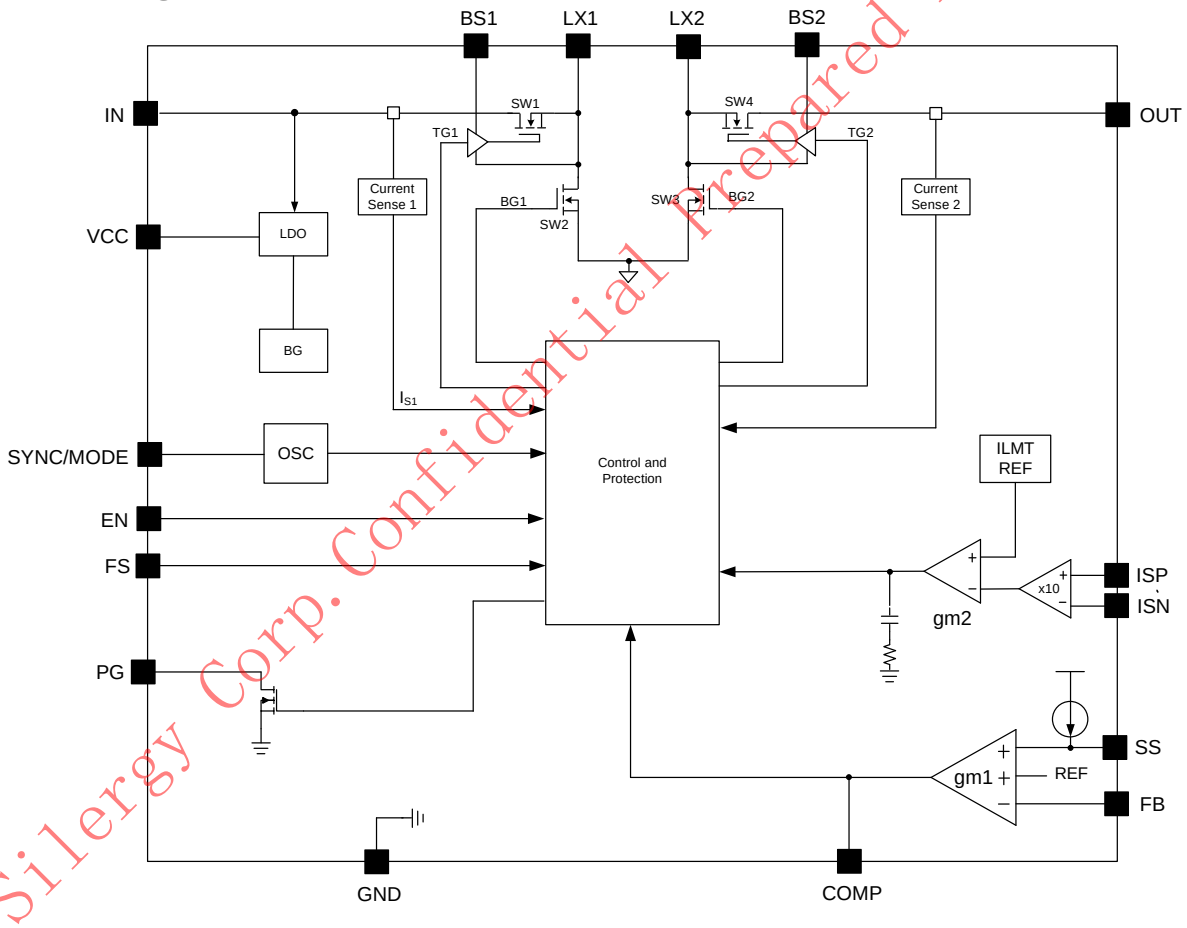
Pin Name	Pin Number	Description
IN	1,2,3,4	Power input pin, decouple this pin to GND with at least a 10μF ceramic capacitor.
LX1	5,28,29	Switching node 1.
EN	6	Enable control. Pull high to enable the device, pull low to disable the device. Do not leave this pin floating.
SYNC /MODE	7	Sync input or operating mode selection under light load. If connected to GND or open, PSM (Power Saving Mode) operation is enabled. If connected to VCC or external clock, force-PWM operation is enabled. When connected to an external clock, the internal oscillator synchronizes to the external clock. This pin has an internal 1MΩ pull down resistor.
NC	8	No connection, tie directly to the GND pin or leave it floating.
SS	9	Soft-start pin. Connect a capacitor from this pin to GND to program the soft-start time. Leave this pin open for default 1.6ms soft-start.
FS	10	Frequency setting pin. Connect a resistor from this pin to GND to program the switching frequency between 200kHz to 600kHz.
VCC	11	Internal 3.3V bias supply. Decouple this pin to GND with a minimum of 1μF ceramic capacitor.
GND	12, 26, 27, Exposed Pad	Ground pin.
FB	13	Output feedback pin. Connect this pin to the center point of the output resistor divider to adjust the V_{OUT} voltage: $V_{OUT}=V_{REF}\times(1+R_{FB1}/R_{FB2})$
COMP	14	Compensation pin. Connect RC network between this pin and ground.
ISN	15	Negative input of average current sense amplifier. Short to ISP and then connect to OUT if it is not used.
ISP	16	Positive input of average current sense amplifier. Short to ISN and then connect to OUT if it is not used.
PG	17	Power good indicator. Open drain output. Externally pulled high when the output voltage is above 93% of regulation voltage. Pulled low otherwise.

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Pin Name	Pin Number	Description
LX2	18,24,25	Switching node 2.
OUT	19,20,21,22	Power output pin. Decouple this pin to GND with at least a 10μF ceramic capacitor.
BS2	23	Boot-strap pin. Supply high side gate driver. Connect a 0.1μF ceramic capacitor between this pin and the LX2 pin. Do not connect a resistor in series with the capacitor.
BS1	30	Boot-strap pin. Supply high side gate driver. Connect a 0.1μF ceramic capacitor between this pin and the LX1 pin. Do not connect a resistor in series with the capacitor.

Block Diagram



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Absolute Maximum Ratings (Note 1)

IN, LX1 ---------- -0.3V to 40V
OUT, LX2, ISP, ISN ---------- -0.3V to 28V
EN, PG, SYNC/MODE ---------- -0.3V to 36V
COMP, VCC, SS, FB, FS ---------- -0.3V to 4V
BS-LX ---------- -0.3V to 4V
Power Dissipation, P_D @ T_A = 25°C, QFN5×5-30 ---------- 3.5W
Package Thermal Resistance (Note 2)
θ_{JA} ---------- 28°C/W
θ_{JC} ---------- 2.8°C/W
Junction Temperature Range ---------- -40°C to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C

Recommended Operating Conditions (Note 3)

Input Voltage Range ---------- 4V to 36V
Output Voltage Range ---------- 3V to 20V
Ambient Temperature Range ---------- -40°C to 125°C

Electrical Characteristics

(V_{IN} = 12V, T_J = -40°C to +125°C, Typical values are at T_J=25°C, unless otherwise specified, the values are guaranteed by test design or statistical correlation)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		4		36	V
Input UVLO Threshold	V_{UVLO}		3.3		3.9	V
Input UVLO Hysteresis	V_{HYS}			0.3		V
LDO Output Voltage	V_{LDO}	V_{IN}=12V, No Load	3.18	3.3	3.4	V
LDO Output Current Limit	$I_{LMT,LDO}$		30	70	130	mA
Quiescent Current	I_Q	No switching		200	260	μA
Shutdown Current	I_{SHDN}	EN=0, T_J = 25°C		1	2	μA
		EN=0, T_J = -40°C to 125°C			5	μA
Feedback Reference Voltage	V_{REF}	T_J = 25°C, internal reference	0.99	1	1.01	V
		T_J = -40°C to 125°C, internal reference	0.98	1	1.02	V
FB Input Current	I_{FB}	V_{FB}=3V	-50		50	nA
Internal FET R_{ON}	$R_{DS(ON)}$			35	60	mΩ
Peak Inductor Current Limitation	$I_{PK,LMT}$		6	7	8.5	A
Reverse Inductor Current Limitation	I_{NEG}	Force-PWM	-2		-3.5	A
Zero Current Detection Threshold	I_{ZERO}	PSM			500	mA
EN Rising Threshold	$V_{EN,R}$		1.1	1.2	1.3	V
EN Falling Threshold	$V_{EN,F}$		0.8	0.9	1	V
Internal Soft-start Time	t_{SS}	SS pin floating	0.7	1.6	3.2	ms
Soft-start Charging Current	I_{SS}		4	5	6	μA
Soft-start Done Threshold	V_{SS}			1		V
Switching Frequency Program Range	$f_{SW,RNG}$	R_{FS}=83.3k~250k	200		600	kHz
Switching Frequency Setting Accuracy	f_{SW}	R_{FS}=100kΩ	430	500	570	kHz
Minimum ON Time	$t_{ON,MIN}$	(Note 4)		120	150	ns
Minimum OFF Time	$t_{OFF,MIN}$	(Note 4)		80	120	ns

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Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Clock Sync Input Voltage High	$V_{SYNC,H}$		1.5			V
Clock Sync Input Voltage Low	$V_{SYNC,L}$				0.8	V
Clock Sync Input Duty	D_{CLK}		20		80	%
Power Good Threshold	V_{PG}	V_{FB} falling, PG from high to low	87	91	94	$\%V_{REF}$
		V_{FB} rising, PG from low to high	90	93	97	$\%V_{REF}$
Power Good Delay Time	$t_{PG,R}$	Low to high (Note 4)		200		μs
	$t_{PG,F}$	High to low (Note 4)		20		μs
Power Good Output Low	$V_{PG,L}$	I_{PG}=2mA			0.3	V
OUT Pin Over Voltage Protection Threshold	$V_{OUT,OVP1}$		22		26	V
Output Over Voltage Protection Threshold	$V_{OUT,OVP2}$	V_{FB} rising	115	120	125	$\%V_{REF}$
Output OVP Delay	$t_{OVP,DLY}$	(Note 4)		15		μs
Output Under Voltage Protection Threshold	V_{UVP}	V_{FB} falling	40	50	60	$\%V_{REF}$
Output UVP Delay	$t_{UVP,DLY}$	(Note 4)		200		μs
Thermal Shutdown Temperature	T_{SD}		150	160	170	°C
Thermal Shutdown Hysteresis	T_{HYS}			15		°C
Average Current Regulation Range	$V_{ISP} - V_{ISN}$		48	55	62	mV

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θ_{JA} is measured in the natural convection at T_A = 25°C on a four-layer Silergy Evaluation Board.

Note 3: The device is not guaranteed to function outside its operating conditions.

Note 4: Based on simulation result.

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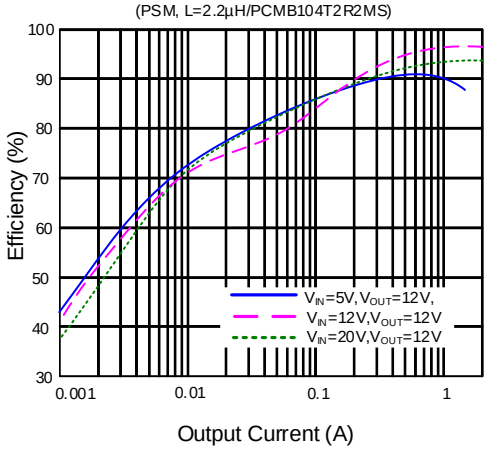
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Typical Performance Characteristics

(fsw=500kHz, T_A=25°C)

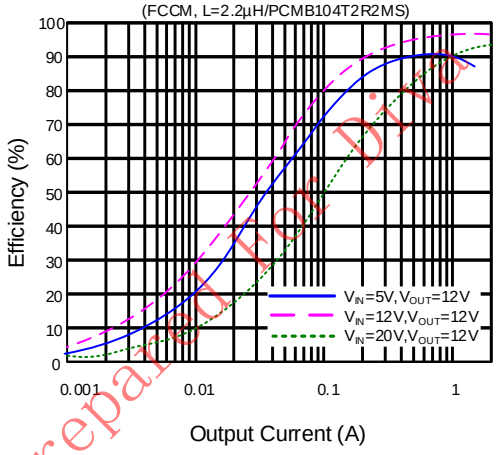
Efficiency vs. Output Current

(PSM, L=2.2µH/PCMB104T2R2MS)

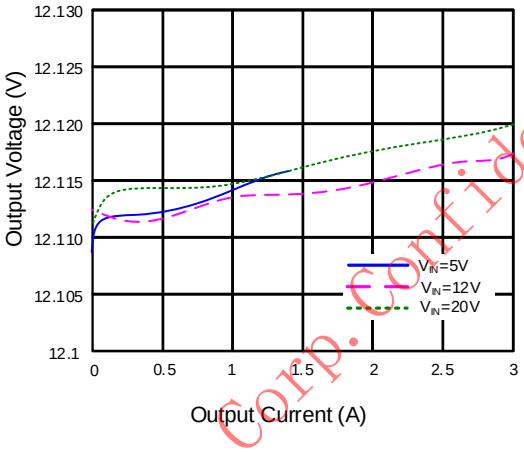


Efficiency vs. Output Current

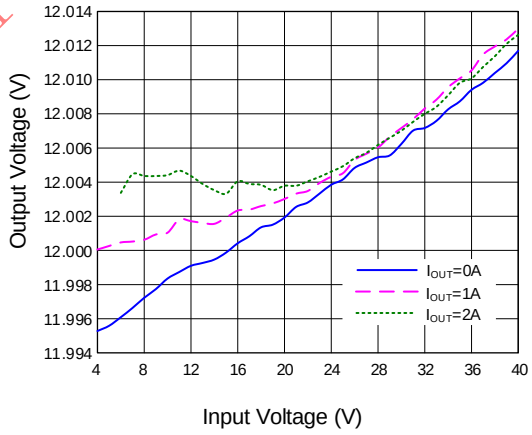
(FCCM, L=2.2µH/PCMB104T2R2MS)



Output Voltage vs. Output Current

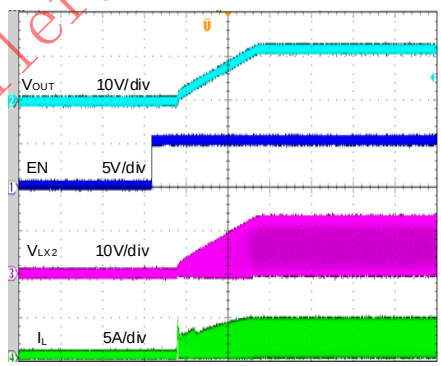


Output Voltage vs. Input Voltage



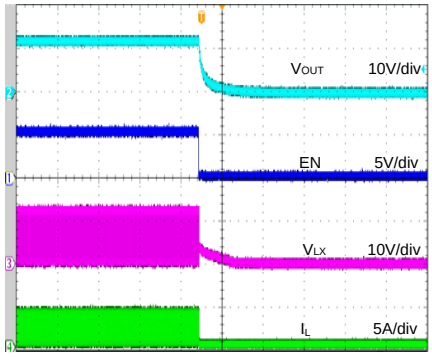
Startup from Enable

(V_{IN}=20V, V_{OUT}=12V, R_{LOAD}=6Ω)



Shutdown from Enable

(V_{IN}=20V, V_{OUT}=12V, R_{LOAD}=6Ω)

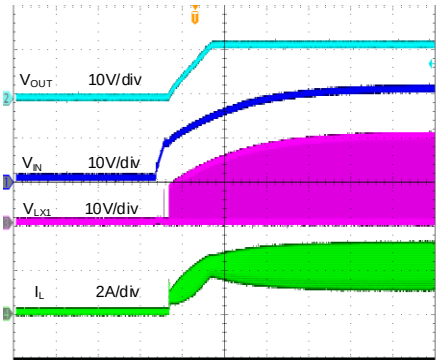


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Startup from V_{IN}

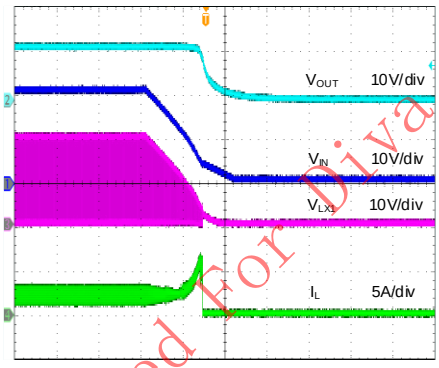
(V_{IN}=20V, V_{OUT}=12V, R_{LOAD}=6Ω)



Time (2ms/div)

Shutdown from V_{IN}

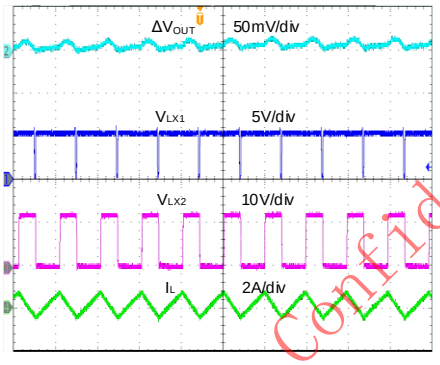
(V_{IN}=20V, V_{OUT}=12V, R_{LOAD}=6Ω)



Time (800μs/div)

Output Ripple

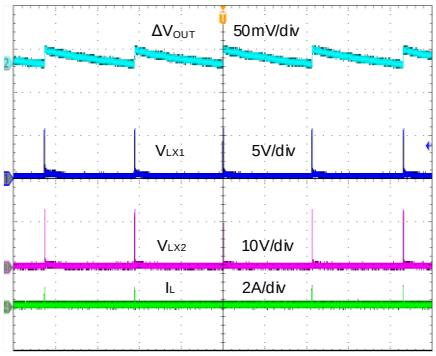
(V_{IN}=5V, V_{OUT}=12V, I_{OUT}= 0A, FCCM)



Time (2μs/div)

Output Ripple

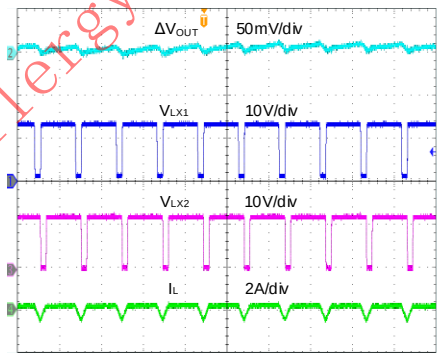
(V_{IN}=5V, V_{OUT}=12V, I_{OUT}= 0A, PSM)



Time (200μs/div)

Output Ripple

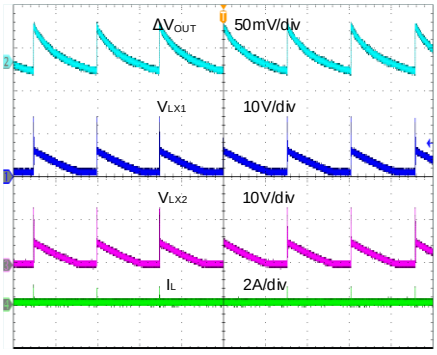
(V_{IN}=12V, V_{OUT}=12V, I_{OUT}= 0A, FCCM)



Time (2μs/div)

Output Ripple

(V_{IN}=12V, V_{OUT}=12V, I_{OUT}= 0A, PSM)

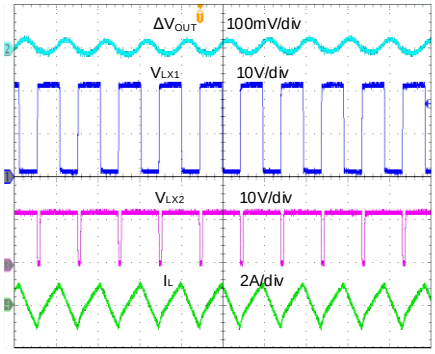


Time (800μs/div)

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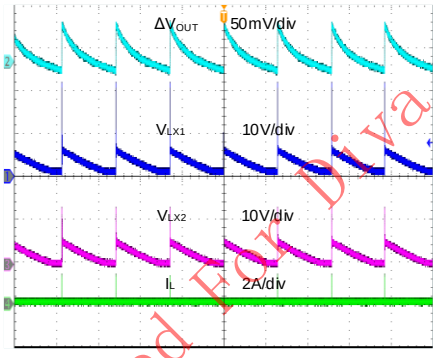
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Output Ripple
(V_{IN}=20V, V_{OUT}=12V, I_{OUT}= 0A, FCCM)



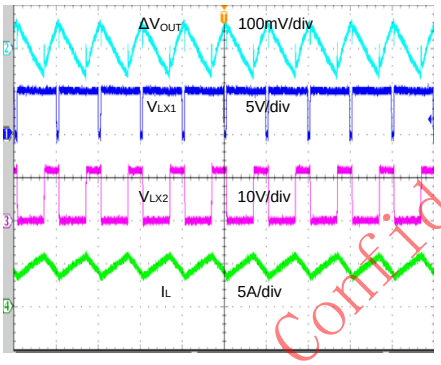
Time (2μs/div)

Output Ripple
(V_{IN}=20V, V_{OUT}=12V, I_{OUT}= 0A, PSM)



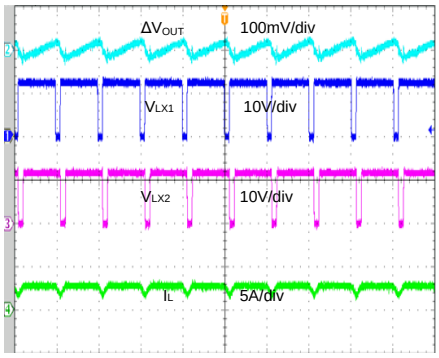
Time (800μs/div)

Output Ripple
(V_{IN}=5V, V_{OUT}=12V, I_{OUT}= 1.5A)



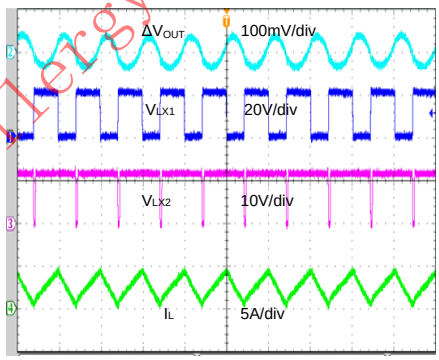
Time (2μs/div)

Output Ripple
(V_{IN}=12V, V_{OUT}=12V, I_{OUT}= 2A)



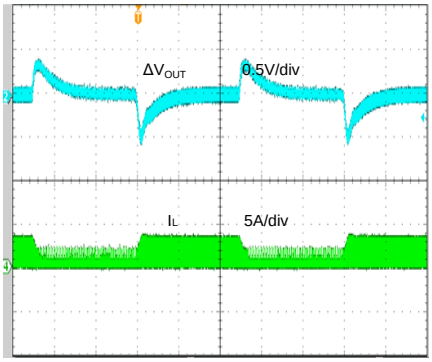
Time (2μs/div)

Output Ripple
(V_{IN}=20V, V_{OUT}=12V, I_{OUT}= 2A)



Time (2μs/div)

Load Transient
(V_{IN}=20V, V_{OUT}=12V, I_{OUT}=0.1A ~ 1A)



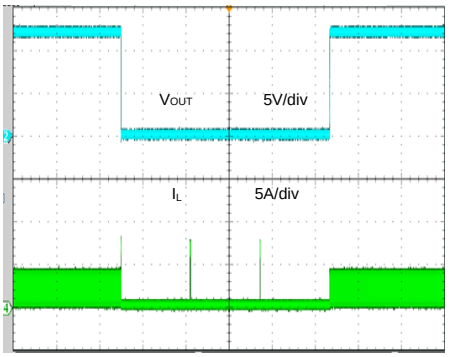
Time (200μs/div)

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Short Circuit Protection

(V_{IN}=20V, V_{OUT}=12V, R_{LOAD}=6Ω)



Time (2s/div)

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Application Information

Input Under-voltage Lock-out

To prevent operation before all internal circuitry is ready and to ensure that the power and synchronous rectifier switches may be sufficiently enhanced, the IC incorporates input under-voltage lock-out (UVLO) protection. The device remains in a low current state and all switching is inhibited until V_{IN} exceeds V_{UVLO}, the input UVLO (rising) threshold. At that time, if EN is enabled, the device will start-up by initiating a soft-start ramp. If V_{IN} falls below V_{UVLO} less the UVLO hysteresis, switching will be suppressed again.

Enable Control

The EN input is a high-voltage capable input with logic-compatible threshold. When EN is driven above 1.3V normal device operation will be enabled. When driven < 0.8V the device will be shut down, reducing input current to typical 1μA. In applications where EN is pulled high to the power input V_{IN}, a 10kΩ to 100kΩ resistor should be added between power input and EN.

Soft-start

The SA22307 provides an external soft-start pin to smoothly ramp the output to the desired voltage whenever the device enabled. The soft-start time can be programmed by external capacitor connected between SS pin and GND, as given in equation (1).

$$t_{ss}(ms)=C_{SS}(nF)\times\frac{1V}{5\mu A} \quad (1)$$

Leave SS pin open for default 1.6ms soft-start.

External Bootstrap Capacitor Connection

This device integrates a floating power supply for the gate driver that operates the high-side power switch. Proper operation requires a 100nF low ESR ceramic capacitor to be connected between BS1 and LX1, BS2 and LX2. This bootstrap capacitor provides the gate driver supply voltage for the high-side N-channel power MOSFET switch. Do not connect a resistor in series with the bootstrap capacitor.

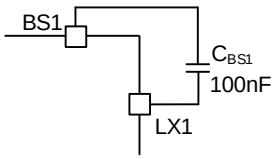


Fig. 3. External Bootstrap Capacitor Connection

VCC Linear Regulator

An internal 3.3V linear regulator (VCC) provides the power supply for the internal gate drivers, PWM logic, analog circuitry, and other blocks. Connect a minimum of 1μF low ESR ceramic capacitor from VCC to GND.

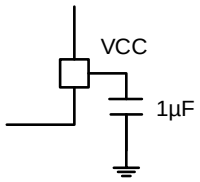


Fig. 4. VCC Regulator

Feedback Resistor Selection

Choose R1 and R2 to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R1 and R2. A value of between 10kΩ and 100kΩ is highly recommended for both resistors. The output voltage VOUT is programmed by external voltage divider with the 1V internal voltage reference as given in equation (2).

$$V_{OUT}=1V\times\frac{R_1+R_2}{R_2} \quad (2)$$

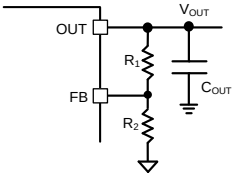


Fig. 5. V_{OUT} Programming

Light Load Operation Mode

PSM or force-PWM light load operation is selected by SYNC/MODE pin. Pull SYNC/MODE pin low or floating for PSM operation, and connect this pin to VCC or external clock for force-PWM operation.

Adjustable Switching Frequency and Synchronization

The FS pin can be used to set the switching frequency of the device by connecting a resistor R_{FS} between this pin and GND. The switching frequency is programmable from 200kHz to 600kHz, as given in equation (3). The switching frequency can also be synchronized to external clock by applying a clock signal to the SYNC/MODE pin.

$$f_S(kHz)=\frac{50000}{R_{FS}(k\Omega)} \quad (3)$$

Peak Inductor Current Limit

The device incorporates a cycle-by-cycle peak current limit. Inductor current is measured in SW1 when it is on. If the current exceeds the current limit, both SW1 and SW3 turn off, and SW2 and SW4 turn on.

Reverse Inductor Current Limit

The device incorporates reverse inductor current limit under force-PWM mode. Inductor current is measured in SW4 when it is on. If the reverse current exceeds the current limit, SW4 turn off, and SW3 turn on.

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Average Output Current Limit

The SA22307 provides output current limit function by sensing the voltage drop between ISP and ISN pins (as shown in fig.1). The value of the limit voltage between the ISP and the ISN pins is 55mV. The current sense resistor (R_{SENSE}) between the ISP and ISN pins should be selected to ensure that the output current limit is set high enough for output. The output current limit setting resistor is given by Equation (4). Short the ISP to the ISN and then connect to OUT pin if this function is not used.

$$R_{SENSE} = \frac{V_{LIM_SENSE}}{I_{OUT_LIMIT}} \quad (4)$$

Where V_{LIM_SENSE} is the current limit setting voltage between the ISP and ISN pins. I_{OUT_LIMIT} is the desired output current limit.

Short-circuit Protection

If V_{OUT} < 50% of the set-point continuously for approximately 200μs, the short-circuit protection mode will be initiated, and the device will shut down for about 2.6s. The device will then restart and keep working for about 2.4ms. If the short circuit condition remains, another 'hiccup' cycle of shutdown and restart will continue indefinitely.

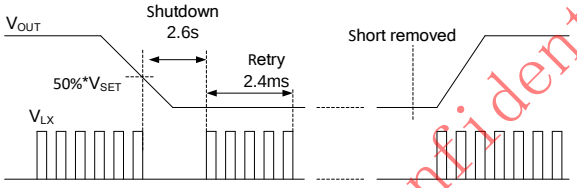


Fig. 6. Description of Short-circuit Protection

Output Over-voltage Protection (OVP)

This device includes output over-voltage protection (OVP). If the output voltage rises above the feedback regulation level, SW1 and SW3 turn off and the synchronous rectifier turns on. If the output voltage remains high the SW2 and SW4 remain on until the inductor current reaches zero. If the output voltage continues to rise and exceeds the output over- voltage threshold for more the 15μs, the output over-voltage protection mode is triggered. The device resumes regulation once the overvoltage condition is removed.

Over-temperature Protection (OTP)

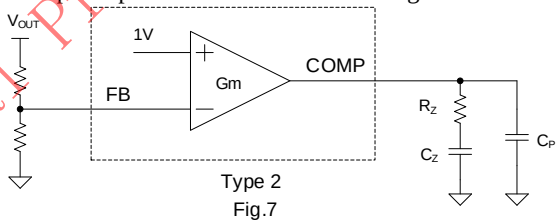
SA22307 includes over-temperature protection (OTP) circuitry to prevent over heating due to excessive power dissipation. This will shut down switching operation when the junction temperature exceeds 160°C. Once the junction temperature cools down by approximately 15°C the IC will resume normal operation after a complete soft-start cycle. For continuous operation, provide adequate cooling so that the junction temperature does not exceed the OTP threshold.

Loop Compensation

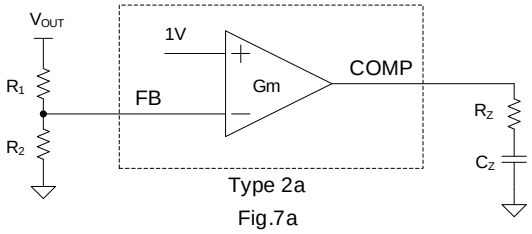
The SA22307 incorporates average current control scheme. The inner current loop uses internal compensation. The outer loop, voltage loop, is compensated with external components.

The IC operates in buck mode or boost mode. Therefore, both buck and boost operating modes require loop compensations. The restrictive one of both compensations is selected as the overall compensation from a loop stability point of view. Typically for a converter designed either work in buck mode or boost mode, the boost mode compensation design is more restrictive due to presence of a right half plan zero (RHPZ).

In most applications, a Type 2 or Type 2a compensation network as show in Fig.7 and Fig.7a can be used to stabilize the voltage loop. The Type 2 is the most widely used and works fine for power stages lagging down to -90˚ and where the converter brought by the output capacitor ESR must be canceled. Type 2a is used where the output capacitor ESR effect can be neglected.



Type 2
Fig.7



Type 2a
Fig.7a

To calculate the value of external components for the outer voltage loop, follow the following steps.

1. Select the crossover frequency fc of the closed loop. It is recommended that the crossover frequency is chosen 1/5 of right half plane zero (f_{RHPZ}) and 1/10 of switching frequency for the tradeoff of stability and transient response of the system. The system has faster response at higher crossover frequency. For boost mode:

$$f_{RHPZ} = \frac{(1-D)^2 \times V_{OUT}}{2\pi \times L \times I_{OUT}} \quad (5)$$

2. Select a Rz value of the R-C series combination connected to the COMP pin.

$$R_Z = \frac{V_{OUT}}{G_m \times G_{fc} \times V_{REF}} \quad (6)$$

Where G_m is the error amplifier trans-conductance, which is typically 88uS; G_{fc} is gain of the power stage at crossover frequency.

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$$G_{fc} = \frac{(1-D)}{2\pi \times fc \times C_{OUT} \times R_S} \quad (7)$$

Where Rs is the current sense gain, which is typically 100mΩ.

3. Select a Cz value of the R-C series combination connected to the COMP pin. The compensation zero decides phase margin at the crossover frequency. Place a compensation zero at or before the dominant pole of R_L and C_{OUT}. R_L is the load resistance.

$$C_Z = \frac{R_L \times C_{OUT}}{R_Z} \quad (8)$$

4. A high frequency pole is recommended to attenuate the high frequency noise. Place this pole to cancel the ESR zero of C_{OUT}

$$C_P = \frac{R_{ESR} \times C_{OUT}}{R_Z} \quad (9)$$

Input Capacitor C_{IN}

In the buck mode, the input capacitor supplies high ripple current. The RMS current in the input capacitor is calculated as:

$$I_{CIN_RMS} = I_{OUT} \times \sqrt{D \times (1\text{-}D)} \quad (10)$$

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor close to the IN and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and IN/GND pins. For most applications, a 22μF low ESR ceramic capacitor is recommended.

Output Capacitor C_{OUT}

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For most applications, it is recommended to use more than 66μF capacitance with X5R or better grade ceramic capacitor. The capacitance derating with DC voltage must be considered.

Inductor Selection

For the Buck-Boost converter, the inductor must support buck applications with the maximum input voltage and boost applications with the minimum input voltage. The critical inductance values for buck mode is calculated with Equation (11):

$$L_{BUCK} = \frac{V_{OUT} \times (1 - V_{OUT}/V_{IN,MAX})}{f_{SW} \times \Delta I_L} \quad (11)$$

Where ΔI_L is the peak-to-peak inductor ripple current, and it is about 30% to 50% of the maximum output current.

The critical inductance for boost mode is calculated with Equation (12) and Equation (13):

$$L_{BOOST} = \frac{V_{IN,MIN} \times (V_{OUT} - V_{IN,MIN})}{V_{OUT} \times f_{SW} \times \Delta I_L} \quad (12)$$

$$I_{IN,MAX} = \frac{V_{OUT} \times I_{OUT}}{V_{IN,MIN} \times \eta} \quad (13)$$

Where η is the efficiency, and ΔI_L is the peak-to-peak inductor ripple current, it is about 30% to 50% of the maximum input current ($I_{IN,MAX}$). The recommended minimum inductor values are either L_{BUCK} or L_{BOOST} whichever is higher.

In addition to the inductance value, the inductor must support the peak current based on Equation (14) and Equation (15) to avoid saturation:

$$I_{PEAK\text{-}BUCK} = I_{OUT} + \frac{V_{OUT} \times (1 - V_{OUT}/V_{IN,MAX})}{2 \times f_{SW} \times L} \quad (14)$$

$$I_{PEAK\text{-}BOOST} = \frac{V_{OUT} \times I_{OUT}}{V_{IN,MIN} \times \eta} + \frac{V_{IN,MIN} \times (V_{OUT} - V_{IN,MIN})}{2 \times V_{OUT} \times f_{SW} \times L} \quad (15)$$

Choosing a larger inductance reduces the ripple current but also increase the size of the inductor and reduces the achievable bandwidth of the converter by moving the right half-plane zero to lower frequency. The appropriate balance should be chosen based on the application requirements

Layout Design

For the best efficiency and minimum noise problem, we should place the following components close to the IC: C_{IN}, C_{VCC}, C_{OUT}, C_{BS}, L, R_{TOP} and R_{BOT}.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve the best thermal and noise performance. If the board space allowed, a ground plane is highly desirable. Reasonable vias are suggested to be placed underneath the ground pad to enhance the soldering quality and thermal performance.

2) The decoupling capacitor of VIN must be placed close enough to the IN pin and GND pin. The loop area formed by the input capacitors, IN pin and GND pins must be minimized.

3) The decoupling capacitor of VOUT also must be placed close enough to the OUT pin and GND pin. The loop area formed by the output capacitors, OUT pin and GND pins also must be minimized.

4) BS pin is sensitive. Bootstrap cap must be placed between BS and LX as close as possible.

5) To prevent the circulating currents in the ground plane from disrupting operation of the regulator, all small-signal grounds should return to GND by a separation way. This main includes the ground

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connection for the FB pin resistor and the feedback network.

6) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the IN pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1MΩ resistor between the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

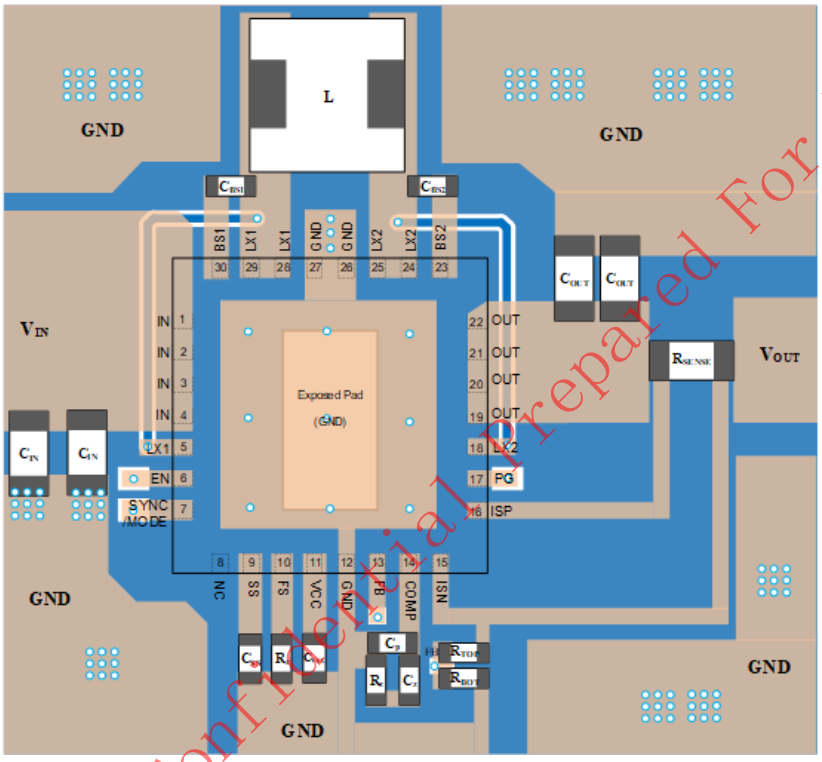
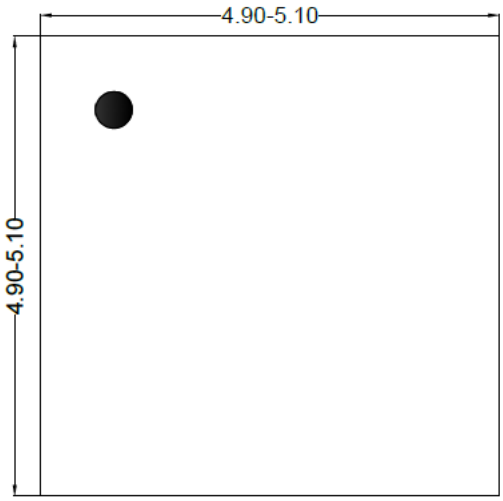


Figure8. PCB Layout Suggestion

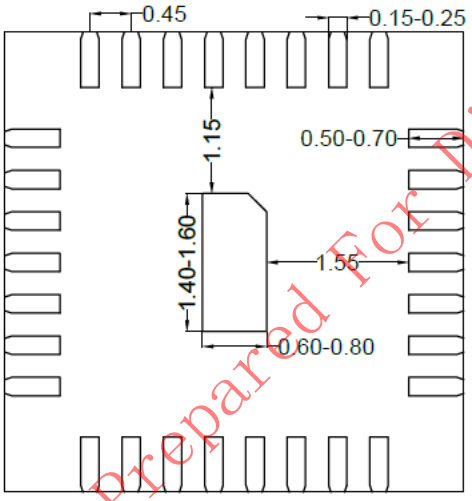
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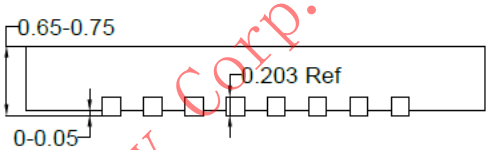
QFN5×5-30 Package Outline Drawing



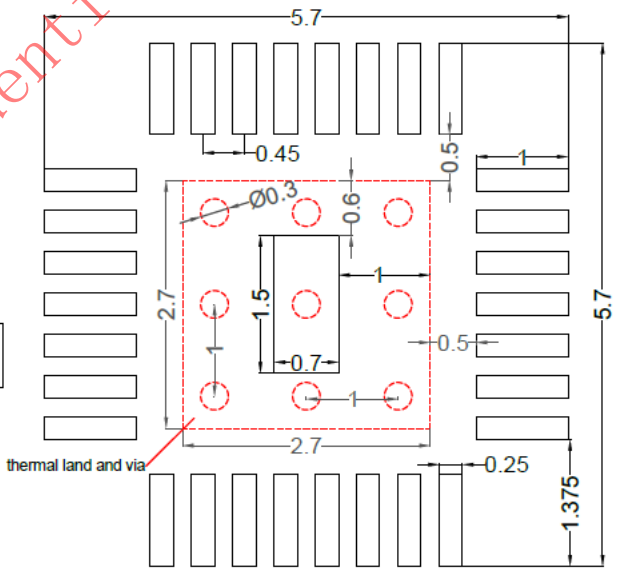
Top View



Bottom View



Front View



Recommended PCB layout
(Reference only)

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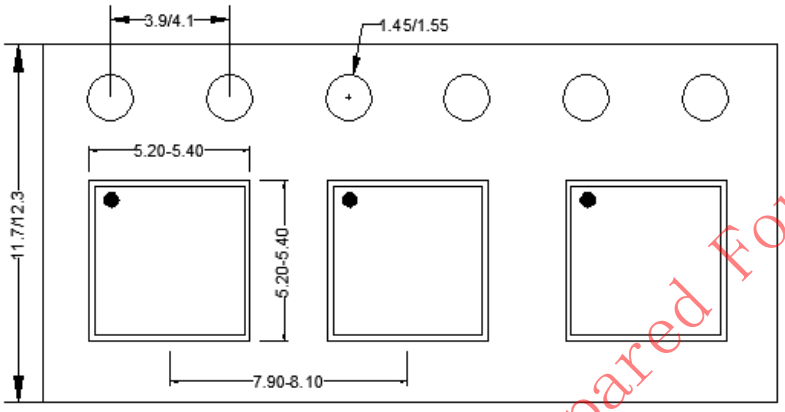
Notes: **All dimension in millimeter and exclude mold flash & metal burr.**

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Taping & Reel Specification

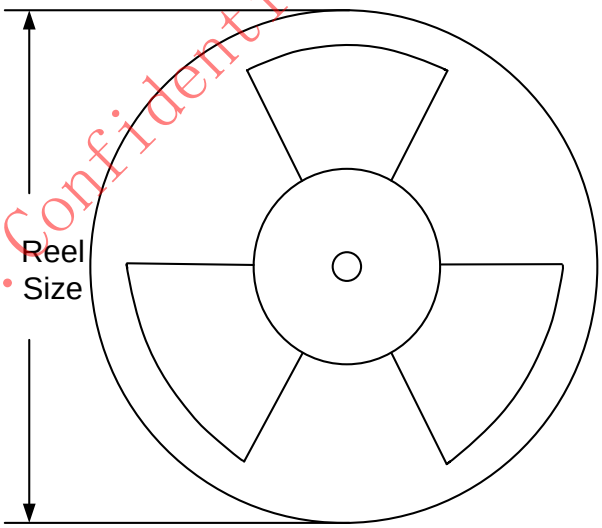
1. Taping orientation

QFN5×5



Feeding direction →

2. Carrier Tape & Reel specification for packages



Package type	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Trailer length(mm)	Leader length (mm)	Qty per reel
QFN5×5	12	8	13"	400	400	5000

3. Others: NA

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Revision History

The revision history provided is for informational purpose only and is believed to be accurate, however, not warranted. Please make sure that you have the latest revision.

Date	Revision	Change
June 13, 2025	Revision 1.0A	Add the following description to the BS2/BS1 pin description (Page3) and the **External Bootstrap Capacitor Connection** application information (page 10): ---- Do not connect a resistor in series with the capacitor.
July 17, 2024	Revision 1.0	1. Update the Block Diagram (page 3); 2. Update the Peak Inductor Current Limit description (page 10); 3. Modify the Short Circuit Protection cycle (page 11)
Aug.01, 2022	Revision 0.9	Initial Release

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