GS12270 SDI/HDMI Bridge Datasheet

The GS12270 is a fully featured SDI/HDMI bridge chip for SDI link conversion applications. The GS12270 can be hardware configured to operate in one of three modes: SDI to HDMI Bridge Mode, HDMI to SDI Bridge Mode, or SDI Gearbox Mode.

Description

The device fully supports SDI interface standards from HD-SDI (ST 292) to UHD-SDI at 12Gb/s (ST 2082-1), including all Multi-Link SDI standards at these rates. When configured for HDMI bridging, the GS12270 fully supports the HDMI 2.0 standard (up to 4Kp60 4:4:4 format). The color space and subsampling conversion feature of the GS12270 allows all the formats support.

The G12270 is the ideal solution for chip-to-chip connectivity using TMDS signaling for UHDTV products requiring a 12Gb/s UHD-SDI interface. For example, add a 12Gb/s UHD-SDI input interface to a UHDTV monitor simply by adding the GS12270 in SDI to HDMI Mode, with TMDS connection directly into off-the-shelf image processing ASICs.

For applications requiring multi-channel audio, the GS12270 includes a full 16-channel audio de-embedding and embedding feature. Up to 16 channels of digital audio at 48kHz sampling, or up to 8 channels at 96kHz sampling, can be extracted from the input video, and output on dedicated balls in AES/EBU or I2S serial digital formats. Existing audio is also simultaneously re-embedded in the selected output interface format. Users may also choose to insert up to 8 channels of new audio using dedicated audio input balls.

In HDMI to SDI Mode, the GS12270 can extract all HDMI InfoFrames, including HDR meta data. Video payload information is automatically converted to SMPTE ST 352 packets. Similarly, in SDI to HDMI Mode, SDI SMPTE ST 352 packets are extracted and converted to equivalent InfoFrames. All InfoFrame and ancillary data packets can be read via the GSPI host interface. Users can also choose to insert new SDI ancillary data packets via the GSPI.

In SDI Gearbox Mode, the device will automatically reorder the output serial stream according to the received ST 352 packets, and may also duplicate outputs to unused serial output ports, or route any input channel to an unused output.

The device will also automatically compensate for up to 400ns of skew between Multi-Link SDI inputs. This aids in any lane-to-lane variance introduced by cable mismatch or upstream routing and distribution equipment.

Its small package and low power operation make the device ideal for adding UHD-SDI interfaces to existing HDMI 2.0 based UHDTV products, and for low-cost SDI/HDMI converters and extenders.

Key Features

- Fully standards compliant SDI interface bridging to and from HDMI 2.0
  - Support for 4K video formats up to 60Hz at 10-bit 4:2:2 and 8-bit 4:4:4 sampling
- Converts between Single-Link and Multi-Link SDI interfaces from HD-SDI to 12Gb/s UHD-SDI
- Supports up to 16 channels of digital audio de-embedding and embedding at 48kHz or 96kHz
  - Simultaneous de-embedding and embedding in all modes of operation
- Dedicated AES/EBU or I2S serial digital audio inputs and outputs
- Extraction and insertion of HDMI InfoFrames
- Extraction and insertion of SDI ancillary data packets
- Extraction and insertion of Time Code (TC) data packets
- Automatic and manual handling of SMPTE ST 352 packets
- Automatic skew compensation for multi-link SDI inputs
- Automatic input link order handling for multi-link SDI inputs
- Four 100Ω differential inputs with input trace equalization up to 12dB
- Four 100Ω differential outputs with individually selectable output swing adjust

Improvements Compared to GS12170

- Added color space and sub-sampling conversion, allowing full support of the HDMI 2.0 standard
- Enhanced HDMI video input change and format detection (based on video timings, not only on 5V and InfoFrames)
- Enhanced HDMI output EDID read, 5V and SCDC management
- Added the following 3G SDI conversion support:
  - Data structure 1 (1080p50/59/60 YUV 422 10bit) Level B to Level A (S2H and S2S modes of operation)
  - Data structure 2-4 Level B to Level A
- Added HD-SDI ST352 PID packet absence detection support to automatically switch to flywheel format detection in that case
- Added pattern generator support for all 3 modes of operation
- Added automatic transfer support of audio channel status words and HDR packets between HDMI and SDI
- Added support for the following insertions while video is unchanged (applicable to S2S mode of operation)
  - Audio insertion
  - Time code insertion

Performance

For optimal SDI performance, the GS12270 is designed to interface directly with Semtech's UHD-SDI equalizers and cable drivers. For HDMI connectivity, the TMDS inputs and outputs are designed for direct chip-to-chip connectivity. The device can be connected to physical HDMI connectors using an HDMI re-driver device.

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GS SDI/HDMI Bridge

Applications

- UHDTV monitors & displays
- UHDTV cameras & camcorders
- SDI/HDMI converters
- HDMI extenders
- SDI I/O adapters

Peripheral Interface

- Gennum Serial Peripheral Interface (GSPI) serial control and monitoring interface

General

- Package: 11mm x 11mm 325 ball TFBGA (0.5mm pitch, variable)
- Pb-free, Halogen-free, RoHS / WEEE compliant

Functionality

- Three different modes of operation

Mode of Operation	Inputs	Outputs
SDI to HDMI Bridge	SL, DL or QL SDI	HDMI
HDMI to SDI Bridge	HDMI	SL, DL or QL SDI
SDI to SDI Gearbox	SL, DL or QL SDI	SL, DL or QL SDI

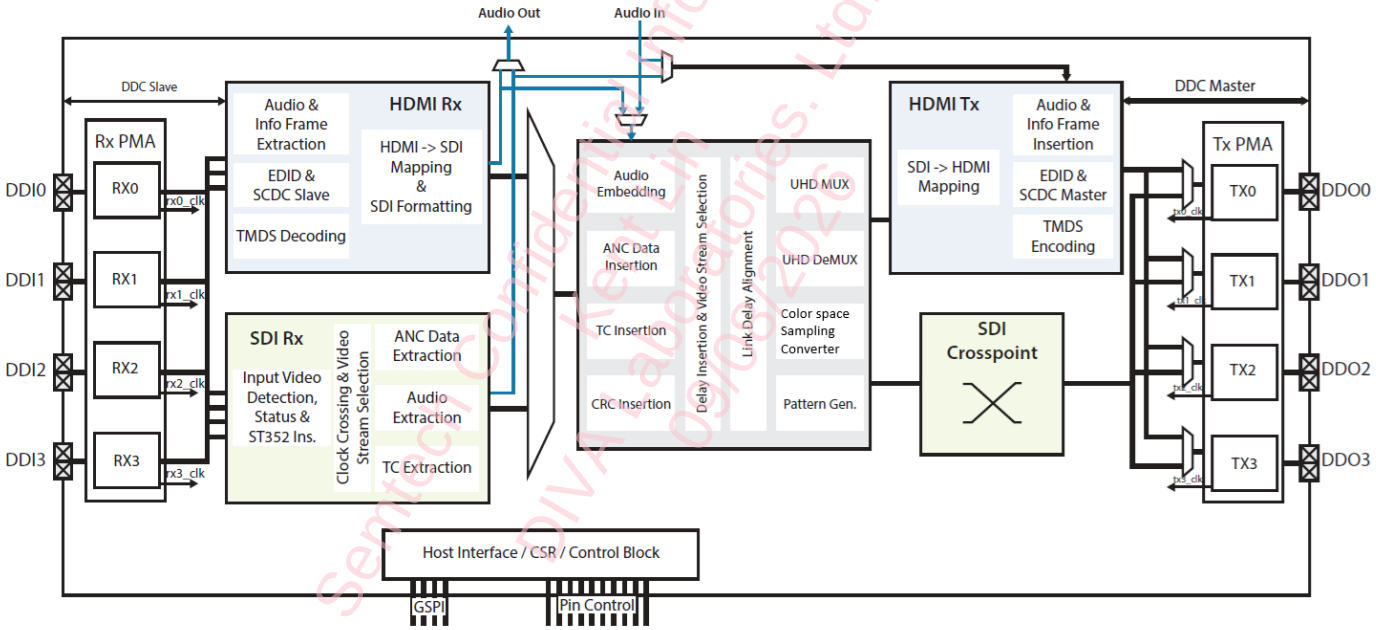

Figure A: Functional Block Diagram

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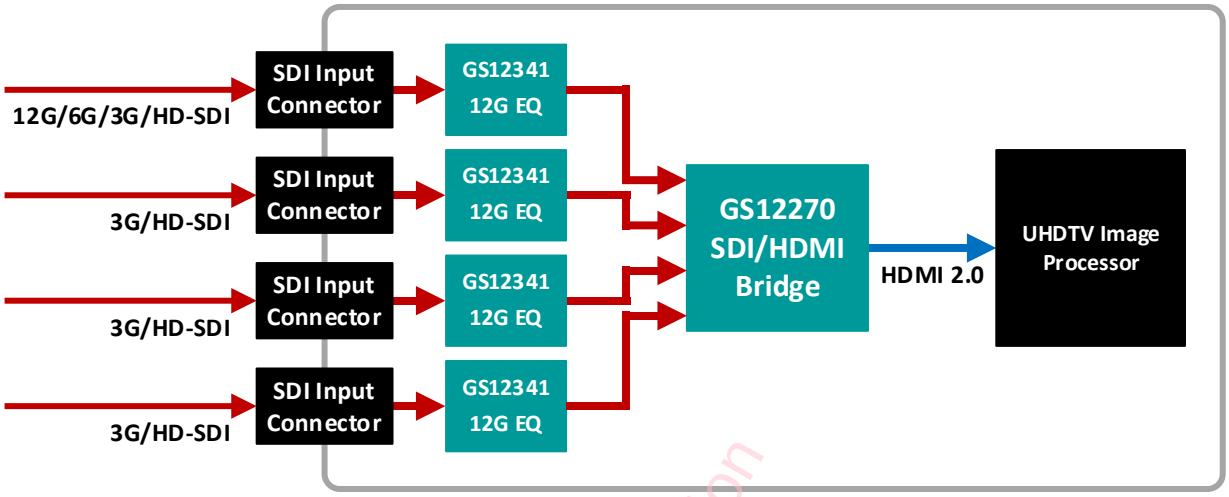

Figure B: GS12270 UHDTV Monitor Application

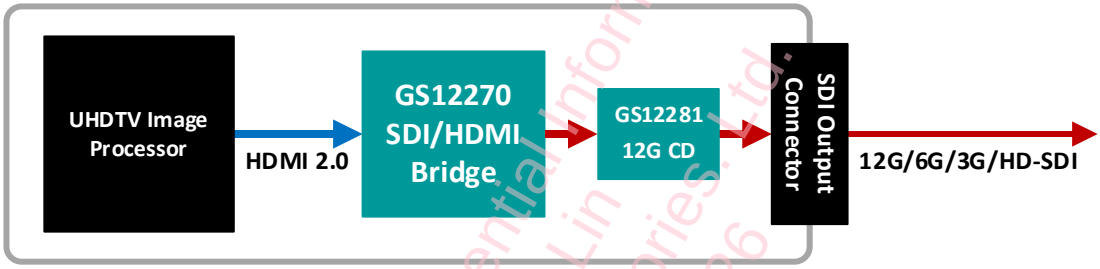

Figure C: GS12270 UHDTV Camcorder Application

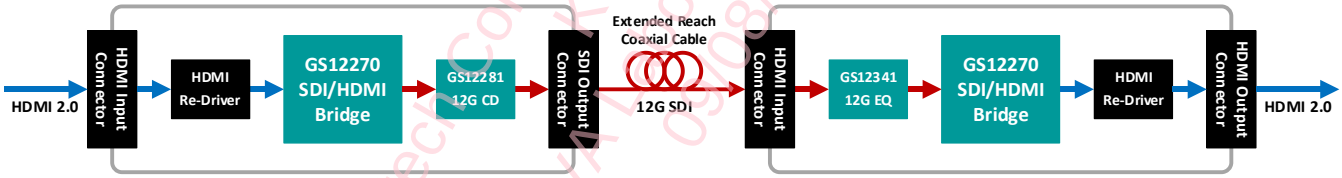

Figure D: GS12270 UHDTV HDMI Extender Application

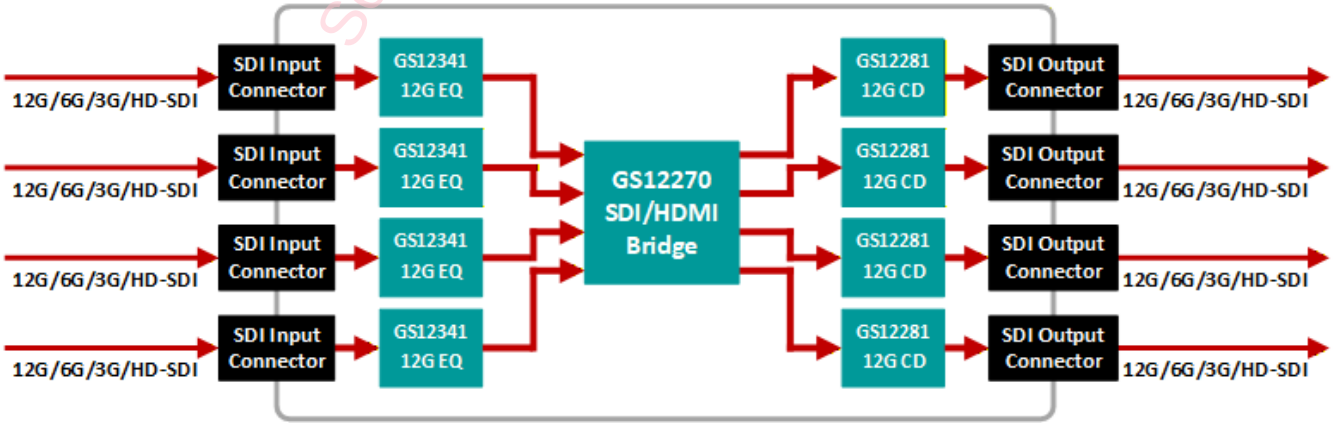

Figure E: SDI to SDI Gearbox

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Revision History

Version	ECO	PCN	Date	Changes and/or Modifications
0.2	080413	—	July 2026	Reversed the DDO pins index order, see Figure 1-1: Ball Assignment. This affects SDI output directly when the device is in HDMI to SDI or SDI to SDI modes and the default mapping to the HDMI output TMDS lanes when the device is in SDI to HDMI mode, see section 3.3.4 HDMI Transmitter. Renamed pin D15 from SYS_CLK_P to SYS_CLK and pin C16 from SYS_CLK_N to UNUSED (SYS_CLK is not differential). Renamed pin E13 from UNUSED to LPRB_A and pin D13 from UNUSED to LPRB_B (reserved for internal use, do not connect). Modified A_IN*/WCLK_IN*/A_CLK_IN* pins description to add mention to connect to ground instead of do not connect if audio input is unused. Fixed typo in Table 3-1: Configuration Mode Selection CONF_MODE index (first column CONF_MODE_0 instead of CONF_MODE_1 and vice versa for second column). Updated section 2.1 Absolute Maximum Ratings. Added section 2.2 Recommended Operating Conditions. Added section 2.5 Power Consumption.
0.1	078951	—	March 2026	New document.

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Contents

1. Ball Out 8
   1.1. Ball Assignment 8
   1.2. Ball Descriptions 9
2. Electrical Characteristics 16
   2.1. Absolute Maximum Ratings 16
   2.2. Recommended Operating Conditions 17
   2.3. Thermal Characteristics 18
   2.4. DC Electrical Characteristics 18
   2.5. Power Consumption 19
   2.6. AC Electrical Characteristics 20
   2.7. Latency 21
3. Detailed Description 22
   3.1. Configuration Modes 22
      3.1.1. Initialization on Power-up 22
   3.2. Serial Data Inputs 24
      3.2.1. Serial Inputs 24
      3.2.2. SDI Receiver 26
      3.2.3. HDMI Receiver 31
   3.3. Serial Data Outputs 33
      3.3.1. Serial Outputs 33
      3.3.2. Transmitter (Tx) Reference Clock 36
      3.3.3. SDI Transmitter 36
      3.3.4. HDMI Transmitter 37
   3.4. SDI to SDI Configuration 38
      3.4.1. SDI-SDI Mode Functions 38
      3.4.2. Operational Mode Selection 38
      3.4.3. Multiplex Mode 39
      3.4.4. Demultiplex Mode 47
      3.4.5. Bypass Mode 54
      3.4.6. Payload ID Handling 55
      3.4.7. Data Rate Selection in Gearbox Mode 62
      3.4.8. Output Assignment 63
      3.4.9. PI Clock Selection 64
      3.4.10. SDI SMPTE Data Rates and Source Image Formats Supported 65
   3.5. SDI-HDMI Configuration 68
      3.5.1. SDI-HDMI Mode Functions 69
      3.5.2. SDI Inputs 69
      3.5.3. Output Format Selection 70
      3.5.4. SDI-HDMI Output Loop Bandwidth 75
      3.5.5. Handling of Audio 75
      3.5.6. Handling of ANC Data 78
      3.5.7. InfoFrames 78
      3.5.8. DDC, HPD, and Output Ready 81
   3.6. HDMI-SDI Configuration 82
      3.6.1. HDMI-SDI Mode Functions 82
      3.6.2. DDC, EDID and HPD 83
      3.6.3. HDMI Data Rate Detection 84
      3.6.4. HDMI Receiver 84
      3.6.5. Output Format Selection 85
      3.6.6. Handling of Audio 86
      3.6.7. Handling of ANC Data 87
      3.6.8. PID Calculation 87

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09/08/2026

3.6.9. InfoFrames 87
3.7. SDI Audio Embedding 88
3.7.1. Audio Register Offset 88
3.7.2. Input Data Stream Selection 89
3.7.3. Audio Embedding Operating Modes 89
3.7.4. Serial Audio Data Inputs 90
3.7.5. Serial Audio Data Format Support 91
3.7.6. Audio Packet Detection and Deletion 93
3.7.7. Audio Word Clock 93
3.7.8. Channel & Group Activation 94
3.7.9. Audio Crosspoint 94
3.7.10. Frame Sequence Detection 94
3.7.11. ECC Error Detection and Correction 95
3.7.12. Audio Control Packet Embedding 95
3.7.13. Audio Data Packet Embedding 96
3.7.14. Audio Mute 97
3.7.15. Audio Channel Status 97
3.7.16. Audio Interrupt Control 97
3.8. SDI Audio De-Embedding 98
3.8.1. Audio Register Offset 98
3.8.2. Input Data Stream Selection 98
3.8.3. Serial Audio Data Output Signals 98
3.8.4. Serial Data Format Support 100
3.8.5. Audio Processing 102
3.8.6. Error Reporting 107
3.8.7. Audio Interrupt Control 107
3.9. ANC Data Processing 108
3.9.1. ANC Data Detection 108
3.9.2. ANC Data Deletion 109
3.9.3. ANC Data Extraction 109
3.9.4. ANC Data Insertion 110
3.10. Time Code (TC) Processing 112
3.10.1. Time Code Insertion 112
3.10.2. Time Code Extraction 112
3.11. STAT Balls 112
3.12. Reference Clock 115
3.13. Digital I/O 116
3.14. Power Supply Considerations 116
3.14.1. Power Connections 116
3.14.2. Power On Sequence 116
3.14.3. Device Initialization 116
3.15. GSPI Host Interface 116
3.15.1. CTRL_CSB Ball 116
3.15.2. CTRL_SDIN Ball 117
3.15.3. CTRL_SDOUT Ball 117
3.15.4. CTRL_SCLK Ball 118
3.15.5. Command Word 1 Description 119
3.15.6. GSPI Transaction Timing 120
3.15.7. Single Read/Write Access 121
3.15.8. Auto-increment Read/Write Access 123
3.15.9. Setting a Device Unit Address 123
3.15.10. Default GSPI Operation 123
4. Host Interface Register Map 125

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4.1. Control Registers 125
4.1.1. Audio Register Offset 125
4.2. Register Descriptions 129
4.2.1. GS12270 Control and Status Registers 129
4.2.2. Rx Control and Status Registers 198
4.2.3. Tx Control and Status Registers 202
4.2.4. Pattern Generator Control Registers 208
4.2.5. SDI Audio De-Embedding Control Registers 211
4.2.6. SDI Audio Embedding Control Registers 225
4.2.7. HDMI Rx Control Registers 237
4.2.8. HDMI Tx Control Registers 266
4.2.9. ANC Insertion Control Registers 297
4.2.10. ANC Insertion Memory Control and Status Registers 303
4.2.11. ANC Extraction Control and Status Registers 304
4.2.12. ANC Extraction Memory Control and Status Registers 347
5. Applications Information 348
5.1. Typical Application Circuits 348
5.1.1. Power Pins 348
5.1.2. SDI-to-SDI Configuration 348
5.1.3. SDI-to-HDMI Configuration 348
5.1.4. HDMI-to-SDI Configuration 348
5.2. Programming via SPI or JTAG Interface 348
5.3. Power Supply 349
5.3.1. Power Supply Decoupling 349
5.3.2. Power Supply Sequencing 349
6. Package and Ordering Information 350
6.1. Package Dimensions 350
6.2. Marking and Ordering Information 351

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1. Ball Out

1.1. Ball Assignment

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21
A	VSS	UART_RX	UART_TX	ISP0_N	ISP1_N	VSS	FLASH_CSB	FLASH_SDOUT	FLASH_IO_CFG_INTF	FLASH_SPI_EN	VSS	RESET_N	TX_PI_EXT	I2C_SDA	I2C_SCL	VSS	EXT_PLL_REF_CLK_P	UNUSED	UNUSED	DDI_REF_CLK_OUT_P	VSS
B	ANC_SI_DATA	ANC_SI_VALID	VDDI2	ISP2_N	ISP3_N	CTRL_CSB	CTRL_SDOUT	VDDI2	RSVD	FLASH_SDIN	CTRL_SDIN	UNUSED	VDDI2	UNUSED	UNUSED	RX_CLK_2	EXT_PLL_REF_CLK_N	VDDI2	DDI_REF_CLK_OUT_N	UNUSED	UNUSED
C	ANC_SI_CLK	STAND BY				CTRL_SPI_EN					LINK_ASGMT_SEL					SYS_CLK_N				VSS	VSS
D	ACLK_IN_2	VDDI4		VSS	UNUSED	DDC_DATA	DDC_CLK	TMS	VSS	TCK	REF_CLK_MUX_0	REF_CLK_MUX_1	UNUSED	VSS	SYS_CLK_P	RX_CLK_0	UNUSED	UNUSED		DDO3_N	DDO3_P
E	UNUSED	A_IN_15_16		UNUSED	SDI_INPUT_SELECT	VDDAUX2	CTRL_SCLK	TDO	TDI	DEVRST_N	VDDI2	UNUSED	UNUSED	UNUSED	UNUSED	VDDI2	UNUSED	UNUSED		XCVR_VREF	VSS
F	VSS	A_IN_13_14	WCLK_IN_2	SEC_LINK_EN	HPD												VDDAUX2	A1	XCVR_VREF	DDI0_N	DDI0_P
G	A_IN_11_12	A_IN_9_10		UNUSED	VDDI4		VDD25	VDDAUX2	FLASH_SCLK	TRSTB	VDDI3	UNUSED	VDDAUX2	VSS	VDD25		UNUSED	A0		VDDA	VSS
H	UNUSED	VDDI4		UNUSED	UNUSED		VSS								VDD		VSS	VSS		DDI1_P	DDI1_N
J	UNUSED	UNUSED		VSS	ACLK_IN_1		VDDAUX4		VSS	VDDI3	VSS	VDD	VSS		VSS		UNUSED	UNUSED		VDDA	VSS
K	UNUSED	UNUSED		UNUSED	UNUSED		UNUSED		VDD	VSS	VDD	VSS	VDD		VDD		VDD_XCVR_CLK	VSS		DDO2_P	DDO2_N
L	VSS	A_IN_7_8	WCLK_IN_1	UNUSED	VDDI4		UNUSED		VSS	VDD	VSS	VDD	VSS		VSS		DDO_REF_CLK_N	DDO_REF_CLK_P	VDDA25	VDDA25	VSS
M	A_IN_5_6	A_IN_3_4		UNUSED	UNUSED		VDDAUX4		VDD25	VSS	VDD	VSS	VDD		VDD		VDD_XCVR_CLK	VSS		DDO1_P	DDO1_N
N	A_IN_1_2	VDDI0		VSS	UNUSED		UNUSED		VSS	VDD	VSS	VDD	VSS		VSS		DDI_REF_CLK_P	DDI_REF_CLK_N		VDDA	VSS
P	UNUSED	UNUSED		UNUSED	UNUSED		VDD18								VDD18		VSS	VSS		DDI2_P	DDI2_N
R	UNUSED	UNUSED		UNUSED	VDDI0		VDD25	VSS	UNUSED	VDD18	UNUSED	VDDI1	UNUSED	VDD18	VDD25		SYS_CLK_OUT_P	SYS_CLK_OUT_N		VDDA	VSS
T	VSS	SD_BYPASS0	SD_BYPASS1	SD_BYPASS2	SD_BYPASS3												UNUSED	UNUSED	VSS	DDI3_N	DDI3_P
U	CONF_MODE_1	BYPASS		UNUSED	UNUSED	VDDI0	UNUSED	UNUSED	UNUSED	UNUSED	VDDI1	UNUSED	UNUSED	ACLK_OUT	UNUSED	VDDI1	UNUSED	UNUSED		VDDA	VSS
V	CONF_MODE_0	VDDI0		VSS	EXT_PLL_LOCK	HDMI_5V_EN	MUX_DEMUX_N	UNUSED	VSS	UNUSED	UNUSED	UNUSED	UNUSED	VSS	AMCLK	UNUSED	UNUSED	SLAVE_MCLK		DDO0_N	DDO0_P
W	STAT7	STAT6				GB_MODE_SEL2					UNUSED					UNUSED				VSS	VSS
Y	STAT5	STAT0	VDDI0	GB_MODE_SEL0	GB_MODE_SEL1	WCLK_OUT_1	WCLK_OUT_2	VDDI1	A_OUT_9_10	UNUSED	A_OUT_5_6	A_OUT_3_4	VDDI1	UNUSED	UNUSED	UNUSED	DEBUG_6	VDDI1	DEBUG_3	DEBUG_1	DEBUG_0
AA	VSS	STAT3	STAT2	STAT1	STAT4	VSS	A_OUT_15_16	A_OUT_13_14	A_OUT_11_12	A_OUT_1_2	VSS	A_OUT_7_8	UNUSED	UNUSED	UNUSED	VSS	DEBUG_7	DEBUG_5	DEBUG_4	DEBUG_2	VSS

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High-speed differential inputs
Clock Inputs/Outputs
1.8V supply
1.8V I/O supply
High-speed differential outputs
Audio Input
2.5V supply
2.5V I/O aux supply
Reference clock
Audio Output
1.05V TX RX supply
GND
Digital control and status
1.05V VDD core supply
2.5V TX RX PLL and ref clk buffer supply
RESET

Figure 1-1: Ball Assignment

1.2. Ball Descriptions

Table 1-1: Ball Descriptions

Pin Number	Name	Type	Description
A1, A11, A16, A21, A6, AA1, AA11, AA16, AA21, AA6, C16, C20, C21, D14, D4, D9, E21, F1, G14, G21, H17, H18, H7, J11, J13, J15, J21, J4, J9, K10, K12, K18, L1, L11, L13, L15, L21, L9, M10, M12, M18, N11, N13, N15, N21, N4, N9, P17, P18, R21, R8, T1, T19, U21, V14, V4, V9, W20, W21	VSS	Power	Device ground. Connect to GND.
N2, R5, U6, V2, Y3	VDDI0	Power	Power Supply connection for the IO circuits in bank 0. Connect to 1.8V. [1]
R12, U11, U16, Y13, Y18, Y8	VDDI1	Power	Power Supply connection for the IO circuits in bank 1. Connect to 1.8V. [1]
B13, B18, B3, B8, E11, E16	VDDI2	Power	Power Supply connection for the IO circuits in bank 2. Connect to 1.8V. [1]
G11, J10	VDDI3	Power	Power Supply connection for the IO circuits in bank 3. Connect to 1.8V. [1]
D2, G5, H2, L5	VDDI4	Power	Power Supply connection for the IO circuits in bank 4. Connect to 1.8V. [1]
E6, F17, G13, G8	VDDAUX2	Power	Auxiliary supply for I/O circuits. Connect to 2.5V. [1]
J7, M7	VDDAUX4	Power	Auxiliary supply for I/O circuits. Connect to 2.5V. [1]
G20, J20, N20, R20, U20	VDDA	Power	Power supply connection for the transceiver Tx and Rx lanes. Connect to 1.05V. [1]
L19, L20	VDDA25	Power	Power supply connection for the transceiver PLL. Connect to 2.5V. [1]
H15, J12, K11, K13, K15, K9, L10, L12, M11, M13, M15, N10, N12	VDD	Power	Power supply connection for the core, 1.05V. [1]
P15, P7, R10, R14	VDD18	Power	Power for programming and HSIO receiver. HSIO auxiliary power supply. Connect to 1.8V. [1]
G15, G7, M9, R15, R7	VDD25	Power	Power for corner PLLs and PNVM. Connect to 2.5V. [1]
K17, M17	VDD_XCVR_CLK	Power	Provides common power to all transceiver reference clock buffers. Connect to 2.5V. [1]
E20, F19	XCVR_VREF	—	These balls are not used. Pull down through a 10k resistor.
B9	RESERVED	—	These balls are not used. Do not connect.

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Pin Number	Name	Type	Description
A18, A19, AA13, AA14, AA15, B12, B14, B15, B20, B21, D17, D18, D5, E1, E12, E14, E15, E17, E18, E4, J17, J18, G12, G17, G4, H1, H4, H5, J1, J2, K1, K2, K4, K5, K7, L4, L7, M4, M5, N5, N7, P1, P2, P4, P5, R1, R11, R13, R2, R4, R9, T17, T18, U10, U12, U13, U15, U17, U18, U4, U5, U7, U8, U9, V10, V11, V12, V13, V16, V17, V8, W11, W16, Y10, Y14, Y15, Y16	UNUSED	—	These balls are not used. Do not connect.
AA17, Y17, AA18, AA19, Y19, AA20, Y20, Y21	DEBUG [7:0]	Digital Input/ Output	These balls are reserved for internal use. Do not connect.
E13 D13	LPRB_A LPRB_B	Digital Input/ Output	These balls are reserved for internal use. Do not connect.
A7	FLASH_CSB	Digital Input/ Output	Internal flash SPI chip select.
A9	FLASH_IO_CFG_INTG	Digital Input	Must be pulled down through a resistor or driven to 0 from an external source to indicate the shared SPI interface is a target.
G9	FLASH_SCLK	Digital Input/ Output	Internal flash SPI clock.
B10	FLASH_SDIN	Digital Input	Internal flash SPI data input.
A8	FLASH_SDOUT	Digital Output	Internal flash SPI data output.
A10	FLASH_SPI_EN	Digital Output	Internal flash SPI Enable. 0: FLASH_SDOUT is tri-state 1: FLASH _SDOUT is output This ball has an internal pull-down resistor.
A2	UART_RX	Digital Input	UART RX. Reserved for future use. This ball has an internal pull-down resistor. When the UART interface is not used, this ball should be left open (do not connect).
A3	UART_TX	Digital Output	UART TX. Reserved for future use. When the UART interface is not used, this ball should be left open (do not connect).
A15	I2C_SCL	Bidirectional	Control I2C clock. Could be used as optional alternative instead of CTRL_SPI of the GSPI interface. Reserved for future use. This ball has an internal pull-up resistor. When the I2C interface is not used, this ball should be left open (do not connect).

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Pin Number	Name	Type	Description
A14	I2C_SDA	Bidirectional	Control I2C data. Could be used as optional alternative instead of CTRL_SPI of the GSPI interface. Reserved for future use. This ball has an internal pull-up resistor. When the I2C interface is not used, this ball should be left open (do not connect).
G18 F18	A0 A1	Digital Input	Used to select 2 LSB of I^2C register slave address. These balls have an internal pull-down resistor.
V1 U1	CONF_MODE_O CONF_MODE_1	Digital Input	Sets configuration mode. See Section 3.1 Configuration Modes and Table 3-1: Configuration Mode Selection. These balls have an internal pull-down resistor.
V7	MUX_DEMUX_N	Digital Input	Selects between Multiplex and Demultiplex Mode. This ball has an internal pull-down resistor. This function can be overridden by the CSR. See 3.4.2 Operational Mode Selection and Table 3-17: Operational Mode Selection.
U2	BYPASS	Digital Input	When HIGH, BYPASS is active and all inputs pass data directly to the outputs. This ball has an internal pull-down resistor. This function can be overridden by the CSR. See Section 3.4.5 Bypass Mode.
T5, T4, T3, T2	SD_BYPASS [3:0]	Digital Input	Selects the SD data rate per channel when in Bypass Mode. SD_BYPASS is only available when BYPASS is set to 1. These balls have an internal pull-down resistor. This function can be overridden by the CSR.
W6, Y5, Y4	GB_MODE_SEL [2:0]	Digital Input	Multiplex or De-multiplex Gearbox Mode selection. These balls have internal pull-up resistors. This function can be overridden by the CSR. See Table 3-19: MUX Mode SMPTE Compatibility for details when in the MUX operation mode. See Table 3-21: DEMUX Mode Down Conversion for details when in the DEMUX operation mode.
N17 N18	DDI_REF_CLK_P DDI_REF_CLK_N	Input	Input SERDES Reference clock. SDI to HDMI: • Must be connected to a 148.5MHz oscillator (internal digital system clock is derived from that clock) HDMI to SDI: • Must be connected to TMDS clock from HDMI input SDI to SDI: • Must be connected to a 148.5MHz oscillator (internal digital system clock is derived from that clock)
A20 B19	DDI_REF_CLK_OUT_P DDI_REF_CLK_OUT_N	Output	Forwarding DDI_REF_CLK_P/N. When not used, these ball should be left open (do not connect).
T21, T20 P20, P21 H20, H21 F21, F20	DDI3_P, DDI3_N DDI2_P, DDI2_N DDI1_P, DDI1_N DDI0_P, DDI0_N	Input	High-speed, differential serial inputs. When not used, these balls should be left open (do not connect).

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Pin Number	Name	Type	Description
L18 L17	DDO_REF_CLK_P DDO_REF_CLK_N	Input	Output SERDES Reference clock. SDI to HDMI: • leave unconnected HDMI to SDI: • must be connected to a 148.5MHz oscillator (internal digital system clock is derived from that clock) SDI to SDI: • leave unconnected
D21, D20 K20, K21 M20, M21 V21, V20	DDO3_P, DDO3_N DDO2_P, DDO2_N DDO1_P, DDO1_N DDO0_P, DDO0_N	Output	High-speed, differential serial outputs.
D16 B16	RX_CLK_0 RX_CLK_2	Output	The extracted parallel clock from the respective DDI_P/DDI_N inputs. It is possible to MUX the clock extracted from Rx0 and Rx1 to RX_CLK_0 and from Rx2 and Rx3 to RX_CLK_2. When not used, these ball should be left open (do not connect).
E10	DEVRST_N	Input	The DEVRST_N assertion results in full re-initialization of the device. Active low. During the assertion of DEVRST_N, the state of I/Os (Input/Output pins) enters a high-impedance state (tri state). Drive the signal with a POR chip or an external device and keep the DEVRST_N asserted until the system/clocks are stable and the chip is properly powered up. This ball has an internal pull-up resistor.
D11 D12	REF_CLK_MUX_0 REF_CLK_MUX_1	Digital Input	Controls multiplexers used for Tx common reference clock selection. These balls have internal pull-down resistors.
Y2 AA4 AA3 AA2 AA5 Y1 W2 W1	STAT0 STAT1 STAT2 STAT3 STAT4 STAT5 STAT6 STAT7	Digital Output	Multi-function status outputs.
C11	LINK_ASGMT_SEL	Digital Input	Multi-link input order handling. When HIGH the input order is independent of the input connection order (based on ST 352 embedded PID). When LOW, the output is multiplexed based on the physical input connection order. This ball has an internal pull-down resistor. This function can be overridden by the CSR.
A12	RESET_N	Digital Input	Active LOW, device wide reset signal. This ball has an internal pull-up resistor.
D8	TMS	Digital Input	JTAG interface Test Mode Select input. This ball has an internal pull-up resistor. **Note:** This ball can be left unconnected if not used.

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Pin Number	Name	Type	Description
E9	TDI	Digital Input	JTAG interface Test Data Input in ATPG or test mode, when using a 4-bit TDI bus this I/O is used as TDI[0]. This ball has an internal pull-up resistor. **Note:** This ball can be left unconnected if not used.
E8	TDO	Digital Output	JTAG interface Test Data Output. **Note:** This ball can be left unconnected if not used.
D10	TCK	Digital Input	JTAG interface Test Clock input. **Note:** This ball must be pulled down if not used.
G10	TRSTB	Digital Input	JTAG interface Test Reset. This ball has an internal pull-up resistor. Must be held low during device operation.
F4	SEC_LINK_ENABLE	Digital Input	When HIGH the secondary paths for DL-SL MUX/DEMUX will be enabled. This function can be overridden by the CSR. This ball has an internal pull-down resistor.
E5	SDI_INPUT_SELECT	Digital Input	Select between DDI0 and DDI2 in the SL input modes or DDI0 and DD1 and DDI2 and DD3 for DL input modes. This function can be overridden by the CSR. This ball has an internal pull-down resistor.
A13	TX_PI_EXT	Input	Tx PI input clock. The input clock has to be synchronized to the extracted Rx clock. Tie to VSS if not used.
B6	CTRL_CSB	Digital Input	Chip Select input for the GSPI interface. Active low. This ball has an internal pull-up resistor.
E7	CTRL_SCLK	Digital Input	GSPI Data Clock input.
B11	CTRL_SDIN	Digital Input	GSPI Digital Data Input for the GSPI interface.
B7	CTRL_SDOUT	Digital Output	GSPI Digital Data Output for the GSPI interface.
C6	CTRL_SPI_EN	Digital Input	Control SPI Enable. 0: CTRL_SDOUT is tri-state 1: CTRL_SDOUT is output This ball has an internal pull-down resistor.
A4	ISP0_N	Digital Input	Dual function input: Loss of signal in SDI-SDI and SDI-HDMI modes. HDMI_SINK_5V in HDMI-SDI mode. Active low. This ball has an internal pull-down resistor.
A5	ISP1_N	Digital Input	Dual function input: Loss of signal for DDI1 in SDI-SDI and SDI-HDMI modes. SEL_EXT_EDID in HDMI-SDI mode. Setting it to HIGH will disable the internal EDID in the GS12270. Active low. This ball has an internal pull-down resistor. Both functions can be overridden through corresponding registers.
B4 B5	ISP2_N ISP3_N	Digital Input	Loss of signal. Set LOW when the input signal is valid. When HIGH the input section is in Standby Mode in order to minimize power consumption. Active low. These balls have internal pull-down resistors. These balls can be overridden by the CSR. **Note:** N12 and N13 have no function in HDMI-SDI mode.
A17 B17	EXT_PLL_REF_CLK_P EXT_PLL_REF_CLK_N	Differential Output	The differential clock output frequency locked to the TMDS clock.

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Pin Number	Name	Type	Description
V5	EXT_PLL_LOCK	Digital Input	Lock signal from the external PLL. This ball has an internal pull-down resistor.
F5	HPD	Digital Input/ Output	Hot Plug Detect, input or output depending on the mode. No function, do not connect in SDI-SDI Mode.
V6	HDMI_5V_EN	Output	Used to enable 5V on HDMI cable when in SDI-HDMI Mode, high-impedance otherwise.
D6	DDC_DATA	Bidirectional	DDC data (I^2C data), master or slave. Configuration mode balls select between master (SDI-HDMI) and slave (HDMI-SDI).
D7	DDC_CLK	Bidirectional	DDC clock (I^2C clock), master or slave. Configuration mode balls select between master (SDI-HDMI) and slave (HDMI-SDI).
C1	ANC_SI_CLK	Digital Output	Clock for ANC serial interface.
B1	ANC_SI_DATA	Digital Output	Data output for ANC serial interface.
B2	ANC_SI_VALID	Digital Output	Data valid output for ANC serial interface.
N1 M2 M1 L2	A_IN_1_2 A_IN_3_4 A_IN_5_6 A_IN_7_8	Digital Input	Serial Audio input; Channels 1 and 2. Serial Audio input; Channels 3 and 4. Serial Audio input; Channels 5 and 6. Serial Audio input; Channels 7 and 8. When the Audio input is not used, these balls should be connected to ground.
L3	WCLK_IN_1	Digital Input	Word clock associated to channels 1-8 at the Audio Core 1. When the Audio input is not used, this ball should be connected to ground.
J5	ACLK_IN_1	Digital Input	Audio sampling clock associated to channels 1-8 at the Audio Core 1. When the Audio input is not used, this ball should be connected to ground.
G2 G1 F2 E2	A_IN_9_10 A_IN_11_12 A_IN_13_14 A_IN_15_16	Digital Input	Serial Audio input; Channels 9 and 10. Serial Audio input; Channels 11 and 12. Serial Audio input; Channels 13 and 14. Serial Audio input; Channels 15 and 16. Inputs 9-16 are not active at 96kHz sample rate. Leave unconnected if unused. When the Audio input is not used, these balls should connected to ground.
F3	WCLK_IN_2	Digital Input	Word clock associated to channels 9-16 at the Audio Core 2. When the Audio input is not used, this ball should be connected to ground
D1	ACLK_IN_2	Digital Input	Audio sampling clock associated to channels 9-16. When the Audio input is not used, this ball should be connected to ground
AA10 Y12 Y11 AA12	A_OUT_1_2 A_OUT_3_4 A_OUT_5_6 A_OUT_7_8	Digital Output	Serial Audio output; Channels 1 and 2. Serial Audio output; Channels 3 and 4. Serial Audio Output; Channels 5 and 6. Serial Audio Output; Channels 7 and 8.
Y6	WCLK_OUT_1	Digital Output	Word clock associated to channels 1-8.

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Pin Number	Name	Type	Description
Y9 AA9 AA8 AA7	A_OUT_9_10, A_OUT_11_12, A_OUT_13_14, A_OUT_15_16	Digital Output	Serial Audio output; Channels 9 and 10. Serial Audio output; Channels 11 and 12. Serial Audio Output; Channels 13 and 14. Serial Audio Output; Channels 15 and 16. Outputs 9-16 are not active at 96kHz sample rate.
Y7	WCLK_OUT_2	Digital Output	Word clock associated to channels 9-16 (disabled for 96kHz sample rate).
U14	ACLK_OUT	Digital Output	Audio sampling clock associated with all channels.
V15	AMCLK	Digital Output	Audio Master Clock, selectable 24.576, 12.288 and 6.144MHz.
V18	SLAVE_MCLK	Digital Input	Input clock at 1x or 2x MCLK, locked to AMCLK, used to reduce jitter on audio clock and data outputs. When not used, this ball should be pulled down.
C2	STANDBY	Digital Input	This ball will put the GS12270 into power save mode. This ball has an internal pull-down resistor.
D15	SYS_CLK	Input	Optional 27MHz clock. When unused, SYS_CLK must be pulled down.
R17 R18	SYS_CLK_OUT_P SYS_CLK_OUT_N	Output	Buffered version of 27MHz reference clock.

Notes:

1. See polarfire_fpga_packaging_and_pin_descriptions_ug0722_v12.pdf.

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2. Electrical Characteristics

2.1. Absolute Maximum Ratings[1,2]

Table 2-1: Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
FPGA core power supply	V_{DD}	-0.5	1.13	V
Transceiver Tx and Rx lanes supply	V_{DDA}	-0.5	1.13	V
Programming and HSIO receiver supply	V_{DD18}	-0.5	2.0	V
FPGA core and FPGA PLL high-voltage supply	V_{DD25}	-0.5	2.7	V
Transceiver PLL high-voltage supply	V_{DDA25}	-0.5	2.7	V
Transceiver reference clock supply	$V_{DD_XCVR_CLK}$	-0.5	3.6	V
Global VREF for transceiver reference clocks	$XCVR_{VREF}$	-0.5	3.6	V
GPIO DC I/O supply[3]	V_{DDIx}	-0.5	3.6	V
Dedicated I/O DC supply for JTAG and SPI	V_{DDI3}	-0.5	3.6	V
GPIO auxiliary power supply for I/O bank x[3]	V_{DDAUXx}	-0.5	3.6	V
Maximum DC input voltage on GPIO	V_{IN}	-0.5	3.8	V
Transceiver receiver absolute input voltage	Transceiver V_{IN}	-0.5	1.41	V
Transceiver reference clock absolute input voltage	Transceiver REFCLK V_{IN}	-0.5	3.6	V
Storage Temperature	T_{STG}	-65	150	°C
Junction Temperature	T_J	-55	135	°C
Maximum soldering temperature RoHS	$T_{SOLROHS}$	—	260	°C

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[1] Refer to Microchip's PolarFire® FPGA Datasheet DS00003831. In case of discrepancy with DS00003831, information from DS00003831 prevails.

[2] Absolute maximum ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the recommended operating conditions specified in Table 4-2. Recommended Operating Conditions is not implied. Stresses beyond those listed in the following table might cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[3] The power supplies for a given I/O bank x are shown as VDDIx and VDDAUXx.

2.2. Recommended Operating Conditions[4]

Table 2-2: Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
FPGA core power supply (1.05V mode)[5,6]	V_{DD}	1.02	1.05	1.08	V
Transceiver Tx and Rx lanes supply (1.05V mode)[1,6]	V_{DDA}	1.02	1.05	1.08	V
Programming and HSIO receiver supply[6]	V_{DD18}	1.71	1.80	1.89	V
FPGA core and FPGA PLL high-voltage supply[6]	V_{DD25}	2.425	2.5	2.575	V
Transceiver PLL high-voltage supply[6]	V_{DDA25}	2.425	2.5	2.575	V
Transceiver reference clock supply[6,7,8]	$V_{DD_XCVR_CLK}$	2.375	2.5	2.625	V
Global VREF for transceiver reference clocks[9]	$XCVR_{VREF}$	—	GND	—	V
GPIO DC I/O supply[6,10]	V_{DDIx}	1.71	1.8	1.89	V
Dedicated I/O DC supply for JTAG and SPI[6,10,11]	V_{DDI3}	1.71	1.8	1.89	V
GPIO auxiliary power supply for I/O bank x[6,10,11,12]	V_{DDAUXx}	2.375	2.5	2.625	V
Junction Temperature[13]	T_J	0	—	100	°C

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[4] Refer to Microchip's PolarFire® FPGA Datasheet DS00003831. In case of discrepancy with DS00003831, information from DS00003831 prevails.

[5] VDD and VDDA must operate at 1.05V nominal to achieve required timing and transceiver lane rate.

[6] The recommended power supply tolerances include DC offset of the supply plus any power supply ripple over the customer design frequencies of interest, as measured at the device package pins. An example for a valid power supply that meets the recommendations for the VDD supply is 1.0V ±10 mV or 1.05V ±10 mV for DC offset with an additional power supply ripple of ±20 mV for a total of 1.0V ±30 mV or 1.05V ±30 mV.

[7] Both VDDA and VDD_XCVR_CLK supplies must be powered when any of the transceivers are used. VDD_XCVR_CLK must power on within the XCVR calibration time. VDDA and VDD_XCVR_CLK must both then remain powered during operation. If VDDA needs to be powered down, VDD_XCVR_CLK must also be powered down. There is no required sequence for powering up or down VDDA and VDD_XCVR_CLK.

[8] $V_{DD_XCVR_CLK}$ must operate at 2.5V nominal.

[9] $XCVR_{VREF}$ is unused and must be pulled low through a 10k to prevent noise hits on the pad.

[10] V_{DDIx} must operate at 1.8V nominal.

[11] At power-up and power-down, the VDDIx and VDDAUXx supply sequencing can cause signal glitches. Refer to PolarFire Family User I/O User Guide and UG0726: PolarFire FPGA Board Design User Guide for detailed explanation and recommended steps.

[12] Supported V_{DDIx} is 1.8V nominal in which case VDDAUXx per I/O bank must be powered at 2.5V nominal.

2.3. Thermal Characteristics

Refer to Microchip's PolarFire® FPGA Datasheet DS00003831.

2.4. DC Electrical Characteristics

Refer to Microchip's PolarFire® FPGA Datasheet DS00003831.

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2.5. Power Consumption

Tables below show typical power consumption in different configurations, no margins were added, subject to change with firmware updates.

Table 2-3: Power – SDI to HDMI, 4 x 12G SDI SL IN, 6G HDMI OUT

Parameter	Symbol	Condition	Typ	Unit
FPGA core power supply	I_{DD}	1.05V	1213	mA
Transceiver Tx and Rx lanes supply	I_{DDA}	1.05V	212	mA
Programming and GPIO supply	I_{DD18} / I_{DDIx} / I_{DDI3}	1.8V	145	mA
FPGA core and FPGA PLL high-voltage supply	I_{DD25} / I_{DDA25} / $I_{DD_XCVR_CLK}$ / I_{DDAUXx}	2.5V	104	mA
Total Power	—	—	2016	mW

Table 2-4: Power – SDI to HDMI, 4 x 6G SDI SL IN, 3G HDMI OUT

Parameter	Symbol	Condition	Typ	Unit
FPGA core power supply	I_{DD}	1.05V	702	mA
Transceiver Tx and Rx lanes supply	I_{DDA}	1.05V	139	mA
Programming and GPIO receiver supply	I_{DD18} / I_{DDIx} / I_{DDI3}	1.8V	145	mA
FPGA core and FPGA PLL high-voltage supply	I_{DD25} / I_{DDA25} / $I_{DD_XCVR_CLK}$ / I_{DDAUXx}	2.5V	69	mA
Total Power	—	—	1317	mW

Table 2-5: Power – SDI to HDMI, 2 x 12G SDI SL IN, 6G HDMI OUT

Parameter	Symbol	Condition	Typ	Unit
FPGA core power supply	I_{DD}	1.05V	1060	mA
Transceiver Tx and Rx lanes supply	I_{DDA}	1.05V	174	mA
Programming and GPIO supply	I_{DD18} / I_{DDIx} / I_{DDI3}	1.8V	145	mA
FPGA core and FPGA PLL high-voltage supply	I_{DD25} / I_{DDA25} / $I_{DD_XCVR_CLK}$ / I_{DDAUXx}	2.5V	88	mA
Total Power	—	—	1724	mW

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Table 2-6: Power – SDI to HDMI, 2 x 6G SDI SL IN, 3G HDMI OUT

Parameter	Symbol	Condition	Typ	Unit
FPGA core power supply	I_{DD}	1.05V	610	mA
Transceiver Tx and Rx lanes supply	I_{DDA}	1.05V	130	mA
Programming and GPIO receiver supply	I_{DD18} / I_{DDIx} / I_{DDI3}	1.8V	145	mA
FPGA core and FPGA PLL high-voltage supply	I_{DD25} / I_{DDA25} / $I_{DD_XCVR_CLK}$ / I_{DDAUXx}	2.5V	69	mA
Total Power	—	—	1209	mW

Table 2-7: Power – SDI to HDMI, 1 x 12G SDI SL IN, 6G HDMI OUT

Parameter	Symbol	Condition	Typ	Unit
FPGA core power supply	I_{DD}	1.05V	964	mA
Transceiver Tx and Rx lanes supply	I_{DDA}	1.05V	162	mA
Programming and GPIO supply	I_{DD18} / I_{DDIx} / I_{DDI3}	1.8V	145	mA
FPGA core and FPGA PLL high-voltage supply	I_{DD25} / I_{DDA25} / $I_{DD_XCVR_CLK}$ / I_{DDAUXx}	2.5V	85	mA
Total Power	—	—	1655	mW

Table 2-8: Power – SDI to HDMI, 1 x 6G SDI SL IN, 3G HDMI OUT

Parameter	Symbol	Condition	Typ	Unit
FPGA core power supply	I_{DD}	1.05V	586	mA
Transceiver Tx and Rx lanes supply	I_{DDA}	1.05V	130	mA
Programming and GPIO supply	I_{DD18} / I_{DDIx} / I_{DDI3}	1.8V	145	mA
FPGA core and FPGA PLL high-voltage supply	I_{DD25} / I_{DDA25} / $I_{DD_XCVR_CLK}$ / I_{DDAUXx}	2.5V	72	mA
Total Power	—	—	1192	mW

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2.6. AC Electrical Characteristics

Refer to Microchip's PolarFire® FPGA Datasheet DS00003831.

2.7. Latency

Device Latency depends on the mode of operation. Table 2-9 lists latencies per mode measured in PCLK periods. Base latency does not include Audio and ANC insertion. Latency will increase with ANC or audio enabled.

Table 2-9: Latencies Per Mode in SDI-SDI Gearbox Operation

Mode		PCLK (MHz)	Min Latency [# PCLK Periods]	Typ Latency [# PCLK Periods]	Max Latency [# PCLK Periods]
MUX	QL3G→SL12G	148.5	TBD	TBD	TBD
	QLHD→SL6G	74.25	TBD	TBD	TBD
	QL6G→DL12G	148.5	TBD	TBD	TBD
	QL3G→DL6G	148.5	TBD	TBD	TBD
	DL6G→SL12G	148.5	TBD	TBD	TBD
	DL3G→SL6G	148.5	TBD	TBD	TBD
	DLHD→SL3G	74.25	TBD	TBD	TBD
DEMUX	SL12G→QL3G	148.5	TBD	TBD	TBD
	SL6G→QLHD	74.25	TBD	TBD	TBD
	DL12G→QL6G	148.5	TBD	TBD	TBD
	DL6G→QL3G	148.5	TBD	TBD	TBD
	SL12G→DL6G	148.5	TBD	TBD	TBD
	SL6G→DL3G	148.5	TBD	TBD	TBD
	SL3G→DLHD	74.25	TBD	TBD	TBD

Note:
ANC and audio insertion are both disabled for all values.

When generic ancillary data insertion or time code insertion are enabled, 22 PCLK cycles of latency are added to the base latency in Table 2-9. If one audio core is enabled (up to 8 channels of 48kHz audio), an additional delay of 1055 ±2 PCLK cycles is added to the base latency in Table 2-9. If both audio cores are enabled for insertion on one stream (up to 16 channels of 48kHz audio), an additional delay of 2082 ±2 PCLK cycles is added to the base in Table 2-9.

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3. Detailed Description

3.1. Configuration Modes

The GS12270 operates in three distinct configuration modes:

- Gearbox Mode (SDI-SDI)
- SDI-HDMI Mode
- HDMI-SDI Mode

The configuration mode is set at power-up through two balls: CONF_MODE_0 and CONF_MODE_1, as shown in Table 3-1, assuming that the associated firmware was programmed in the GS12270.

Table 3-1: Configuration Mode Selection

Ball		Mode
CONF_MODE_0	CONF_MODE_1	
0	X	SDI to SDI Configuration
1	0	HDMI-SDI Configuration
1	1	SDI-HDMI Configuration

To save power, clock gating of blocks which are not shared between modes is used.

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3.1.1. Initialization on Power-up

The GS12270 requires an initialization on power-up. In each mode, different registers need to be written upon power-up.

3.1.1.1. HDMI-SDI

The following registers need to be written in the given order:

Table 3-2: HDMI-SDI Initialization Registers

Address	Data
1065	0007
101C	0800
1043	0220
1044	8888
1018	0E41
102A	0008
1082	4239
1084	5FFF
1073	096C
10E4	5FFF
10E5	5FFF
10E6	2800
10E7	8004
10E8	2000

10FD	0001
1101	0000
1103	0000
1102	00F0
1100	C138
10FE	0001
1102	00F0
1100	C538
10FE	0001
1102	00F0
1100	C938
10FE	0001
1102	0004
1100	C028
10FE	0001
1102	0021
1100	41CC
10FE	0001
1102	0004
1100	C428
10FE	0001
1102	0021
1100	61CC
10FE	0001
1102	0004
1100	C828
10FE	0001
1102	0021
1100	81CC
10FE	0001
10FD	0000
1102	0000
1100	0000
1065	0006

3.1.1.2. SDI-HDMI

The following registers need to be written in the given order:

Table 3-3: HDMI-SDI Initialization Registers

Address	Data
007C	3668
00DC	0002
1065	0007
10F4	0001
10F8	0000
10FA	0000
10F9	0078
10F7	0810
10F5	0001
10F9	0078
10F7	0C10
10F5	0001
10F9	0078
10F7	1010
10F5	0001
10F9	0078
10F7	1410
10F5	0001
10F4	0000
10F9	0000
10F7	0000
1067	050D
1079	4239
1082	4239

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1084	5FFF
1085	5FFF
1091	4239
1093	4A39
1065	0006
7069	0187

3.2. Serial Data Inputs

3.2.1. Serial Inputs

The GS12270's high-speed inputs, DDI0 to DDI3, feature a differential input buffer with 100Ω differential on-chip input termination, which includes a trace equalizer.

The differential input signal must be AC-coupled—a 4.7µF capacitor is recommended. The balanced input circuit is compatible with industry standard LVPECL, PECL, CML and LVDS transmitters when AC-coupled using 100Ω differential termination circuitry.

3.2.1.1. Input Trace Equalization

The GS12270 features per-channel adjustable trace equalization to compensate for PCB trace dielectric losses.

For a 12Gb/s data rate, the trace equalizer's initial settings can be tuned to one of three specific trace loss bands. The trace EQ is adaptive within the specified band. To optimize the trace EQ settings, first the EQ setting value for required loss compensation needs to be written to the INPUT_EQ<n> register and then the DDI<n>_EQ_UPDATE parameter bit must be asserted. Table 3-4 contains the parameter values for the supported trace EQ settings.

Table 3-4: Trace Equalizer Settings (Register INPUT_EQ<n>)

Trace Loss Compensation	Input Data Rate		Notes
	12Gb/s Register Value$_h$	SD - 6Gb/s Register Value$_h$	
0-4dB	Setting 3468 (F468)	Setting 3468 (F468)	1
4-8dB	Setting 2C58 (EC58)		1
8-12dB	Setting 2448 (E448)		1

Note:

1. The value in brackets is the value that includes the two update bits (15:14). It is the value that will be read back when updated bits are set but the EQ settings have not been updated. The first value is the read-back value after the EQ settings have been updated.

The register location for the equalizer settings associated with each input channel is described in Table 3-5.

Table 3-5: Trace Equalizer Register Locations

Input Channel	Register Name	Address$_h$
DDI0	DDI0_EQ_UPDT	1023
DDI1	DDI1_EQ_UPDT	1024
DDI2	DDI2_EQ_UPDT	1025
DDI3	DDI3_EQ_UPDT	1026

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3.2.1.2. Input Power-Down

Inputs that are not intended to be used can be powered down through the host interface. The DDI<n>_PWR_DOWN registers provide per-lane control of the power-down options.

There are two different power-down modes:

- Partial Sleep Mode—lower power savings and quick turn-on time; only some parts of the receivers are powered-down.
- Deep Sleep Mode—higher power savings and higher turn-on latency. The power-down mode is controlled by two bits per input channel.

Table 3-6: Trace Equalizer Settings (Register INPUT_EQ<n>)

DDI<n>_PWR_DOWN	Sleep Mode
00	ON
01	Partial Sleep
1x	Deep Sleep

When the GS12270 is powered-up in SDI-SDI or SDI-HDMI Mode, inactive inputs are set into the deep sleep mode and partial sleep mode is controlled by the *ISP_N* input signal. If the *ISP_N* signal is HIGH on an active input (i.e. SL→QL SDI-SDI DEMUX), it will be set to Partial Sleep mode.

Input Power-down can be overwritten via the **DDI<n>_PWR_DOWN_REG** register by setting the MSB bit HIGH. The corresponding bit in the **DDI_PWR_DOWN_REG_SEL** register must also be set HIGH for input sleep control to be taken from the **DDI<n>_PWR_DOWN_REG** register.

When the GS12270 is powered-up in the HDMI-SDI Mode, input DDI3 is set to deep sleep mode. See Table 3-7 for more details on which inputs are set to Deep Sleep or Partial Sleep.

Table 3-7: Input Power Down per Configuration/Operational Mode

Configuration Mode	Operational Mode	DDI0	DDI1	DDI2	DDI3
Bypass	N/A	ON/partial sleep	ON/partial sleep	ON/partial sleep	ON/partial sleep
SDI-SDI MUX	QL→SL QL→DL	ON/partial sleep	ON/partial sleep	ON/partial sleep	ON/partial sleep
	DL→SL	ON/partial sleep	ON/partial sleep	ON/partial sleep [1]	ON/partial sleep [1]
SDI-SDI DEMUX	SL→DL	ON/partial sleep	Deep sleep	ON/partial sleep [1]	Deep sleep
	SL→QL	ON/partial sleep	Deep sleep	ON/partial sleep [1]	Deep sleep
	DL→QL	ON/partial sleep	ON/partial sleep	ON/partial sleep [1]	ON/partial sleep [1]
SDI-HDMI	SL→HDMI	ON/partial sleep	Deep sleep	ON/partial sleep [1]	Deep sleep
	DL→HDMI	ON/partial sleep	ON/partial sleep	ON/partial sleep [1]	ON/partial sleep [1]
	QL→HDMI	ON/partial sleep	ON/partial sleep	ON/partial sleep	ON/partial sleep
HDMI-SDI	HDMI→SL/DL/QL	ON/deep sleep	ON/deep sleep	ON/deep sleep	Deep sleep

Note:

1. If the second SL-DL MUX/DEMUX is enabled through **SEC_LINK_EN**.

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3.2.1.3. Input Polarity Inversion

The input pin polarity can be inverted for each input channel via the host interface. Registers PORT<n>_RX_POLARITY control DDI<n> polarity.

3.2.2. SDI Receiver

3.2.2.1. SDI-HDMI and SDI-SDI Modes

When the GS12270 is powered-up in the SDI-SDI or SDI-HDMI Mode, the DDI0:DDI4 inputs are configured as SDI receivers.

The GS12270 will detect, lock to, and process the following SDI serial data streams:

- SL and DL 12G
- SL, DL, 2xDL and QL 6G
- SL, DL, 2xDL and QL 3G
- SL, DL, 2xDL and QL 1.5G (HD)
- Up to 4 SD streams (supported only in SD Bypass Mode)

When powered-up in the SDI-SDI Mode (Gearbox Mode) or in the SDI-HDMI Bridge Mode:

- The device can be connected to a serial digital input signal serialized in compliance with SMPTE 259M-C, ST292-1, ST424, ST2081-1, and ST2082-1.
- The serial digital input can operate at the nominal rates of 270MHz, 1.485Gb/s, 1.485/1.001Gb/s, 2.97Gb/s, 2.97/1.001Gb/s, 5.94Gb/s, 5.94/1.001Gb/s, 11.88Gb/s, and 11.88/1.001Gb/s.
- The serial data input signal is connected to the *DDI0_P/DDI0_N*, *DDI1_P/DDI1_N*, *DDI2_P/DDI2_N*, and *DDI3_P/DDI3_N* input balls of the device.
- Each input has an associated control input called ISP. This control sets the input channel into a sleep state to save power. This function can be overridden via the host interface, as defined in Section 3.2.1.2.

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3.2.2.2. Input Data Rate

There are two different gearbox mode selections in SDI-SDI configuration, the manual selection (*GB_MODE_SEL[2:0]* and *MUX_DEMUX_N* pins or registers need to be set). In semi-auto mode only *MUX_DEMUX_N* needs to be set. In manual mode, the data rate is set when the gearbox mode is set, based on the selected gearbox mode. When in SDI-HDMI configuration, the data rate is automatically set based on the connected input video.

The data rate at the input is automatically configured based on the input format, when a specified MUX or DEMUX Mode is selected. The maximum data rate supported for each *DDI<n>* input is shown in Table 3-8.

Table 3-8: Serial Data Input Supported Data Rates

Input	Mode		
	MUX	DEMUX	BYPASS
DDI0	—	12Gb/s	12Gb/s
	6Gb/s	6Gb/s	6Gb/s
	3Gb/s	3Gb/s	3Gb/s
	1.5Gb/s	—	1.5Gb/s
	—	—	270Mb/s
DDI1	—	—	12Gb/s
	6Gb/s	—	6Gb/s
	3Gb/s	—	3Gb/s
	1.5Gb/s	—	1.5Gb/s
	—	—	270Mb/s
DDI2	—	12Gb/s	12Gb/s
	6Gb/s	6Gb/s	6Gb/s
	3Gb/s	3Gb/s	3Gb/s
	1.5Gb/s	—	1.5Gb/s
	—	—	270Mb/s
DDI3	—	—	12Gb/s
	6Gb/s	—	6Gb/s
	3Gb/s	—	3Gb/s
	1.5Gb/s	—	1.5Gb/s
	—	—	270Mb/s

By default, in semi-auto mode and BYPASS mode, in the SDI-SDI configuration and in the SDI-HDMI configuration, the device searches for 12G, 6G, 3G, and HD data rates at the input. If a valid SDI signal is found, and lock is achieved, the data rate will be reported (per input) in the parameters within the **DATA_RATE_REPORT** register as a 2-bit value. Table 3-9 describes the reported data rates and their parameter values. Note that SD is not reported as it must be set manually.

In BYPASS Mode, the SD rate is not automatically detected and must be manually set for each individual input. This can be achieved by asserting the *SD_BYPASS[3:0]* balls or through the host interface using the **SD_BYPASS_SEL_REG** register.

The automatic data rate detection can be overridden and can be manually set through the **MANUAL_RATE** register. A parameter is available for each individual input. Table 3-9 applies for both reported data rate and the manual setting of the data rate.

Table 3-9: Data Rate Register Values for Setting and Reporting

Nominal Data Rate	Register Value[b]
12G	11
6G	10
3G	01
HD	00

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3.2.2.3. Input Loop Bandwidth

The loop bandwidth of the input is individually configured on a per-channel basis. The default loop bandwidth is optimized, and it is not recommended that this value be changed. When configured as an HDMI input, the loop bandwidth of all three receivers is set to 4MHz.

There may be specific cases where the input loop bandwidth needs adjustment. This can be set through **DDI_CDR_LBW**. See Table 3-10 for CDR loop bandwidth settings.

Table 3-10: CDR Bandwidth Settings

Data Rate	CDR Bandwidth	Bandwidth (MHz)	CDR Lock to Data Time (µs)
12Gb/s	Low	3.26	5.2
	Recommended	4.88	4.4
	High	5.58	4.1
6Gb/s	Low	1.22	9.3
	Recommended	1.63	7.6
	High	4.88	4.4
3Gb/s	Low	0.61	18.6
	Recommended	0.81	15.3
	High	2.44	8.7
1.5Gb/s	Low	0.31	37.1
	Recommended	0.41	30.6
	High	1.22	17.5

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3.2.2.4. Automatic Inter Link Delay (Skew) Adjustment and Reporting

When the SDI serial interface is set as DL or QL, the GS12270 automatically adjusts skews between multiple SDI input links. Table 3-11 lists the maximum skew supported for the various MUX/DEMUX modes.

Table 3-11: Input Skew Compensation

Mode Conversion	Time of Skew
DL 6Gb/s → SL 12Gb/s DL	800ns
3Gb/s → SL 6Gb/s	800ns
DL 1.5Gb/s → SL 3Gb/s	1600ns
QL 3Gb/s → SL 12Gb/s	800ns
QL 3Gb/s → DL 6Gb/s	800ns
QL 1.5Gb/s → SL 6Gb/s	1600ns
DL 6Gb/s → QL 3Gb/s	800ns
DL 12Gb/s → QL 6Gb/s	400ns
QL 6Gb/s → DL 12Gb/s	400ns

The relative delay between the links is measured and reported via the host interface, parameters CH0_DELAY - CH3_DELAY. Please note that a delay introduced by the link delay adjustment block is reported for each channel, not the relative delay of a channel. When in the SDI-SDI MUX mode and if the audio embedding is not utilized, there is an option to delay each input independently before the inter link delay adjustment block for up to 2/3 of the line length. The delay can be programmed via the host interface (DELAY_ DS1_REG).

3.2.2.5. Status Reporting

The GS12270 has status monitoring of the following parameters:

- LOCK
- PID ERROR
- PID DETECTED
- TRS ERROR
- CRC ERROR
- DATA RATE
- INTERLEAVED INPUT STREAM

Table 3-12 describes the parameter and the register that reports that parameter.

Table 3-12: Input Status Reporting Parameters for SDI

Reporting Parameter	Register Name	Description	STAT Output Ball Availability
LOCK	INPUT_ LOCK_REG	Asserts when the input has locked to the input data rate and detect three TRS sequences within a 2.5 line window. LOCK is available for each individual input.	Assignment to STAT ball is set through STAT_CH[3:0] registers.
PID ERROR	PID_ERROR	Asserts when the PID embedded in the input stream does not match the expected PID value. PID ERROR Indication is available for each of the individual data streams and for each individual input.	
PID DETECTED	PID_ DETECTED	Asserts when the PID is present in the input stream. PID DETECTED Indication is available for each of the individual data streams and for each individual input.	
TRS_ERROR	NA	Asserts when the received TRS's protection bit is incorrect. TRS_PERR indication is available for each of the individual data streams and for each individual input.	
CRC ERROR	CRC ERROR	Asserts when a CRC error has been detected in the input stream. This register is a logical OR of each DDI CRC error, if detected.	Assignment to STAT ball is set through STAT_CH[3:0] register.
DATA_RATE	DATA_RATE_ REPORT	Indicates the data rate on the DDI[3:0] inputs, two bits per input.	
CRC ERROR COUNTER	CRC_ERROR_ CH<n> COUNTER	Reports CRC count per input since last CRC counter reset. No STAT output.	N/A
INTERLEAVED_ INPUT_DET	VID_STREAM_ INTERLEAVED_ STAT	Indicates that the input video stream is interleaved when HIGH. One bit per stream, two streams per input.	Assignment to STAT ball is set through STAT_CH[3:0] register.

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Note: See Figure 3-1: Input Data Stream Paths.

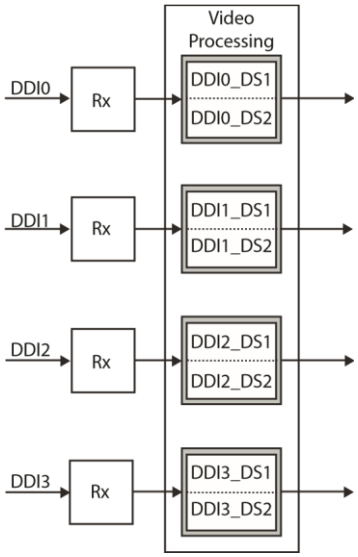

Figure 3-1: Input Data Stream Paths

3.2.2.6. CRC Error Detection

The GS12270 calculates line-based CRCs for SDI video signals. The CRCs are calculated for each data stream and compared with CRC values embedded in the stream. If a mismatch is detected between the calculated and received CRC values in the stream, the CRC error for the stream is flagged. If the data stream consists of two interleaved streams, CRC values are calculated and compared with the embedded CRCs for both streams.

The detected CRC error is reported per input channel via the host interface and *STAT* balls. The host interface CRC error bit will stay HIGH until cleared by the user. The error pulse at STAT outputs is one system clock (27MHz) long.

Besides the CRC error per channel, a combined CRC error is also reported via the host interface and *STAT* pins. The contributing channels, which CRC error signals are logically ORed to yield combined CRC error signal, can be selected using **CRC_ERROR_MASK** register. The default register value is 1111_b, meaning all input channels are selected.

3.2.2.6.1. CRC Error Counter

For each input, there is a CRC error counter which will count the CRC error signal occurrence for a channel. The maximum increment is +1 per line. The value of the counter is reported via the host interface (CRC_ERROR_CH0_COUNTER).

The CRC counter can be reset via the host interface.

3.2.2.7. HVF Timing Signal Extraction

When the input is configured as an SDI receiver, the GS12270 extracts the timing parameters from the received TRS signals. Horizontal blanking period/active line (H), Vertical blanking period (V), and Field odd/even (F) timing are extracted. The extracted timing signals are available to the application layer via the *STAT* output balls. It is possible to select timing signals from different blocks (with different delay as signal passes through the part) to be sent to the *STAT* outputs.

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3.2.2.8. TRS Error Detection

TRS error flags are generated when the received TRS hamming codes are incorrect. Both SAV and EAV TRS words are checked for timing and data integrity errors. A TRS error indication is provided when an SAV and/or EAV error is detected, available on the *STAT* balls as a minimum one PCLK cycle pulse.

3.2.2.9. Video Format Detection

The video format is determined from the extracted PID data packet.

The total samples per line, active samples per line, total lines per field/frame and active lines per field/frame are measured and reported via the four **RASTER_STRUC_*** registers. The line and sample count registers are updated once per frame at the end of line 12. The registers also contain an **INT/$\overline{\text{PROG}}$** bit. By using timing parameters extracted from the received TRS signals, the GS12270 calculates the video format for HD rates only (PID data packet is not required to be embedded for HD data rates).

For the multi-link standards, the video format calculation is done on the master channel only.

Please note that for 6Gb/s and 12Gb/s SDI links, values reported in **RASTER_STRUC_*** will reflect measurements taken on SMPTE Virtual Interfaces for each link mapping.

3.2.2.10. Input Signal Present

Each input has an associated active LOW control input ball called ISP, which needs to be driven LOW when a valid input signal is applied. When a valid input signal is not present, this signal is driven HIGH.

The ISP_REG register can also be used to control this signal as well as change its polarity and report on the state of the *ISP_N[3:0]* input ball.

An example of how to use this ball in the application is to connect it to the lock signal of a re-clocker that drives the respective serial input.

In the DEMUX Mode, it is recommended to leave the associated *ISP_N[3:0]* HIGH for inputs that are not used.

3.2.3. HDMI Receiver

3.2.3.1. HDMI-SDI Mode

When powered in the HDMI-SDI Mode, the high-speed inputs DDI0:DDI2 are initialized as an HDMI receiver. The DDI3 input is powered down.

When configured as an HDMI receiver:

- Three high-speed inputs are functional, allowing the device to receive TMDS data from a re-clocker device (AC-coupled).
- The serial high-speed inputs can operate with HDMI1.4b and HDMI2.0 compatible, TMDS coded signals at line data rates ranging from 740Mb/s to 5.94Gb/s.
- By default, the TMDS data signals Data0, Data1, and Data2 are connected to the *DDI0_P/DDI0_N*, *DDI1_P/DDI1_N*, and *DDI2_P/DDI2_N* input balls, respectively. The default mapping can be rearranged via the host interface, register STREAM_SEL. The TMDS clock is connected to *TMDS_CLK_P/TMDS_CLK_N* reference clock input.

The block diagram of HDMI Receiver is shown in Figure 3-2.

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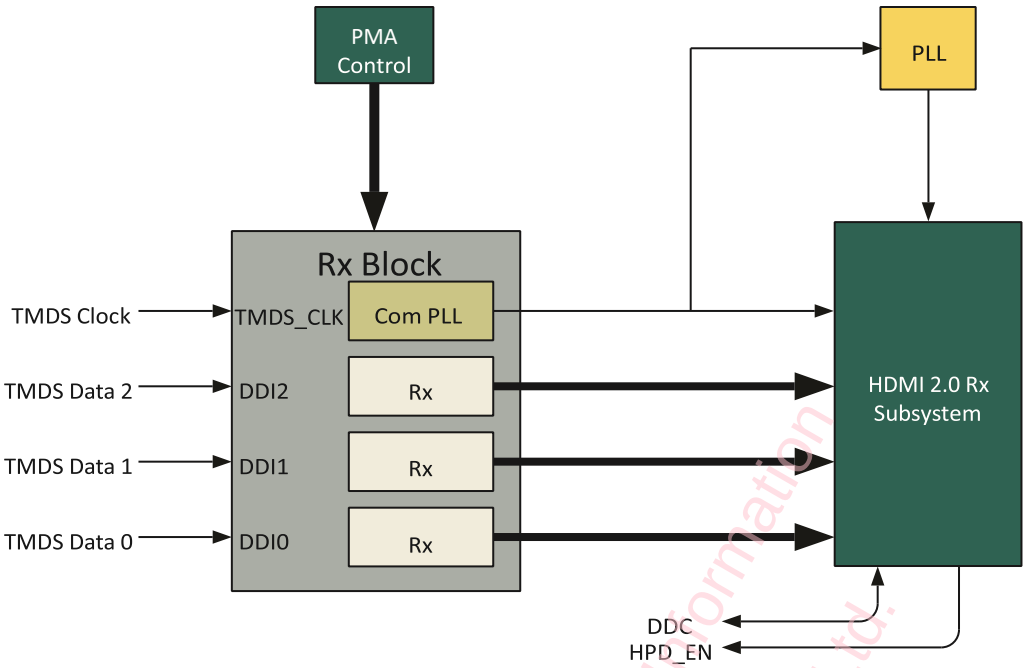

Figure 3-2: HDMI Receiver

The GS12270 supports HDCP unencrypted TMDS inputs encoded in accordance with the HDMI1.4b and HDMI2.0 specification. The HDMI receiver contains DDC I^2C slave functionality and generates a HPD_EN signal when it is ready to respond to the DDC source.

3.2.3.2. Supported Image Formats

HDMI receivers support all HDMI1.4b and HDMI2.0 compatible input formats supported by the SDI output arranged in the format more common for HDMI in Table 3-13 below.

Table 3-13: HDMI Receiver Supported Formats

Video Format	Pixel Encoding								
	4:2:2			4:2:0			4:4:4		
	Colour Depth			Colour Depth			Colour Depth		
720p25	24	30	—	—	—	—	24	30	—
720p30/29.97	24	30	—	—	—	—	24	30	—
720p50	24	30	—	—	—	—	24	30	—
720p60/59.94	24	30	—	—	—	—	24	30	—
1080i50	24	30	36	—	—	—	24	30	36
1080i60/59.94	24	30	36	—	—	—	24	30	36
1080p24/23.98	24	30	36	—	—	—	24	30	36
1080p25	24	30	36	—	—	—	24	30	36

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1080p30/29.97	24	30	36	—	—	—	24	30	36
1080p50	24	30	36	—	—	—	24	30	36
1080p60/59.94	24	30	36	—	—	—	24	30	36
1080p100	24	30	36	—	—	—	24	30	36
1080p120/119.88	24	30	36	—	—	—	24	30	36
2160p24/23.976	24	30	36	—	—	—	24	30	36
2160p25	24	30	36	—	—	—	24	30	36
2160p30/29.97	24	30	36	—	—	—	24	30	36
2160p48/47.98	24	30	—	24	30	36	—	—	—
2160p50	24	30	—	24	30	36	—	—	—
2160p60/59.94	24	30	—	24	30	36	—	—	—

The 2160p based standards include 3840x2160 and 4096x2160 formats. The 1080p based standards include 1920x1080 and 2048x1080 formats.

3.2.3.3. Input Data Rate Detection

The source reads the sinks E-EDID information to understand the capabilities of the sink. The **MAX_TMDS_CHARACTER_RATE** byte is used to determine the data rate supported. Depending on the value, the source writes to slave address $A8_h$, offset 20_h bit 1, the **TMDS_CLOCK_RATIO_STATUS** info.

The GS12270 uses this information to determine the TMDS clock ratio and set its own TMDS clock ratio bit accordingly. If a '1' is written, the TMDS bit period is 1/40th of the TMDS clock period. If a '0' is written, the TMDS bit period is set to 1/10th of the TMDS clock period.

By default, the GS12270 selects 1/10th of the clock period unless a '1' is written to the address above. When the +5V signal from the source is de-asserted, the bit is reset to its default value.

The GS12270 measures the TMDS clock frequency and uses the determined clock ratio to select data rate.

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3.3. Serial Data Outputs

3.3.1. Serial Outputs

3.3.1.1. Output Polarity Inversion

The output pin polarity can be inverted for each output channel via the host interface. Registers **PORT<n>_TX_POLARITY** and **PORT<n>_TX_POLARITY_OVR_EN** (address 203A) control *DDO<n>* polarity.

3.3.1.2. DDO Output Swing

By default, the output swing is set to 800mV$_{pp}$ differential.

In the SDI-SDI configuration, the swing can be changed by setting the **DDO<n>_AMP** parameter in the **DDO_DRV_AMP** register, as shown in Table 3-14. Once the value is set to the desired amplitude value for the selected output, set the

DDO<n>_DRV_AMP_UPDATE parameter HIGH for this value to be loaded into the GS12270.

Note: If the output swing needs to be controlled in SDI-HDMI or HDMI-SDI configuration, please contact Semtech's FAE group.

Table 3-14: Output Swing Settings

DDO<n>_AMP Value$_h$	Nominal DDO Amplitude (mV$_{pp}$)
0	400
1	500
2	600
3	700
4	800
5	900
6	1000
7	400

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3.3.1.3. Output Idle

Serial outputs can be individually set to idle. When an output is set to idle, its voltage will be set to the common mode voltage. These functions are programmed through the **DDO_IDLE** register.

3.3.1.4. Output Power-Down

Outputs that are not intended to be used can be powered-down through the host interface. The **OUTPUT_PWR_DOWN** register provides per-lane control of the power-down options.

In SDI-HDMI configuration, if the SDI receiver is not locked all four DDOs are powered-down and the HDMI_5V_EN output is set LOW.

The **OUTPUT_PWR_DOWN** register contains 16 bits which can be broken down into four groups of four bits each. Each bit in the group of four bits is assigned to a *DDO<n>* output. Thus, there are multiple bits required to power down a particular *DDO<n>* output. The power-down bits assigned to a *DDO<n>* output in each four-bit group must be the same.

Shown in Table 3-16 is an example of the value that is written to enable *DDO0* and *DDO2*, but disable *DDO1* and *DDO3*. For convenience, Table 3-15 is showing the HEX register value for all possible combinations of output power-down.

Table 3-15: DDO<n> Power-Down Control

Note: Powered down output lanes denoted as PD.

Register Value	DDO Lane 0	DDO Lane 1	DDO Lane 2	DDO Lane 3
0000	Active	Active	Active	Active
1111	Active	Active	Active	PD
2222	Active	Active	PD	Active
3333	Active	Active	PD	PD
4444	Active	PD	Active	Active
5555	Active	PD	Active	PD
6666	Active	PD	PD	Active
7777	Active	PD	PD	PD
8888	PD	Active	Active	Active
9999	PD	Active	Active	PD
AAAA	PD	Active	PD	Active
BBBB	PD	Active	PD	PD
CCCC	PD	PD	Active	Active
DDDD	PD	PD	Active	PD
EEEE	PD	PD	PD	Active
FFFF	PD	PD	PD	PD

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Table 3-16: Example of Register Value Required to Power Down DDO1 and DDO3

OUTPUT_PWR_DOWN Bit Slice	[15:12]				[11:8]				[7:4]				[3:0]			
DDO<n> Power Down Bit Assignment	DDO0	DDO1	DDO2	DDO3	DDO0	DDO1	DDO2	DDO3	DDO0	DDO1	DDO2	DDO3	DDO0	DDO1	DDO2	DDO3
Register Bit Value	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
Register Hex Value	5				5				5				5			

3.3.1.5. Output Driver Disable

The serial output driver can be disabled. This feature can be used in combination with Output Power Down to realize additional power savings as the output driver is shut down.

This function can be programmed through the **DDO_DRIVER_DISABLE** register.

3.3.1.6. Output Mute

In SDI-SDI and HDMI-SDI configurations, outputs are muted automatically if the output video data stream is not valid.

For each GS12270 output, there is a MUTE control in the host interface which will override mute signals automatically generated, if necessary.

3.3.2. Transmitter (Tx) Reference Clock

In the transmitter block, the Tx data stream needs to be frequency-locked to the incoming Rx data stream. The common PLL reference is a 148.5MHz, free-running external clock. Internal jitter attenuation is used to produce the output reference clock.

3.3.3. SDI Transmitter

3.3.3.1. SDI-SDI Gearbox and HDMI-SDI Modes

When the device is powered in UHD-SDI Gearbox or HDMI-SDI Mode, outputs DDO0:DDO3 are configured as SDI transmitters. The GS12270 SDI transmitter is able to process and transmit the following SDI serial data streams:

- SL and DL 12G
- SL, DL, 2xDL and QL 6G
- SL, DL, 2xDL and QL 3G
- SL, DL, 2xDL and QL 1.5G (HD)
- Up to 4 SD streams (supported only in SD bypass mode)

The GS12270 has four high-speed digital differential data outputs capable of operating at nominal rates of:

- 12G (11.88Gb/s, and 11.88/1.001Gb/s)
- 6G (5.94Gb/s and 5.94/1.001Gb/s)
- 3G (2.97Gb/s and 2.97/1.001Gb/s)
- HD (1.485Gb/s and 1.485/1.001Gb/s)
- SD (270MHz)

Each output has a driver capable of driving a 100 Ω differential load. The serial data output signal is connected to the *DDO0_P/DDO0_N, DDO1_P/DDO1_N, DDO2_P/DDO2_N, DDO3_P/DDO3_N* output balls of the device.

3.3.3.2. SMPTE Scrambler

For each serial output (*DDO0*:*DDO3*), the signal is scrambled by the SMPTE scrambler block before the 40-bit or 20-bit parallel data is serialized. The block carries out NRZ to NRZI encoding and scrambles the data according to SMPTE 424M / SMPTE 299M / SMPTE 259M-C. The scrambler block can be bypassed via the host interface.

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3.3.3.3. Sync Bit Insertion

SMPTE standards defining 6Gb/s and 12Gb/s SDI interface (SMTE ST2081-1 and ST2082-1) require inversion of the one bit in all 3FF and 000 words in the video stream, keeping only one 3FF 000 000 sequence in the TRS words; a process called Sync-bit insertion. The GS12270 inserts the sync-bit into the video stream immediately before the scrambling process, for SL, DL, or QL UHDI interfaces at 6Gb/s and 12Gb/s data rates.

3.3.3.4. CRC Insertion

The GS12270 calculates and inserts line-based CRC words into all VI video streams. If the VI video streams contain interleaved video streams, CRC words are calculated and inserted for each interleaved video stream separately. There is a register to enable CRC insertion per video stream. By default, it is set to enable CRC insertion.

3.3.4. HDMI Transmitter

When the device is powered in the SDI-HDMI Mode, the high-speed outputs *DDO1*:*DDO3* are initialized as the HDMI TMDS source. The *DDO0* transmitter is used to source the TMDS output clock. The TMDS interface supports TMDS bit rates up to 6.0Gb/s in accordance with HDMI1.4b and HDMI2.0 specification.

The reference clock for the common PLL is generated by the digital PLL locked to the pixel clock.

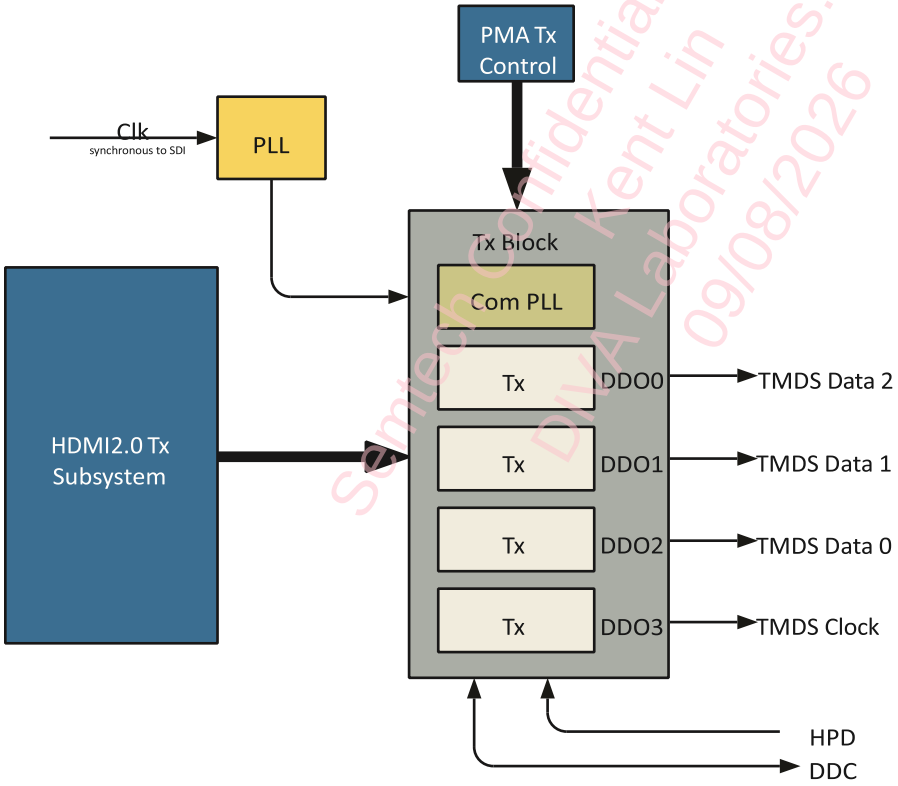

Figure 3-3: HDMI Transmitter

The GS12270's HDMI Transmitter implements Enhanced DDC Source functionality in accordance with HDMI1.4b and HDMI2.0 specification. For more info, see 3.5 SDI-HDMI Configuration.

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3.4. SDI to SDI Configuration

Under Gearbox (SDI-SDI) Mode, the GS12270 operates in three distinctive operational modes:

- MUX (Multiplex)
- DEMUX (De-Multiplex)
- Bypass (Input to Output)

3.4.1. SDI-SDI Mode Functions

In the SDI-SDI configuration mode, when either MUX or DEMUX mode is selected the device will:

- Apply selected equalization to the input signals
- Check and report on CRC errors in each data stream
- Read PID values in each data stream
- When in Semi Auto mode, determine the input format based on the PID values and select the proper SDI output format
- De-embed audio from data streams
- Extract time code from data streams
- Extract embedded ANC data from data streams
- Delete ANC data streams
- Overwrite embedded PIDs
- Embed audio in the SDI mapped data streams
- Embed time code in the SDI mapped data streams
- Embed ANC data in the SDI mapped data streams
- Align data streams based on TRS words
- Re-calculate and insert CRCs
- Multiplex the parallel signals as defined by the device's setup
- Perform sync bit insertion at the selected output multiplex and rate
- Serialize the signal to the selected output rate
- Copy the signal to multiple outputs as instructed by the user
- Apply programmed emphasis to each output

Please note that majority of the functions listed above are not enabled by default and need to be enabled/selected.

Audio, ANC data and time code insertion/extraction is not supported when either DL12G → QL6G DEMUX or QL6G → DL12G MUX mode is selected.

When the BYPASS mode is selected most of processing are turned off. Parallel data from each receiver is routed directly to the crosspoint. There is still an option to enable CRC check and PID reporting.

3.4.2. Operational Mode Selection

The *MUX_DEMUX_N* and BYPASS balls configure the operational mode of the device.

In BYPASS Mode, the device automatically searches for the data-rates, 12G, 6G, 3G and HD at the input. Operation at SD (270Mb/s) must be manually set using the SD_BYPASS ball. This selection is available per lane and only active when the device is in BYPASS Mode. When BYPASS Mode is selected, the *MUX_DEMUX_N* ball is ignored.

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The settings for mode selection are described in Table 3-17. The default ball settings for the GS12270 mode selection is set to DEMUX Mode through a pull-down resistor. Alternatively, mode selection can be set through the **OPERATING_MODE_SEL_REG** registers in the CSR.

Note: Register control of the **MUX_DEMUX**, **MODE_SEL**, **PID_MODE** and **BYPASS** parameters are grouped. All three functions must either be ball-controlled or register-controlled through **REG_CTRL_OP_MODE_EN**.

Table 3-17: Operational Mode Selection

Ball			Mode
MUX/DEMUX	BYPASS	SD_BYPASS	
0	0	0	DEMUX
1	0	0	MUX
X	1	0	Bypass
X	1	1	SD Bypass (only available when BYPASS = 1)

3.4.3. Multiplex Mode

3.4.3.1. Conversion Selection

In MUX Mode, conversion modes are illustrated in Figure 3-4. Conversion modes can be selected either manually (default) or a semi-auto option can be selected using register **MANUAL_RATE** bit.

The soft reset (**CORE_RESET** register 0079_h, bit 6) is required when switching between MUX and DEMUX modes while in semi-auto mode.

When manual selection is chosen, register **SDI_AUTO_MODE_EN** = 0, the conversion mode needs to be set through the *MODE_SEL[2:0]* balls.

The **OPERATING_MODE_SEL _REG** register can also be used to select the conversion mode and override the ball settings. The **MODE_SEL** parameter is used to set the mode and the **REG_CTRL_MODE_SEL_EN** parameter is used to enable the ball override.

The mode selection settings are listed in Table 3-18.

Table 3-18: Operational Mode Selection

Balls				MUX Mode		Notes (Refer to Figure 3-4)
MUX/DEMUX	MODE_SEL2	MODE_SEL1	MODE_SEL0	Input	Output	
1	1	1	1	QL 3Gb/s	SL 12Gb/s	(a)
1	1	1	0	QL 1.5Gb/s	SL 6Gb/s	(b)

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1	1	0	1	QL 6Gb/s	DL 12Gb/s	(c)
1	1	0	0	QL 3Gb/s	DL 6Gb/s	(d)
1	0	1	1	DL 6Gb/s	SL 12Gb/s	(e)
1	0	1	0	DL 3Gb/s	SL 6Gb/s	(f)
1	0	0	1	DL 1.5Gb/s	SL 3Gb/s	(g)
1	0	0	0	RSVD	RSVD	—

When semi-auto option is selected, register **SDI_AUTO_MODE_EN** = 1, the *MODE_SEL[2:0]* ball settings are ignored and the MUX mode conversion is selected based on the detected PID in the input data stream and values of

SDI_AUTO_MODE_FORCE_DLHD_3G and **SDI_AUTO_MODE_OUT_INTERF** registers.

The input data stream for PID detection is the data stream from DDI0 input when **INPUT_SELECT** is 0 or from *DDI2* input when **INPUT_SELECT** is 1. The detected PID, used for mode conversion selection when semi-auto option is selected, can be overridden using **PID_BYTE1_AUTO** and **PID_BYTE1_AUTO_OVR**. Additionally, if **REG_CTRL_MODE_SEL_EN** is set the semi-auto, selection is overridden by **MODE_SEL** parameter.

In the case where selection can be ambiguous, for example: QL3G inputs can be multiplexed either as SL12G or DL6G, register bit **SDI_AUTO_MODE_OUT_INTERF** can be used to select the preferred interface.

Since SMPTE standards do not specify different PID byte 1 for SLHD, DLHD or QLHD video formats, it is not possible to differentiate those formats based on PIDs. The GS12270 will recognize a video input as QLHD if HD data rates are detected at all four inputs (no missing link replacement supported) and as SLHD case if HD data rate is detected at the DDI0 input but not at the three remaining inputs (can be still detected at some of them). The DLHD → SL3G conversion can still be enabled by selecting the **SDI_AUTO_MODE_FORCE_DLHD_3G** register bit.

Users should select either manual or semi-auto conversion selection based on application requirements.

For example: manual selection will better suit applications were inputs are mostly at the same data rate and interface (QL, DL) but data streams can be switched upstream or disconnected-connected and if faster lock is required.

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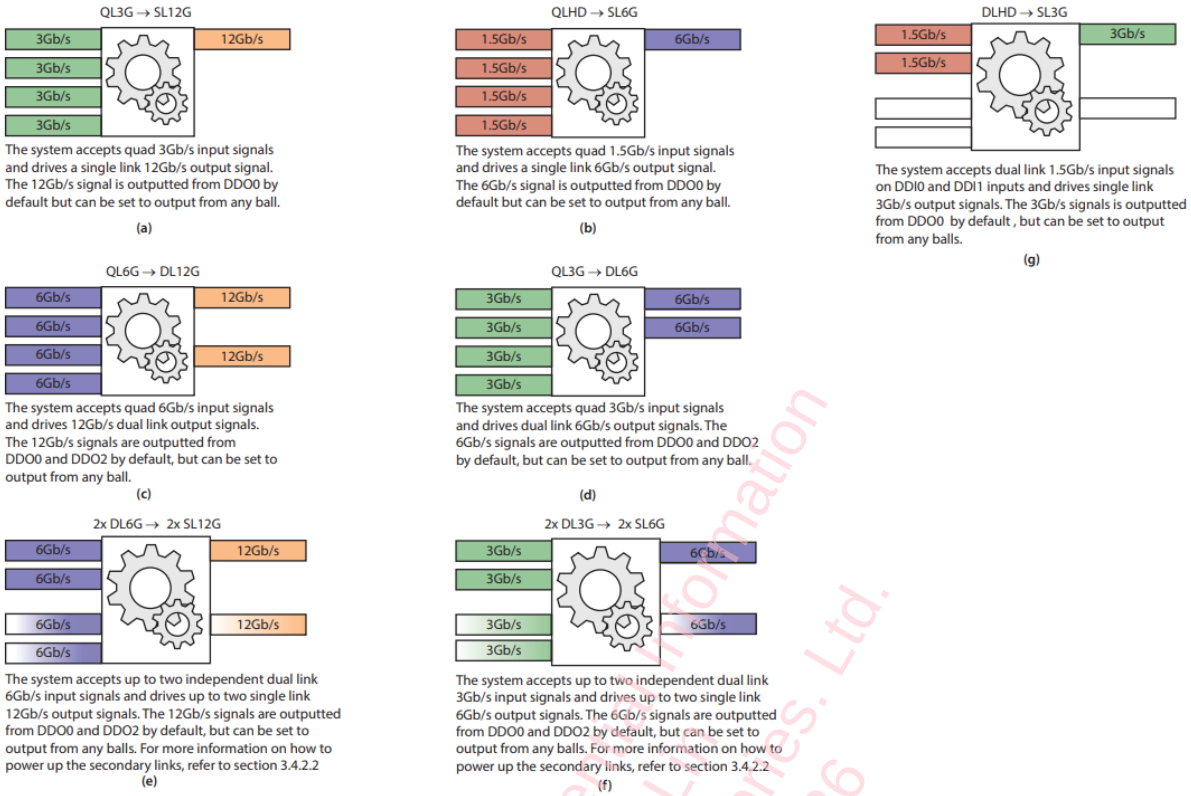

Figure 3-4: Multiplex Conversion Modes

Note:

- In Figure 3-4 e) and f), solid coloured inputs use path M0 and gradient coloured inputs use path M1. See Section 3.4.3.2 for further details.
- Audio, ANC and TC extraction/insertion is supported only in M0 path.
- In QL6G □ DL12G mode, audio, ANC and TC extraction/insertion is not supported.

3.4.3.2. Multiplexing Paths

The MUX modes will enable one of two paths based on the selected conversion mode.

For quad link inputs the M0 path is used.

For dual link inputs, both M0 and M1can be used based on the application requirement. By default, M1 is powered-down. To enable the M1 path, the *SEC_LINK_ENABLE* ball should be driven HIGH. There is a major difference between M0 and M1 paths such that the additional processing, audio, ANC and TC insertion/extraction, is supported only in M0 path.

Alternatively, the parameter **SEC_LINK_REG** within the **OPERATING_MODE_SEL_REG** register can be used to override the *SEC_LINK_ENABLE* ball setting. The parameter **REG_CTRL_SEC_LINK_EN** is used to override the ball control and enable the register selection of this feature. It is not required that dual links at M0 and M1 path are frequency-locked, they can even have different frame rates (59.94 vs 60&50) but they have to be same data rate, because the mode selection is common for both paths M0 and M1.

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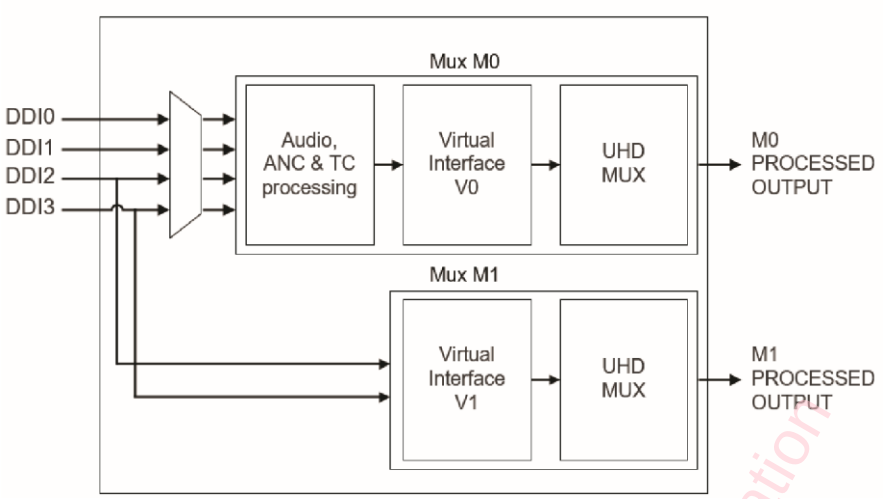

Figure 3-5: Multiplexing Pahts

3.4.3.3. Input Selection in DL → SL Modes

When in DL→SL mode, inputs DDI2 and DDI3 instead of DDI0 and DDI1 can be selected to go to the MUX0 (i.e. route them through audio, ANC and TC processing blocks). In order to be able to select DDI2 and DDI3 inputs, secondary link needs to be powered-up, either by **SEC_LINK_ENABLE** ball or through registers. When secondary link is enabled, either ball **INPUT_SELECT** (*L14*) or registers **SDI_IN_SEL**, parameters **SDI_IN_0_2_SEL** to select and **REG_CTRL_SDI_IN_SEL** to enable register override, can be used to select inputs on M0 path.

Please note that manual conversion selection should be used if the input selection is required.

3.4.3.4. SMPTE Compatibility

Table 3-19 outlines the conversion mappings that are compatible to the SMPTE UHD standards.

By default, the input streams will be multiplexed according to the mappings defined by the SMPTE UHDTV standards. The Payload ID can be inserted manually, if required.

If the **PID_MODE_REG** parameter is set to '11' in the **OPERATING_MODE_SEL_REG** register, Automatic PID Insertion is disabled. Note that the **REG_CTRL_OP_MODE_EN** parameter must be set HIGH for Automatic PID Insertion to be handled by the **PID_MODE_REG** parameter.

Table 3-19: MUX Mode SMPTE Compatibility

MUX Mode		Supported SMPTE Mapping	
Input	**Output**	**Input Mapping**	**Output Mapping**
QL 1.5Gb/s	SL 6Gb/s	ST274 – 30/25/24 FR, progressive	ST2081-10 2160-line Mode 1
DL 3Gb/s	SL 6Gb/s	ST425-3 1080-line Level A Mapping ST425-3 2160-line Mapping	ST2081-10 1080-line Mode 2 ST2081-10 2160-line Mode 1
QL 3Gb/s	DL 6Gb/s	ST425-5 2160-line Level A Mapping	ST2081-11 2160-line Mode 1
QL 3Gb/s	SL 12Gb/s	ST425-5 2160-line Level A Mapping	ST2082-10 2160-line Mode 1

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DL 6Gb/s	SL 12Gb/s	ST2081-11 2160-line Mode 1 ST2081-11 1080-line Mode 2	ST2082-10 2160-line Mode 1 ST2082-10 1080-line Mode 2
QL 6Gb/s	DL 12Gb/s	ST2081-12 4320-line Mode 1 ST2081-12 2160-line Mode 2	ST2082-11 4320-line Mode 1 ST2082-11 2160-line Mode 2

3.4.3.5. Lost Input

In MUX Mode, if the GS12270 fails to detect LOCK on an input, the primary input is copied to the missing input(s). By default, *DDI0* is the primary channel. This function is enabled on all inputs. The **LOST_INPUT_IGNORE_CTRL** register allows for customization of this feature. The primary input can be configured through the **M0_PRIM_CH** parameter for Quad-Link inputs appearing on *DDI[3:0]* and Dual-Link inputs appearing on *DDI[1:0]*. For Dual-Link inputs appearing on *DDI[3:2]* this feature is not supported.

The feature can be disabled on a per-input basis through the **IGNORE_LOST_INPUT** parameter.

3.4.3.6. Automatic Input Link Ordering

The SMPTE multi-link standards define the Link numbers within Byte 4 of the SMPTE ST 352M Payload ID.

By default, the GS12270 will associate the Link number with the respective *DDI[3:0]* input:

- Input on DDI0 is treated as Link 1
- Input on DDI1 is treated as Link 2
- Input on DDI2 is treated as Link 3
- Input on DDI3 is treated as Link 4

The GS12270 can use the Payload ID to identify the Link number and dissociate the Link number with the *DDI[3:0]* inputs and multiplex the Input in the correct SMPTE defined order. To enable this function, the *LINK_ASGMT* ball must be set HIGH. Alternatively this can be set through the **VI_ASGMT_0** register using the **LNK_ASGMT_SEL** parameter. The parameter **REG_CTRL_LNK _ASGMT_SEL_EN** can be used to override the ball setting.

Note: Link ordering is done in the Virtual Interface, see Figure 3-6, after audio, ANC and TC insertion/extraction. Although links will be reordered and MUXed correctly on output, the streams used in the processing blocks will keep input order.

3.4.3.7. MUX Manual Input Channel Assignment

In cases where the PID is not defined, incorrect, or missing, the input can be manually rearranged into the UHD multiplexer. The virtual interface allows manual reassignment of an input. Manual input assignment can be enabled through the

MANUAL_CTRL_LNK_ASGMT parameter in the **VI_ASGMT_0** register for M0 and M1 path. For the M0 path, the **VI0_CH<n>_SEL** parameter can be used to select which input is assigned to each channel container. For the M1 path, the **VI1_CH<n>_SEL** parameter can be used to select which input is assigned to each channel container.

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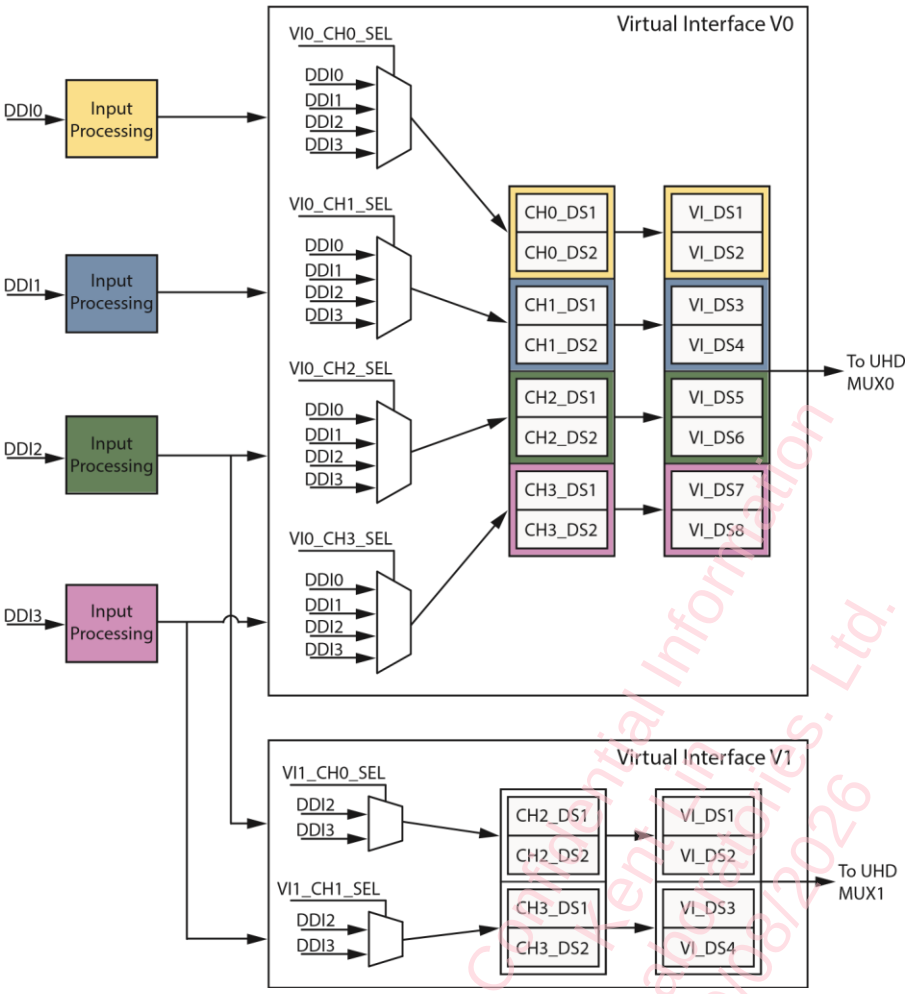

Figure 3-6: Virtual Interface

3.4.3.8. Signal Processing in MUX Mode

3.4.3.8.1. Sync-Bit Insertion Decoding

The inserted sync-bit in the input 6Gb/s and 12Gb/s video stream are reversed in the receiver, restoring the original $3FF_h$ and 000_h data patterns.

The sync-bit reversing block is placed on the input immediately after the word alignment block.

3.4.3.8.2. Audio

Both the SDI audio de-embedding from the input video streams and the SDI audio embedding into the output SDI video streams are available when the GS12270 is in MUX Mode. By default, both functions are disabled on power-up. See 3.7 SDI Audio Embedding and 3.8 SDI Audio De-Embedding for details.

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3.4.3.8.3. ANC Data

ANC data detection, extraction, deletion and insertion are available when the GS12270 is in MUX Mode. By default, both functions are disabled on power-up. See 3.9 ANC Data Processing for details.

3.4.3.8.4. Time Code (TC)

Both TC insertion and TC extraction are available when the GS12270 is in MUX Mode. By default, both functions are disabled on power-up. See 3.10 Time Code (TC) Processing for details.

3.4.3.8.5. Line Numbers

Embedded line numbers in original input streams are not changed.

3.4.3.8.6. Timing Signals

Embedded EAV (End of Active Video) and SAV (Start of Active Video) timing references are not altered.

3.4.3.8.7. Output Line CRC Generation

New CRC (Cyclic Redundancy Check) codes are calculated for each output data stream after all signal processing is performed.

3.4.3.9. Embedded Video Pattern Generator

The GS12270 contains a video pattern generator (PG) capable of generating various 4K video patterns on DL6G and 12GUHD interfaces for video system debug, design bring-up, and optimization. The PG does not utilize any shaping (rise and fall times) for individual bars or for custom patterns.

PG can be enabled via the **OPERATING_MODE_SEL_REG** register, address 0001_h, by setting bit 13 to '1' (parameter **SEL_PG**). The device must then be set to MUX Operating Mode, and the Gearbox Mode should be set to desired output standard (i.e. QL3G□SL12G, QL3G□DL6G or QL1.5□SL6G).

If parameter **PG_REF_INT_EXTB** is set to 1, timing signals used to generate patterns are extracted from a video stream via *DDI0*. A valid SDI signal must be connected to the *DDI0* input and its data rate must match the input data rate of the selected Gearbox Mode (i.e. 3G input for QL3G□SL12G mode). In the case when parameter **PG_REF_INT_EXTB** is set to 0 timing signals are generated internally and there is no need for a signal at DDI0.

The default pattern after reset or power-up is Colour Bars 75%, but there are additional patterns that can be selected through register 3000_h: Colour Bars 100%, several flat field patterns, Luma/Chroma ramp, and a few repetitive patterns allowing generation of pathological patterns on 12G and 6G SDI interface. The Luma/Chroma ramp pattern can also be inserted as a box in the existing pattern. Dimensions and position of the box can be set through the CSR. Predefined patterns are listed in Table 3-20.

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Table 3-20: Predefined Pattern Selection

PG_PATTERN_SEL	Pattern	Visual Representation
0000	Colour bars 70%	
0001	Colour bars 100%	
0010	Checkfield	
0011	Luma/Chroma (Y/C) ramp	
0100	EQ test signal	
0101	PLL test signal	
0110	—	—
0111	Reserved	—
1000	White	
1001	Yellow	

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1010	Cyan	
1011	Green	
1100	Magenta	
1101	Red	
1110	Blue	
1111	Black	

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3.4.4. Demultiplex Mode

3.4.4.1. Conversion Selection

In DEMUX Mode, conversion modes are illustrated in Figure 3-7. Conversion modes can be selected either manually (default) or a semi-auto option can be selected using register **MANUAL_RATE** bit **SDI_AUTO_MODE_EN**.

When manual selection is chosen, register **SDI_AUTO_MODE_EN** = 0, the conversion mode can be set through the *MODE_SEL[2:0]* balls. The **OPERATING_MODE_SEL _REG** register can also be used to select the conversion mode and override the ball settings. The **MODE_SEL** parameter is used to set the mode and the **REG_CTRL_MODE_SEL_EN** parameter is used to enable the ball override.

The mode selection settings are listed in Table 3-21.

Table 3-21: DEMUX Mode Down Conversion

Balls				DEMUX Mode		Notes (Refer to Figure 3-7)
MUX/DEMUX	MODE_SEL2	MODE_SEL1	MODE_SEL0	Input	Output	
0	1	1	1	SL 12Gb/s	QL 3Gb/s	(a)
0	1	1	0	SL 6Gb/s	QL 1.5Gb/s	(b)
0	1	0	1	DL 12Gb/s	QL 6Gb/s	(c)
0	1	0	0	DL 6Gb/s	QL 3Gb/s	(d)
0	0	1	1	SL 12Gb/s	DL 6Gb/s	(e)
0	0	1	0	SL 6Gb/s	DL 3Gb/s	(f)
0	0	0	1	SL 3Gb/s	DL 1.5Gb/s	(g)
0	0	0	0	RSVD	RSVD	—

When the semi-auto option is selected, register **SDI_AUTO_MODE_EN** = 1, the DEMUX mode conversion is selected based on the detected PID in the input data stream and the value of the **SDI_AUTO_MODE_OUT_INTERF** registers.

The input data stream for PID detection is the data stream from the DDI0 input when **INPUT_SELECT** is 0 or from DDI2 input when **INPUT_SELECT** is 1. The detected PID, used for mode conversion selection when semi-auto option is selected, can be overridden using **PID_BYTE1_AUTO** and **PID_BYTE1_AUTO_OVR**. Additionally, if **REG_CTRL_MODE_SEL_EN** is set, the semi-auto selection is overridden by **MODE_SEL** parameter.

In the case where output selection can be ambiguous, for example: SL12G input can be demultiplexed either as DL6G or QL3G, register bit **SDI_AUTO_MODE_OUT_INTERF** can be used to select the preferred interface.

Users should select either manual or semi-auto conversion selection based on their application requirements.

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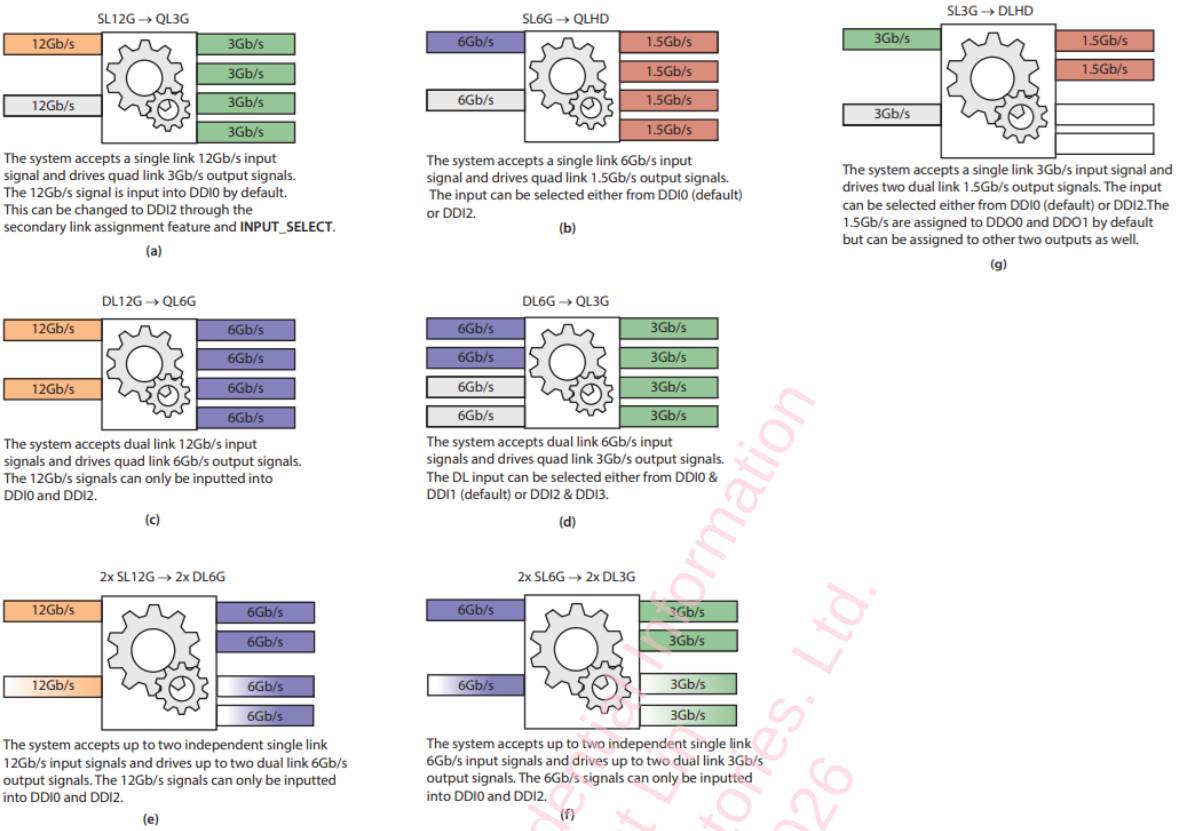

Figure 3-7: DEMUX Conversion Modes

Note:

- In Figure 3-7, e) and f), solid coloured inputs use path DM0 and gradient coloured inputs use path DM1. See Section 3.4.4.2 for further details.
- Audio, ANC and TC extraction/insertion is supported only in DM0 path.
- In DL12G □ QL6G mode audio, ANC and TC extraction/insertion is not supported.

3.4.4.2. Demultiplexing Paths

The DEMUX modes will enable one of two paths based on the selected conversion mode.

For quad link outputs the DM0 path is used.

For dual link outputs both DM0 and DM1can be used based on the application requirement. By default, DM1 is powered-down. To enable DM1, the *SEC_LINK_ENABLE* ball should be driven HIGH. There is a major difference between DM0 and DM1 paths such that the additional processing, audio, ANC and TC insertion/extraction, is supported only in DM0 path.

Alternatively, the parameter **SEC_LINK_REG** within the **OPERATING_MODE_SEL_REG** register can be used. The parameter **REG_CTRL_SEC_LINK_EN** is used to override the ball control and enable the register selection of this feature.

It is not required that data streams (SL or DL) at DM0 and DM1 path are frequency-locked, they can even have different frame rates (59.94 vs 60&50) but they have to be same data rate because the mode selection is common for both DM0 and DM1 paths.

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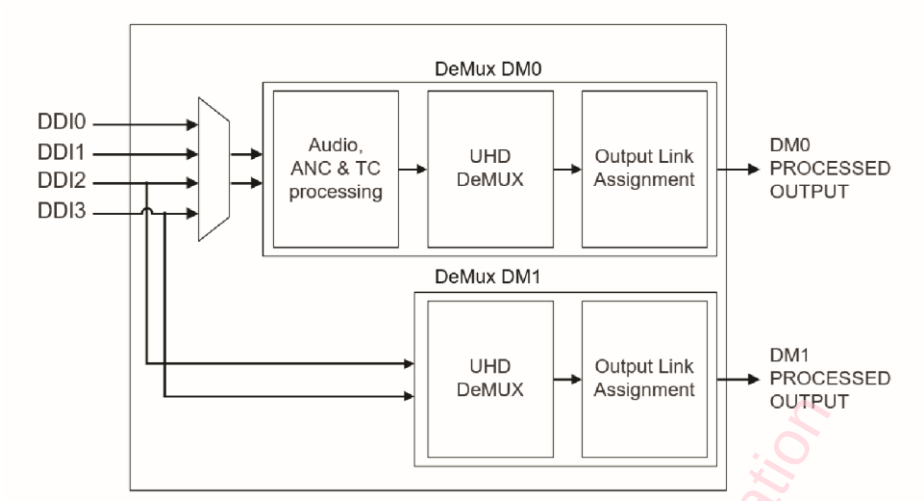

Figure 3-8: Demultiplexing Paths

The DL12G □ QL6G DEMUX case differs from all other DL input DEMUX cases in the way data is routed, and as a consequence the audio, ANC and time code processing is not supported in the DL12G □ QL6G mode. Figure 3-12 illustrate DL12G □ QL6G signal flow. Please note that DL input connection is at DDI0 and DDI2 versus DDI0 and DDI1 for all other DL inputs.

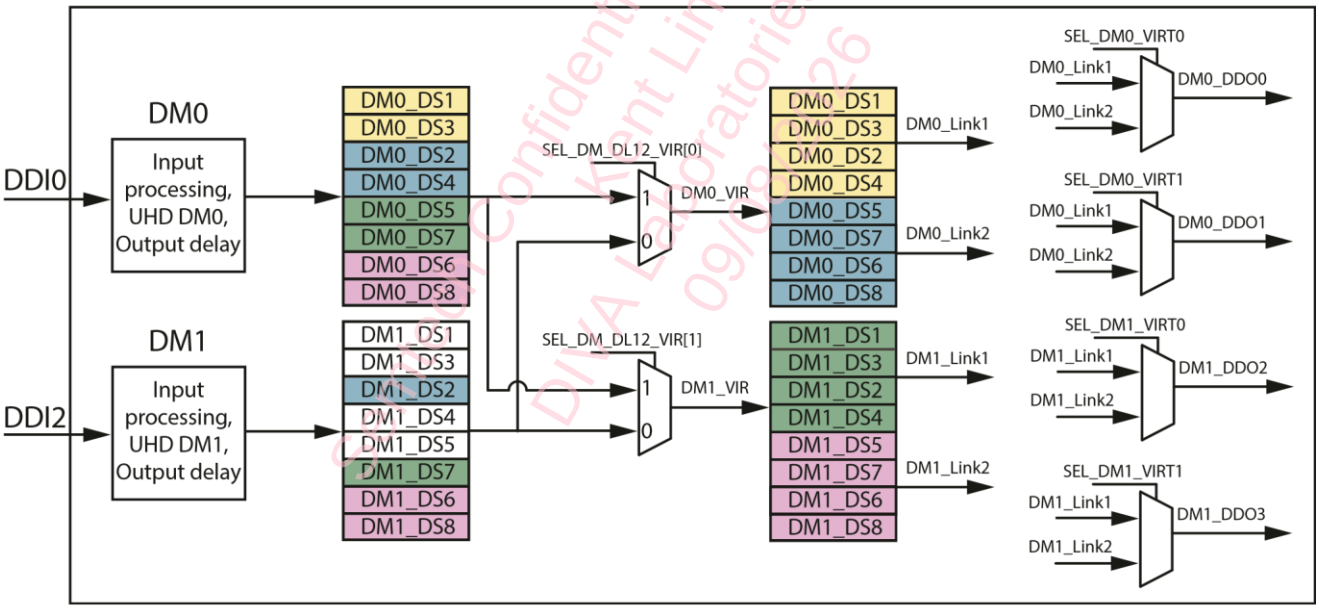

Figure 3-9: DL12G-QL6G Output Link Assignment

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3.4.4.3. SMPTE Compatibility

Table 3-22 outlines the conversion mappings that are compatible to the SMPTE UHD standards.

By default, the input streams will be de-multiplexed according to the mappings defined by the SMPTE UHDTV standards. The Payload ID can be inserted manually, if required.

If the **PID_MODE_REG** parameter is set to '11' in the **OPERATING_MODE_SEL_REG** register, Automatic PID Insertion is disabled. Note that the **REG_CTRL_OP_MODE_EN** parameter must be set HIGH for Automatic PID Insertion to be handled by the **PID_MODE_REG** parameter.

Table 3-22: DEMUX Mode SMPTE Compatibility

DEMUX Mode		Supported SMPTE Mapping	
Input	**Output**	**Input Mapping**	**Output Mapping**
SL 6Gb/s	QL 1.5Gb/s	ST2081-10 2160-line Mode 1	ST274 – 30/25/24 FR, progressive
SL 6Gb/s	DL 3Gb/s	ST2081-10 1080-line Mode 2 ST2081-10 2160-line Mode 1	ST425-3 1080-line Level A Mapping ST425-3 2160-line Mapping
SL 12Gb/s	DL 6Gb/s	ST2082-10 2160-line Mode 1 ST2082-10 1080-line Mode 2	ST2081-11 2160-line Mode 1 ST2081-11 1080-line Mode 2
DL 12Gb/s	QL 6Gb/s	ST2082-11 4320-line Mode 1 ST2082-11 2160-line Mode 2 ST-2082-11 2160-line Mode 3	ST2081-12 4320-line Mode 1 ST2081-12 2160-line Mode 2 ST2081-12 2160-line Mode 3

3.4.4.4. DEMUX Output Link Assignment

By default, the SMPTE multi-link outputs are mapped as follows:

Table 3-23: Default Output Assignment of Multi-link Standards

Output	Quad Link Outputs	Dual Link Outputs
DDO0	Link 1	DM0 Link 1
DDO1	Link 2	DM0 Link 2
DDO2	Link 3	DM1 Link 1
DDO3	Link 4	DM1 Link 2

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The default output assignment can be custom defined. Manual output link assignment can be enabled through the parameter **REG_CTRL_SEL_DM0_VIRT** in the **SEL_DM0_VIRT** register for DM0 path.

For the DM1 path, the parameter **REG_CTRL_SEL_DM1_VIRT** in the **SEL_DM1_VIRT** register should be used.

For the DM0 path, **SEL_DM0_VIRT<n>** parameter can be used to select which link is assigned to each DDO Output.

For the DM1 path, **SEL_DM1_VIRT<n>** parameter can be used to select which input is assigned to each DDO Output.

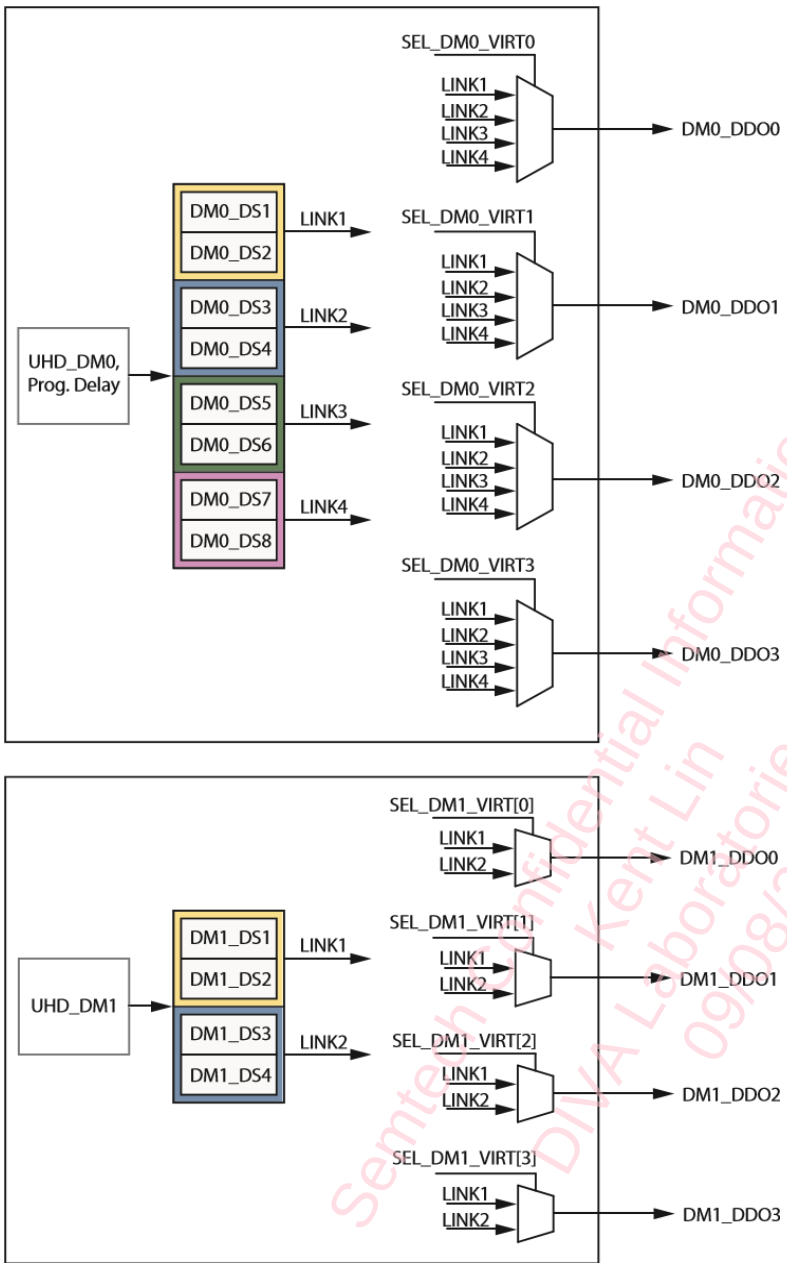

Figure 3-10: Output Link Assignment Selection

3.4.4.5. Secondary Input Selection

By default, in the SL→DL and SL→QL Mode, the data selected to DM0 is from DDI0 input and in the DL □ QL Mode from the DDI0 & DDI1 inputs. However, it is possible to change the DM0 input to DDI2 for SL inputs or DD2 & DDI3 for DL inputs. In order to be able to switch input(s), secondary link needs to be powered-up (if it isn't already, either by **SEC_LINK_ENABLE** ball or through registers). When secondary link is enabled, either ball *INPUT_SELECT* (L14) or register **SDI_IN_SEL**, can be used to select inputs on DM0 path. Please note that manual conversion selection, instead of semi-auto, should be used if the input selection is required.

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3.4.4.6. DEMUX Mode Supported SMPTE Standards

In the DEMUX Mode the GS12270 de-multiplexes video input stream or streams according to the mapping process described in SMPTE UHDTV standard suite and as listed in Table 3-24.

Table 3-24: Supported SMPTE Compatible DEMUX Modes

DEMUX Mode		Supported SMPTE Mapping	
Input	**Output**	**Input Mapping**	**Output Mapping**
SL 6Gb/s	QL 1.5Gb/s	ST2081-10 2160-line Mode 1	ST274 – 30/25/24 FR, progressive
SL 6Gb/s	DL 3Gb/s	ST2081-10 1080-line Mode 2 Not Supported ST2081-10 2160-line Mode 1	ST425-3 1080-line Level A Mapping ST425-3 1080-line Level B DL Mapping ST425-3 2160-line Mapping
DL 6Gb/s	QL 3Gb/s	ST2081-11 2160-line Mode 1 Not supported	ST425-5 2160-line Level A Mapping ST425-5 2160-line Level B Mapping
SL 12Gb/s	QL 3Gb/s	ST2082-10 2160-line Mode 1 Not Supported	ST425-5 2160-line Level A Mapping ST425-5 2160-line Level B Mapping
SL 12Gb/s	DL 6Gb/s	ST2082-10 2160-line Mode 1 ST2082-10 1080-line Mode 2	ST2082-11 2160-line Mode 1 ST2082-11 1080-line Mode 2
DL 12Gb/s	QL 6Gb/s	ST2082-11 4320-line Mode 1 ST2082-11 2160-line Mode 2 ST2082-11 2160-line Mode 3	ST2081-12 4320-line Mode 1 ST2081-12 2160-line Mode 2 ST2081-12 2160-line Mode 3

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3.4.4.7. Signal Processing in DEMUX Mode

3.4.4.7.1. Audio

Both the SDI audio de-embedding from the input video streams and the SDI audio embedding into the output SDI video streams are available when the GS12270 is in the DEMUX Mode. By default, both functions are disabled on power-up. See 3.7 SDI Audio Embedding and 3.8 SDI Audio De-Embedding for details.

3.4.4.7.2. ANC Data

ANC data detection, extraction, deletion and insertion are available when the GS12270 is in DEMUX Mode. By default, both functions are disabled on power-up. See 3.9 ANC Data Processing for details.

3.4.4.7.3. Time Code (TC)

Both TC insertion and TC extraction are available when the GS12270 is in DEMUX Mode. By default, both functions are disabled on power-up. See 3.10 Time Code (TC) Processing for details.

3.4.4.7.4. Line Numbers

Embedded line numbers in the original input video data for each embedded data stream are not changed.

3.4.4.7.5. Timing Signals

Embedded EAV (End of Active Video) and SAV (Start of Active Video) timing references in the original input video data for each embedded data stream are not altered.

3.4.4.7.6. Input Line CRC Checking

CRC codes are checked for each input data stream and errors are reported via the host interface.

3.4.5. Bypass Mode

In Bypass Mode, the GS12270 automatically bypasses 12Gb/s, 6Gb/s, 3Gb/s, and 1.5Gb/s video data from the input to the output, if all the inputs are synchronous. By default, the input to output assignment:

- DDI0 is assigned to DDO0
- DDI1 is assigned to DDO1
- DDI2 is assigned to DDO2
- DDI3 is assigned to DDO3

If required, any of the synchronous inputs can be assigned to any of the outputs using Output Assignment feature, Section 3.4.8.

If the inputs are asynchronous, only 3 clock domains can be supported in output.

CRC error and PID detection can be enabled in Bypass Mode. CRC and PID insertion as well as Audio, ANC data and Time Code insertion/extraction is not available in Bypass Mode.

Note: In manual mode, the device need to be in MUX mode in order to select bypass mode. If in DEMUX mode, both signals (bypass and MUX) need to be selected to enable bypass. In semi-auto mode, bypass *must* be selected.

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3.4.5.1. Input Stream Data Rate Detection in Bypass Mode

In Bypass Mode, when the input is 1.5G, 3G, 6G, or 12G, the GS12270 is able to automatically determine each input data rate and report it in the **DATA_RATE_REPORT** register, in the parameters **DATA_RATE_RX<n>**.

The data rate can be set manually through the parameter **REG_CTRL_MANUAL_RATE** in the **MANUAL_RATE** register.

3.4.5.2. SD Bypass Mode

The device is capable of passing through signals serialized as per SMPTE 259 at 270Mb/s rate in SD Bypass Mode only. SD Bypass Mode is manually selectable on a per-channel basis and only available when *BYPASS* is set HIGH.

The *SD_BYPASS* ball can be overwritten via the controls found in the **SD_BYPASS_SEL_REG** register.

When in the SD Bypass Mode, input data is oversampled. The default oversampling data rate is 3Gb/s. The oversampling introduces periodic jitter, with the p-p value proportional to the oversampling rate. The jitter can be reduced by increasing the oversampling rate to 6Gb/s. The oversampling rate can be set to 6Gb/s by setting **SD_BYPASS_ RATE_6G_3Gb** in register **SD_BYPASS_ SEL_REG** to 1.

3.4.5.3. PRBS Data Bypass

In the data rate detection process, the data rate detection block searches for TRS data words in the input data stream. Hence, the GS12270 is able to automatically determine input data rate only if the input is SDI video.

If the input is PRBS data, the GS12270 data rate has to be set manually to pass data.

In order to pass PRBS data, the following GS12270 registers need to be set:

- Address = 0006_h (**MANUAL_RATE**) data = depends on the data rate (should always be written first)
  - The register **MANUAL_RATE** should be set as the following for the different data rates:
  - 12G - $0FFF_h$
  - 6G - $0AAF_h$
  - 3G - $055F_h$
  - HD - $000F_h$
- Address = 0003_h (**INPUT_ LOCK_REG**) data = $0FF0_h$ - Input lock overwrite
- Address = $000A_h$ (**DDO_IDLE**) data = $0F00_h$ - Tx power down overwrite
- Address = 0008_h (**RSVD**) data = $00F0_h$ - Set internal ready signal HIGH (should always be written last)

3.4.5.4. Tx PLL's Clock Selection in Bypass Mode

The default clock for the transmitter's PLLs are the extracted clock from the receiver, from which, data connected to the transmitter are de-serialized.

3.4.6. Payload ID Handling

The GS12270 will automatically detect and replace the appropriate PID based on the selected mode. PID handling can be disabled through the **PID_MODE_REG** parameter in the **OPERATING _MODE_SEL _REG** register.

Note 1: Register control of the **MUX_DEMUX**, **PID_MODE_REG** and **BYPASS** are grouped. All three functions must either be Register controlled or ball controlled.

Note 2: PID handling is not available when the device is in the Bypass mode.

3.4.6.1. Detection of Payload ID

If a Payload ID is detected in the incoming video input, it can be read through the CSR. Based on the input format. Table 3-25 through Table 3-28 describe the registers where the Payload ID is stored.

Table 3-25: DEMUX Mode DM0 Payload ID Detected Registers

Input	Register	SL12→QL3	SL6→QLHD	DL12→QL6	SL12→DL6	DL6→QL3	SL6→DL3	SL6→DLHD
DDI0	PID_DET_CH0A_DS1_*	DDI0_DS1	DDI0_DS1	DDI0_DS1	DDI0_DS1	DDI0_DS1	DDI0_DS1	NA
	PID_DET_CH0A_DS2_*	DDI0_DS5	DDI0_DS3	DDI0_DS5	DDI0_DS5	DDI0_DS3	DDI0_DS3	NA
	PID_DET_CH0B_DS1_*	DDI0_DS3	DDI0_DS2	DDI0_DS3	DDI0_DS3	DDI0_DS2	DDI0_DS2	DDI0_DS1
	PID_DET_CH0B_DS2_*	DDI0_DS7	DDI0_DS4	DDI0_DS7	DDI0_DS7	DDI0_DS4	DDI0_DS4	DDI0_DS2
DDI1	PID_DET_CH1A_DS1_*	DDI0_DS2	NA	DDI0_DS2	DDI0_DS2	NA	NA	NA

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	PID_DET_CH1A_DS2_*	DDI0_DS6	NA	DDI0_DS6	DDI0_DS6	NA	NA	NA
	PID_DET_CH1B_DS1_*	DDI0_DS4	NA	DDI0_DS4	DDI0_DS4	NA	NA	NA
	PID_DET_CH1B_DS2_*	DDI0_DS8	NA	DDI0_DS8	DDI0_DS8	NA	NA	NA
DDI2	PID_DET_CH2A_DS1_*	NA	NA	DDI2_DS1	NA	DDI2_DS1	NA	NA
	PID_DET_CH2A_DS2_*	NA	NA	DDI2_DS5	NA	DDI2_DS3	NA	NA
	PID_DET_CH2B_DS1_*	NA	NA	DDI2_DS3	NA	DDI2_DS2	NA	NA
	PID_DET_CH2B_DS2_*	NA	NA	DDI2_DS7	NA	DDI2_DS4	NA	NA
DDI3	PID_DET_CH3A_DS1_*	NA	NA	DDI2_DS2	NA	NA	NA	NA
	PID_DET_CH3A_DS2_*	NA	NA	DDI2_DS6	NA	NA	NA	NA
	PID_DET_CH3B_DS1_*	NA	NA	DDI2_DS4	NA	NA	NA	NA
	PID_DET_CH3B_DS2_*	NA	NA	DDI2_DS8	NA	NA	NA	NA

Table 3-26: DEMUX Mode DM1 Payload ID Detected Registers

Input	Register	SL12→QL3	SL6→DL3
DDI2	PID_DET_CH2A_DS1_*	DDI2_DS1	DDI2_DS1
	PID_DET_CH2A_DS2_*	DDI2_DS5	DDI2_DS3
	PID_DET_CH2B_DS1_*	DDI2_DS3	DDI2_DS2
	PID_DET_CH2B_DS2_*	DDI2_DS7	DDI2_DS4
DDI3	PID_DET_CH3A_DS1_*	DDI2_DS2	NA
	PID_DET_CH3A_DS2_*	DDI2_DS6	NA
	PID_DET_CH3B_DS1_*	DDI2_DS4	NA
	PID_DET_CH3B_DS2_*	DDI2_DS8	NA

Table 3-27: MUX Mode M0 Payload ID Detected Registers

Input	Register	QL3→SL12	QLHD→SL6	QL6→DL12	DL6→SL12	QL3→DL6	DL3→SL6	DLHD→SL3
DDI0	PID_DET_CH0A_DS1_*	DDI0_DS1	DDI0_DS1	DDI0_DS1	DDI0_DS1	DDI0_DS1	DDI0_DS1	DDI0_DS1
	PID_DET_CH0A_DS2_*	DDI0_DS2	NA	DDI0_DS3	DDI0_DS3	DDI0_DS1	DDI0_DS1	NA
	PID_DET_CH0B_DS1_*	NA	NA	DDI0_DS2	DDI0_DS2	NA	NA	NA
	PID_DET_CH0B_DS2_*	NA	NA	DDI0_DS4	DDI0_DS4	NA	NA	NA

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DDI1	PID_DET_CH1A_DS1_*	DDI1_DS1	DDI1_DS1	DDI1_DS1	DDI1_DS1	DDI1_DS1	DDI1_DS1	DDI1_DS1
	PID_DET_CH1A_DS2_*	DDI1_DS2	NA	DDI1_DS3	DDI1_DS3	DDI1_DS2	DDI1_DS2	NA
	PID_DET_CH1B_DS1_*	NA	NA	DDI1_DS2	DDI1_DS2	NA	NA	NA
	PID_DET_CH1B_DS2_*	NA	NA	DDI1_DS4	DDI1_DS4	NA	NA	NA
DDI2	PID_DET_CH2A_DS1_*	DDI2_DS1	DDI2_DS1	DDI2_DS1	NA	DDI2_DS1	NA	NA
	PID_DET_CH2A_DS2_*	DDI2_DS2	NA	DDI2_DS3	NA	DDI2_DS2	NA	NA
	PID_DET_CH2B_DS1_*	NA	NA	DDI2_DS2	NA	NA	NA	NA
	PID_DET_CH2B_DS2_*	NA	NA	DDI2_DS4	NA	NA	NA	NA
DDI3	PID_DET_CH3A_DS1_*	DDI3_DS1	DDI3_DS1	DDI3_DS1	NA	DDI3_DS1	NA	NA
	PID_DET_CH3A_DS2_*	DDI3_DS2	NA	DDI3_DS3	NA	DDI3_DS2	NA	NA
	PID_DET_CH3B_DS1_*	NA	NA	DDI3_DS2	NA	NA	NA	NA
	PID_DET_CH3B_DS2_*	NA	NA	DDI3_DS4	NA	NA	NA	NA

Table 3-28: MUX Mode M1 Payload ID Detected Registers

Input	Register	DL6→SL12	DL3→SL6
DDI2	PID_DET_CH2A_DS1_*	DDI2_DS1	DDI2_DS1
	PID_DET_CH2A_DS2_*	DDI2_DS3	DDI2_DS2
	PID_DET_CH2B_DS1_*	DDI2_DS2	NA
	PID_DET_CH2B_DS2_*	DDI2_DS4	NA
DDI3	PID_DET_CH3A_DS1_*	DDI3_DS1	DDI3_DS1
	PID_DET_CH3A_DS2_*	DDI3_DS3	DDI3_DS2
	PID_DET_CH3B_DS1_*	DDI3_DS2	NA
	PID_DET_CH3B_DS2_*	DDI3_DS4	NA

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3.4.6.2. Automatic Insertion of Payload ID

Automatic insertion of SMPTE ST 352 Payload ID by the GS12270 involves the replacement of PID Byte 1 and modification of the Link number bits in PID Byte 4.

The structure of the inserted Payload ID is shown in Table 3-29 for DEMUX mode and Table 3-30 for MUX mode.

If the detected Payload ID (Byte 1) is valid for the selected conversion mode, the GS12270 will replace the outgoing Payload ID with the appropriate value.

If the detected Payload ID does not match the expected value for the selected conversion mode or if it is missing, the GS12270 will insert a default Payload ID value.

The Payload ID will be inserted in every data stream of the Virtual Interface. If the data stream carries a full 4:2:2 sub image with multiplexed Luma (Y) and Chroma (C) data, the payload ID will be inserted in the Y channel only. The Payload ID will be inserted once per frame in Line 10, immediately following an EAV word sequence as defined in ST352, ST2082-10 (11 and12), ST2081-10 (and 11) and ST425-5. If needed, the **PID_BYTE_OVERRIDE**, default 1111, can be used as a mask to disable insertion of masked bytes. For example, if the user wants to replace only PID byte1 she can set **PID_BYTE_OVERRIDE** to 0001.

If there are any other data already in the ancillary space in Line 10 immediately after the last EAV word (CRC1), they will be overwritten by the Payload ID words. In such a case, the user can set **REPLACE_EXISTING_PID**. **REPLACE_EXISTING_PID** will enable replacement of PID placed anywhere in ANC space.

Table 3-29: DEMUX Mode PID Auto Replacement Definition

Mode	Input	Output	PID Byte 1 Detected	PID Inserted			
				BYTE1	BYTE 2	BYTE 3	BYTE 4
SL12→QL3	2160 Mode 1	2160 Level A	CEh	97h	BYTE2_DET	BYTE3_DET	LINK#&0& BYTE4_DET[4:0]
			All others	97h	C0h	80h	LINK#&000001
SL6→QL1.5	2160 Mode 1	1080 30/29.94	C0h	85h	BYTE2_DET	0 & BYTE3_DET[6:7] & BYTE3_DET[3:0]	010&BYTE4_ DET[4:0]
			All others	85h	C0h	80h	41h
DL12→QL6	4320 Mode 1	4320 Mode 1	D0h	C4h	BYTE2_DET	BYTE3_DET	0&LINK#& BYTE4_DET[4:0]
	2160 Mode 2	2160 Mode 2	D1h	C5h	BYTE2_DET	BYTE3_DET	0&LINK#& BYTE4_DET[4:0]
			All others	C4h (data interleaved) or C5h	C0h	80h	0&LINK#&00001
SL12→DL6	2160 Mode 1	2160 Mode 1	CEh	C2h	BYTE2_DET	BYTE3_DET	0&LINK#& BYTE4_DET[4:0]
	1080 Mode 2	1080 Mode 2	CFh	C3h	BYTE2_DET	BYTE3_DET	0&LINK#& BYTE4_DET[4:0]
			All others	C2h	C0h	80h	0&LINK#&00001
DL6→QL3	2160 Mode 1	2160 Level A	C2h	97h	BYTE2_DET	BYTE3_DET	LINK#&0& BYTE4_DET[4:0]
			All others	97h	C0h	80h	LINK#&000001
SL6→DL3	2160 Mode 1	2160 on DL 3G	C0h	96h	BYTE2_DET	BYTE3_DET[5:7] & BYTE3_DET[4:0]	LINK#&0& BYTE4_DET[4:0]
	1080 Mode 2	1080 Level A	C1h	94h	BYTE2_DET	BYTE3_DET[7:6] & 00 & BYTE3_DET[3:0]	LINK#&0& BYTE4_DET[4:0]
			All others	96h (data interleaved) or 94h	C0h	80h	LINK#&000001
SL3→DL1.5	No PID insertion. User should manually insert PIDs if needed						

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Table 3-30: MUX Mode PID Auto Replacement Definition

Mode	Input	Output	PID Byte 1 Detected	PID Inserted			
				BYTE1	BYTE 2	BYTE 3	BYTE 4
QL3→ SL12	2160 Level A	2160 Mode 1	97h	CEh	BYTE2_DET	BYTE3_DET	000 & BYTE4_DET[4:0]
			All others	CEh	C0h	B0h	01h
QL1.5→ SL6	1080 30/29.94	2160 Mode 1	85h	C0h	BYTE2_DET	BYTE3_DET[5:6] & 11 & BYTE3_DET[3:0]	000 & BYTE4_DET[4:0]
			All others	C0h	C0h	B0h	01h
QL6→ DL12	4320 Mode 1	4320 Mode 1	C4h	D0h	BYTE2_DET	BYTE3_DET	0&LINK# & BYTE4_DET[4:0]
	2160 Mode 2	2160 Mode 2	C5h	D1h	BYTE2_DET	BYTE3_DET	0&LINK# & BYTE4_DET[4:0]
			All others	D0h (data interleaved) or D1h	C0h	80h	0&LINK# & 00001
DL6→ SL12	2160 Mode 1	2160 Mode 1	C2h	CEh	BYTE2_DET	BYTE3_DET	000 & BYTE4_DET[4:0]
	1080 Mode 2	1080 Mode 2	C3h	CFh	BYTE2_DET	BYTE3_DET	000 & BYTE4_DET[4:0]
			All others	CEh	C0h	B0h	01h
QL3→ DL6	2160 Level A	2160 Mode 1	97h	C2h	BYTE2_DET	BYTE3_DET	0&LINK# & BYTE4_DET[4:0]
			All others	C2h	C0h	B0h	0&LINK# & 00001
DL3→ SL6	2160 on DL 3G	2160 Mode 1	96h	C0h	BYTE2_DET	BYTE3_DET[5:7] & BYTE3_DET[4:0]	000 & BYTE4_DET[4:0]
			94h	C1h	BYTE2_DET	BYTE3_DET	000 & BYTE4_DET[4:0]
			All others	C0h (data interleaved) or C1h	C0h	B0h	01h
DL1.5→ SL3	No PID insertion. User should manually insert PIDs if needed						

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3.4.6.3. Manual Insertion of Payload ID

Payload ID values can be inserted manually through the **PID_INS<n>** registers.

In addition, specific bytes of Payload ID can be masked so they are not overwritten. The bytes to be masked are defined within the **PID_BYTE_OVERRIDE** parameter in the **PID_PROGRAM_CTRL** register.

For convenience, there are three methods in which this can be accomplished. Table 3-31 shows the register settings for these three modes of operation.

Table 3-31: PID Insertion Mode

	PID_PROGRAM_CTRL Register	
	PID_WR_FAST_MODE Bit	**PID_OVERRIDE Bit**
Automatic PID Insertion	0	0
Manual-Fast Mode	1	0
Manual-Fast Mode with DS Selection	1	1
Full Manual Mode	0	1

In Fast Mode, one Payload ID is defined and inserted in all of the outgoing data streams. The PID values to be inserted must be written to the **PID_INS_CH0A_DS1_BYTE_1_2** and **PID_INS_CH0A_DS1_BYTE_3_4**.

In Fast Mode with Data Stream Selection, one Payload ID is defined and inserted in all of the selected outgoing data streams. The data stream in which the PID is to be inserted is defined by the **PID_PROGRAM_STREAM_MASK** register.

In Full Manual Mode Payload ID for each stream must be set, according to stream mapping defined in Table 3-32 to Table 3-35.

The data stream in which the PID is to be inserted is defined by the **PID_PROGRAM_STREAM_MASK** registers.

Table 3-32 to Table 3-35 define the PID insertion registers for all streams and operating modes.

- Table 3-32: DEMUX Mode DM0 Payload ID Insertion Registers
- Table 3-33: DEMUX Mode DM1 Payload ID Insertion Registers
- Table 3-34: MUX Mode M0 Payload ID Insertion Registers
- Table 3-35: MUX Mode M1 Payload ID Insertion Registers

Table 3-32: DEMUX Mode DM0 Payload ID Insertion Registers

Register	□QL3	SL6□QL1.5	DL12□QL6	SL12□DL6	DL6□QL3	SL6□DL3	SL3□DL1.5
PID_INS_CH0A_DS1_*	DDO0_DS1	DDO0_DS1	DDO0_DS1	DDO0_DS1	DDO0_DS1	DDO0_DS1	DDO0_DS1
PID_INS_CH0A_DS2_*	DDO2_DS1	DDO2_DS1	DDO1_DS1	DDO1_DS1	DDO1_DS1	DDO1_DS1	DDO1_DS1
PID_INS_CH0B_DS1_*	DDO1_DS1	DDO1_DS1	DDO0_DS3	DDO0_DS3	DDO0_DS2	DDO0_DS2	DDO0_DS2
PID_INS_CH0B_DS2_*	DDO3_DS1	DDO3_DS1	DDO1_DS3	DDO1_DS3	DDO1_DS2	DDO1_DS2	DDO1_DS2
PID_INS_CH1A_DS1_*	DDO0_DS2	NA	DDO0_DS2	DDO0_DS2	NA	NA	NA
PID_INS_CH1A_DS2_*	DDO2_DS2	NA	DDO1_DS2	DDO1_DS2	NA	NA	NA
PID_INS_CH1B_DS1_*	DDO1_DS2	NA	DDO0_DS4	DDO0_DS4	NA	NA	NA
PID_INS_CH1B_DS2_*	DDO3_DS2	NA	DDO1_DS4	DDO1_DS4	NA	NA	NA
PID_INS_CH2A_DS1_*	NA	NA	DDO2_DS1	NA	DDO2_DS1	NA	NA
PID_INS_CH2A_DS2_*	NA	NA	DDO3_DS1	NA	DDO3_DS1	NA	NA

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PID_INS_CH2B_DS1_*	NA	NA	DDO2_DS3	NA	DDO2_DS2	NA	NA
PID_INS_CH2B_DS2_*	NA	NA	DDO3_DS3	NA	DDO3_DS2	NA	NA
PID_INS_CH3A_DS1_*	NA	NA	DDO2_DS2	NA	NA	NA	NA
PID_INS_CH3A_DS2_*	NA	NA	DDO3_DS2	NA	NA	NA	NA
PID_INS_CH3B_DS1_*	NA	NA	DDO2_DS4	NA	NA	NA	NA
PID_INS_CH3B_DS2_*	NA	NA	DDO3_DS4	NA	NA	NA	NA

Table 3-33: DEMUX Mode DM1 Payload ID Insertion Registers

Register	SL12□DL6	SL6□DL3
PID_INS_CH2A_DS1_*	DDO2_DS1	DDO2_DS1
PID_INS_CH2A_DS2_*	DDO3_DS1	DDO3_DS1
PID_INS_CH2B_DS1_*	DDO2_DS3	DDO2_DS2
PID_INS_CH2B_DS2_*	DDO3_DS3	DDO3_DS2
PID_INS_CH3A_DS1_*	DDO2_DS2	NA
PID_INS_CH3A_DS2_*	DDO3_DS2	NA
PID_INS_CH3B_DS1_*	DDO2_DS4	NA
PID_INS_CH3B_DS2_*	DDO3_DS4	NA

Table 3-34: MUX Mode M0 Payload ID Insertion Registers

Register	QL3□SL12	QL1.5□SL6	QL6□DL12	DL6□SL12	QL3□DL6	DL3□SL6	DL1.5□SL3
PID_INS_CH0A_DS1_*	DDO0_DS1	DDO0_DS1	DDO0_DS1	DDO0_DS1	DDO0_DS1	DDO0_DS1	DDO0_DS1
PID_INS_CH0A_DS2_*	DDO0_DS2	NA	DDO0_DS3	DDO0_DS3	DDO0_DS2	DDO0_DS2	NA
PID_INS_CH0B_DS1_*	NA	NA	DDO0_DS2	DDO0_DS2	NA	NA	NA
PID_INS_CH0B_DS2_*	NA	NA	DDO0_DS4	DDO0_DS4	NA	NA	NA
PID_INS_CH1A_DS1_*	DDO0_DS3	DDO0_DS2	DDO0_DS5	DDO0_DS5	DDO0_DS3	DDO0_DS3	DDO0_DS2
PID_INS_CH1A_DS2_*	DDO0_DS4	NA	DDO0_DS7	DDO0_DS7	DDO0_DS4	DDO0_DS4	NA
PID_INS_CH1B_DS1_*	NA	NA	DDO0_DS6	DDO0_DS6	NA	NA	NA
PID_INS_CH1B_DS2_*	NA	NA	DDO0_DS8	DDO0_DS8	NA	NA	NA
PID_INS_CH2A_DS1_*	DDO0_DS5	DDO0_DS3	DDO2_DS1	NA	DDO2_DS1	NA	NA

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Kent Lin
DVA Laboratories. Ltd.
09/08/2026

PID_INS_CH2A_DS2_*	DDO0_DS6	NA	DDO2_DS3	NA	DDO2_DS2	NA	NA
PID_INS_CH2B_DS1_*	NA	NA	DDO2_DS2	NA	NA	NA	NA
PID_INS_CH2B_DS2_*	NA	NA	DDO2_DS4	NA	NA	NA	NA
PID_INS_CH3A_DS1_*	DDO0_DS7	DDO0_DS4	DDO2_DS5	NA	DDO2_DS3	NA	NA
PID_INS_CH3A_DS2_*	DDO0_DS8	NA	DDO2_DS7	NA	DDO2_DS4	NA	NA
PID_INS_CH3B_DS1_*	NA	NA	DDO2_DS6	NA	NA	NA	NA
PID_INS_CH3B_DS2_*	NA	NA	DDO2_DS8	NA	NA	NA	NA

Table 3-35: MUX Mode M1 Payload ID Insertion Registers

Register	DL6□SL12	DL3□SL6
PID_INS_CH2A_DS1_*	DDO2_DS1	DDO2_DS1
PID_INS_CH2A_DS2_*	DDO2_DS3	DDO2_DS2
PID_INS_CH2B_DS1_*	DDO2_DS2	NA
PID_INS_CH2B_DS2_*	DDO2_DS4	NA
PID_INS_CH3A_DS1_*	DDO2_DS5	DDO2_DS3
PID_INS_CH3A_DS2_*	DDO2_DS7	DDO2_DS4
PID_INS_CH3B_DS1_*	DDO2_DS6	NA
PID_INS_CH3B_DS2_*	DDO2_DS8	NA

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09/08/2026

3.4.7. Data Rate Selection in Gearbox Mode

The SDI input block has two input data rate selection modes: Auto Data Rate and Manual Data Rate selection mode. The control block will select one or the other depending on the selected Gearbox Mode.

In Bypass Mode, when the input is 1.5G, 3G, 6G or 12G, the GS12270 uses the auto rate detection feature of the SDI input block to automatically determine the input data rate. The output data rate will be set to be same as the input data rate.

In the MUX and DEMUX Mode, the control logic uses MUX/DEMUX settings to select the data rate for the SDI input and output block. In this case, manual data rate selection is used for the SDI input block, based on the selected mode.

There is an alternative “semi-auto” data rate selection mode for the MUX and DEMUX. It uses the extracted PID to determine MUX/DEMUX modes and set the output data rate. It can be selected by setting the **SDI_AUTO_MODE_EN** parameter HIGH.

When in MUX or DEMUX Mode and the semi-auto option is selected, the GS12270 selects the auto data rate detection at the SDI input block. The GS12270 searches for a proper data rate and locks to the correct one. After

the lock is achieved the PID will be extracted. Based on the extracted PID, the GS12270 selects MUX or DEMUX Mode. The data rate detect will only run on *DDI0*, which will be the master input in all cases.

For example, the Gearbox Mode is set to MUX and the QL3G is connected to the input.

In this case, the auto rate detect block detects a 3G data rate at DDI0 and locks to it. Based on the extracted PID, the GS12270 sets MUX mode to QL3G→SL12G.

In the case where selection can be ambiguous, the QL→SL selection (QL→SL for the MUX and SL→QL for DEMUX) is preferred over the QL→DL. There is an option to invert this preference via the **SDI_AUTO_MODE_OUT_INTERF** parameter in the host interface.

3.4.8. Output Assignment

3.4.8.1. Default Output Assignments

Default output assignments are configured as per the modes listed in Table 3-36.

3.4.8.2. Sync-Bit Insertion Encoding

SMPTE standards defining 6Gb/s and 12Gb/s SDI interface, SMTE ST2081-1 and ST2082-1, require inversion of the one bit in all $3FF_h$ and 000_h words in the video stream, keeping only one 3FF 000 000 sequence in the TRS words, a process called Sync-bit insertion.

The GS12270 inserts Sync-bits into the video stream immediately before the scrambling process for SL, DL, or QL UHDI interfaces at 6Gb/s and 12Gb/s data rates.

Table 3-36: Serial Tx Output Assignment

Mode		Tx0	Tx1	Tx2	Tx3	Notes
MUX	QL3G→SL12G	M0	M0 (DDO idle)	M0 (DDO idle)	M0 (DDO idle)	—
	QLHD→SL6G	M0	M0 (DDO idle)	M0 (DDO idle)	M0 (DDO idle)	—
	QL6G→DL12G	M0	M0 (DDO idle)	M1	M1 (DDO idle)	—
	QL3G→DL6G	M0	M0 (DDO idle)	M1	M1 (DDO idle)	—
	DL6G→SL12G	M0	M0 (DDO idle)	M1	M1 (DDO idle)	1
	DL3G→SL6G	M0	M0 (DDO idle)	M1	M1 (DDO idle)	1
	DLHD→SL3G	M0	M0 (DDO idle)	N/A	N/A	—
DEMUX	SL12G→QL3G	DM0	DM0	DM0	DM0	—
	SL6G→QLHD	DM0	DM0	DM0	DM0	—
	DL12G→QL6G	DM0	DM0	DM1	DM1	—
	DL6G→QL3G	DM0	DM0	DM0	DM0	—
	SL12G→DL6G	DM0	DM0	DM1	DM1	2
	SL6G→DL3G	DM0	DM0	DM1	DM1	2

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09/08/2026

SL3G→DLHD	DM0	DM0	N/A	N/A	—

1. By default, Tx2 (M1path) is powered-down. To use Tx2 (M1 path) as a secondary link it must be enabled manually via SEC_LINK_ENABLE ball or through the CSR. See Figure 3-7 and Section 3.4.3.2 for further details.
2. By default, Tx2 (DM1 path) and Tx3 (DM1path) are powered-down. To use Tx2 (DM1 path) and Tx3 (DM1 path) as a secondary link they must be enabled manually via SEC_LINK_ENABLE ball or through the CSR. See Figure 3-10 and Section 3.4.4.2 for further details.

3.4.8.3. Manual Output Assignment

Each output can be assigned to:

- Multiplexed streams in MUX Mode (M0 or M1 processed output)
- Demultiplexed streams in DEMUX Mode (DM0 or DM1 processed output)
- Any of the four input channels

This feature is available in any mode, regardless of the default assignment of the serial output. Assignment of the output is configured through the **OUTPUT_ASGMT_DDO<n>** and enabled through the **REG_CTRL_OUTPUT_ASGMT_EN** register.

Note: Custom output assignments will be retained, even if the mode is changed. To return to the default output assignment, the register **REG_CTRL_OUTPUT_ASGMT_EN** should be set back to "0" (Figure 3-11).

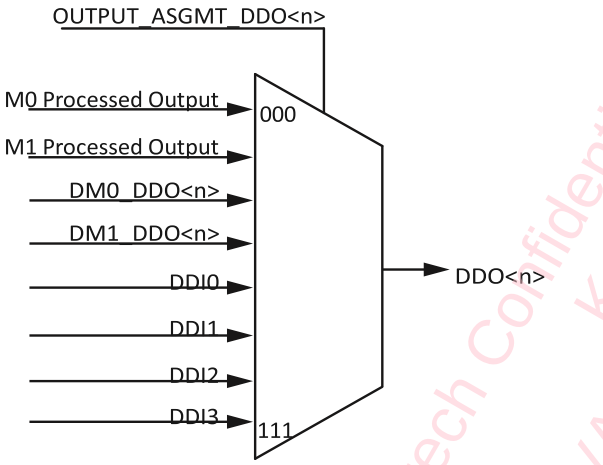

Figure 3-11: Output Assignment Selection

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09/08/2026

3.4.9. PI Clock Selection

The SDI transmitter configuration depends on the GS12270 configuration mode. In SDI-SDI (Gearbox) mode, the Tx Phase Interpolator (PI) is used to frequency-lock Tx data to the incoming data stream by adjusting the frequency difference between the 148.5MHz reference oscillator and the input data stream.

Based on the mode selected and the crosspoint settings, one of Rx extracted clocks is automatically selected as PI reference clock for each enabled Tx lane. In the MUX or DEMUX mode of operation, the clock, as selected as a primary clock, is selected as PI reference. If user changes the primary channel selection, the PI reference clock will change accordingly. By default, the following receiver's clocks will be selected in MUX or DEMUX mode:

- **RX0_CLK** (from DDI0 input)—if M0 or DM0 data are selected as input to the transmitter (all QL→SL, QL→DL muxing/demuxing modes and DL→SL modes forM0/DM0 paths)
- **RX2_CLK** (from DDI2 input)—if M1 or DM1 data are selected as input to the transmitter (DL→SL modes for M1/DM1 paths)

In Bypass Mode, the Tx PLL input clock is taken from the receiver (DDI input) which is connected to the transmitter.

3.4.9.1. Output Loop Bandwidth

The loop bandwidth of the output is individually configured on a per-output basis. The default loop bandwidth should be configured based on the requirements of the device connected to the *DDO[3:0]* serial outputs.

The loop bandwidth can be set through the **DDO_LBW** register and will take effect when the **DDO_LBW_UPDT** register has been written to. Please refer to Table 3-37.

Table 3-37: DDO Loop Bandwidth Setting

DDO_LBW_SETTINGS$_h$	12G LBW (MHz)	6G LBW (MHz)	3G LBW (MHz)	1.5G LBW (MHz)
0	RSVD			
1	0.13	0.13	0.13	0.13
2	0.25	0.25	0.25	0.25
3	0.5	0.5	0.5	0.5
4	1.01	1.01	1.01	1.01
5	2.01	2.01	2.01	2.01
6	4.03	4.03	4.03	2.01
7	8.06	8.06	8.06	2.01
8	16.11	16.11	8.06	2.01
9	32.33	16.11	8.06	2.01
A to F	RSVD			

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Kent Lin
DIVA Laboratories, Ltd.
09/08/2026

3.4.10. SDI SMPTE Data Rates and Source Image Formats Supported

The GS12270 supports the SDI formats listed in Table 3-38 while in SDI-SDI Gearbox Mode.

Table 3-38: SMPTE Data Rate and Source Image Formats Supported

Total Image Data Rate	SDI Serial Interface	P/I	Frame Rate	Active Pixels	Active Lines	Source Image Format	Standard	Formats	SDI Mapping Standard
12G	SL 12G	p	Transport of multiple 6Gb/s, 3Gb/s or 1.5Gb/s on a 12G-SDI link						ST2082-30
	SL 12G DL 6G QL 3G		60/59.94 50	3840	2160	10-bit 4:2:0(Y'C'$_B$C'$_R$) 10-bit 4:2:2(Y'C'$_B$C'$_R$)	ST-2036-1		ST2082-10 ST2081-11

			60/59.94 50 48/47.96	4096		10-bit 4:2:2(Y'C'$_B$C'$_R$)	ST2048-1	ST0425-5
			30/29.97 25 24/23.98	3840 4096		10-bit 4:4:4(Y'C'$_B$C'$_R$) 10-bit 4:4:4(R'G'B') 12-bit 4:2:2(Y'C'$_B$C'$_R$) 12-bit 4:4:4(Y'C'$_B$C'$_R$) 12-bit 4:4:4(R'G'B')	ST2036-1 ST2048-1	
				4096		10-bit 4:4:4:4(Y'C'$_B$C'$_R$+A) 10-bit 4:4:4:4(R'G'B'+A) 12-bit 4:2:2:4(Y'C'$_B$C'$_R$+A)	ST2048-1	
				3840		12-bit 4:2:0(Y'C'$_B$C'$_R$)	ST-2036-1	
			30/29.97 25 24/23.98	3840 4096		3D 10-bit 4:2:2	ST2036-1 ST2048-1	
			60/59.94 50	1920 2048		3D 12-bit 4:2:2 3D 12-bit 4:4:4 3D 10-bit 4:4:4:4	ST274 ST2048-2	ST425-6
			48/47.96	2048		3D 12-bit 4:2:2 3D 12-bit 4:4:4 3D 10-bit 4:4:4:4	ST274 ST2048-2	
			120/119.88 100	1920 2048	1080	12-bit 4:2:2 12-bit 4:4:4 10-bit 4:4:4:4	ST2048-1	ST2082-10
			96/95.9	2048		12-bit 4:2:2 12-bit 4:4:4 10-bit 4:4:4:4		
6G	SL 6G DL 3G QL HD	p	30/29.97 25 24/23.98	3840	2160	10-bit 4:2:0(Y'C'$_B$C'$_R$) 10-bit 4:2:2(Y'C'$_B$C'$_R$)	ST2036-1	ST2081-10 (Mode 1) ST425-3
			30/29.97 25 24/23.98	4096		10-bit 4:2:2(Y'C'$_B$C'$_R$)	ST2048-1	
			60/59.94 50	1920	1080	10-bit 4:4:4(Y'C'$_B$C'$_R$) 10-bit 4:4:4(R'G'B') 12-bit 4:2:2(Y'C'$_B$C'$_R$)	ST274	ST2081-10 (Mode 2) ST425-3 [1]

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Kent Lin
DIVA Laboratories, Ltd.
09/08/2026

						12-bit 4:4:4(Y'C'$_B$C'$_R$) 12-bit 4:4:4(R'G'B') 10-bit 4:4:4:4(Y'C'$_B$C'$_R$+A) 10-bit 4:4:4:4(R'G'B'+A)		
			60/59.94 50 48/47.96	2048		10-bit 4:4:4(Y'C'$_B$C'$_R$) 10-bit 4:4:4(R'G'B') 12-bit 4:2:2(Y'C'$_B$C'$_R$) 12-bit 4:4:4(Y'C'$_B$C'$_R$) 12-bit 4:4:4(R'G'B') 10-bit 4:4:4:4(Y'C'$_B$C'$_R$+A) 10-bit 4:4:4:4(R'G'B'+A) 12-bit 4:2:2:4(Y'C'$_B$C'$_R$+A)	ST2048-2	ST2081-10 (Mode 2) ST425-3
	SL 6G		120/119.88 100	1920 2048		10-bit 4:2:2	ST2048-1	ST2081-10
			96/95.9	2048		10-bit 4:2:2 10-bit 4:2:0	ST2048-1	
	SL 6G DL 3G		60/59.94 50	1920 2048		3D 10-bit 4:2:2	ST274 ST2048-2	ST425-4 [1]
			48/47.96	2048		3D 10-bit 4:2:2	ST2048-2	
			30/29.97 25 24/23.98	1920 2048		3D 12-bit 4:2:2 3D 12-bit 4:4:4 3D 10-bit 4:4:4:4	ST274 ST2048-2	
	DL 3G		60/59.94 50 30/29.97 25 24/23.98	1280	720	3D 12-bit 4:2:2 3D 12-bit 4:4:4 3D 10-bit 4:4:4:4	ST296	
3G	3G	p	60/59.94 50	1920 2048	1080	10-bit 4:2:2	ST274 ST2048-2	ST425-1
			48/47.96	2048		10-bit 4:2:2	ST2048-2	ST425-1

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Kent Lin
09/08/2026

			30/29.97 25 24/23.98	1920 2048		10-bit 4:4:4(Y’C’$_B$C’$_R$) 10-bit 4:4:4(R’G’B’) 12-bit 4:2:2(Y’C’$_B$C’$_R$) 12-bit 4:4:4(Y’C’$_B$C’$_R$) 12-bit 4:4:4(R’G’B’) 10-bit 4:4:4:4(Y'C'$_B$C'$_R$+A) 10-bit 4:4:4:4(R'G'B'+A)	ST274 ST2048-2	ST425-1 [2]
			30/29.97 25 24/23.98	1920 2048	1080	12-bit 4:2:2:4(Y’C’$_B$C’$_R$)	ST2048-2	ST425-1 [2]
			60/59.94 50, 30/29.97 25, 24/23.98	1280	720	10-bit 4:4:4(Y’C’$_B$C’$_R$) 10-bit 4:4:4(R’G’B’) 10-bit 4:4:4:4(Y'C'$_B$C'$_R$+A) 10-bit 4:4:4:4(R'G'B'+A)	ST296	ST425-1
			30/29.97 25 24/23.98	1920 2048	1080	3D 10-bit 4:2:2(Y’C’$_B$C’$_R$)	ST274	ST425-2
			60/59.94, 50, 30/29.97 25, 24/23.98	1280	720	3D 10-bit 4:2:2(Y’C’$_B$C’$_R$)	ST296	ST425-2
		Transport of two HD streams on a 3G link					—	ST425-1 [3]
HD	HD	p	30/29.97 25 24/23.98	1920 2048	1080	10-bit 4:2:2(Y’C’$_B$C’$_R$)	ST274	ST292-1
		i	60/59.94 50	1920 2048		10-bit 4:2:2(Y’C’$_B$C’$_R$)	ST274	ST292-1
		p	60/59.94, 50, 30/29.97, 25, 24/23.98	1280	720	10-bit 4:2:2(Y’C’$_B$C’$_R$)	ST296	ST292-1

1. Level B inputs are supported in SDI-SDI configuration, but there is no support for Level B to Level A conversion. Level B inputs are not supported in SDI-HDMI and HDMI-SDI configurations.
2. There is no support for PsF mapping structure.
3. Only in SDI-SDI Configuration.

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3.5. SDI-HDMI Configuration

When in the SDI-HDMI Configuration Mode, the GS12270 receives an SDI video stream and converts it into an HDMI TMDS compatible video stream. Only straight conversion of the SDI data formats and data rates into corresponding HDMI ones are supported. The output format control is strictly input driven.

Note: The HDMI specification requires an HDMI source to be able to support at least one of the following formats: 640x480p@59.94/60Hz, 720x480p@59.94/60Hz and 720x480p@50Hz

However, the GS12270 doesn't support these formats, because there are no SDI equivalents.

3.5.1. SDI-HDMI Mode Functions

In the SDI-HDMI configuration mode, the device will:

- Apply selected equalization to the input signals.
- Check and report on CRC errors in each data stream.
- Read PID values in each data stream.
- Determine the input format based on the PID values and select the proper HDMI output format.
- Extract time code from data streams.
- Extract embedded ANC data from data streams.
- De-embed audio from input data streams.
- Convert the UHD video mapped as 2SI into the native image and convert it to the format expected by the HDMI Tx block.
- Calculate a subset of audio InfoFrame data from the audio control words and make them ready for embedding.
- Calculate a subset of AVI InfoFrame data from the extracted PID values and make them ready for insertion.
- Embed de-embedded SDI audio or external I^2S audio from the audio input pins in the HDMI TMDS streams.
- Embed audio and video InfoFrames in the HDMI TMDS streams.
- Embed additional InfoFrames if programmed by the user.
- Perform DDC handshake with the connected HDMI sink (skip if overridden via the host).
- Pack and encode the video stream in the HDMI TMDS streams.
- Serialize outputs.

3.5.2. SDI Inputs

The SDI inputs retain all functionality they have in the SDI-SDI Mode. Audio, ANC and TC extraction can be enabled via host interface. Specific blocks, like Audio, ANC and TC insertion are disabled to save power since they have no function.

In the SDI-HDMI configuration, the auto rate detection feature of the SDI input block is used to automatically determine the input data rate and embedded PIDs are used to determine input video format.

The quad link (QL) HD format doesn't have a defined PID byte 1 which differentiates it from the single link (SL) HD format. If the HD (1.5G) data rate is detected on the master input, the QLHD format is selected if and only if all four inputs are locked; for all other cases, SLHD format is selected. Please note that dual link (DL) HD is not supported.

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3.5.2.1. Input Selection

It is possible to select different inputs for SDI-HDMI conversion:

- For SL inputs, it is possible to select a video stream from either DDI0 (primary) input or DDI2 (secondary) input, DDI0 being default.
- For DL inputs, it is possible to select a video streams from either DDI0 and DDI1 (primary) input or DDI2 and DDI3 (secondary) input, DDI0 and DDI1 being default.
- For QL, all inputs are used and there is no secondary input switching available.

In order to be able to select DDI2 and DDI3 inputs, secondary link needs to be powered-up. Secondary link can be powered up either by *SEC_LINK_ENABLE* ball or registers **OPERATING_MODE_SEL_REG** (**SEC_LINK_EN_REG_SEL** parameter enables override and **SEC_LINK_EN_REG** parameter enables secondary link). When the secondary link is enabled, the input(s) can be switched either using ball *INPUT_SELECT* (L14) or via host interface, register **SDI_IN_SEL** (parameters **SDI_IN_0_2_SEL** and **REG_CTRL_SDI_IN_SEL** are used to select and to enable register override respectively).

The switching procedure is identical to similar switching when GS12270 is set in SDI-SDI configuration.

The input data rate and PID detection (format detection is based on it) is performed only at the master input. The master input is DDI0 input by default. If the secondary input is selected the input DDI2 becomes the master input.

Note: There was an issue identified where if there is SL3G connected at DDI0 and SL12G at DDI2 at the same time. To avoid this situation, either power-down DDI2 or override its lock indication signal (in case the user still wants to monitor inputs) until the DDI2 input is selected.

3.5.3. Output Format Selection

The input video format is determined based on the input data rate and the info from the embedded PIDs in the input data stream. Based on the input video format the appropriate video conversion and an HDMI output format are selected. The detected SMPTE data rate, colour depth, colour sub-sampling and selected HDMI Tx rate and VIC number are reported in registers: **HDMI_TX_MAPP_DETECTED, HDMI_TX_COLOR_SETT_RAST_DETECTED** and **VIC_NUM_SELECTED,** parameters

SMPTE_DATA_RATE_DET, **COLOR_DEPTH_DET**, **COLOR_SUBSAMPL_DET**, **HDMI_TX_DATA_RATE_DET** and **VIC_NUM_SELECTED** respectively.

The HDMI output colour depth can alternatively be forced to 8-bit using the register parameter **FORCE_RGB_8B**. The 8-bit colour depth force is valid only for 4:4:4 10-bit pixel sampling.

There are two ways to manually change selected settings:

- Each of the detected/selected parameters listed above can be manually and independently overridden using registers: **HDMI_TX_MAPPING_SETTINGS**, **HDMI_TX_COLOR_SETTINGS**, **HDMI_TX_DIV_SETTINGS** and **VIC_NUM_SETTING**. It can be used to change some of detected/selected parameters if the info is missing in the input data PIDs or all of them for full manual programming.
- The detected PID words, used for input SDI video format detection and output HDMI format selection, can be overwritten using registers **PID_DET_REG_1** and **PID_DET_REG_2**. It can be used to override the detected PIDs but also it can be used if there are no PIDs embedded into the input video stream to set SDI-HDMI conversion.

HDMI data rate selected and SMPTE data rate detected values based on the input data rate and PID selected are listed in Table 3-39. If support for QLHD is required, the user needs to override default **EXT_PLL_REF_SEL** setting (LOW) and set it HIGH. The empty cells in the table mean that the condition is not checked to determine HDMI data rate selected and SMPTE data rate detected, usually because only one setting is possible for that cell value in that particular case.

Table 3-39: HDMI Data Rate Selected and SMPTE Data Rate Detected Values Based on the Input Data rate and PID Selected

Data Rate	PID Byte 1	PID Byte 2 [3:0] (Frame Rate HFR)	BID Byte 3 [3:0] (Sampling Structure)	PID Byte 4 [1] (12-bit)	QLHD	EXT_PLL_REF_SEL	HDMI Data Rate Selected [Gb/s]	SMPTE Data Rate Detected
HD	85 (1080 @ 1.5G 4:2:2-10)	—	—	—	1	1	0111 - 2.97	100 - 6G Mode 1
		—	—	—	0	1	0001 - 0.7425	000 - HD
		—	—	—	0	0	0000 - 0.7425	
	84 (720p@1.5G 4:2:2-10) and others	—	—	—	—	1	0001 - 0.7425	000 - HD
		—	4:2:2 & 4:2:0	1	—	0	0000 - 0.7425	

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3G	88 (720p@ 3G A 4:4:4-10)	—	—	—	—	—	0010 - 0.9281	001 - 3G
	89 (1080@ 3G A)	—	4:2:2 & 4:2:0	1	—	—	0001 - 0.7425	001 - 3G
		—		0	—	—	0100 - 1.485	
		—	4:4:4	1	—	—	0011 - 1.1138	
		—		0	—	—	0010 - 0.9281	
	94 (1080p DL3G A)	—	4:2:2 & 4:2:0	—	—	—	0100 - 1.485	011 - 6G Mode 2
		—	4:4:4	1	—	—	0110 - 2.2275	
		—		0	—	—	0101 - 1. 8563	
	96 (2160p DL3G B-DS 4:2:2-10)	—	—	—	—	—	0111 - 2.97	100 - 6G Mode 1
	97 (2160p QL3G A	—	4:2:2	1	—	—	0111 - 2.97	110 - 12G Mode 1
		—		0	—	—	1101 - 5.94	
		—	4:2:0	—	—	—	1001 - 3.715	
		—	4:4:4	1	—	—	1011 - 4.455	
		—		0	—	—	1001 - 3.715	
	Others	—	—	—	—	—	0100 - 1.485	001 - 3G
6G	C0 (2160p SL6G 4:2:2 - 10)	—	—	—	—	—	0111 - 2.97	100 - 6G Mode 1
	C1 (1080p SL6G)	Y	—	—	—	—	0111 - 2.97	010 - 6G Mode 3
		N	4:2:2 & 4:2:0	—	—	—	0100 - 1.485	011 - 6G Mode 2
		N	4:4:4	1	—	—	0110 - 2.2275	
				0	—	—	0101 - 1. 8563	
	C2 (2160p DL6G)	—	4:2:2	1	—	—	0111 - 2.97	110 - 12G Mode 1
		—		0	—	—	1101 - 5.94	
		—	4:2:0	—	—	—	1001 - 3.715	
		—	4:4:4	1	—	—	1011 - 4.455	
		—		0	—	—	1001 - 3.715	
	C3 (1080p DL6G HFR) not defined by SMPTE	—	4:2:2 & 4:2:0	—	—	—	0111 - 2.97	101 - 12G Mode 2
		—	4:4:4	1	—	—	1011 - 4.455	
		—		0	—	—	1001 - 3.715	
	Others	Y	—	—	—	—	0111 - 2.97	010 - 6G Mode3
		N	—	—	—	—	0111 - 2.97	100 - 6G Mode1
12G	CE (2160p SL12G)	—	4:2:2	1	—	0	1000 - 2.97	110 - 12G Mode 1
		—		1	—	1	0111 - 2.97	
		—		0	—	0	1110 - 5.94	

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09/08/2026

	—		0	—	1	1101 - 5.94	
	—	4:2:0	—	—	0	1010 - 3.715	
	—		—	—	1	1001 - 3.715	
	—	4:4:4	1	—	0	1100 - 4.455	
	—		1	—	1	1011 - 4.455	
	—		0	—	0	1010 - 3.715	
	—		0	—	1	0111 - 2.97	
CF (1080p SL12G HFR)	—	4:2:2 & 4:2:0	—	—	0	1000 - 2.97	101 - 12G Mode 2
	—		—	—	1	0111 - 2.97	
	—	4:4:4	1	—	0	1100 - 4.455	
	—			—	1	1011 - 4.455	
	—		0	—	0	1010 - 3.715	
	—			—	1	1001 - 3.715	
Others	—		—	—	—	1110 - 5.94	110 - 12G Mode 1
	—		—	—	—	1101 - 5.94	

Table 3-40: Selected VIC Numbers

Data Rate	PID Byte 1			PID Byte 2 [3:0] (Frame Rate)	BID Byte 3 [6] (2048-1 or 1920-0)	VIC Selected
HD	84 (720p@1.5G 4:2:2-10)			25Hz	—	61
				30Hz	—	62
				50Hz	—	19
				Other	—	4
	85 (1080@1.5G 4:2:2-10)	QLHD - x	i	50Hz	—	20
				Other	—	5
		QLHD - 1	p	24Hz	1	98
				25Hz		99
				Other		100
				24Hz	0	93
				25Hz		94
				Other		95
		QLHD - 0		24Hz	0	32
				25Hz		33
				Other		34
	Others (No PID)	1280x720p60		—	—	4

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			1280x720p30	—	—	62
			1280x720p50	—	—	19
			1280x720p25	—	—	61
			1920x1080p24	—	—	32
			1920x1080p25	—	—	33
			1920x1080p30	—	—	34
			1920x1080p50	—	—	20
			1920x1080p60	—	—	5
			Others	—	—	34
3G	88 (720p@ 3G A 4:4:4-10)			25Hz	—	61
				30Hz	—	62
				50Hz	—	19
				Other	—	4
	89 (1080@ 3G A)	4:2:2 or 4:2:0 10-bit	i	48Hz	—	111
				50Hz	—	31
				Other	—	16
		4:4:4 10/12 or 4:2:2 12-bit		50Hz	—	20
				Other	—	5
			p	24Hz	—	32
				25Hz	—	34
				Other	—	34
	94 (1080p DL3G A)			48Hz	—	111
				50Hz	—	31
				Other	—	16
	96 (2160p DL3G B-DS 4:2:2-10)			24Hz	—	93
				25Hz	—	94
				Other	—	95
				24Hz	—	98
				25Hz	—	99
				Other	—	100
	97 (2160p QL3G A)			24Hz	—	93
				25Hz	—	94
				30Hz	—	95
				48Hz	—	114
				50Hz	—	96

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09/08/2026

		Other	—	97
		24Hz	—	98
		25Hz	—	99
		30Hz	—	100
		48Hz	—	115
		50Hz	—	101
		Other	—	102
	Other	—	—	16
6G	C0 (2160p SL6G Mode1 4:2:2-10)	24Hz	0	93
		25Hz		94
		Other		95
		24Hz	1	98
		25Hz		99
		Other		10
	C1 (1080p SL6G Mode2&3)	48Hz	—	111
		50Hz	—	31
		100Hz	—	64
		120Hz	—	63
		Other	—	16
	C2 (2160p DL6G Mode1)	24Hz	0	93
		25Hz		94
		30Hz		95
		48Hz		114
		50Hz		96
		Other		97
		24Hz	1	98
		25Hz		99
		30Hz		100
		48Hz		115
		50Hz		101
		Other		102
	C3 (1080p DL6G HFR) not defined by SMPTE	100Hz	—	100
		120Hz	—	120
		Other	—	16
	Other	—	—	95

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09/08/2026

12G	CE (2160p SL12G)	24Hz	0	93
		25Hz		94
		30Hz		95
		48Hz		114
		50Hz		96
		Other		97
		24Hz	1	98
		25Hz		99
		30Hz		100
		48Hz		115
		50Hz		101
		Other		102
	CF (1080p SL12G HFR 4:4:4 10&12-bit)	100Hz	—	64
		120Hz	—	63
		Other	—	16
	Others	—	—	97

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3.5.4. SDI-HDMI Output Loop Bandwidth

The output loop bandwidth is fixed for a given data rate. The output loop bandwidth for supported data rates are listed in the Table 3-41.

Table 3-41: Output Loop Bandwidth in SDI-HDMI Mode

SDI Input Data Rate	SDI-HDMI Loop Bandwidth (MHz)
11.8Gb/s	7.2
5.94Gb/s	7
2.97Gb/s	4
1.485Gb/s	2.1

3.5.5. Handling of Audio

Up to 16 channels of audio can be de-embedded from the SDI input and made available in I^2S serial format at the serial audio outputs, *A_OUT_1/2* to *A_OUT_15/16*. By default, the serial audio outputs are not enabled. It is possible for the user to select any audio

group for de-embedding and to enable serial audio outputs via the host interface using the **AUDIO_DATA_OUT_EN_OVRD**, **AUDIO_DATA_1TO8_OEN** and

AUDIO_DATA_9TO16_OEN parameters in the **OUTPUT_ENABLE** register. Audio clock outputs can be controlled separately using the **AUDIO_CLK_OUT_EN_OVRD** and **AUDIO_CLK_OEN** parameters in the **OUTPUT_ENABLE** register. For more information on extracting audio from the SDI input stream, refer to 3.8 SDI Audio De-Embedding.

3.5.5.1. HDMI Audio Embedding

The GS12270 supports embedding of up to eight channels of L-PCM audio data at sample rates of 48kHz and 96kHz as Audio Sample Packet. The supported serial audio formats are I^2S and Left Justified.

The eight channels of audio to be embedded can be selected either from the audio extracted from the SDI video stream or the external audio from the serial audio inputs, *A_IN_1_2* to *A_IN_15_16*. By default, it will be set to insert the de-embedded audio. The register **REG42**, parameter **AUDIO_SEL_EXT_SDI**, can be used to override the default and the parameter **AUDIO_SEL_9TO16_1TO8B** can be used to select between audio from the *A_IN_1_2* through *A_IN_7_8* pins and audio from the *A_IN_9_10* through *A_IN_15_16* pins. Parameters **A_IN_STREAM_1_2_SEL** to **A_IN_STREAM_7_8_SEL** can be used to rearrange audio data pairs connected to inputs of the HDMI audio embedding block.

Figure 3-12 illustrates audio source selection for HDMI audio embedding.

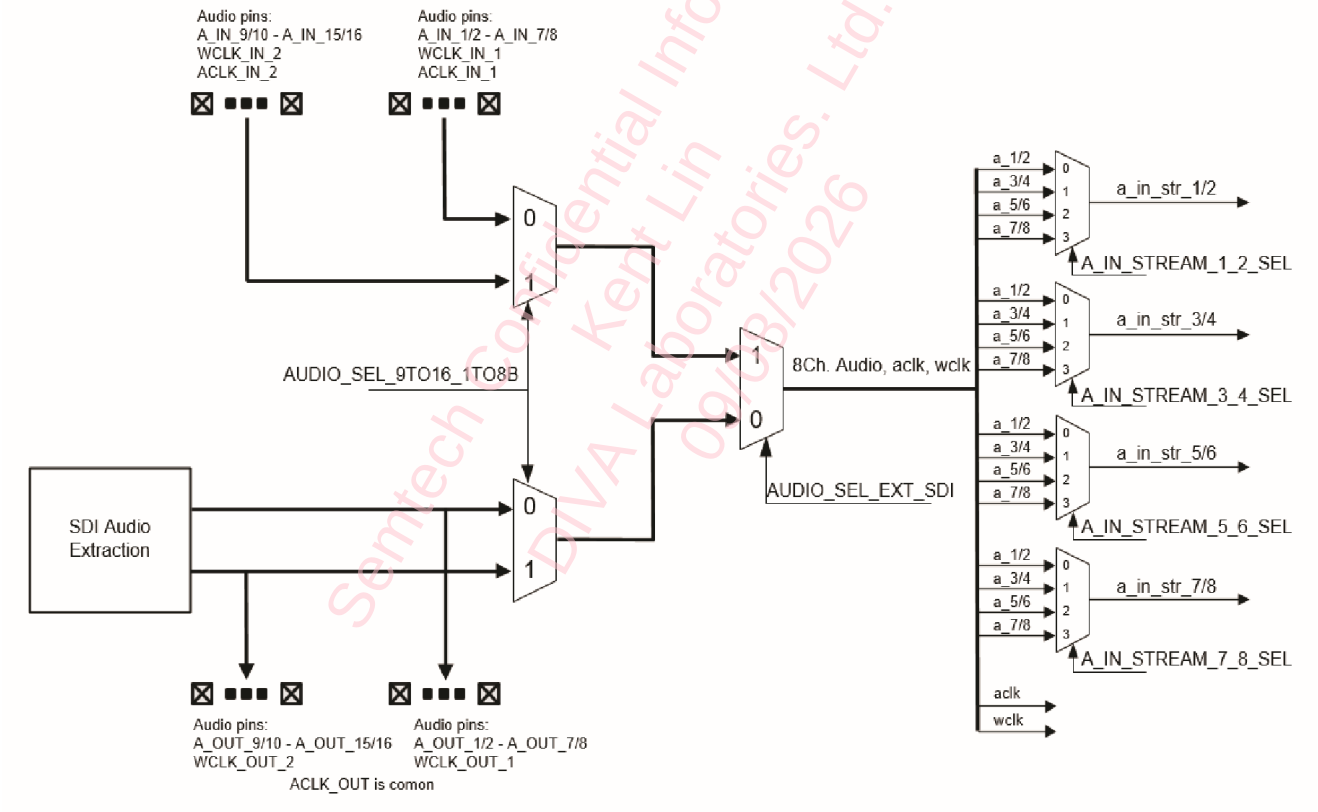

Figure 3-12: Audio Source Selection for HDMI Audio Insertion

By default, when in the SDI-HDMI configuration, the audio Audio Sample Packet and also Audio Clock and Regeneration packet (N and CTS parameters) insertion is enabled, however **REG48**, parameter **HDMI_TX_AUDIO_SAMPLE_PKT_ENABLE** and **HDMI_TX_AUDIO_CLK_REGEN_PKT_ENABLE** can be used to change it.

Parameter **HDMI_TX_AUDIO_PKT_LAYOUT_BIT**, **REG48**, is used to set the audio layout. The default value is set as 8-channel (Layout1). The **HDMI_TX_AUDIO_SAMPLE_PRESENT** and **HDMI_TX_AUDIO_SAMPLE_FLAT**

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09/03/2026

indicate if a channel pair is valid and if it contains audio or mute samples, default is that all eight channels carry valid audio samples.

The register **REG48** can be used to change defaults for SCLK and WCLK polarity as well as serial audio format.

If the input audio is IEC 61937 compressed formats, parameter **HDMI_TX_AUDIO_PKT_TYPE** can be changed to value 9 to indicate HBR Audio Stream Packer (IEC 61937).

3.5.5.1.1. Audio InfoFrame

The Audio InfoFrame insertion is automatically enabled when the Audio Sample Packet insertion is enabled and Audio is detected. The Audio InfoFrame is inserted with selected or default values, though it can be changed through CSR. There are two ways the Audio InfoFrame can be altered, each field can be changed independently through CSR or the whole Audio InfoFrame can be change through CSR using the InfoFrame replacement function.

Table 3-42 lists the default values for Audio InfoFrame values and register used to override it. For more info about replacing the whole Audio InfoFrame see 3.5.7.3 Audio InfoFrame.

Table 3-42: Audio InfoFrame Default Settings and Registers

Field Name	Description	Default Value	CSR Parameter
CC2-CC0	Channel Count	8 (111) If external audio selected 8(111) SDI audio two Group 4(011) SDI audio one Group 000 SDI audio no Groups	**HDMI_AUDIO_CHANNEL_COUNT_OVR** **HDMI_AUDIO_CHANNEL_COUNT**
CT3-CT0	Coding Type	Always 0 (Refer to Stream Header)	**HDMI_AUDIO_FORMAT**
SS1-SS0	Sample Size	Always 0 (Refer to Stream Header)	**HDMI_AUDIO_SMPL_SIZE**
SF2-SF0	Sample Frequency	Always 0 (Refer to Stream Header)	**HDMI_AUDIO_SMPL_FREQ**
CA7-CA0	Channel/Speaker allocation	0x13 - RRC, RLC, RS, LS, FC, LFE1, FR, FL	**HDMI_AUDIO_CHSP_ALLOC**
LSV3-LSV0	Level Shift Value	0000 - 0dB	**HDMI_AUDIO_LVL_SHIFT_VAL**
DM_INH	Down-mix Inhibit	0	—
LFEPBL1-0	LFE Playback level	00 - No Info	**HDMI_AUDIO_LFE_PLBK_LVL**

3.5.5.1.2. Audio Channel Status

Audio Channel status is a part of the AES block, consisting of AES channel pairs, carried in Audio Data Packets in the SDI video stream. The audio channel status data is extracted from the input SDI video stream, reported through CSR (see 3.8 SDI Audio De-Embedding for more information), formatted and passed to the HDMI transmitter.

If the audio extracted from the SDI video stream is selected for the embedding, the extracted audio channel status from the SDI video will be embedded in the HDMI video stream as a part of the Audio Sample Packet.

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If, on the other hand, the external audio from the serial audio inputs is selected— because the input audio format is either I^2S or Left Justified and therefore no audio channel status data are available—the audio channel status data have to be set manually through the CSR interface. Register **REG51**, parameter

HDMI_TX_AUDIO_CH_STAT_OVR_EN is used to enable CSR override of the audio channel status data and **REG52 - REG99**, parameters **HDMI_TX_AUDIO_CH_STAT_1_2_BYTE_1_OVR** to **HDMI_TX_AUDIO_CH_STAT_7_8_BYTE_22_OVR**, to set the status data.

The same registers, **REG51** - **REG99**, can be used in the case where the audio extracted from the SDI video stream is selected for embedding but the channel status needs to be modified.

3.5.6. Handling of ANC Data

By default, ANC extraction is disabled. It can be enabled via the host interface using the **ANC_EXT_ENABLE** parameter in the **ANC_DATA_EXT_ENABLE_REG** register. For more information on extracting ANC data from the SDI stream, refer to 3.9.3 ANC Data Extraction.

3.5.7. InfoFrames

3.5.7.1. InfoFrame Insertion

The HDMI transmitter provides a mechanism for InfoFrame insertion. It is possible to insert the following InfoFrames: AVI InfoFrame, Audio InfoFrame, HDMI Vendor Specific InfoFrame, Dynamic Range and Mastering InfoFrame, Generic InfoFrame.

The specific InfoFrame insertion is enabled based on the standard and PID HDR info detected. The Generic InfoFrame is a user defined InfoFrame and can be enabled only manually. Parameters **INFO_FRAME_EN_OVR** and **INFO_FRAME_EN[7:0]** are used to enable override/manual selection and to select the InfoFrame to be embedded when the override mode is selected. Each bit in **INFO_FRAME_EN** selects one specific InfoFrame to be embedded, bit mapping is as following:

0 = General Control Packet

1 = AVI InfoFrame

2 = Audio InfoFrame

3 = HDMI Vendor Specific InfoFrame

4 = Dynamic Range and Mastering InfoFrame

5 = Generic InfoFrame

A bit value 1 enables the corresponding InfoFrame. Not all combinations of zeros and ones are allowed, the ones have to be consecutive, and therefore valid settings are only: 0000_0001, 0000_0011 … 0001_1111.

The specific InfoFrame byte values inserted are determined based on the detected data rate and PID words. There is an option for users to override bits in the InfoFrames that are set automatically by the control logic. Parameters **AVI_INFOFRAME_DATA_OVR**, **AUDIO_INFOFRAME_DATA_OVR,** **HDMI_V_S_INFOFRAME_DATA_OVR**,

DYN_RANGE_INFOFRAME_DATA_OVR can be used to enable override through CSR. In both cases, the insertion block performs checksum (CS) calculations, removing the need for users to manually calculate the CS words in the override mode.

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3.5.7.2. AVI Video InfoFrame

Auxiliary Video information (AVI) InfoFrame data bytes PB1-PB5 are automatically determined and set based on info from extracted PIDs. Some fields in the AVI Info Frame can be changed independently. Table 3-43 describes AVI InfoFrame selection and override option.

Table 3-43: AVI InfoFrame Selected/Default Fields and Override Parameters

Field Name	Description	Default Value	CSR Parameter Override
Y2-Y0	Colour sub-sampling	Detected	**COLOR_SMPL_DEPTH_OVR COLOR_SUBSAMPL**
A0	Active format info present	Detected	**ACTIVE_FORMAT_OVR ACTIVE_FORMAT_INF_PRESENT**
B1-B0	Bar Data Present	Set to 00 (no Bar Data)	—
S1-S0	Scan Info	Set to 00 (No Data)	—
C1-C0	Colorimetry	Detected	—
M1-M0	Picture Aspect Ratio	Set to 10 (16:9)	—
R3-R0	Active Aspect Ratio	Set to 1000 if Active format info present else 0000	**ACTIVE_FORMAT_OVR ACTIVE_ASPECT_RATIO**
ITC	IT Content	Set to 0	—
EC2-EC0	Extended Colorimetry	Detected	—
Q1-Q0	RGB Quantization Range	Detected	—
SC1-SC0	Non-Uniform Picture Scaling	Set to 00	—
VIC6-VIC0	VIC	Detected	**VIC_NUM_OVR VIC_NUM_REG**
YQ1-YQ0	YCC Quantization Range	Detected	—
CN1-CN0	IT Content Type	Set to 10 (Cinema)	—
PR3-PR0	Pixel Repetition Factor	Set to 0000 - No Repetition	—

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In additional to the independent field value override, the whole AVI InfoFrame can be replaced. To replace the whole AVI InfoFrame, parameter **AVI_INFOFRAME_DATA_OVR** needs to be set to 1. When selected, values from parameters **AVI_INFOFRAME_PB1** - **AVI_INFOFRAME_PB13** will be used for the AVI InfoFrame insertion.

3.5.7.3. Audio InfoFrame

The Audio InfoFrame insertion and the InfoFrame single field values override are described in 3.5.5.1.1 Audio InfoFrame.

Additionally to the independent field value override, the whole Audio InfoFrame can be replaced. To replace the whole Audio InfoFrame, parameter

AUDIO_INFOFRAME_DATA_OVR needs to be set to 1. When selected, the values from parameters **AUDIO_INFOFRAME_PB1** - **AUDIO_INFOFRAME_PB5** will be used for the Audio InfoFrame insertion.

3.5.7.4. HDMI Vendor Specific InfoFrame

HDMI Vendor Specific InfoFrame data bytes PB1-PB6 are inserted automatically, based on detected PIDs. Table 3-44 describes HDMI Vendor Specific InfoFrame selection.

Table 3-44: HDMI Vendor Specific InfoFrame Detected/Default Fields

Packet Byte	Field Name/Description	Default Value
PB1	24bit IEE Registration Identifier (0x000C03)	0x03
PB2		0x0C
PB3		0x00
PB4[7:5]	HDMI_VIDEO_FORMAT	Detected
PB4[4:0]	RSVD	Set to 0000
PB5	HDMI_VIC	Detected
PB6[7:4]	3D_EXT_DATA	Set to 0000
PB6[3:0]	RSVD	Set to 0000

If needed the whole HDMI Vendor Specific InfoFrame can be override. To replace the whole HDMI Vendor Specific InfoFrame, parameter

HDMI_V_S_INFOFRAME_DATA_OVR needs to be set to 1. When selected, values from parameters **HDMI_V_S_INFOFRAME_PB1** - **HDMI_V_S_INFOFRAME_PB27** will be used for the HDMI Vendor Specific InfoFrame insertion.

3.5.7.5. Dynamic Range and Mastering InfoFrame

Insertion of the Dynamic Range InfoFrame will be automatically enabled if transfer characteristic in PID byte 2 is set to PQ or HLG. In this automatic mode only PB1(EOTF) and PB2 (**STATIC_METADATA_DESCRIPTOR_ID** = 0, Type1) will be set. The display primaries and mastering data, PB3-PB26, should be set manually if needed. Please note that, due a bug in the GS12270, EOTF will be always set to 2 (SMPTE ST 2084) if the automatic insertion of the Dynamic Range is enabled. The EOTF needs to be manually overridden if it needs to be set to 1 (Traditional gamma - HDR Luminance Range) or 3 (Hybrid Log-Gamma).

In order to override the whole Dynamic Range InfoFrame, parameter **DYN_RANGE_INFOFRAME_DATA_OVR** needs to be set to 1. When selected, values from parameters **DYN_RANGE_INFOFRAME_PB1** - **DYN_RANGE_INFOFRAME_PB26** will be used for the Dynamic Range InfoFrame insertion.

3.5.7.6. Generic InfoFrame

The user can define any InfoFrame to be inserted using parameters **GENERIC_INFOFRAME_HEADER_HB0 - GENERIC_INFOFRAME_HEADER_HB3**. The InfoFrame type can be any of the InfoFrame types defined by HDMI 1.4 and 2.0 and CTA-861-G specification or a custom one. The generic InfoFrame insertion can be enabled only manually. To enable it, the parameter **INFO_FRAME_EN_OVR** needs to be set to 1 and **INFO_FRAME_EN[7:0]** to 0001_1111. When enabled values from

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parameters **GENERIC_INFOFRAME_PB1** - **GENERIC_INFOFRAME_PB26** will be used for to insert an InfoFrame of the type, version and length defined in **GENERIC_INFOFRAME_HEADER_HB0** - **GENERIC_INFOFRAME_HEADER_HB3**.

Please note that if the generic InfoFrame insertion is enabled all other InfoFrames listed above will be enabled too, because **INFO_FRAME_EN[7:0]** is set to 0001_1111.

3.5.7.7. General Control Sub-packet

The General Control Sub-packet will always be inserted if the valid video is detected. If the HDMI output mode is Deep Colour Pixel Packing, the Pixel Packing Phase will be determined and set. Also the values for Default phase and Colour Depth will be set but they can also be overridden through following parameters:

GEN_CTRL_PCK_COLOR_DEPTH_OVR, **GEN_CTRL_PCK_COLOR_DEPTH_REG**, **DEFAULT_PHASE_OVR** and **DEFAULT_PHASE_REG**.

Bits **CLEAR_AVMUTE** and **SET_AVMUTE** in SB0 of General Control Sub-packet can be set through parameters **CLEAR_AVMUTE** and **SET_AVMUTE**.

3.5.8. DDC, HPD, and Output Ready

When a valid SDI input is connected, output video format detected, and the transmitter's PLLs locked, the device sets an output ready signal (*HDMI_5V_EN*) HIGH and waits for the HPD signal from an HDMI sink connected to it. The input HPD from the pin can also be overridden using parameters: **HDMI_HPD_OVR** and **HDMI_HPD_REG**. The output ready signal can be used by the user to control the +5V on the HDMI connector. The output ready signal can be overridden using parameters: **HDMI_5V_EN_OVR** and **HDMI_5V_EN_REG**.

When the HPD signal is set HIGH (on the ball or programmed via the host) the device reads EDID (it will be available to the user via the host) and, depending on the output format, set bits **TMDS_BIT_CLOCK_RATIO** and **SCRAMBLING_ENABLE** in the sink's EDID. For TMDS bit rates greater than 3.4Gb/s HDMI 2.0 requires the TMDS clock to be 1/40 of the bit rates and the data to be scrambled and leaves optional to scramble data for TMDS bit rates lower than 3.4Gb/s. The GS12270 will according set clock ratio and enabled scrambling for greater than 3.4Gb/s. Additionally, scrambling setting can be overridden by **SCRAMBLER_OVR** and **SCRAMBLER_EN** for HDMI encoder and values set to SCDC by **SCDC_SCRAMBL_EN_OVR** and **SCDC_SCRAMBL_EN_OVR**.

3.5.8.1. Display Data Channel (DDC) and Status and Control Data Channel (SCDC)

The GS12270 responds to the HPD signal from the HDMI sink by reading EDID, provided by the sink and, if output is at data rates greater than 3.4Gb/s, setting

TMDS_BIT_CLOCK_RATIO and **SCRAMBLING_ENABLE** bits in the SCDC interface.

Please note that the GS12270 doesn't disable its outputs when the

TMDS_BIT_CLOCK_RATIO and **SCRAMBLING_ENABLE** bits are written through the SCDC interface as it might be required by some HDMI sources (or HDMI drivers/re-timers used in front of the GS12270). If desired, this can be implemented using manual SCDC read/write and monitoring HPD and the internal HDMI_TX_TMDS_CLK_RATIO signal on a *STAT* pin. For more information, please refer to the Application Note “GS12270 Manual SCDC TMDS Bit Clock Ratio Control”.

The received E-EDID is stored in RAM and is available via the host interface. The RAM size is 512 bytes. The stored EDID can be obtained by reading address space $7F00_h$-$7FFF_h$. The EDID base block is stored in $7F00_h$-$7F7F_h$ and EDID CTA block in $7F80_h$ - $7FFF_h$. It is recommend to use auto-increment read. The stored EDID values will not be reset and if it is need to clear them 0 should be written to all addresses.

The sink EDID read can be manually initiated at any time by writing 1 to the **EDID_UPDATE_REG** parameter. Parameters **DDC_DONE**, **EDID_DONE** and **EDID_NO_ACK** indicates the status of the I^2C read.

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The HDMI sink's SCDC registers can be manually read or written using:

SCDC_UPDATE_REG, **SCDC_READ_WRITE_N_REG**, **CDC_UPDATE_REG_ADDRESSS**, **SCDC_UPDATE_REG_WDATA** and **SCDC_UPDATE_REG_RDATA**. If the user wants to read an SCDC register, the SCDC register address should be written to **CDC_UPDATE_REG_ADDRESSS, SCDC_READ_WRITE_N_REG** should be set to 1, and **SCDC_UPDATE_REG** should be set to start SCDC read.

When the SCDC read is done, **SCDC_DONE** = 1 and **SCDC_NO_ACK** = 0, the received data can be read from **SCDC_UPDATE_REG_RDATA**. The steps to write an SCDC address are similar just that data to be written to SCDC has to be first written to **SCDC_UPDATE_REG_WDATA** and **SCDC_READ_WRITE_N_REG** should be set to 0 before **SCDC_UPDATE_REG** is set.

The *HPD* ball is shared between the HDMI output block and the HDMI input block. The *HPD* is configured as an input in HDMI Transmitter Mode.

3.6. HDMI-SDI Configuration

When configured in the HDMI-SDI configuration mode, the GS12270 receives an HDMI TMDS compatible video stream and converts it into an SDI video stream. Only straight conversion of the HDMI data formats and data rates into corresponding SDI formats are supported.

3.6.1. HDMI-SDI Mode Functions

In HDMI-SDI configuration mode the device can:

- Communicate EDID and perform DDC handshake with the connected HDMI source (skip if overridden via the host)
- Detect input rate and set receivers accordingly
- Apply selected equalization to the input signals
- Decode TMDS signals
- Time-align the input signals
- De-embed audio
- Extract InfoFrames
- Determine the input format based on the InfoFrame data and select the proper SDI output format
- Calculate PID data values based on the AVI InfoFrame data and insert PID values in each data stream based on the detected format and the selected output rate
- Calculate audio info data based on the audio
- Insert PID data in the SDI video
- Embed de-embedded HDMI audio (in I^2S format) in the SDI video.
- Embed additional audio if required by the user.
- Insert additional ANC data if programmed by the user.
- Calculate and insert CRCs
- Multiplex the parallel signals as defined by the device's setup
- Copy the signal to multiple outputs as instructed by the user
- Apply selected emphasis to each output

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3.6.2. DDC, EDID and HPD

3.6.2.1. Hot Plug Detect and +5V (Cable Detect) Signal

The GS12270's HDMI Receiver supports the Hot Plug Detect (HPD) feature, which is a communication mechanism between the HDMI source and HDMI sink devices. When an HDMI cable is inserted (the +5V signal at the HDMI connector is set), the cable-detect signal is asserted, and the device will come out of sleep mode, set the HPD signal and wait for a HDMI source to start DDC communication. Based on the received **TMDS_BIT_CLOCK_RATIO** and **SCRAMBLING_ENABLE**, the frequency range of the TMDS clock will be set and the TMDS rate detection process will be started.

There is an override for both HPD signal (HPD_CSR_OVR, HPD_CSR) and cable detect, +5V connected to *ISP_0*, signal (HDMI_RX_CABLE_DETECT_OVR, HDMI_RX_CABLE_DETECT)

The *HPD* ball is shared between the HDMI output block and HDMI input block. The HPD is an output in HDMI Receiver Mode.

3.6.2.2. Display Data Channel (DDC) and Status and Control Data Channel (SCDC)

The GS12270 enables the end-user to build an HDMI sink device which negotiates with the targeted HDMI source device for supported features and capabilities. The communication between the source device(s) and the sink device is through the DDC, which is an I^2C bus included on the HDMI cable.

The GS12270's HDMI Receiver implements the Enhanced DDC Sink functionality in accordance with HDMI1.4b and 2.0 specification. It provides E-EDID information over the DDC channel within 20ms after the +5V signal is detected.

The SCDC makes use of the same I^2C interface used for the DDC. I^2C slave addresses for the SCDC are $A8_h$ and $A9_h$. The GS12270 supports the following two bits in the SCDC register address, offset 20_h, for TMDS configurations:

Bit '1' = **TMDS_CLOCK_RATIO_STATUS Bit '0' = SCRAMBLING_ENABLE**

Note that DDC clock and data balls are shared between the HDMI input and HDMI output blocks (when in HDMI-SDI mode or SDI-HDMI mode).

3.6.2.3. EDID

The default Extended Display Identification Data (EDID) is stored in the device and can be changed via the host interface.

The default, after power-up or reset, EDID values are:

Table 3-45: Stored EDID Base Block

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
620	00	FF	FF	FF	FF	FF	FF	00	4E	88	01	00	11	11	11	11
621	1A	1E	01	03	80	34	1D	78	0A	01	C1	A0	57	47	98	27
622	12	4C	4C	00	00	00	D1	C0	01	01	01	01	01	01	01	01
623	01	01	01	01	01	01	08	E8	00	30	F2	70	5A	80	B0	58
624	8A	00	40	84	63	00	00	1E	04	74	00	30	F2	70	5A	80
625	B0	58	8A	00	40	84	63	00	00	1E	00	00	00	FC	00	48

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09/08/2026

626	44	4D	49	53	44	49	42	52	49	44	47	45	00	00	00	FD
627	00	18	78	1C	87	3C	00	00	00	00	00	00	00	00	01	4E

Table 3-46: Stored EDID CTA Block

	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
630	02	03	44	70	5E	61	60	72	66	65	73	5F	5E	5D	3F	40
631	10	1F	6F	22	21	20	05	14	2F	29	84	13	6C	3E	3D	3C
632	64	63	62	23	0F	14	07	83	8F	00	00	6D	03	0C	00	10
633	00	38	3C	20	00	60	01	02	03	67	D8	5D	C4	01	78	80
634	03	E2	0F	3F	02	3A	80	D0	72	38	2D	40	10	2C	45	80
635	40	84	63	00	00	1E	01	1D	00	72	51	D0	1E	20	6E	28
636	55	00	40	84	63	00	00	1E	01	1D	00	BC	52	D0	1E	20
637	B8	28	55	40	40	84	63	00	00	1E	00	00	00	00	00	1D

The user can also disable EDID read from the slave to facilitate the use of an external EEPROM for EDID, using register **EXTERNAL_EDID_SEL**.

Please note that if the external EDID option is selected the SCDC functionality will still be retained.

3.6.3. HDMI Data Rate Detection

After the HPD is set, device will measure TMDS clock frequency. Based on the

TMDS_CLOCK_RATIO_STATUS value, set by the HDMI source through the SCDC, and the calculated TMDS clock frequency, one out of the ten supported input data rates is selected.

Table 3-47: Supported HDMI Input Data Rates

Bit Rate [Gb/s]	0.74	0.93	1.11	1.49	1.86	2.23	2.97	3.71	4.46	5.94
TMDS Clock Frequency [MHz]	74.25	92.81	111.38	148.50	185.63	222.75	297.00	92.81	111.38	148.50
TMDS_CLOCK_RATIO_STATUS	0	0	0	0	0	0	0	1	1	1

When the input data rate is selected and receiver are programmed accordingly, they will lock to and de-serialize three input TMDS data channels.

3.6.4. HDMI Receiver

The de-serialized data from the PMA receivers go through a process of byte alignment and channel de-skew to compensate for any inter-pair skew introduced by the TMDS link or de-serialization process. Once the TMDS

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characters are properly aligned, they go through the decoding process to recover the video and auxiliary data of the HDMI input stream.

The TMDS decoding process supports scrambling as described in section 6.1.2 of the HDMI 2.0a specification.

After decoding audio and InfoFrame data are extracted and, based on the detected video format, the video data are mapped and formatted to a SDI video stream.

3.6.5. Output Format Selection

Based on detected data rate and video format from the Info Frame (VIC, colour sub-sampling, frame rate, colour depth), the output format and adequate SDI mapping (2SI, HFR, etc) are selected.

Table 3-48 lists the relation between the HDMI video formats and selected SDI formats.

Table 3-48: Selected Output SDI Data Rates and PID Byte1 Depending on Detected Video Formats

Image Format	Frame Rate	Colour Sub-sampling	Colour Depth	SMPTE Data Rate	PID
1280x720	25, 50, 60	4:2:2	30 or 24	HD	84
		Other	—	3G	88
1920x1080 and 2048x1080	24, 25 or 30	4:2:2	30 or 24	HD	85
			36	3G	89
		4:4:4	30 or 24	3G	89
			36		
	48, 50 or 60 interlaced	4:2:2	30 or 24	HD	85
			36	3G	89
		4:4:4	30 or 24	3G	89
			36		
	48, 50 or 60	4:2:2	30 or 24	3G	89
			36	6G Mode 2	C1-6GSL, 94-3GDL
		4:4:4	30 or 24	6G Mode 2	C1-6GSL, 94-3GDL
			36		
	96, 100 or 120	4:2:2	30 or 24	6G Mode 3	C1
			36	12G Mode 2	CF-12GSL, C3 -6GDL
		4:4:4	30 or 24	12G Mode 2	CF-12GSL, C3 -6GDL
			36		
3840x2160 or 4096x2160	24, 25 or 30	4:2:2	30 or 24	6G Mode 1	C0-6GSL, 96-3GDL, 85-HDQL
			36	12G Mode 1	CE-12GSL, C2-6GDL, 97-3GQL
		4:4:4	30 or 24	12G Mode 1	CE-12GSL, C2-6GDL, 97-3GQL
			36		

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	48, 50 or 60	4:2:2	30 or 24	12G Mode 1	CE-12GSL, C2-6GDL, 97-3GQL
		4:2:0	30 or 24		
Others		—		12G Mode 1	CE-12GSL, C2-6GDL, 97-3GQL

Some video formats (higher data rates) can be mapped as SL, DL or QL SDI interface. By default SL interface is selected. However, parameter **SDI_OUTPUT_INTERFACE_REG** controls the output interface selection and it can be selected as required (00 & 01 = SL, 11 = DL, 10 = QL).

The detected video format parameters used for output format selection are reported in registers **GB_COLOR_SPACE**, **TMDS_DC_COLOR_DEPTH**, **BIT_DEPTH_DET**, **COLOR_SMPL_DET**, **FRAME_RATE_DET**, **FRAME_RASTER_SEL_DET**, **HDMI_RX_DATA_RATE_DET**.

In the case that they need to be overridden or there are no InfoFrames embedded (internal usage of not fully HDMI compliant TMDS stream), parameters used for mode/output format selection can be overwritten/set through registers: **CDEPTH_OVR**, **COLOR_DEPTH_REG, CSPACE_OVR, COLOR_SPACE_REG, VIC_OVR, VIC_REG, FRAME_RASTER_SEL_OVR, FRAME_RASTER_SEL_REG,**

INTERLACED_INFFRAME_OVR, **INTERLACED_INFFRAME_REG**. In the case if there are no frames detected parameters **INFFRAME_DETECTED_OVR** and **INFFRAME_DETECTED_REG** need to be set as well.

After the HDMI to SDI conversion, data streams are formatted into SMPTE defined virtual interface, depending on the video format as 2, 4 or 8, 10-bit data streams and go through different SDI processing block, PID insertion, ANC blanking and data insertion, Audio and TC insertion.

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3.6.6. Handling of Audio

In HDMI-SDI mode, the GS12270 supports audio data extraction, audio clock regeneration based on N and CTD parameters and audio InfoFrame extraction from HDMI input stream as well as audio insertion in SDI output stream.

From the input HDMI video, up to 8 channels of audio at sample rates of 32kHz, 44.1kHz,

48kHz, 88.2kHz, 96kHz, 176.4kHz or 192kHz, as I^2S or Right Justified serial audio can be de-embedded.

By default, de-embedded audio is sent to SDI audio embedder for re-embedding. The SDI audio block supports embedding of up to 16 audio channels at 48kHz and 8 audio channels at 96kHz. Alternatively different audio inputs can be selected for embedding using parameter **AUDIO_SEL_EXT_HDMI**. The following **AUDIO_SEL_EXT_HDMI** values are possible:

- 01_b (default) – up to 8 channel of audio from the HDMI stream selected.
- $1X_b$ - 8 more channels from the *A_IN_** balls for a combined total of 16 channels are selected (in case of 48kHz audio).
- 00_b - All 16 channels are selected from the *A_IN_** balls. (If the input sampling rate is 96kHz, up to 8 channels of audio can be supplied on either *A_IN_1_2* through *A_IN_7_8* or *A_IN_9_10* through *A_IN_15_16*. CSR parameter **SDI_AUDIO_SEL_9TO16_1TO8B** can be used to make this selection)

Note: If support for HDMI video with embedded audio having sampling rates other than 48kHz or 96kHz is required, audio can be extracted to the balls, sample rate converted to 48kHz/96kHz with a external sample rate converter, and embedded back into SDI video from the balls.

Refer to 3.7 SDI Audio Embedding for more information on embedding audio in the SDI stream.

By default, the serial audio outputs are not enabled. The parameters **AUDIO_DATA_OUT_EN_OVRD, AUDIO_DATA_1TO8_OEN** and **AUDIO_DATA_9TO16_OEN** can be used to enable serial audio outputs via the host interface. Audio clock outputs can be controlled separately using the **AUDIO_CLK_OUT_EN_OVRD** and **AUDIO_CLK_OEN** parameters.

The audio channel status of the de-embedded audio is extracted and reported per

channel base in registers **HDMI_RX_AUDIO_CH_STAT_BYTE_0** to **HDMI_RX_AUDIO_CH_STAT_BYTE_23**. The parameter

HDMI_RX_AUD_CH_STATUS_SELECT can be used to select the channel to read the channel status data from. The value 000_h selects channel status for channel 1 and 111_h for channel 8.

3.6.7. Handling of ANC Data

By default, in the HDMI to SDI video data conversion process PIDs and ANC blanking data are inserted and the user ANC data insertion is disabled. It can be enabled via the **ANC_INS_EN** parameter in the host. For more information on inserting ancillary data into the SDI stream, refer to 3.9.4 ANC Data Insertion.

Default values for ANC blanking data used in HDMI - SDI conversion can be changed using parameters: **BLANK_EN**, **BLANK_Y_RGB**, **BLANK_Y_RGB_FULL**, **BLANK_CB_CR**, **BLANK_CB_CR_FULL**, **FULL_RANGE_OVR**, **FULL_RANGE**.

In addition to overwriting the default ANC blanking values, the blanking data can be customized per stream base after the conversion using **HDMI_RX_DS<n>_BLANK_0** and **HDMI_RX_DS<n>_BLANK_1**, (n =1-8, determines data stream).

In the case of SDI output formats having the alpha channel, the default alpha channel value is set by parameter **DEFAULT_ALPHA_VALUE_REG**. The default value, after reset, is 40_h and can be changed by the user.

3.6.8. PID Calculation

The PID byte values are calculated based on the format detected from the InfoFrames and the output interface selected (SL, DL or QL).

The following detected PID entries can be set/modified by user:

TRANSFER_CHAR_OVR, **TRANSFER_CHAR_REG**, **ICTCP_YCBCR_OVR**, **ICTCP_YCBCR_REG**, **PID_COLORIMETRY_OVR**, **PID_COLORIMETRY_REG**, **AUDIO_COPY_STATUS**.

Alternatively, the whole PID, all bits, can be replaced. The PID replacement differs from the PID insertion described in 3.4.6.3 Manual Insertion of Payload ID. Parameter **PID_OVERRIDE** is used to enable manual insertion. The parameter **PID_BYTE_OVERRIDE** is used to mask PID bytes for insertion, and **PID_PROGRAM_VID_STREAM_MASK[7:0]** to select a stream in which the PID is to be replaced, one bit per stream bit[0] stream 1.

Two different set of PIDs (set of four bytes) can be specified for PID replacement: PIDA (defined through parameters **PID_INS_CH0A_DS1_BYTE_1** to **PID_INS_CH0A_DS1_BYTE_4**) and PIDB (**PID_INS_CH0A_DS2_BYTE_1** to **PID_INS_CH0A_DS2_BYTE_4**).

Parameter **PID_PROGRAM_VID_STREAM_MASK[15:8]** is used to select PIDA or PIDB per stream base, bit[8] stream 1, bit value 0 selects PIDA and 1 PIDB.

Additionally the Link number can be override too. Parameter **OVERRIDE_STREAM_NUMBER_SEL[7:0]** controls enabling of the link number override (one bit per stream) and parameter **LINK_N_0_7B** sets the link number (16-bit parameter, two bits per stream for link number, bits[1:0] for stream 1).

3.6.9. InfoFrames

The following InfoFrames are extracted and available via the host interface:

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- AVI InfoFrame
- Audio InfoFrame
- HDMI Vendor Specific InfoFrame
- Dynamic Range and Mastering InfoFrame
- Generic InfoFrame

For the AVI InfoFrame, Header information is stored from registers $700C_h$ to $700D_h$, with bits 8 to 15 of register $700D_h$ set as reserved. PB data is stored in registers $700E_h$ to 7014_h, with bits 8 to 15 of register 7014_h set as reserved. This structure is applicable for all InfoFrames. See Section 3.6 and Section 4. Register Descriptions for more details.

The audio info frame fields are reported in registers **HDMI_RX_AUDIO_INFOFRAME_PKT_FIELDS** and **HDMI_RX_AUDIO_INFOFRAME_PKT_FIELDS**. The HDMI Vendor specific InfoFrame header information is stored in **HDMI_RX_VENDOR_INFOFRAME_IEEE_REG_ID** and **HDMI_RX_VENDOR_INFOFRAME_IEEE_REG_ID_2** and PB data, as packet fields, are stored in **HDMI_RX_VDR_INFO_HDMI_VIC** and **HDMI_RX_VDR_INFO_VIDEO_FORMAT**.

For the AVI InfoFrame, PB data is stored in registers $601E_h$ to 6021_h, split into defined InfoFrame fields.

The Dynamic Range and Mastering InfoFrame PB data is stored in registers 6023_h to $602F_h$.

The user can use the Generic InfoFrame to define any InfoFrame to be extracted. The InfoFrame type to be selected can be defined using **HDMI_RX_GEN_PKT_HEADER**. The extracted InfoFrame data for the type selected will be stored in registers 6048_h to 6059_h.

3.6.9.1. HDMI-SDI Output Loop Bandwidth

The output loop bandwidth in HDMI-SDI mode is determined by the loop bandwidth of the external PLL.

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3.7. SDI Audio Embedding

When the GS12270 is in SDI-SDI or HDMI-SDI configurations, up to 16 channels of audio in eight pairs are embedded in the serial output signal, according to SMPTE ST 299. The 16 channels will be in four groups, which are selectable via the host interface from the groups allowed by SMPTE ST 299, ST 299-1, and ST 299-2.

3.7.1. Audio Register Offset

SDI Audio Embedding is handled by two identical Audio blocks to allow up to 16 channels of Audio Embedding. Each audio 'core' has an identical block of registers which is offset by 2048 (800_h). Table 3-49 shows the GS12270 block names and their associated block offsets.

Table 3-49: Audio Core Address Offset

Name	Address Offset Value$_h$
SDI Audio Embedding Core 1	5000
SDI Audio Embedding Core 2	5800

All lane registers are labelled as: *, where * is a value that is either 0 or 8 for Register Names and 1 or 2 for Parameter Names, respectively.

For example: to program **HD_STATUS_1** on lane 2, write to register:

$800_h + 5000_h = 5800_h$

$2048_d + 20480_d = 22528_d$

3.7.2. Input Data Stream Selection

All 16 channels of audio can be embedded on one data stream, or up to 8 channels of audio can be embedded on each of two data streams. The data stream selection can be made using the **AUD_INS_*_CH_SEL** parameters.

3.7.3. Audio Embedding Operating Modes

Audio Embedding operates in one of three distinct modes.

3.7.3.1. Normal Mode (Default)

All previously embedded audio packets are deleted from the video stream. Arbitrary packets and SMPTE ST 352 packets are not deleted. Up to two audio groups can be added to the video output. SMPTE ST 352 packets are placed before the audio packets. Arbitrary packets are placed after the audio packets.

Note: 16 channels of audio can be implemented by setting the first audio core to 'Normal Mode' and setting the second audio core to 'Cascade Mode'.

3.7.3.2. Cascade Mode

No previously embedded packets are deleted from the video stream. Up to four audio groups can be added to the video output. The added audio groups will not replace existing embedded audio groups. The added audio packets are appended to the last packet in the video input.

3.7.3.3. Group Replacement Mode

All packets associated with the groups being replaced are deleted. Up to four audio groups can be added to the video output. The added audio groups replace any embedded audio groups with the same group number. This will not affect any of the other audio groups, and they will remain in the data stream. The embedded audio groups are sorted in ascending order by audio group number. SMPTE ST 352 packets are placed before the audio packets. Arbitrary packets are placed after the audio packets. The operating mode is selected using a combination of the **AUD_INS_*_EN_CASCADE** and the **AUD_INS_*_AGR** bits in the host interface, as stated in Table 3-50 below.

Table 3-50: Audio Embedding Operating Mode Selection

Control Signals	Operating Mode
EN_CASCADE = 0, AGR = 0	Normal Mode
EN_CASCADE = 1, AGR = 0	Cascade Mode
EN_CASCADE = 0, AGR = 1	Group Replacement Mode
EN_CASCADE = 1, AGR = 1	Group Replacement Mode

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3.7.4. Serial Audio Data Inputs

The GS12270 supports the embedding of up to 16 channels of embedded audio, in four groups of four channels.

Each audio group has a dedicated audio group enable input ball; two Word Clock (*WCLK*) input balls operating at 48kHz or 96kHz; two Audio Clock (*ACLK*) input balls operating at 3.072MHz or 6.144MHz (64 x WCLK); and eight serial digital audio input balls (*A_IN_1_2*, etc.), supporting one stereo audio signal pair per ball.

When the **AUD_INS_1_EN_GRP1/2** parameter is set HIGH, audio embedding is enabled in the first or second group of the first audio embedding core. When the **AUD_INS_2_EN_GRP1/2** parameter is set HIGH, audio embedding is enabled in the first or second group of the second audio embedding core. The Serial Audio Data Inputs for each audio group are listed in Table 3-51.

Table 3-51: Serial Audio Input Ball Description

Ball Name	Description
	Audio Group A
A_IN_1_2	Serial Audio Input; Channels 1 and 2
A_IN_3_4	Serial Audio Input; Channels 3 and 4
ACLK_IN_1	64 x WCLK associated with A_IN_1_2 to A_IN_7_8 (channels 1 to 8) (for Group A and B)
WCLK_IN_1	48kHz or 96kHz Word Clock associated with A_IN_1_2 to A_IN_7_8 (channels 1 to 8) (for Group A and B)
	Audio Group B
A_IN_5_6	Serial Audio Input; Channels 5 and 6
A_IN_7_8	Serial Audio Input; Channels 7 and 8
	Audio Group C
A_IN_9_10	Serial Audio Input; Channels 9 and 10
A_IN_11_12	Serial Audio Input; Channels 11 and 12
ACLK_IN_2	64 x WCLK associated with A_IN_9_10 to A_IN_15_16 (channels 9 to 16) (for Group C and D)
WCLK_IN_2	48kHz or 96kHz Word Clock associated with A_IN_9_10 to A_IN_15_16 (channels 9 to 16) (for Group C and D)
	Audio Group D
A_IN_13_14	Serial Audio Input; Channels 13 and 14
A_IN_15_16	Serial Audio Input; Channels 15 and 16

The serial audio input signals and WCLK input signals will enter the device on the rising edge of ACLK as shown in Figure 3-13.

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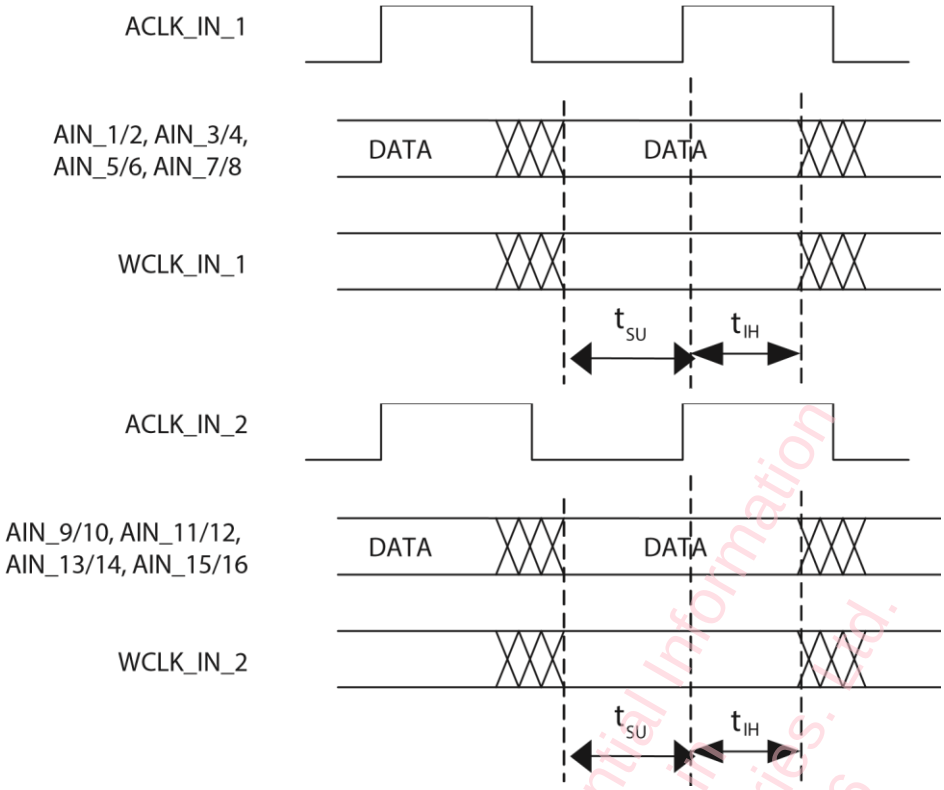

Figure 3-13: ACLK to Data and Control Signal Input Timing

When **AUD_INS_*_EN_GRP1/2** is set HIGH, the respective audio group is enabled, and the audio input signals associated with that group are processed and embedded into the video data stream.

When **AUD_INS_*_EN_GRP1/2** is set LOW, the respective audio group is disabled and the audio input signals associated with that group are ignored. In addition, all functional logic associated with audio embedding for the disabled audio group is placed in a static operating mode, such that system power is reduced while the device configuration is retained.

3.7.5. Serial Audio Data Format Support

The GS12270 supports the following serial audio data formats:

- I^2S Audio (default)
- AES/EBU (**Note:** applies to 48kHz audio sampling rate only)
- Serial Audio, Left Justified, MSB First
- Serial Audio, Left Justified, LSB First
- Serial Audio, Right Justified, MSB First
- Serial Audio, Right Justified, LSB First

By default, the I^2S data format is enabled (at power-up or after system reset).

The audio format can be different for all audio groups. Normally, *A_IN_1_2* and *A_IN_3_4* are embedded in Audio Group A, and *A_IN_5_6* and *A_IN_7_8* are embedded in Audio Group B, etc.

For register 5007_h:

AUD_INS_1_AMA sets the audio format for *A_IN_1_2* **AUD_INS_1_AMB** sets the audio format for *A_IN_3_4*

AUD_INS_1_AMC sets the audio format for *A_IN_5_6*

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AUD_INS_1_AMD sets the audio format for *A_IN_7_8* For register 5807_h:
AUD_INS_2_AMA sets the audio format for *A_IN_9_10*
AUD_INS_2_AMB sets the audio format for *A_IN_11_12*
AUD_INS_2_AMC sets the audio format for *A_IN_13_14*
AUD_INS_2_AMD sets the audio format for *A_IN_15_16*

Note: These eight formats can all be set to different modes if desired.

Table 3-52 shows the audio input formats for the GS12270. Note that the same values apply for **AUD_INS_*_AMB** + **AUD_INS_*_LSB_FIRSTB**, **AUD_INS_*_AMC** + **AUD_INS_*_LSB_FIRSTC** and **AUD_INS_*_AMD** + **AUD_INS_*_LSB_FIRSTD**.

Table 3-52: Audio Input Formats

AMA[1:0] (Address 5007_h and 5807_h)	LSB_FIRSTA (Address $500C_h$ and $580C_h$)	Audio Input Formats
00	X	AES/EBU audio input
01	0	Serial audio input; Left Justified; MSB First
01	1	Serial audio input; Left Justified; LSB First
10	0	Serial audio input; Right Justified; MSB First
10	1	Serial audio input; Right Justified; LSB First
11	X	I^2S (default)

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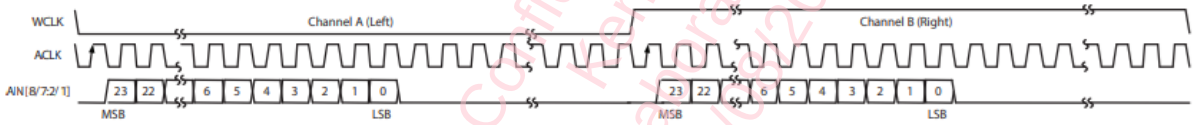

Figure 3-14: I^2S Audio Input Format

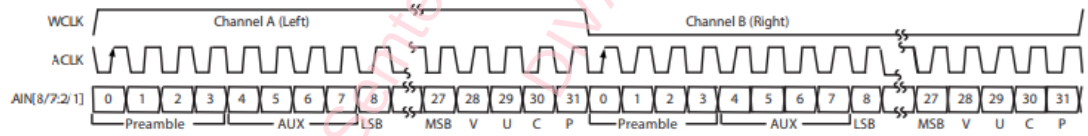

Figure 3-15: AES/EBU Audio Input Format

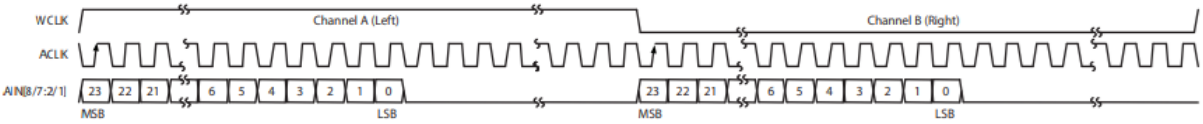

Figure 3-16: Serial Audio, Left Justified, MSB First

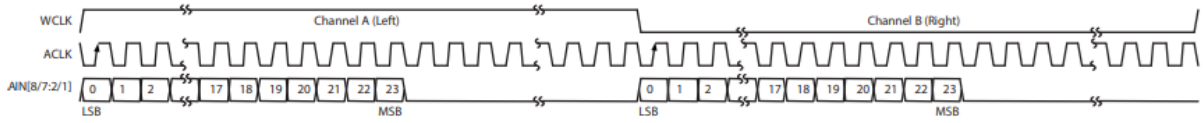

Figure 3-17: Serial Audio, Left Justified, LSB First

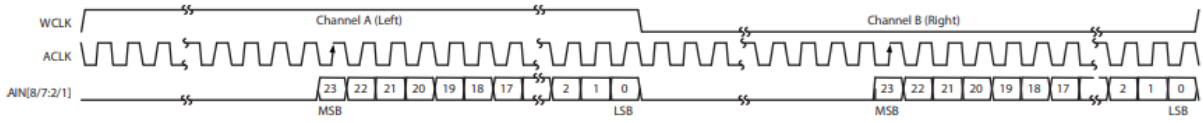

Figure 3-18: Serial Audio, Right Justified, MSB First

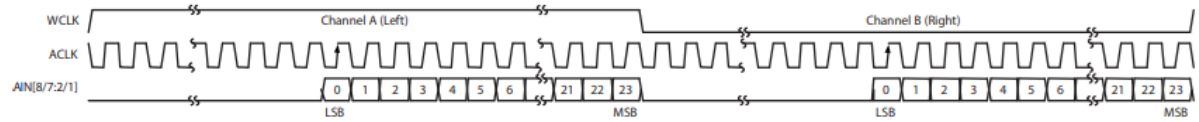

Figure 3-19: Serial Audio, Right Justified, LSB First

3.7.6. Audio Packet Detection and Deletion

The input video stream to the GS12270 may already contain embedded audio packets.

The GS12270 detects these embedded packets, and signals their presence to the host interface.

Registers 5004_h and 5005_h contain embedded packet info for the datastream input chosen for audio core 1.

Registers 5804_h and 5805_h contain embedded packet info for the datastream input chosen for audio core 2.

The first ADF must always be contiguous after the two line CRC words.

Ancillary data packets with non-audio data ID words such as arbitrary and SMPTE ST 352 are not deleted from the data stream. On lines where SMPTE ST 352 packets exist, the audio data packets must be contiguous from the ST 352 packets. If this is not the case, all existing audio data and control packets will be deleted.

When **CASCADE** is set HIGH, all pre-existing audio data and control packets remain in the video stream.

When the **AUD_INS_*_AGR** bit in the host interface is set HIGH, Audio Group Replacement mode is selected. In this mode, existing audio data and control packets are not deleted from the data stream.

In cases where the ADF is not placed immediately after the CRC words, or there are gaps between the packets, the GS12270 deletes all existing audio data and control packets, regardless of the **CASCADE** or **AUD_INS_*_AGR** setting.

3.7.7. Audio Word Clock

When the GS12270 combines two stereo pair inputs into one audio group, the format allows for only one Word Clock, or sampling clock.

For Group A, the GS12270 uses the Word Clock associated with the source selected by the **AUD_INS_*_GPA_WCLK_SRC[14:12]** host interface field. The register can be found under addresses 5008_h and 5808_h.

For Group B, the GS12270 uses the Word Clock associated with the source selected by the **AUD_INS_*_GPB_WCLK_SRC[14:12]** host interface field. The register can be found under addresses 5009_h and 5809_h.

For proper operation, the combined Stereo Pair inputs must have identical Word Clocks. WCLK is not required for AES/EBU audio.

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3.7.8. Channel & Group Activation

The GS12270 embeds Group A packets when any of the following host interface bits are set and the associated audio group enable register is HIGH (Registers $500C_h$ and $580C_h$):

AUD_INS_*_ACT1 embeds Group A audio channel 1

AUD_INS_*_ACT2 embeds Group A audio channel 2

AUD_INS_*_ACT3 embeds Group A audio channel 3

AUD_INS_*_ACT4 embeds Group A audio channel 4

If none of the bits are set, then no audio will be embedded.

The GS12270 embeds Group B packets when any of the following host interface bits are set and the associated audio group enable register is HIGH (Registers $500C_h$ and $580C_h$):

AUD_INS_*_ACT5 embeds Group B audio channel 1

AUD_INS_*_ACT6 embeds Group B audio channel 2

AUD_INS_*_ACT7 embeds Group B audio channel 3

AUD_INS_*_ACT8 embeds Group B audio channel 4

When an embedded packet contains one or more channels with the

AUD_INS_*_ACT<n> bit set to zero, the GS12270 replaces the data for those channels with null samples (all bits set to zero).

In the default state, the GS12270 embeds all audio channels in accordance with the setting of the respective audio group enable registers of the device.

3.7.9. Audio Crosspoint

There is a crosspoint in each audio embedding core which allows each output channel for Group A and Group B to be selected from any of the input channels to that embedding core. This can be configured using the **AUD_INS_*_GP*_CH*_SRC** parameters. Audio channels can be paired only when both channels are derived from the same WCLK and are synchronous. The same audio channel can not be used in both Group A and Group B at the same time. The status output **AUD_INS_*_XPOINT_ERROR** shall be asserted in this case.

3.7.10. Frame Sequence Detection

The GS12270 detects the frame sequence that describes the sample distribution for synchronous audio.

The frame sequence is only used in the generation of audio control packets; where the Audio Frame Number (AFN) field describes the position of the current frame within the frame sequence.

The GS12270 sets the AFN of the Primary group control packets to zero when the ASXA host interface bit is set for asynchronous audio. The GS12270 sets the AFN of the Primary group control packets to zero, unless the **AUD_INS_*_AFNA_AUTO** host interface bit is set to produce automatic AFN generation.

The GS12270 sets the AFN of the Secondary group control packets to zero, when the

ASXB host interface bit is set for asynchronous audio. The GS12270 sets the AFN of the Secondary group control packets to zero, unless the **AUD_INS_*_AFNB_AUTO** host interface bit is set to produce automatic AFN generation.

The GS12270 sets the AFN to one when every frame has the same number of samples:

Frame Rate 23.976Hz - Each frame has exactly 2002 samples

Frame Rate 24.000Hz - Each frame has exactly 2000 samples

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Frame Rate 25.000Hz - Each frame has exactly 1920 samples

Frame Rate 30.000Hz - Each frame has exactly 1600 samples

Frame Rate 50.000Hz - Each frame has exactly 960 samples

Frame Rate 60.000Hz - Each frame has exactly 800 samples

When the frame rate is 29.97Hz, an even number of samples (8008) are distributed over five frames in the following sequence: 1602 1601 1602 1601 1602

When the frame rate is 59.94Hz, an even number of samples (4004) are distributed over five frames in the following sequence: 801 800 801 801 801

The GS12270 sets the AFN field to a number between one and five, depending on where the current frame lies within the sequence.

The GS12270 adds the offset specified in the **AUD_INS_*_AFN_OFS** host interface field to the generated AFN. The result of the addition wraps around such that the AFN will always be in the range of one to five.

3.7.11. ECC Error Detection and Correction

The GS12270 generates the error detection and correction fields in the audio data packets.

The error detection and correction complies with SMPTE ST 299.

3.7.12. Audio Control Packet Embedding

The GS12270 embeds audio control packets associated with all four audio groups.

The Group A audio to be embedded is specified using the **AUD_INS_*_IDA[1:0]** host interface field.

The Group B audio to be embedded is specified using the **AUD_INS_*_IDB[1:0]** host interface field.

The Group A audio control packets are embedded as commanded by the **AUD_INS_*_CTRA_ON** host interface bit.

The Group B audio control packets are embedded as commanded by the **AUD_INS_*_CTRB_ON** host interface bit.

The Group A audio control packets are replaced as commanded by the **AUD_INS_*_CTR_AGR** host interface bit.

The Group B audio control packets are replaced as commanded by the **AUD_INS_*_CTR_AGR** and **AUD_INS_*_ONE_AGR** host interface bits.

The Group A audio control packets are not embedded or replaced unless one or more of the **AUD_INS_*_ACT(1-4**) host interface bits are set.

The Group B audio control packets are not embedded or replaced unless one or more of the **AUD_INS_*_ACT(5-8)** host interface bits are set.

The contents of the Group A audio control packet is specified using the following host interface fields:

AUD_INS_*_AUDIO_RATE — Group A audio sampling rate

AUD_INS_*_AFNA_AUTO — Group A audio frame number auto-generation.

AUD_INS_*_ASXA — Group A asynchronous mode.

AUD_INS_*_DEL1_2A[25:0] — Group A audio delay for channels 1 and 2.

AUD_INS_*_DEL3_4A[25:0] — Group A audio delay for channels 3 and 4.

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The contents of the Group B audio control packet is specified using the following host interface fields:

AUD_INS_*_AUDIO_RATE — Group B audio sampling rate

AUD_INS_*_AFNB_AUTO — Group B audio frame number auto-generation.

AUD_INS_*_ASXB — Group B asynchronous mode.

AUD_INS_*_DEL1_2B[25:0] — Group B audio delay for channels 1 and 2.

AUD_INS_*_DEL3_4B[25:0] — Group B audio delay for channels 3 and 4.

3.7.13. Audio Data Packet Embedding

In Normal Mode, the GS12270 embeds audio data packets into a space where all pre-existing embedded audio data packets have been removed.

In Cascade Mode, the GS12270 embeds audio data packets contiguously after all of the pre-existing audio data packets. The GS12270 does not replace any pre-existing audio data packets with new audio packets, even if the new audio packets have the same group number. In this situation, the new audio data packets are appended to the last packet, and there is an illegal mix of different groups using the same group number. This condition will be indicated by the following host interface bits:

AUD_INS_*_EN_MUX_ERRA: Set in Cascade Mode when Group A audio data packets are added to video that already contains audio data packets with the same group number.

AUD_INS_*_EN_MUX_ERRB: Set in Cascade Mode when Group B audio data packets are added to video that already contains audio data packets with the same group number.

In Group Replacement Mode, the GS12270 embeds audio data packets and sorts all of the embedded audio data packets in order of group number. If there are any pre-existing audio data packets with the same group number as the new audio packets, then the pre-existing packets will be replaced.

In Group Replacement Mode, the GS12270 replaces only the Group A audio if the **AUD_INS_*_ONE_AGR** host interface bit is set.

The GS12270 deletes arbitrary data packets if there is not enough room in the horizontal ancillary data space to embed the selected audio data packets.

The GS12270 does not embed audio data packets when there is insufficient room in the horizontal ancillary data space after deleting arbitrary data packets.

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3.7.13.1. Blanking Values Following Audio Data Packet Embedding

For $Y'C'_BC'_R$ 4:2:2 10-bit formats, the audio embedding block will embed blanking data in accordance with the original video format.

For all other video formats (for example: RGB 4:4:4 10-bit or 12-bit, $Y'C'_BC'_R$ 12-bit), the audio block will embed blanking values of 200_h and 040_h, which may not match the

blanking data of the original format. If no audio is being deleted, the parameter **AUD_INS_*_DISABLE_ANC_BLANKING** can be set HIGH to prevent blanking values from being updated.

3.7.14. Audio Mute

All embedded audio is muted when the parameter **AUD_INS_*_MUTE_ALL** is set HIGH. To mute individual audio channels, the **AUD_INS_*_MUTE*** parameters can be used. Note that the **AUD_INS_*_MUTE*** parameters mute the audio channels prior to the crosspoint.

3.7.15. Audio Channel Status

When the parameter **ACS_REGEN** is set LOW and the incoming audio format is AES/EBU, the incoming audio channel status from the input is embedded in the audio packets.

In HDMI-SDI configuration, when the parameter **AUD_INS_*_OVERRIDE_HDMI_CH_STAT** is LOW, the channel status from the HDMI input is first converted from consumer to professional and then embedded in the SDI audio packets. To embed the HDMI channel status without conversion, the parameter **AUD_INS_*_CHANNEL_STATUS_INS_NO_MOD** must be set HIGH.

In all other cases, the audio channel status to be embedded should be provided via the **ACSR_*** parameters and then **ACS_REGEN** should be set HIGH.

3.7.16. Audio Interrupt Control

The GS12270 will assert the interrupt signal when an internal interrupt condition becomes true. By default, the interrupts will be displayed on their corresponding registers. The interrupts can also be selected to be displayed on the *STAT* balls. By default, the interrupts are all disabled.

The following host interface bits enable the various interrupt sources:

Table 3-53: Audio Interrupt Control Addresses

Bit Name	Description	Bit Address
EN_MUX_ERRB	Asserts interrupt when EN_MUX_ERRB flag is set	$5*0B_h$[13:13]
EN_MUX_ERRA	Asserts interrupt when EN_MUX_ERRA flag is set	$5*0B_h$[12:12]
EN_AES_ERRD	Asserts interrupt when EN_AES_ERRD flag is set	$5*0B_h$[11:11]
EN_AES_ERRC	Asserts interrupt when EN_AES_ERRC flag is set	$5*0B_h$[10:10]
EN_AES_ERRB	Asserts interrupt when EN_AES_ERRB flag is set	$5*0B_h$[9:9]
EN_AES_ERRA	Asserts interrupt when EN_AES_ERRA flag is set	$5*0B_h$[8:8]
EN_ACPG4_DET	Asserts interrupt when ACPG4_DET flag is set	$5*0A_h$[7:7]
EN_ACPG3_DET	Asserts interrupt when ACPG3_DET flag is set	$5*0A_h$[6:6]
EN_ACPG2_DET	Asserts interrupt when ACPG2_DET flag is set	$5*0A_h$[5:5]
EN_ACPG1_DET	Asserts interrupt when ACPG1_DET flag is set	$5*0A_h$[4:4]
EN_ADPG4_DET	Asserts interrupt when ADPG4_DET flag is set	$5*0A_h$[3:3]
EN_ADPG3_DET	Asserts interrupt when ADPG3_DET flag is set	$5*0A_h$[2:2]
EN_ADPG2_DET	Asserts interrupt when ADPG2_DET flag is set	$5*0A_h$[1:1]
EN_ADPG1_DET	Asserts interrupt when ADPG1_DET flag is set	$5*0A_h$[0:0]

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3.8. SDI Audio De-Embedding

Up to 16 channels of audio may be de-embedded from the received serial digital video stream. The output signal formats supported by the device include AES/EBU, I²S (default), and industry standard serial digital formats.

16, 20, and 24-bit audio bit depths are supported for 48kHz and 96kHz audio sampling rates. The audio may be synchronous or asynchronous to the video.

For formats carried over 3G, 6G and 12G, Audio Control Packets are de-embedded from Data Stream 1 and all Audio Data Packets are de-embedded from Data Stream 2, in accordance with SMPTE ST 425. For HD at 1.5G, Audio Control Packets are embedded in the Luma channel and Audio Data Packets in the Chroma channel.

Additional audio processing features include audio mute on loss of lock, group selection, audio output remapping, and audio channel status de-embedding.

3.8.1. Audio Register Offset

SDI Audio De-Embedding is handled by two identical Audio blocks to allow up to 16 channels of Audio De-Embedding. Each audio 'core' has an identical block of registers which is offset by 2048 (800_h). Table 3-54 shows the GS12270 block names and their associated block offsets.

Table 3-54: Audio Core Address Offset

Name	Address Offset Value$_h$
SDI Audio De-embedding Core 1	4000
SDI Audio De-embedding Core 2	4800

All lane registers are labelled as: *, where * is a value that is either 0 or 8 for Register Names and 1 or 2 for Parameter Names, respectively.

For example: to program **CFG_AUD** on lane 2, write to register:

$800_h + 4001_h = 4801_h$

$2048_d + 16385_d = 18433_d$

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3.8.2. Input Data Stream Selection

All 16 channels of audio can be de-embedded from one data stream, or up to 8 channels of audio can be de-embedded from each of two data streams. The data stream selection can be made using the **AUD_EXT_*_CH_SEL** parameters.

3.8.3. Serial Audio Data Output Signals

The Serial Audio Data Output balls are listed in Table 3-55.

Table 3-55: Serial Audio Ball Descriptions

Ball Name	Description
A_OUT_1/2	Serial Audio Output; Channels 1 and 2
A_OUT_3/4	Serial Audio Output; Channels 3 and 4
A_OUT_5/6	Serial Audio Output; Channels 5 and 6
A_OUT_7/8	Serial Audio Output; Channels 7 and 8
A_OUT_9/10	Serial Audio Output; Channels 9 and 10
A_OUT_11/12	Serial Audio Output; Channels 11 and 12
A_OUT_13/14	Serial Audio Output; Channels 13 and 14
A_OUT_15/16	Serial Audio Output; Channels 15 and 16
ACLK_OUT	64fs Audio Bit Clock
WCLK_OUT_1/2	Word Clock
AMCLK	Audio Master Clock, selectable 128fs, 256fs, or 512fs

The timing of the serial audio out signals, the WCLK output signal and the ACLK output is shown in Figure 3-20.

When the **AUD_EXT_1_EN** parameter in the **AUDIO_ENABLE** register is set HIGH, audio de-embedding is enabled for the first audio de-embedding core and the audio output signals are de-embedded from the video data stream. When the **AUD_EXT_2_EN** parameter is set HIGH, audio de-embedding is enabled for the second audio de-embedding core. See Table 4-6 for detailed information.

When **AUD_EXT_*_EN** is set LOW, the respective audio group is disabled and all functional logic associated with audio de-embedding for the disabled group is placed in a static operating mode, such that system power is reduced while the device configuration is retained.

Note: When the second audio de-embedding core is enabled and the input is 96kHz audio, the channel pairs in the second audio de-embedding core's audio crosspoint must be swapped. Refer to Section 3.8.5.2 for more detail.

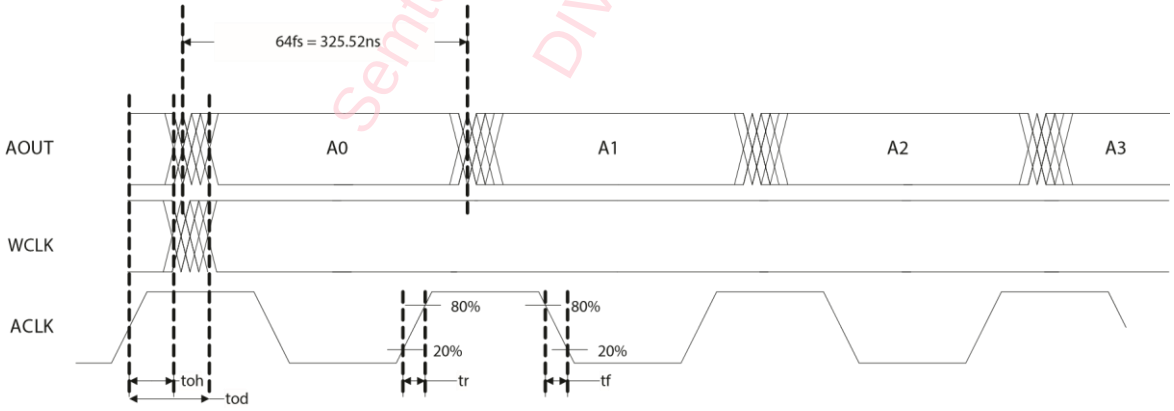

Figure 3-20: ACLK to Data Signal Output Timing

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3.8.4. Serial Data Format Support

The GS12270 supports the following serial audio data formats:

- I²S (default)
- AES/EBU
- Serial Audio Left Justified, MSB First
- Serial Audio Right Justified, MSB First

By default (at power-up or after system reset), I²S is selected. The other data formats are selectable via **AUD_EXT_*_AMA/AMB[1:0]** of **CFG_AUD** (Address 4001_h and 4801_h, bit[7:6]/bit[9:8]).

Note: The **AMA[1:0]** register must be set to I²S when the GS12270 is set to SDI-HDMI Mode. This also applies for **AMB**, **AMC**, and **AMD**.

Table 3-56: Audio Output Formats

AMA/AMB/AMC/ AMD[3:0]	Audio Output Format
00	AES/EBU audio output
01	Serial audio output; Left Justified; MSB first
10	Serial audio output; Right Justified; MSB first
11	I²S (Default)

When I²S format is desired, all groups must be set to I²S

(i.e. AMA = AMB = 11). This is because they share the same WCLK for each register offset (5007_h or 5807_h).

3.8.4.1. AES/EBU Mode

In AES/EBU output mode, the audio de-embedder uses a 128fs (6.144MHz audio bit clock for a 48kHz sampling rate) clock as shown in Figure 3-21.

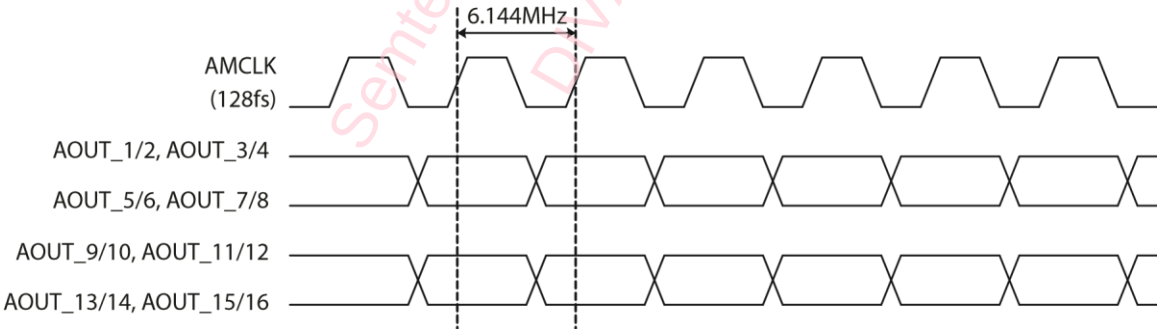

Figure 3-21: AES/EBU Audio Output to Bit Clock Timing

3.8.4.2. Audio Data Packet De-Embedding Block

The audio de-embedder looks for audio data packets on every line of the incoming video.

The audio data must be embedded according to SMPTE ST 299/299-1/299-2.

The audio data packets must be embedded only in Data Stream 2.

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The Audio Group Detect registers are set HIGH when audio data packets with a corresponding group DID are detected in the input video stream. The host interface reports the individual audio groups detected.

Table 3-57: Audio Data Packet Detect Register

Name	Description	Default
ADPG8_DET	Audio Group Eight Data Packet Detection (1: Detected)	0
ADPG7_DET	Audio Group Seven Data Packet Detection (1: Detected)	0
ADPG6_DET	Audio Group Six Data Packet Detection (1: Detected)	0
ADPG5_DET	Audio Group Five Data Packet Detection (1: Detected)	0
ADPG4_DET	Audio Group Four Data Packet Detection (1: Detected)	0
ADPG3_DET	Audio Group Three Data Packet Detection (1: Detected)	0
ADPG2_DET	Audio Group Two Data Packet Detection (1: Detected)	0
ADPG1_DET	Audio Group One Data Packet Detection (1: Detected)	0

AUD_EXT_*_EXTEND_IDA and AUD_EXT_*_EXTEND_IDB in **CFG_AUD** Audio de-embedding registers (Address 4001_h and 4801_h, bits 2 and 5) are used in addition to **AUD_EXT_*_IDA[1:0]** and **AUD_EXT_*_IDB[4:3]** in **CFG_AUD** Audio de-embedding registers (Address 4001_h and 4801_h, bits [1:0] and [4:3]) to select one of 8 audio groups.

The embedded audio group in register 4001_h, selected by **AUD_EXT_1_IDA[1:0]**, is described henceforth in this document as Group A. The embedded audio group in register 4001_h, selected by **AUD_EXT_1_IDB[4:3],** is described henceforth in this document as Group B. The embedded audio group in register 4801_h, selected by **AUD_EXT_2_IDA[1:0]**, is described henceforth in this document as Group C. The embedded audio group in register 4801_h, selected by **AUD_EXT_2_IDB[4:3]**, is described henceforth in this document as Group D.

3.8.4.3. Audio Control Packets

The audio de-embedder automatically detects the presence of audio control packets in the video stream. When audio control packets for audio Group A are detected, **AUD_EXT_1_CTRA_DET** (Address 4003_h, bit 4) is set HIGH. When audio control packets for audio Group B are detected, **AUD_EXT_1_CTRB_DET** (Address 4003_h, bit 5) is set

HIGH. When audio control packets for audio Group C are detected,

AUD_EXT_2_CTRA_DET (Address 4803_h, bit 4) is set HIGH. When audio control packets for audio Group D are detected, **AUD_EXT_2_CTRB_DET** (Address 4803_h, bit 5) is set HIGH.

The audio control packet data is accessible via the host interface.

The audio control packets must be embedded according to SMPTE ST 299. The audio control packets must be embedded in Data Stream 1.

Note 1: The audio control packet reporting via the host interface updates automatically when a new control packet is detected.

Note 2: If there is an audio packet checksum error, no audio is de-embedded. The audio packet is not recognized, and the audio stays in the video stream. If only the CLK phase parity bit is incorrect, the audio can still be de-embedded.

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3.8.4.4. Setting Packet DID

Table 3-59 below shows the 2-bit host interface setting for the audio group DIDs.

The audio de-embedder defaults to audio Groups One, Two, Three, and Four, where Group A is extracted from packets with audio Group One DID, Group B from packets with audio Group Two DID, Group C from packets with audio Group Three DID, and Group D from packets with audio Group Four DID.

Table 3-58: Audio Group DID Host Interface Settings

Audio Group	Data DID	Control DID	EXTEND_ID*	ID*
1	$2E7_h$	$1E3_h$	0	00_b
2	$1E6_h$	$2E2_h$	0	01_b
3	$1E5_h$	$2E1_h$	0	10_b
4	$2E4_h$	$1E0_h$	0	11_b
5	$1A7_h$	$2A3_h$	1	00_b
6	$2A6_h$	$1A2_h$	1	01_b
7	$2A5_h$	$1A1_h$	1	10_b
8	$1A4_h$	$2A0_h$	1	11_b

Table 3-59: Audio Data and Control Packet DID Setting Register

Name	Description	Default
IDA[1:0]	Group A Audio data and control packet DID setting	00_b
EXTEND_IDA[0:0]		00_b
IDB[1:0]	Group B Audio data and control packet DID setting	01_b
EXTEND_IDB[0:0]		01_b

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3.8.5. Audio Processing

3.8.5.1. Audio Clock Generation

A single set of audio frequencies is generated for all audio channels.

An Audio Master Clock (AMCLK) is also generated. The frequency is selectable via the host interface **AUDIO_CLK_OUT_SEL** as:

- fs x 128
- fs x 256
- fs x 512

Audio clocks are derived from the two embedded audio clock phase words in the audio data packet.

The audio de-embedder also includes a Flywheel block to overcome any inconsistencies in the embedded audio clock phase information.

If the audio digital PLL is locked to phase data and audio data packets are lost or corrupted, the Clock Generator will flywheel for up to four audio data packets.

If the audio phase data is not present or incorrect, the **AUD_EXT_*_INVALID_EMBEDDED_PHASE[B:A]** (Address $400C_h$ and $480C_h$, bit [3:2]) bits will be asserted and audio will be de-embedded using a clock derived from PCLK and the M value.

Alternatively, when the **AUD_EXT_*_PHASE_IGNORED[B:A]** (Address $400C_h$ and $480C_h$, bit [1:0]) in the host interface is set HIGH, the M value can be programmed via the host interface. This can be done by setting the **AUD_EXT_*_FORCE_M** (Address $400B_h$ and $480B_h$, bit 7) HIGH and programming the desired value into **AUD_EXT_*_FORCE_MEQ1001** (Address $400B_h$, bit 6). The correct value can be obtained by reading the M bit from the Video Core Registers.

If the **AUD_EXT_*_PHASE_IGNORED[B:A]** bit in the host interface is HIGH, the clock will free-run based on the video format, the PCLK and the M value, independent of the **AUD_EXT_*_INVALID_EMBEDDED_PHASE[B:A]** bits.

In the 720p/24 video format, the total line length is 4125 pixels, which requires a resolution of 13 bits for the audio clock phase words in the embedded audio data packets. SMPTE ST 299 only specifies a maximum of 12 bits resolution. The revised versions of SMPTE ST 299 require using bit 5 of UDW1 in the audio data packet as the MSB for the audio clock phase data, providing 13 bits resolution.

Some audio encoders may hold the clock phase value at a maximum value when reached, until reset at the end of the line. This produces a small amount of audio phase jitter for the period of one sample. To overcome this issue, the audio de-embedder checks for all cases. On detection of the maximum value, a comparison is made between previous clock phases and the correct position interpolated. If the clock phase data value starts to decrease, the de-embedder checks to see if bit 5 of UDW1 in the audio data packet is asserted. If bit 5 is asserted, the correct value is used. If bit 5 is not set, the correct position is interpolated.

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3.8.5.2. Audio Crosspoint Block

The Audio Crosspoint is used for audio output channel remapping. This feature allows any of the selected audio channels in Group A or Group B to be output on any of the 16 output channels. The default setting is for one to one mapping, where *A_OUT_1_2* is extracted from Group A CH1 and CH2, *A_OUT_3_4* is extracted from Group A CH3 and CH4, and so on.

Note: If audio samples from embedded audio packets with the group set in

AUD_EXT_*_IDA[1:0] are to be paired with samples from the group set in **AUD_EXT_*_IDB[1:0]**, all of the channels must have been derived from the same Word Clock and must be synchronous.

The output channel is set in the **AUD_EXT_*_OP[8:1]_SRC** parameter of the **OUTPUT_SEL_[2:1]** (Address $400D_h$/$400E_h$ and $480D_h$/$480E_h$) registers. Table 3-60 lists the 3-bit address for audio channel mapping.

For 96kHz audio, both channel pairs are used for one 96kHz audio channel. As such, pairs must be kept together for proper operation. Furthermore, when the second audio de-embedding core is enabled for 96kHz audio, the channel pairs must be swapped for proper operation as shown in Figure 3-22.

Table 3-60: Audio Channel Mapping Codes

Audio Output Channel	3-bit Host Interface Source Address	Audio Group
1	000_b	Primary audio group channel 1
2	001_b	Primary audio group channel 2

3	010_b	Primary audio group channel 3
4	011_b	Primary audio group channel 4
5	100_b	Secondary audio group channel 1
6	101_b	Secondary audio group channel 2
7	110_b	Secondary audio group channel 3
8	111_b	Secondary audio group channel 4



Figure 3-22: Channel Pair Swapping

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3.8.5.3. Serial Audio Output Word Length

The audio output, in Serial mode, has a selectable 24, 20, or 16-bit sample word length. The **AUD_EXT_*_ASWL[D:A]** (Address 4001_h and 4801_h) parameters are used to configure the audio output sample word length. Table 3-61 shows the host interface 2-bit code for setting the audio sample word length.

Table 3-61: Audio Sample Word Lengths

ASWL[D:A]	Audio Sample Word Length
00_b	24-bit (default)
01_b	20-bit
10_b	16-bit
11_b	Reserved

3.8.5.4. Audio Channel Status

The GS12270 detects the AES/EBU Audio Channel Status (ACS) block information for each of the selected channel pairs.

ACS data detection is indicated by corresponding **ACS_DET** (Address 4003_h and 4803_h) registers. The flag is cleared by writing to the same location.

3.8.5.5. Audio Channel Status Read

AES/EBU ACS data is available separately for each of the channels in a stereo pair. The

GS12270 defaults to reading the first channel of each pair. There are 184 bits in each

ACS packet, which are written to twelve 16-bit right-justified registers

AUD_EXT_*_ACSR[1_2:3_4]A/B_BYTE[0_1:22] (Address 4040_h to $407B_h$ and 4840_h to $487B_h$).

The **AUD_EXT_*_ACS_USE_SECOND** in **CFG_AUD2** (default LOW) selects the second channel in each audio pair when set HIGH.

Once all of the ACS data for a channel has been acquired, the corresponding **ACS_DET** bit is asserted and acquisition stops. The ACS data is overwritten with new data when the **ACS_DET** bit is cleared in the system.

In SDI-HDMI mode, the channel status extracted from the SDI audio packets is passed to HDMI. By default the channel status is converted from professional to consumer. To keep the channel status unchanged, the

AUD_EXT_*_CHANNEL_STATUS_EXT_NO_MOD parameter must be set HIGH.

3.8.5.5.1. Audio Channel Status Regeneration

When the **AUD_EXT_*_ACS_REGEN** in **REGEN** (Address 4006_h and 4806_h, bit 0) is set HIGH, the GS12270 embeds the 24 bytes of the Audio Channel Status information programmed in the **AUD_EXT_*_ACSR[183:0]** registers into the 'C' bit of the AES/EBU outputs. The same Audio Channel Status information is used for all output channels.

In order to apply ACSR data:

1. Set the **AUD_EXT_*_ACS_REGEN** bit to logic HIGH.
2. Write the desired ACSR data to the **AUD_EXT_*_ACSR** registers.
3. Set the **AUD_EXT_*_ACS_APPLY** bit to HIGH.

At the next status boundary, the device outputs the contents of the **AUD_EXT_*_ACSR** registers as ACS data. This event may occur at a different time for each of the output channels. While waiting for the status boundary, the device sets the appropriate flag: **AUD_EXT_*_ACS_APPLY_WAIT** (Address 4004_h and 4804_h, bit 0).

Table 3-62 shows the host interface default settings for the Audio Channel Status block. The audio de-embedder automatically generates the CRC word.

Table 3-62: Audio Channel Status Information Registers

Name	Description	Default
AUD_EXT_*_ACSR1	Audio channel status block byte 0 set. Used when ACS_REGEN is set HIGH	85_h
AUD_EXT_*_ACSR2	Audio channel status block byte 1 set. Used when ACS_REGEN is set HIGH	08_h
AUD_EXT_*_ACSR3	Audio channel status block byte 2 set. Used when ACS_REGEN is set HIGH	$2C_h$

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AUD_EXT_*_ACSR[4:22]	Audio channel status block data for bytes 3 to 22. Used when ACS_REGEN is set HIGH	00_h
AUD_EXT_*_ACS_REGEN	Audio channel status regenerate	00_h
AUD_EXT_*_ACS_APPLY	Apply new ACSR data	00_h
AUD_EXT_*_ACS_APPLY_WAIT[D:A]	Waiting to apply new ACSR data	00_h
AUD_EXT_*_ACSR[1_2:3_4][B:A]_BYTE[0_1:22]	Audio channel status block data for bytes 0 to 22	00_h: 00_h

Table 3-63: Audio Channel Status Block for Regenerate Mode Default Settings

Name	Byte	Bit	Default	Mode
PRO	0	0	1_b	Professional use of channel status block
Emphasis	0	4:2	100_b	100_b None. Manual override disabled
Sample Frequency	0	7:6	01_b	48kHz. Manual override or auto disabled
Channel Mode	1	3:0	0001_b	Two channels. Manual override disabled
AUX	2	2:0	000_b	Maximum audio word length is 20 bits
			001_b	Maximum audio word length is 24 bits
Source Word Length	2	5:3	101_b	Maximum word length (based on AUX setting)
All other bits set to zero				

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3.8.5.6. Audio Mute

When **AUD_EXT_*_MUTE[B:A]** in **CH_MUTE** (Address 4007_h and 4807_h) are set HIGH, the audio outputs are muted (all audio sample bits are set to zero). To set all the audio output channels to mute, set **AUD_EXT_*_MUTE_ALL** (Address 4002_h and 4802_h, bit 1) HIGH.

Table 3-64: Audio Mute Control Bits

Parameter Name	Description	Default
AUD_EXT_*_MUTEB	Mute Secondary output channels 4 to 1; bits 3:0 = channel 4:1 0 = Normal 1 = Muted	0
AUD_EXT_*_MUTEA	Mute Primary output channels 4 to 1; bits 3:0 = channel 4:1 0 = Normal 1 = Muted	0

3.8.6. Error Reporting

3.8.6.1. Data Block Number Error

When the 1_d to 255_d count sequence in the Data Block Number (DBN) word of Primary/Secondary audio data packets is discontinuous, the **AUD_EXT_*_DBN[B:A]_ERR** bit in **ACS_DET** register is set HIGH.

The **AUD_EXT_*_DBN[B:A]_ERR** flags also have associated **AUDIO_INT_ENABLE2** register flags for configuration of error reporting. The **AUD_EXT_*_DBN[B:A]_ERR** flags remain set until cleared by writing to these locations.

3.8.7. Audio Interrupt Control

The GS12270 will assert the interrupt signal when an internal interrupt condition becomes true. By default, the interrupts will be displayed on their corresponding registers. The interrupts can also be selected to be displayed on the *STAT* balls.

The following host interface bits enable the various interrupt sources:

Table 3-65: Audio Interrupt Control Addresses

Bit Name	Description	Bit Address
AUD_EXT_*_EN_ADPG8_DET	When enabled, interrupt will assert when ADPG8_DET is set.	0x4*09$_h$ [7:7]
AUD_EXT_*_EN_ADPG7_DET	When enabled, interrupt will assert when ADPG7_DET is set.	0x4*09$_h$ [6:6]
AUD_EXT_*_EN_ADPG6_DET	When enabled, interrupt will assert when ADPG6_DET is set.	0x4*09$_h$ [5:5]
AUD_EXT_*_EN_ADPG5_DET	When enabled, interrupt will assert when ADPG5_DET is set.	0x4*09$_h$ [4:4]
AUD_EXT_*_EN_ADPG4_DET	When enabled, interrupt will assert when ADPG4_DET is set.	0x4*09$_h$ [3:3]
AUD_EXT_*_EN_ADPG3_DET	When enabled, interrupt will assert when ADPG3_DET is set.	0x4*09$_h$ [2:2]
AUD_EXT_*_EN_ADPG2_DET	When enabled, interrupt will assert when ADPG2_DET is set.	0x4*09$_h$ [1:1]
AUD_EXT_*_EN_ADPG1_DET	When enabled, interrupt will assert when ADPG1_DET is set.	0x4*09$_h$ [0:0]
AUD_EXT_*_EN_MISSING_PHASE	When enabled, interrupt will assert when chosen group's phase data is missing or invalid.	0x4*0A$_h$ [10:10]

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AUD_EXT_*_EN_ACS_DET3_4B	When enabled, interrupt will assert when ACS_DET3_4B is set.	0x4*0A$_h$ [9:9]
AUD_EXT_*_EN_ACS_DET1_2B	When enabled, interrupt will assert when ACS_DET1_2B is set.	0x4*0A$_h$ [8:8]
AUD_EXT_*_EN_ACS_DET3_4A	When enabled, interrupt will assert when ACS_DET3_4A is set.	0x4*0A$_h$ [7:7]
AUD_EXT_*_EN_ACS_DET1_2A	When enabled, interrupt will assert when ACS_DET1_2A is set.	0x4*0A$_h$ [6:6]
AUD_EXT_*_EN_CTRB_DET	When enabled, interrupt will assert when CTRB_DET is set.	0x4*0A$_h$ [5:5]
AUD_EXT_*_EN_CTRA_DET	When enabled, interrupt will assert when CTRA_DET is set.	0x4*0A$_h$ [4:4]
AUD_EXT_*_EN_DBNB_ERR	When enabled, interrupt will assert when DBNB_ERR is set.	0x4*0A$_h$ [3:3]
AUD_EXT_*_EN_DBNA_ERR	When enabled, interrupt will assert when DBNA_ERR is set	0x4*0A$_h$ [2:2]
AUD_EXT_*_EN_ECCB_ERR	When enabled, interrupt will assert when ECCB_ERROR is set.	0x4*0A$_h$ [1:1]
AUD_EXT_*_EN_ECCA_ERR	When enabled, interrupt will assert when ECCA_ERROR is set.	0x4*0A$_h$ [0:0]

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3.9. ANC Data Processing

3.9.1. ANC Data Detection

The GS12270 detects ancillary data packets in the incoming SMPTE video data streams. By default, all ANC data packet types are detected on all video data streams. **ANC_DD_ANC_TYPE*_DS_*_AND_*** parameters in the **ANC_DD_ANC_TYPE*_DS_*_*_REG** registers can be used to select up to 10 specific ANC data types to be selected for detection. All types in these registers must be set to zero for all ANC data types to be extracted.

When ANC data packets are detected, indicators shall be set in the **ANC_DD_DS*_LIVE_*ANC_ANC** CSRs. There are separate indicators for HANC and VANC for each data stream. Additionally, the indicators can also be selected to be brought out on the STAT pins by selecting **DS_LIVE_*ANC_ANC_***.

The GS12270 also reports the ANC data packet word count and the ANC data packet count for all detected ANC packets in each data stream. These are available through the ANC_DD_DS*_*ANC_ANC_PKT_COUNT and ANC_DD_DS*_*ANC_ANC_COUNT CSRs.

Checksums are verified and any errors reported on the **ANC_DD_DS*_CS_ERR** CSRs.

3.9.2. ANC Data Deletion

ANC data can be deleted from any of the data streams by setting the **ANC_DATA_DELETE_DS_*_AND_*** parameter HIGH. The parameter **ANC_MARKED_DELETE_DS_*_AND_*** selects between replacing the DIDs with the SMPTE “marked for deletion” DID or replacing the packet with blanking values. By default, the GS12270 calculates the blanking values based on the incoming standard. It is possible to overwrite these values using the **BLANK_OVERWRITE_EN_DS_*_AND_*** and **DS*_BLANK_*** parameters.

Once deletion has been enabled, all ANC packets except for audio data, audio control, PID and Time Code packets will be deleted from the stream. To delete all ANC packets including audio, PID and Time Code, the **ANC_DELETE_ALL_DS_*_AND_*** parameter must be set HIGH.

It is also possible to select specific packets to be deleted by using the **ANC_DEL_ANC_TYPE*_DS_*_AND_*** parameters to specify the DID and SDID of the packets to be deleted.

3.9.3. ANC Data Extraction

The GS12270 includes a FIFO, which extracts ancillary data using read access via the host interface to ease system implementation. The FIFO stores up to 2048 x 16-bit words of ancillary data in two separate 1024 word memory banks.

The device writes the contents of ANC packets into the FIFO, starting with the first Ancillary Data Flag (ADF), followed by up to 1024 words.

All Data Identification (DID), Secondary Data Identification (SDID), Data Count (DC), user data, and checksum words are written into the device memory.

The device detects ancillary data packet DIDs placed anywhere in the video data stream, including the active picture area.

Ancillary data packets are extracted from two of 8 data streams. The user can select the streams via the **ANC_DATA_EXT_DATA_STREAM_SEL_*** registers.

Ancillary data from Data Stream A is placed in the Least Significant Word (LSW) of the FIFO, allocated to the lower 8 bits of each FIFO address.

Ancillary data from Data Stream B is placed in the Most Significant Word (MSW) (upper 8 bits) of each FIFO address.

Note: Please contact a Semtech FAE for further information about ANC insertion and extraction and an example of ancillary data extraction using the GS12270.

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3.9.3.1. Extracting Through ANC Serial Interface

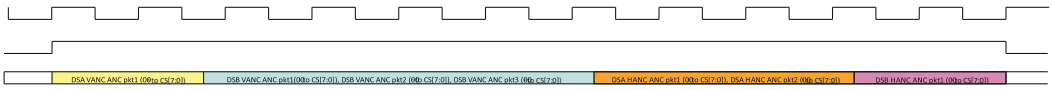

Figure 3-23: ANC Serial Interface Timing

The ANC Serial Interface can be selected by setting the **ANC_EXT_GSPI_$\overline{\text{SERIAL_IF}}$** register LOW. It can be enabled by setting the **ANC_DATA_SERIAL_IF_ENABLE** parameter HIGH. The timing of the ANC Serial Interface block is shown in Figure 3-23. It shows the order in which the block sends packets.The first packets that are sent out are the ones that were located inside the VANC part of data stream A. The packets that were stored in the VANC part of data stream B are then sent out followed by the packets that were stored respectively in the HANC part of data stream A and in the HANC part of data stream B. If no packets were embedded in the given location, the block will be sending packets that were extracted in the next location.

When the block starts the data transfer, the *ANC_SI_VALID* is set HIGH and remains HIGH for the duration of the ANC data transfer. The block starts by sending the ADF part of the ANC packet followed by the DID, SDID/DBN, DC, the UDWs and finally the CS.

Note: The frequency of ANC_SI_CLK is by default ½ of the internal PCLK, but can be further divided-down using ANC_DATA_SERIAL_CLK_DIV. PCLK frequencies are: 148.5MHz for 12G, 6G & 3G, and 74.25MHz for HD.

3.9.3.2. Extracting Through Host Interface

When the **ANC_EXT_GSPI_$\overline{\text{SERIAL_IF}}$** parameter is set to HIGH, the extracted ANC data can be read through the host interface.

3.9.4. ANC Data Insertion

Horizontal or vertical ancillary data words may be inserted on up to four different lines per video frame.

Up to 2560 data words may be inserted per frame with all Data Words — including the ANC packet ADF, DBN, DCNT, DID, SDID and CSUM words — being provided by the user via host interface configuration.

The CSUM word is re-calculated and inserted by the ANC Data Checksum Calculation and Insertion function.

Note that any value may be used for the CSUM word, provided that it is outside the protected ranges from 000_h to 003_h and from $3FC_h$ to $3FF_h$. If a CSUM value in either of these ranges is used, it will not be corrected by the device.

The GS12270 does not provide error checking or correction to the ANC data provided by user via the host interface. It is the responsibility of the user to ensure that all data provided for insertion is fully standard compliant.

Ancillary data packets are inserted into each line from one of 8 data streams. The user can select the stream for each line via the **DATA_STREAM_INS_SEL_LINE_X** registers.

If the user wants to select the 5th data stream to insert for the first line, write '100' to the **DATA_STREAM_INS_SEL_LINE_1** register.

The **ANC_INS_RAM_REG** register (9000_h - $99FF_h$) is used to program the ANC data words for ANC data insertion.

3.9.4.1. ANC Insertion Operating Modes

User selection of one of the two operating modes is provided through host interface configuration, using the **ANC_INS_MODE** register bit.

The supported operating modes are Concatenated Mode and Separate Line Operating Mode.

By default (at power-up or after system reset), the Separate Line Operating Mode is enabled.

Ancillary data packets are programmed into the **ANC_INS_RAM_REG** host register at addresses 9000_h - $99FF_h$.

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3.9.4.1.1. Separate Line Operating Mode

Separate Line Mode is selected by setting the **ANC_INS_MODE** bit in the host interface LOW. By default, at power-up, Separate Line Mode is selected.

In Separate Line Mode, it is possible to insert horizontal or vertical ancillary data on up to four lines per video frame. In this mode, the ancillary data words to be inserted are separated in four sections, one for each line, as shown in Figure 3-24.

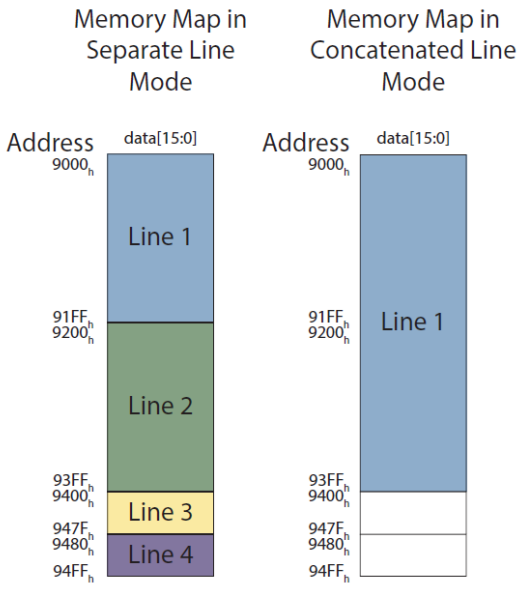

Figure 3-24: Memory Partitioning

For the lines that match **FIRST_LINE_NUMBER** or **SECOND_LINE_NUMBER**, up to 1024 8-bit words can be inserted. For the lines that match **THIRD_LINE_NUMBER** or **FOURTH_LINE_NUMBER**, up to 256 8-bit words can be inserted. The number of words to insert for each line must be specified in the ***_LINE_NUMBER_OF_WORDS** registers. HANC or VANC can be specified, independently of each other, on a per-line basis using the **ANC_TYPE_LINE_*** registers.

The lines on which ancillary data is to be inserted is programmed in the ***_LINE_NUMBER** registers.

The stream into which the ancillary data is to be inserted (DS1 - DSB) is also programmed on a per-line basis in the **DATA_STREAM_INS_SEL_LINE_*** registers.

The video line numbers on which to insert the ancillary data, the ancillary data type (HANC or VANC), and the total number of words to insert per line must be provided via the host interface. At power-up, or after system reset, all ancillary data insertion line numbers and total number of words default to zero.

If the total number of Data Words specified exceeds the amount of available HANC/VANC space on the selected line, any remaining words will not be inserted.

The data words are programmed as two 8-bit values per address. The device automatically converts the provided 8-bit Data Words into the 10-bit data, formatted according to SMPTE ST 291 prior to insertion.

3.9.4.1.2. Concatenated Operating Mode

In Concatenated Operating Mode, it is possible to insert up to 2048 8-bit horizontal or vertical ancillary Data Words on one line per video frame. This mode can be selected by setting the **ANC_INS_MODE** bit in the host interface HIGH.

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In Concatenated Operating Mode, only the **FIRST_LINE_NUMBER** registers of the host interface need to be programmed.

The video line number on which to insert the ancillary data, the ancillary data type (HANC or VANC), and the total number of words to insert must be provided via the host interface. At power-up, or after system reset, the ancillary data insertion line number and total number of words default to zero.

If the total number of data words specified exceeds 2048, only the first 2048 Data Words will be inserted, the rest will be ignored.

The data words are programmed as two 8-bit values per address, starting at host interface address 9000_h in the **ANC_INS_RAM_REG** registers.

The device automatically converts the provided 8-bit data words into the 10-bit data formatted according to SMPTE ST 291 prior to insertion.

3.10. Time Code (TC) Processing

3.10.1. Time Code Insertion

Time Codes can be inserted in one of the data streams, selected by the parameter **TC_INS_DS_SELECT**. After the initial Time Address is provided, the time address values will be automatically incremented. Drop frame counting, frame-pair counting and sub/super frame counting are supported. A single ATC packet will be inserted per field/frame, selectable as LTC, VITC or HFRTC.

Note: Please contact a Semtech FAE for further information about time code insertion and an example of how to insert time codes using GS12270.

3.10.2. Time Code Extraction

The GS12270 extracts the time code data from the video stream selected as the master channel (by default, video stream 1, but selectable using **TC_EXT_DS_SELECT** register). The time code will be in the HANC space of the Y' data channel of data stream one and conforms with SMPTE ST 12-2. The 16 time code data packets are available via the host interface.

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3.11. STAT Balls

The GS12270 has eight *STAT* balls, with two of them (*STAT[0]* and *STAT[1]*) that are assignable to user-selectable signals for reporting, the remaining (*STAT[7:2]*) are reserved. The following parameters are available for selection on *STAT[0]* and *STAT[1]* balls using the **STAT_*_SEL** parameters:

Table 3-66: STAT_SEL

Register Value	Signal Selected
0 to 3	LOCK RX0 to LOCK RX3
4 to 7	CRC_ERROR CH0 to CRC_ERROR CH3
12 to 15	PID_ERROR CH0 to PID_ERROR CH3

17:16	DATA_RATE_0 [1:0]
19:18	DATA_RATE_1 [1:0]
21:20	DATA_RATE_2 [1:0]
23:22	DATA_RATE_3 [1:0]
24	CRC_ERROR_COMB
31	AUD_EXT_1_INTERRUPT
32	AUD_EXT_2_INTERRUPT
33	AUD_INS_1_INTERRUPT
34	AUD_INS_2_INTERRUPT
35	MEMORY_WRITE_ACTIVE_BANK
36	DS1_HANC_BANK1_3QUARTER_FULL
37	DS1_VANC_BANK1_3QUARTER_FULL
38	DS1_HANC_BANK2_3QUARTER_FULL
39	DS1_VANC_BANK2_3QUARTER_FULL
40	DS2_HANC_BANK1_3QUARTER_FULL
41	DS2_VANC_BANK1_3QUARTER_FULL
42	DS2_HANC_BANK2_3QUARTER_FULL
43	DS2_VANC_BANK2_3QUARTER_FULL
44	DS1_HANC_BANK1_FILLED_UP
45	DS1_VANC_BANK1_FILLED_UP
46	DS1_HANC_BANK2_FILLED_UP
47	DS1_VANC_BANK2_FILLED_UP
48	DS2_HANC_BANK1_FILLED_UP
49	DS2_VANC_BANK1_FILLED_UP
50	DS2_HANC_BANK2_FILLED_UP
51	DS2_VANC_BANK2_FILLED_UP
52	SERIAL_CLOCK_NOT_FAST_ENOUGH
60:53	DS_LIVE_HANC_ANC [7:0]
68:61	DS_LIVE_VANC_ANC [7:0]
76:69	DS_FRAME_ANC [7:0]
77	PACKET_MISSED
78	INS_COMPLETE
79	H_LOCK
80	V_LOCK
84	FIFO_297_TO_TMDS_DISTURBANCE

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85	OB_UNDERFLOW (TX_HDMI_FLYWHEEL_HLOCK)
89:86	H_OUT [3:0]
93:90	V_OUT[3:0]
97:94	F_OUT[3:0]
101:98	H_IN[3:0]
105:102	V_IN[3:0]
109:106	F_IN[3:0]
113:110	FRAME_HD[3:0]
138	DISTURBANCE
139	TC_EXT_LTC_CAPTURED_FLAG
140	TC_EXT_VITC_CAPTURED_FLAG
141	TC_EXT_HFRTC_CAPTURED_FLAG
145	TC_INS_ATC_INS_COMPLETE
172	FPLL1_LOCK
173	FPLL2_LOCK
176	HDMI_TX_TMDS_CLK_RATIO
182	HDMI_TX_FLYWHEEL_LOCK
184	STANDBY
190	RX_TMDS_CLK_CHANGE
191	RX_TMDS_CLK_STABLE
192	RX_TMDS_LINE_STABLE
193	RX_TMDS_VIDEO_STABLE

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Additionally on the *HFV_IN* and *HVF_OUT* pins the timing signals from different spots through the device can be selected as listed in Table 3-67 and Table 3-68.

Table 3-67: SDI HVF Pre-Selection

Register Address	Parameter Name	Value [bits]	00	01	10	11
0073_h	SEL_HVF_IN_0	1:0	HVF_CH0	HVF_CH1	HVF_CH2	HVF_CH3
	SEL_HVF_IN_1	3:2	HVF_CH0_M0	HVF_CH1_M0	HVF_CH2_M0	HVF_CH3_M0
	SEL_HVF_IN_2	5:4	HVF_ANC_EXT_DS1	HVF_ANC_EXT_DS2	HVF_ANC_EXT_DS3	HVF_ANC_EXT_DS4
	SEL_HVF_IN_3	7:6	HVF_AUD_EXT_DS1	HVF_AUD_EXT_DS2	HVF_AUD_EXT_DS3	HVF_AUD_EXT_DS4
	SEL_HVF_OUT_0	9:8	HVF_ANC_INS_DS1	HVF_ANC_INS_DS2	HVF_ANC_INS_DS3	HVF_ANC_INS_DS4
	SEL_HVF_OUT_1	11:10	HVF_DEL_ADJ_M0	HVF_DEL_ADJ_M1	HVF_DEL_ADJ_DM 0	HVF_DEL_ADJ_DM 1
	SEL_HVF_OUT_2	13:12	HVF_VI0	HVF_VI1	HVF_DEMUX0	HVF_ DEMUX1

SDI input timing signals are selected as following:

- HVF_CH<n>—Timing signals from input channel SDI processing blocks for input DDI<n>
- HVF_CH<n>_M0—Timing signals after clock crossing to the common M0 clock
- HVF_ANC_EXT_DS<n> after ANC data extraction block
- HVF_AUD_EXT_DS<n> after audio extraction block SDI output timing signals are selected as following:
- HVF_ANC_INS_DS<n> after audio insertion block
- HVF_DEL_ADJ_M0/1—after delay adjustment and M0/1 block
- HVF_DEL_ADJ_DM0/1—after delay adjustment and DM0/1 block
- HVF_VI0/1—after Virtual Interface VI0/1 selection
- HVF_DEMUX0/1 after the demultiplexing blocks DEMUX0/1

In HDMI-SDI configuration mode, HVF_IN0, HVF_IN1 and HVF_IN2 will be selected from the HDMI receiver block using parameters in the Table 3-68. The HVF_IN3 signals will be pulled LOW all of the time.

Table 3-68: HDMI Rx HVF Pre-Selection

Register Address	Parameter Name	Bits	Bits Value	Signal from Block
6014	HVF0_SEL	3:0	0000	HDMI_REC
			0001	HDMI_STR_SYNC
			0010	HDMI_AUX_FILT
			0011	HDMI_V_PH_AL
			0100	HDMI_PH_CALC
			0101	TMDS_2_VID
			0110	CLKCROSS_2_PCLK
			0111	MAPP_2SI
			1000	SDI_MAPP
			1001	861_CONV
			1010	HVF_DS_1_2
			1011	HVF_DS_3_4
			1100	HVF_DS_5_6
			1101	HVF_DS_7_8
	HVF1_SEL	7:4	Same as for HVF/DE_in(0)	
	HVF2_SEL	11:8	Same as for HVF/DE_in(0)	

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3.12. Reference Clock

The GS12270 operates from a single differential reference clock. It is recommended to use a third-overtone oscillator (148.5MHz) with ±30ppm frequency tolerance.

3.13. Digital I/O

Refer to the pinout and RDK reference design.

3.14. Power Supply Considerations

3.14.1. Power Connections

Refer to the pinout and RDK reference design.

3.14.2. Power On Sequence

Refer to Microchip's PolarFire® FPGA Datasheet DS00003831.

3.14.3. Device Initialization

After the point of stable power supply levels have been achieved, the $\overline{SYS_RESET}$ ball shall be released for device to start initialization. Completion of Device Initialization will take 900ms and then the device will enter Normal Operation (the $\overline{RESET}$ ball shall be released at the same time as $\overline{SYS_RESET}$ or after, to enter Normal Operation).

This implies that after power-up the device requires a 900ms delay before GSPI transactions can begin.

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3.15. GSPI Host Interface

The GS12270 is configured via the Gennum Serial Peripheral Interface (GSPI).

The GSPI host interface is comprised of a serial data input signal (*CTRL_SDIN* ball), serial data output signal (*CTRL_SDOUT* ball), an active-LOW Chip Select (*CTRL_CSB* ball) and a burst clock (*CTRL_SCLK* ball).

The GS12270 is a slave device, so the *CTRL_SCLK*, *CTRL_SDIN* and *CTRL_CSB* signals must be sourced by the application host processor.

All read and write access to the device is initiated and terminated by the application host processor.

3.15.1. CTRL_CSB Ball

The Chip Select ball (*CTRL_CSB*) is an active-LOW signal provided by the host processor to the GS12270.

The HIGH-to-LOW transition of this ball marks the start of serial communication to the GS12270.

The LOW-to-HIGH transition of this ball marks the end of serial communication to the GS12270.

Each device may use its own separate Chip Select signal from the host processor or up to 32 devices may be connected to a single Chip Select when making use of the Unit Address feature.

Only those devices whose Unit Address matches the **DEVICE_UNIT_ADDRESS** in GSPI Command Word 1 will respond to communication from the host processor.

3.15.2. CTRL_SDIN Ball

The *CTRL_SDIN* ball is the GSPI serial data input ball of the GS12270.

The 32-bit Command and 16-bit Data Words from the host processor or from the *CTRL_SDOUT* ball of other devices are shifted into the device on the rising edge of *CTRL_SCLK* when the *CTRL_CSB* ball is LOW.

3.15.3. CTRL_SDOUT Ball

The *CTRL_SDOUT* ball is the GSPI serial data output of the GS12270.

All data transfers out of the GS12270 to the host processor or to the *CTRL_SDIN* ball of other connected devices occur from this ball.

By default (at power-up or after system reset), the *CTRL_SDOUT* ball provides a non-clocked path directly from the *CTRL_SDIN* ball, regardless of the *CTRL_CSB* ball state, except during the GSPI Data Word portion for read operations from the device. This allows multiple devices to be connected in Loop-Through configuration.

For read operations, the *CTRL_SDOUT* ball is used to output data read from an internal Configuration and Status Register (CSR) when *CTRL_CSB* is LOW. Data is shifted out of the device on the falling edge of *CTRL_SCLK*, so that it can be read by the host processor or other downstream connected device on the subsequent *CTRL_SCLK* rising edge.

Note that the CTRL_SDOUT pin can be set to tri-state by setting the *CTRL_SPI_EN* pin to low:

- *CTRL_SPI_EN* = 0: *CTRL_SDOUT* is tri-state
- *CTRL_SPI_EN* = 1: *CTRL_SDOUT* is output

3.15.3.1. GSPI Link Disable Operation

It is possible to disable the direct *CTRL_SDIN* to *CTRL_SDOUT* (Loop-Through) connection by writing a value of 1 to the **GSPI_LINK_DISABLE** bit in **HOST_CONFIG**. When disabled, any data appearing at the *CTRL_SDIN* ball will not appear at the *CTRL_SDOUT* ball and the *CTRL_SDOUT* ball is HIGH.

Note: Disabling the Loop-Through operation is temporarily required when initializing the Unit Address for up to 32 connected devices.

The time required to enable/disable the Loop-Through operation from assertion of the register bit is less than the GSPI configuration command delay as defined by the parameter $t_{cmd_GSPI_config}$ (4 SCLK cycles).

Table 3-69: GSPI_LINK_DISABLE Bit Operation

Bit State	Description
0	*CTRL_SDIN* ball is looped through to the *CTRL_SDOUT* ball
1	Data appearing at *CTRL_SDIN* does not appear at *CTRL_SDOUT*, and *CTRL_SDOUT* ball is HIGH.

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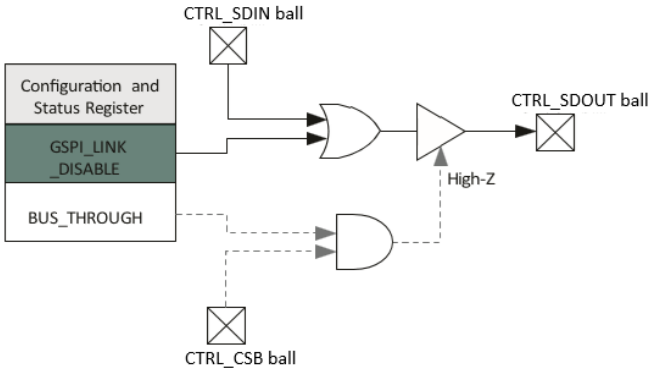

Figure 3-25: GSPI_LINK_DISABLE Operation

3.15.3.2. GSPI Bus-Through Operation

Using GSPI Bus-Through operation, the GS12270 can share a common PCB trace with other GSPI devices for *CTRL_SDOUT* output.

When configured for Bus-Through operation, by setting **GSPI_BUS_THROUGH_ENABLE** bit to 1, the *CTRL_SDOUT* ball will be high-impedance when the *CTRL_CSB* ball is HIGH.

When the *CTRL_CSB* ball is LOW, the *CTRL_SDOUT* ball will be driven and will follow regular read and write operation as described in Section 3.15.3.

Multiple chains of GS12270 devices can share a single *CTRL_SDOUT* bus connection to host by configuring the devices for Bus-Through operation. In such configuration, each chain requires a separate Chip Select (*CTRL_CSB*).

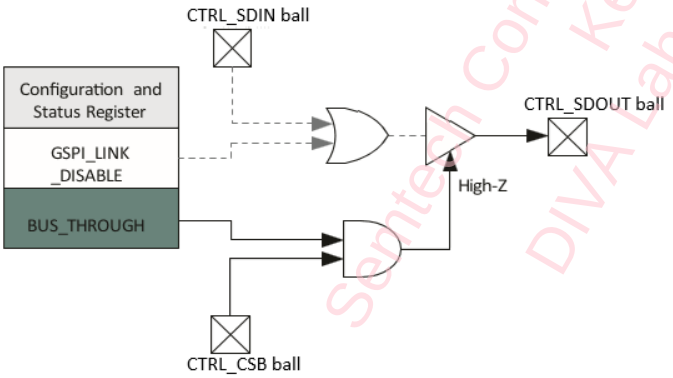

Figure 3-26: GSPI_BUS_THROUGH_ENABLE Operation

3.15.4. CTRL_SCLK Ball

The *CTRL_SCLK* ball is the GSPI serial data shift clock input to the device, and must be provided by the host processor.

Serial data is clocked into the GS12270 *CTRL_SDIN* ball on the rising edge of *CTRL_SCLK*. Serial data is clocked out of the device from the *CTRL_SDOUT* ball on the falling edge of *CTRL_SCLK* (read operation). *CTRL_SCLK* is ignored when *CTRL_CSB* is HIGH.

The maximum interface clock rate is 20MHz.

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3.15.5. Command Word 1 Description

All GSPI accesses are a minimum of 48 bits in length (two 16-bit Command Words followed by a 16-bit Data Word) and the start of each access is indicated by the HIGH-to-LOW transition of the chip select (*CTRL_CSB*) ball of the GS12270.

The format of the Command Words and Data Word are shown in Figure 3-27.

Data received immediately following this HIGH-to-LOW transition will be interpreted as a new Command Word.

3.15.5.1. R/$\overline{W}$ bit – B15 Command Word 1

This bit indicates a read or write operation.

When R/$\overline{W}$ is set to 1, a read operation is indicated, and data is read from the register specified by the ADDRESS field of the Command Word.

When R/$\overline{W}$ is set to 0, a write operation is indicated, and data is written to the register specified by the ADDRESS field of the Command Word.

3.15.5.2. B'CAST ALL—B14 Command Word 1

This bit is used in write operations to configure all devices connected in Loop-Through and Bus-Through configuration with a single command.

When **B'CAST ALL** is set to 1, the following Data Word is written to the register specified by the ADDRESS field of the Command Words, regardless of the setting of the UNIT ADDRESS(es).

When **B'CAST ALL** is set to 0, a normal write operation is indicated. Only those devices that have a Unit Address matching the UNIT ADDRESS field of Command Word 1 write the Data Word to the register specified by the ADDRESS field of the Command Words.

3.15.5.3. EMEM—B13 Command Word 1

The **EMEM** bit must be set to 1 in Command Word 1. When **EMEM** is set to 1, a 23-bit address split between Command Word 1 and Command Word 2 is used to access the registers in this device.

3.15.5.4. AUTOINC—B12 Command Word 1

When the **AUTOINC** bit is set LOW, the GSPI operates in single read/write access mode. When the **AUTOINC** bit is set HIGH, the GSPI operates in burst read/write access mode.

3.15.5.5. UNIT ADDRESS—B11:B7 Command Word 1

The 5 bits of the UNIT ADDRESS field of the Command Word are used to select one of 32 devices connected on a single chip select in Loop-Through or Bus-Through configurations.

Read and write accesses are only accepted if the UNIT ADDRESS field matches the programmed **DEVICE_UNIT_ADDRESS** in **HOST_CONFIG**.

By default (at power-up or after a device reset), the **DEVICE_UNIT_ADDRESS** is set to 00_h.

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3.15.5.6. ADDRESS—B6:B0 Command Word 1 and B15:B0 Command Word 2

The Command and Data Word formats are shown in Figure 3-27 and Figure 3-28 below.

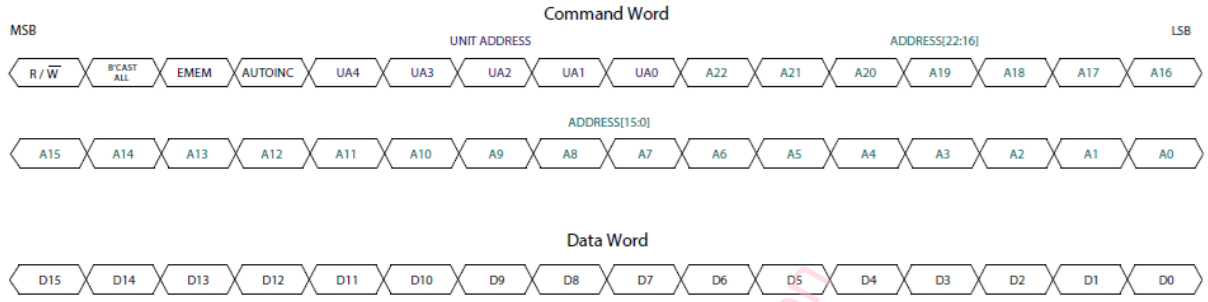

Figure 3-27: Command and Data Word Format

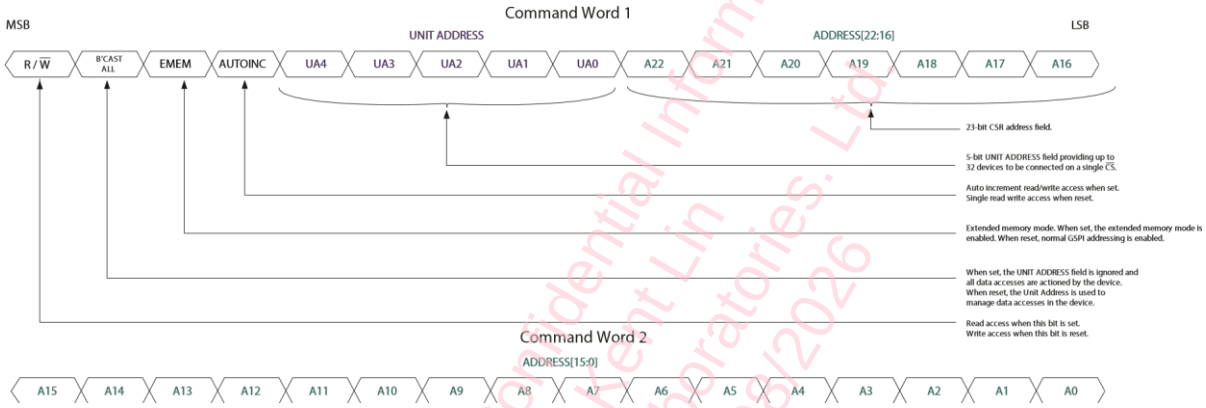

Figure 3-28: Command Word 1 and Command Word 2 Details

3.15.6. GSPI Transaction Timing

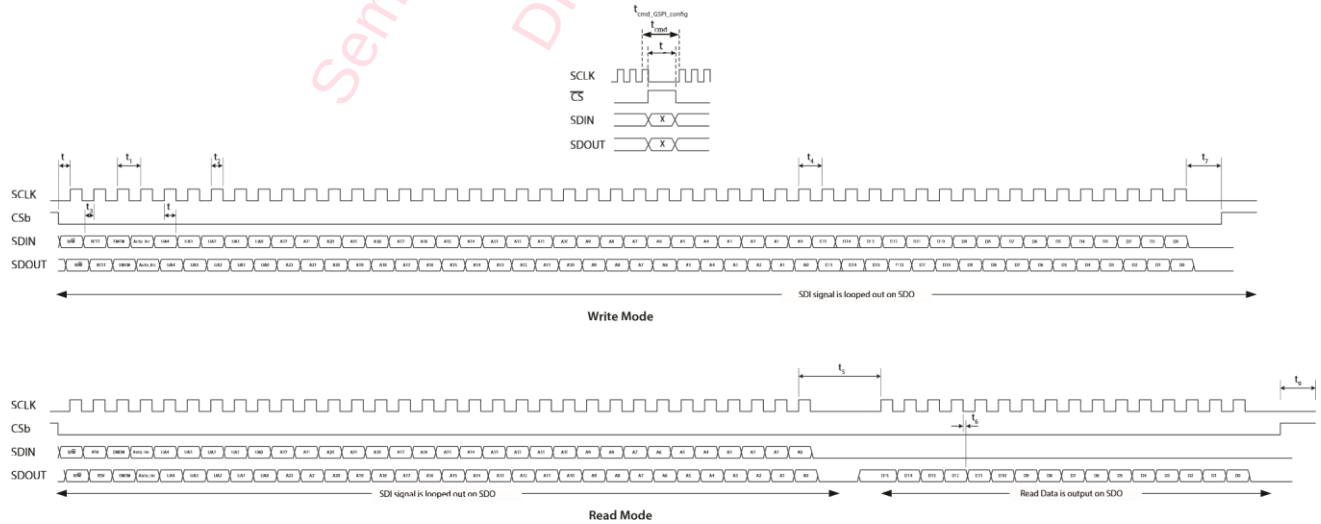

Figure 3-29: GSPI External Interface Timing

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Table 3-70: GSPI Timing Parameters

Parameter	Symbol	Equivalent CTRL_SCLK Cycles	Min	Typ	Max	Units
CTRL_CSB LOW Before CTRL_SCLK Rising Edge	t_0	—	3.2	—	—	ns
CTRL_SCLK Frequency		—	—	—	20	MHz
CTRL_SCLK Period	t_1	—	50	—	—	ns
CTRL_SCLK Duty Cycle	t_2	—	40	50	60	%
Input Data Setup Time	t_3	—	2	—	—	ns
CTRL_SCLK Idle Time – Write	t_4	1	50	—	—	ns
CTRL_SCLK Idle Time – Read	t_5	4	164	—	—	ns
Inter–Command Delay Time	t_{cmd}	3	120	—	—	ns
Inter–Command Delay Time (after GSPI configuration write)	$t_{cmd_GSPI_conf}$ [2]	4	164	—	—	ns
CTRL_SDOUT After CTRL_SCLK Falling Edge	t_6	—	2	—	8	ns
CTRL_CSB HIGH After Final CTRL_SCLK Falling Edge	t_7	—	0	—	—	ns
Input Data Hold Time	t_8	—	1	—	—	ns
CTRL_CSB HIGH Time	t_9	—	75	—	—	ns
CTRL_SDIN to CTRL_SDOUT Combinatorial Delay	—	—	—	—	7.5	ns
Max chips daisy-chained at max CTRL_SCLK frequency (20 MHz)	When host clocks in CTRL_SDOUT data on rising edge of CTRL_SCLK		—	—	1	# of compatible Semtech devices
Max frequency for 16 daisy-chained devices			—	—	2	MHz
Max chips daisy-chained at max CTRL_SCLK frequency (20 MHz)	When host clocks in CTRL_SDOUT data on falling edge of CTRL_SCLK		—	—	4	# of compatible Semtech devices
Max frequency for 16 daisy-chained devices			—	—	2	MHz

Note:

1. Parameter is exactly multiple of CTRL_SCLK periods and scales proportionally.
2. $t_{cmd_GSPI_conf}$ inter-command delay must be used whenever modifying HOST_CONFIG register at address 0x00.

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3.15.7. Single Read/Write Access

Single read/write access timing for the GSPI interface is shown in Figure 3-30 to Figure 3-34.

When performing a single read or write access, one Data Word is read from/written to the device per access. Each access is a minimum of 48-bits long, consisting of two Command Words and a single Data Word. The read or write cycle begins with a HIGH-to-LOW transition of the *CTRL_CSB* ball. The read or write access is terminated by a LOW-to-HIGH transition of the *CTRL_CSB* ball.

The maximum interface clock rate is 20MHz and the inter-command delay time indicated in the figures as t_{cmd}, is a minimum of 3 SCLK clock cycles. After modifying values in **HOST_CONFIG**, the inter-command delay time, $t_{cmd_GSPI_config}$, is a minimum of 4 CTRL_SCLK clock cycles.

For read access, the time from the last bit of Command Word 2 to the start of the data output, as defined by t_5, corresponds to no less than 4 CTRL_SCLK clock cycles at 20MHz.

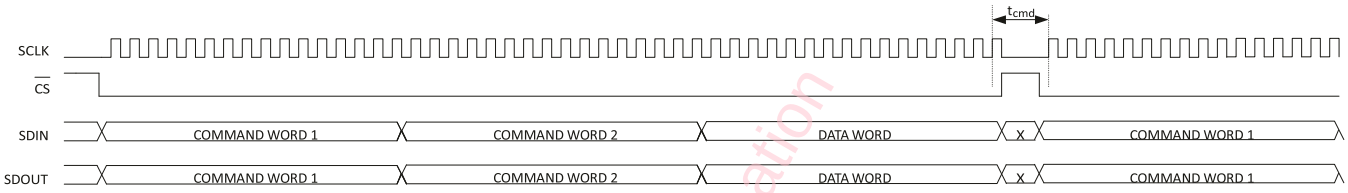

Figure 3-30: GSPI Write Timing—Single Write Access with Loop-Through Operation (default)

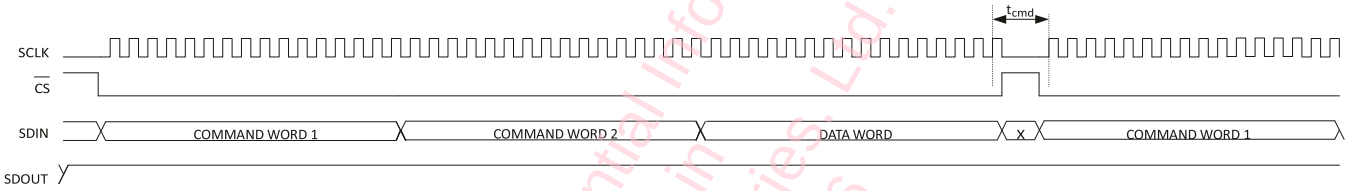

Figure 3-31: GSPI Write Timing—Single Write Access with GSPI Link-Disable Operation

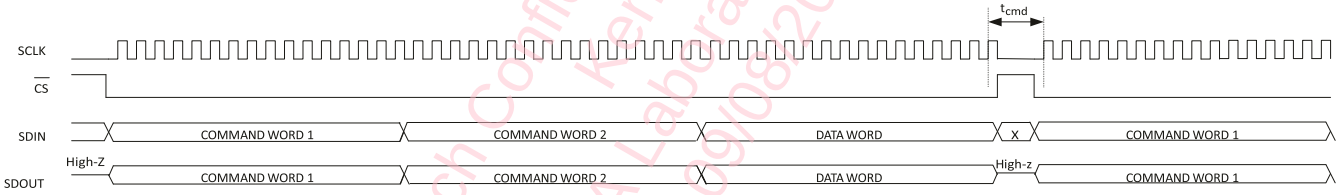

Figure 3-32: GSPI Write Timing—Single Write Access with Bus-Through Operation

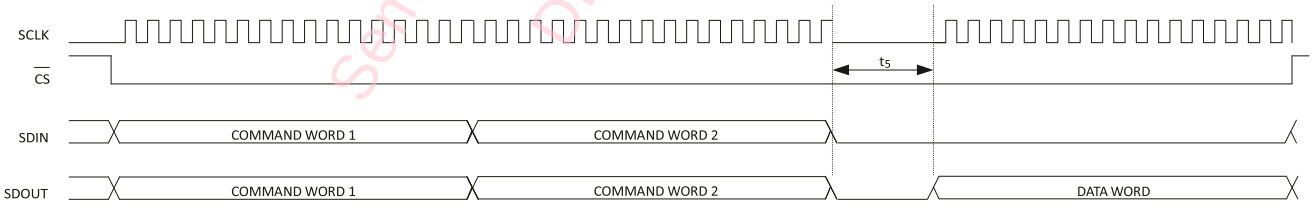

Figure 3-33: GSPI Read Timing—Single Read Access with Loop-Through Operation (default)

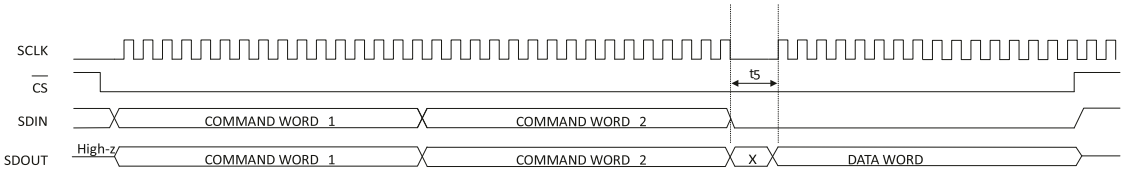

Figure 3-34: GSPI Read Timing—Single Read Access with Bus-Through Operation

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3.15.8. Auto-increment Read/Write Access

Content to be added.

3.15.9. Setting a Device Unit Address

Multiple (up to 32) GS12270 devices can be connected to a common Chip Select (*CTRL_CSB*) in Loop-Through or Bus-Through operation.

To ensure that each device selected by a common *CTRL_CSB* can be separately addressed, a unique Unit Address must be programmed by the host processor at start-up as part of system initialization or following a device reset.

Note: By default (at power up or after a device reset), the **DEVICE_UNIT_ADDRESS** of each device is set to 0_h and the *CTRL_SDIN→CTRL_SDOUT* non-clocked loop-through for each device is enabled.

These are the steps required to set the **DEVICE_UNIT_ADDRESS** of devices in a chain to values other than 0:

1. Write to Unit Address 0 selecting **HOST_CONFIG** (ADDRESS = 0), with the **GSPI_LINK_DISABLE** bit set to 1 and the **DEVICE_UNIT_ADDRESS** field set to 0. This disables the direct *CTRL_SDIN→CTRL_SDOUT* non-clocked path for all devices on chip select.

2. Write to Unit Address 0 selecting **HOST_CONFIG** (ADDRESS = 0), with the **GSPI_LINK_DISABLE** bit set to 0 and the **DEVICE_UNIT_ADDRESS** field set to a unique Unit Address. This configures **DEVICE_UNIT_ADDRESS** for the first device in the chain. Each subsequent such write to Unit Address 0 will configure the next device in the chain. If there are 32 devices in a chain, the last (32nd) device in the chain must use **DEVICE_UNIT_ADDRESS** value 0.

3. Repeat step 2 using new, unique values for the **DEVICE_UNIT_ADDRESS** field in **HOST_CONFIG** until all devices in the chain have been configured with their own unique Unit Address value.

Note: $t_{cmd_GSPI_conf}$ delay must be observed after every write that modifies **HOST_CONFIG**.

All connected devices receive this command (by default, the Unit Address of all devices is 0), and the Loop-Through operation will be re-established for all connected devices.

Once configured, each device will only respond to Command Words with a UNIT ADDRESS field matching the **DEVICE_UNIT_ADDRESS** in **HOST_CONFIG**.

Note: Although the Loop-Through and Bus-Through configurations are compatible with previous generation GSPI enabled devices (backward compatibility), only devices supporting Unit Addressing can share a chip select. All devices on any single chip select must be connected in a contiguous chain with only the last device's *CTRL_SDOUT* connected to the application host processor. Multiple chains configured in Bus-Through Mode can have their final *CTRL_SDOUT* outputs connected to a single application host processor input.

3.15.10. Default GSPI Operation

By default (at power-up or after a device reset), the GS12270 is set for Loop-Through Operation and the internal **DEVICE_UNIT_ADDRESS** field of the device is set to 0.

Figure 3-35 shows a functional block diagram of the Configuration and Status Register (CSR) map in the GS12270.

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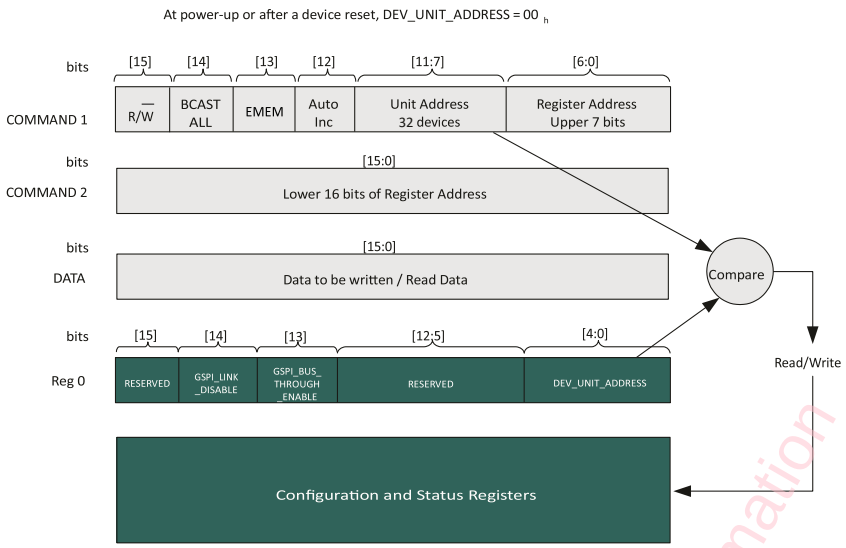

Figure 3-35: Internal Register Map Functional Block Diagram

The steps required for the application host processor to write to the Configuration and Status Registers via the GSPI, are as follows:

1. Set Command Word 1 for write access (R/$\overline{W}$ = 0); set Auto Increment to 0; set EMEM to 1. The Unit Address field in the Command Word 1 to match the configured **DEVICE_UNIT_ADDRESS** which will be zero after power-up. Set the Register Address bits in Command Word 1 to match the upper 7 bits of the register address to be accessed. Set the bits in Command Word 2 to match the lower 16 bits of the register address to be accessed. Write Command Word 1 and Command Word 2.

2. Write the Data Word to be written to the register.

Read access is the same as the above with the exception of step 1, where the Command Word 1 is set for read access (R/$\overline{W}$ = 1).

Note: The UNIT ADDRESS field of Command Word 1 must always match **DEVICE_UNIT_ADDRESS** for an access to be accepted by the device. Changing **DEVICE_UNIT_ADDRESS** to a value other than 0 is only required if multiple devices are connected to a single chip select (in Loop-Through or Bus-Through configuration).

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4. Host Interface Register Map

4.1. Control Registers

Table 4-1: Address Offset

Table	Address Offset Value$_h$
GS12270 Control and Status Registers Table 4-6	0
Rx Control and Status Registers Table 4-7	1000
Tx Control and Status Registers Table 4-8	2000
Pattern Generator and Control Registers Table 4-9	3000
SDI Audio De-Embedding Control Registers Table 4-10	4000
SDI Audio Embedding Control Registers Table 4-11	5000
HDMI Rx Control Registers Table 4-12	6000
HDMI Tx Control Registers Table 4-13	7000
ANC Insertion Control Registers Table 4-14	8000
ANC Insertion Memory Control Registers Table 4-15	9000
ANC Extraction Control Registers Table 4-16	A000
ANC Extraction Memory Control Registers Table 4-17	B000

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4.1.1. Audio Register Offset

SDI Audio Embedding and De-Embedding are handled by two identical Audio blocks to allow up to 16 channels of Audio Embedding and De-Embedding. Each data 'lane' has an identical block of registers which is offset by 2048 (800$_h$). The table shows the GS12270 block names and their associated block offsets.

Table 4-2: Audio Core Address Offset

Name	Address Offset Value$_h$
SDI Audio Extraction Core 1	4000
SDI Audio Extraction Core 2	4800
SDI Audio Insertion Core 1	5000
SDI Audio Insertion Core 2	5800

All lane registers are labelled as: *, where * is a value that is either 0 or 8 for Register Names and 1 or 2 for Parameter Names, respectively.

For example: to program **HD_STATUS_1** on lane 2, write to register:

$800_h + 5000_h = 5800_h$

$2048_d + 20480_d = 22528_d$

Table 4-3: Control Registers

Function	GSPI Address$_h$	Register Name
GSPI	0	HOST_CONFIG
Operating Mode Control	1	OPERATING_ MODE_SEL_ REG
	2	SD_BYPASS_ SEL_REG
	13	SYNC_W_ DISABLE
	19	VID_STREAM_ INTERLEAVE
	1C	DISABLE_CRC_ INS
	6A	TX_ EXTERNAL_REF_ CLK_SEL
	6D	TIM_ OUTPUT_ ENABLE
	6E, 6F, 70, 71	STAT_SEL_A, STAT_SEL_B, STAT_SEL_C, STAT_SEL_D

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	72	STAT_OUTPUT_ ENABLE
	78, 79	RESET_0, RESET_1
Input Control	3	INPUT_LOCK_ REG
	5	ISP_REG
	6	MANUAL_ RATE
	9	DDI_PWR_ DOWN
Status	7	DATA_RATE_ REPORT
	1B	CRC_ERROR
	1D to 3C	PID_DET_CH0A_ DS1_BYTE_1_2 to PID_DET_CH3B_ DS2_BYTE_3_4
	42	PID_ERROR
	43	PID_DETECTED
Output Control	A	DDO_IDLE
	3D	OVERRIDE_ STREAM_ NUMBER
	3E, 3F	LINK_N_ TO_INSERT_ STR_0_7, LINK_N_ TO_INSERT_ STR_8_15
	69	TX_REF_CLK_ SEL
Output Channel Assignment	B	REG_CTRL_OUTPUT_ASGMT_EN
	C	CHAN_ASGMT_ DDO<n>
Demultiplex Configuration	E, F	SEL_DM0_VIRT, SEL_DM1_VIRT
	11	DEMUX_IN_SEL
	73	DM0_DELAY_EN
	74, 75, 76, 77	DM0_DELAY_LINK1, DM0_ DELAY_LINK2, DM0_ DELAY_LINK3, DM0_ DELAY_LINK4
PID Insertion	40	PID_PROGRAM_ CTRL

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	41	PID_PROGRAM_ STREAM_MASK
	44 to 63	PID_INS_CH0A_ DS1_BYTE_1_2 to PID_INS_CH3B_ DS2_BYTE_3_4
Multiplex Configuration	64	VI_ASGMT_0
	66	LOST_INPUT_ IGNORE_CTRL
Reserved	4, 8, D, 10, 12, 14, 15, 16, 17, 18, 1A, 65, 67, 68, 6A, 6B, 6C, 7A to 8B	RSVD

Table 4-4: Rx Control Registers

Function	GSPI Address$_h$	Register Name
Rx Control	101B	DDI_CDR_LBW
	1023, 1024, 1025, 1026	DDI0_EQ_UPDT, DDI1_EQ_UPDT, DDI2_EQ_UPDT, DDI3_EQ_UPDT
RSVD	1000 to 101A, 101C to 1022, 1027 to 10F9	RSVD

Table 4-5: Tx Control Registers

Function	GSPI Address$_h$	Register Name
Tx Control	2014	DDO_DRV_AMP
	201A	DDO_LBW
	201B	DDO_LBW_UPDT
	201C	DDO_DRV_UPDT
	2037	OUTPUT_ PWR_DOWN
	2038	DDO_DRIVER_ DISABLE

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Reserved	2000 to 2013, 2015 to 2019, 201D to 2036, 2039 to 20C7	RSVD

4.2. Register Descriptions

The convention for R/W descriptions is as follows:

RO = Read Only

RW = Read or Write

ROCW = Read Only Clear-on-Write (CSR bit is set when the input from the hardware is asserted. It is cleared when the host writes a "1" to that bit)

ROSW = Read Only Set-on-Write (CSR bit is set when the host writes a "1" to that bit)

RWPT = Read/Write Pass Through (Host reads/writes are routed to a "pass-through" bus. Registers are implemented outside of the CSR)

4.2.1. GS12270 Control and Status Registers

Table 4-6: Control Registers

1. Can be used only in SDI-SDI mode.
2. Can be used in SDI-SDI and SDI-HDMI modes.
3. Can be used in SDI-SDI and HDMI-SDI modes.

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
0000	HOST_CONFIG	RSVD	15:15	RW	0	Reserved. Do not change.
		GSPI_LINK_DISABLE	14:14	RW	0	GSPI loop-through disable.
		GSPI_BUS_ THROUGH_ENABLE	13:13	RW	0	Enables bus-through operation.
		RSVD	12:5	RW	0	Reserved. Do not change.
		DEVICE_UNIT_ ADDRESS	4:0	RW	0	Sets the unit address for the device.
0001 [1]	OPERATING_ MODE_SEL_ REG	SEC_LINK_EN_ REG_SEL	15:15	RW	0	If set to HIGH the SEC_LINK_EN_REG value is used instead of the SEC_LINK_EN pin.
		SEC_LINK_EN_REG	14:14	RW	0	Overrides SEC_LINK_EN pin if SEC_LINK_EN_REG_SEL set HIGH.
		PG_REF_INT_EXTB	13:13	RW	0	If set to HIGH the reference for pg is generated from the external clock reference, if set to LOW reference and all time in is derived from the video stream connected to input 0.
		SEL_PG	12:12	RW	0	Enables pattern generator. 1 = PG enabled. 0 = PG disabled.
		RSVD	11:9	RW	0	Reserved. Do not change.

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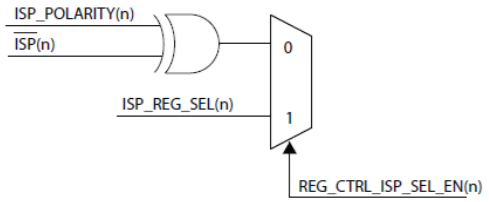
DIV Laboratories. Ltd.
Kent Lin
09/08/2026

		REG_CTRL_ MODE_SEL_EN	8:8	RW	0	Overrides MODE_SEL pins with values in the MODE_SEL register.
		MODE_SEL	7:5	RW	7	Selects operating mode, if REG_CTRL_MODE_SEL is set HIGH. 111 = QL 3Gb/s to SL 12Gb/s 110 = QL 1.5Gb/s to SL 6Gb/s 101 = QL 6Gb/s to DL 12Gb/s 100 = QL 3Gb/s to DL 6Gb/s 011 = DL 6Gb/s to SL 12Gb/s 010 = DL 3Gb/s to SL 6Gb/s 001 = DL 1.5Gb/s to SL 3Gb/s 000 = RSVD
		REG_CTRL_OP_ MODE_EN	4:4	RW	0	When HIGH, MUX_DEMUX_REG, PID_MODE_REG and BYPASS_REG will set operating mode instead of the associated pins.
		PID_MODE_REG	3:2	RW	0	Enabled by REG_CTRL_OP_MODE_EN. 00 = Automatic PID insertion 11 = No PID insertion
		BYPASS_REG	1:1	RW	0	When HIGH, sets the part in the BYPASS. Enabled by REG_CTRL_OP_MODE_EN.
		MUX_DEMUX_REG	0:0	RW	0	When HIGH, sets MUX operation mode. When LOW, sets DeMUX operation mode. Enabled by REG_CTRL_OP_MODE_EN.
0002 [1]	SD_BYPASS_ SEL_REG	RSVD	15:10	RO	0	Reserved.
		SD_BYPASS_ RATE_6G_3Gb	9:9	RW	0	When HIGH, oversampling rate in SD_BYPASS mode is set to 6G data rate. When LOW, it is set to 3G data rate.
		REG_CTRL_ SD_BYPASS	8:8	RW	0	When HIGH, SD_BYPASS control from registers.
		SD_BYPASS_PIN	7:4	RO	0	SD_BYPASS pin status.
		SD_BYPASS_SEL	3:0	RW	0	Only active when REG_CTRL_SD_BYPASS is set HIGH. One bit per input.
0003 [2]	INPUT_LOCK_ REG	RSVD	15:12	RO	0	Reserved.
		REG_CTRL_ INPUT_LOCK	11:8	RW	0	When HIGH, control of lock signal is taken from INPUT_LOCK_REG.
		INPUT_LOCK_REG	7:4	RW	0	Overrides video lock signal if REG_CTRL_ INPUT_LOCK register is set HIGH. One bit per input.
		INPUT_LOCK	3:0	RO	0	Indicates video lock of the input 0 to 3. One bit per input.
0004	RSVD	RSVD	15:0	RW	0	Reserved. Do not change.
0005 [2]	ISP_REG	ISP_POLARITY	15:12	RW	0	When HIGH inverts ISP polarity. One bit per input. 
		ISP_REG_SEL	11:8	RW	0	When HIGH, overrides ISP pin with the value from the ISP_REG_SEL parameter.

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DIVA Laboratories, Ltd.
Kent Lin
09/08/2026

					One bit per input.
		ISP_REG	7:4	RW	0	Sets value of *ISP_N* signal, if REG_CTRL_ISP_SEL_EN is set HIGH. One bit per input.
		ISP_PIN	3:0	RW	0	Reports signal level (HIGH or LOW) applied to the *ISP_N* pin. One bit per input.
0006 [2]	MANUAL_ RATE	RSVD	15:15	RO	0	Reserved.
		SDI_AUTO_MODE_ FORCE_DLHD_3G	14:14	RW	0	Selects DLHD→3G instead of QLHD→6G when input data rate is HD.
		SDI_AUTO_MODE_ OUT_INTERF	13:13	RW	0	Selects the output interface when in SDI_AUTO_MODE 0 = QL output when DEMUX (6G&12G in); SL output when MUX 1 = DL output when DEMUX (6G&12G in); DL output when MUX
		SDI_AUTO_ MODE_EN	12:12	RW	0	Selects the auto rate/mode detection for SDI-SDI configuration.
		MANUAL_RATE_RX3	11:10	RW	0	Manual rate control of Rx3. 00 = HD 01 = 3G 10 = 6G 11 = 12G Only active when REG_CTRL_MANUAL_RATE[3] is set HIGH.
		MANUAL_RATE_RX2	9:8	RW	0	Manual rate control of Rx2. See MANUAL_RATE_RX3 for selection values.
		MANUAL_RATE_RX1	7:6	RW	0	Manual rate control of Rx1. See MANUAL_RATE_RX3 for selection values.
		MANUAL_RATE_RX0	5:4	RW	0	Manual rate control of Rx0. See MANUAL_RATE_RX3 for selection values.
		REG_CTRL_ MANUAL_RATE	3:0	RW	0	Manual rate control override. One bit per input.
0007 [2]	DATA_RATE_ REPORT	AUTO_MODE_DET	15:12	RO	0	Detected operational mode when in the auto mode
		INTERLEAVED_ INPUT_DET	11:8	RO	0	Interleaved stream detected at input (n)
		DATA_RATE_RX3	7:6	RO	3	Indicates data rate of Rx3. 11 = 12G 10 = 6G 01 = 3G 00 = HD **Note:** If the input is not locked, the value reported by this parameter is not valid. If the device is in the DeMUX or MUX mode, the value reported is always the same as the input data rate given by the selected gearbox mode.
		DATA_RATE_RX2	5:4	RO	3	Indicates data rate of Rx2. See DATA_RATE_RX3 for selection values.
		DATA_RATE_RX1	3:2	RO	3	Indicates data rate of Rx1. See DATA_RATE_RX3 for selection values.
		DATA_RATE_RX0	1:0	RO	3	Indicates data rate of Rx0.

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DIVA Laboratories, Ltd.
Kent Lin
09/08/2026

						See DATA_RATE_RX3 for selection values.
0008	RSVD	RSVD	15:0	RW	0	Reserved. Do not change.
0009	DDI_PWR_DOWN	RSVD	15:12	RO	0	Reserved.
		DDI_PWR_DOWN_REG_SEL	11:8	RW	0	Selects the reg settings for power down for corresponding receiver One bit per input.
		DDI3_PWR_DOWN_REG	7:7	RW	0	Power-down for DDI3, if DDI_PWR_DOWN_REG_SEL is set HIGH.
		RSVD	6:6	RW	0	Reserved. Do not change.
		DDI2_PWR_DOWN_REG	5:5	RW	0	Power-down for DDI2, if DDI_PWR_DOWN_REG_SEL is set HIGH.
		RSVD	4:4	RW	0	Reserved. Do not change.
		DDI1_PWR_DOWN_REG	3:3	RW	0	Power-down for DDI1, if DDI_PWR_DOWN_REG_SEL is set HIGH.
		RSVD	2:2	RW	0	Reserved. Do not change.
		DDI0_PWR_DOWN_REG	1:1	RW	0	Power-down for DDI0, if DDI_PWR_DOWN_REG_SEL is set HIGH.
		RSVD	0:0	RW	0	Reserved. Do not change.
000A	DDO_IDLE	RSVD	15:12	RO	0	Reserved.
		DDO_IDLE_OW_EN	11:8	RW	0	Manual transmitter idle override enable. 0 = DDO idle controlled by the GS12270 operation mode 1 = DDO Idle controlled by the DDO[3:0]_IDLE_REG setting One bit per output.
		DDI3_IDLE_REG	7:6	RW	0	Idle for DDO3, if DDO_IDLE_OW_EN is set HIGH.
		DDO2_IDLE_REG	5:4	RW	0	Idle for DDO2, if DDO_IDLE_OW_EN is set HIGH.
		DDO1_IDLE_REG	3:2	RW	0	Idle for DDO1, if DDO_IDLE_OW_EN is set HIGH.
		DDO0_IDLE_REG	1:0	RW	0	Idle for DDO0, if DDO_IDLE_OW_EN is set HIGH.
000B	REG_CTRL_OUTPUT_ASGMT_EN	RSVD	15:4	RO	0	Reserved.
		REG_CTRL_OUTPUT_ASGMT_EN	3:0	RW	0	When the corresponding bit <n> is asserted, the assignment of the DDO<n>serial output is controlled by the settings of the OUTPUT_ASGMT_DDO<n> parameter: DDO0 = Bit 0 DDO1 = Bit 1 DDO2 = Bit 2 DDO3 = Bit 3
000C [1]	CHAN_ASGMT_DDO<n>	RSVD	15:15	RO	0	Reserved.
		OUTPUT_ASGMT_DDO3	14:12	RW	2	Selects the source of the DDO3 output if REG_CTRL_OUTPUT_ASGMT_EN is set HIGH. 000 = M0 Processed Output 001 = M1 Processed Output 010 = DM0 Processed Output 011 = DM1 Processed Output 100 = DDI0 101 = DDI1 110 = DDI2 111 = DDI3

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Kent Lin
DIVA Laboratories, Ltd.
07/08/2026

		RSVD	11:11	RO	0	Reserved.
		OUTPUT_ ASGMT_DDO2	10:8	RW	2	Selects the source of the DDO2 output if REG_CTRL_OUTPUT_ASGMT_EN is set HIGH. See OUTPUT_ASGMT_DDO3 for selection values.
		RSVD	7:7	RO	0	Reserved.
		OUTPUT_ ASGMT_DDO1	6:4	RW	2	Selects the source of the DDO1 output if REG_CTRL_OUTPUT_ASGMT_EN is set HIGH. See OUTPUT_ASGMT_DDO3 for selection values.
		RSVD	3:3	RO	0	Reserved.
		OUTPUT_ ASGMT_DDO0	2:0	RW	2	Selects the source of the DDO0 output if REG_CTRL_OUTPUT_ASGMT_EN is set HIGH. See OUTPUT_ASGMT_DDO3 for selection values.
000D	RSVD	RSVD	15:0	RW	0	Reserved. Do not change.
000E [3]	SEL_DM0_VIRT	RSVD	15:14	RO	0	Reserved.
		REG_CTRL_DM0_ LINES_2_4B	13:13	RW	0	If set to HIGH, DM0_LINES_2_4B_REG selects between 1to2 and 1to4 demuxing in DM0 virtual interface.
		DM0_LINES_ 2_4B_REG	12:12	RW	0	Selects between 1to2 and 1to4 demuxing in DM0 virtual interface when REG_CTRL_DM0_LINES_2_4B set HIGH.
		SEL_DM0_VIRT3	11:10	RW	0	Manual assignment of the data stream on the Tx3, if REG_CTRL_SEL_DM0_VIRT[3] is set HIGH. 00 = Data stream 8/7 01 = Data stream 6/5 10 = Data stream 4/3 00 = Data stream 2/1
		SEL_DM0_VIRT2	9:8	RW	1	Manual assignment of the data stream on the Tx2, if REG_CTRL_SEL_DM0_VIRT[2] is set HIGH. See SEL_DM0_VIRT3 for selection values.
		SEL_DM0_VIRT1	7:6	RW	2	Manual assignment of the data stream on the Tx1, if REG_CTRL_SEL_DM0_VIRT[1] is set HIGH. See SEL_DM0_VIRT3 for selection values.
		SEL_DM0_VIRT0	5:4	RW	3	Manual assignment of the data stream on the Tx0, if REG_CTRL_SEL_DM0_VIRT[0] is set HIGH. See SEL_DM0_VIRT3 for selection values.
		REG_CTRL_ SEL_DM0_VIRT	3:0	RW	0	When HIGH, the control of the DM0 virtual interface output is from register SEL_DM0_VIRT[3:0]. One bit per output channel.
000F [1]	SEL_DM1_VIRT	RSVD	15:5	RO	0	Reserved.
		REG_CTRL_SEL_ DM1_VIRT	4:4	RW	0	When HIGH, enables SEL_DM1_VIRT control.
		SEL_DM1_VIRT	3:0	RW	5	When HIGH, swaps data stream on DM1. One bit per output channel.
0010	RSVD	RSVD	15:0	RW	0	Reserved. Do not change.
0011 [2]	SDI_IN_SEL	RSVD	15:5	RO	0	Reserved.
		UNUSED_0_2_ IN_RESET_EN	4:4	RW	0	if set HIGH input channel which is not selected is reset (doesn't apply on SDI auto modes).
		RSVD	3:2	RO	0	Reserved.

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DIVA Laboratories. Ltd.
Kent Lin
09/08/2026

		REG_CTRL_ SDI_IN_SEL	1:1	RW	0	When HIGH, enables selection of the active input, when input is single or dual link case, through the register DEMUX_IN_0_2_SEL.
		SDI_IN_0_2_SEL	0:0	RW	0	Select the active input, when input is single or dual link case, if REG_CTRL_SDI_IN_SEL is set HIGH. 0 = DDI0 (SL case), DDI0 & DDI1 (DL case) 1 = DDI2 (SL case), DDI2 & DDI3 (DL case) In SDI-SDI mode, DL→SL MUX mode or SL-DL DeMUX mode it selects input for M0/DM0 path (ANC, audio and TC extraction/insertion).
0012	RSVD	RSVD	15:0	RO	1DE6	Reserved.
0013 [1]	SYNC_W_ DISABLE	RSVD	15:4	RO	0	Reserved.
		DEMUX1_SYNC_ W_DISABLE	3:3	RW	0	When HIGH, disables sync word insertion for DEMUX1. Only applies to dual 6G output mode.
		DEMUX0_SYNC_ W_DISABLE	2:2	RW	0	When HIGH, disables sync word insertion for DEMUX0. Only applies to dual and quad 6G output mode.
		MUX1_SYNC_ W_DISABLE	1:1	RW	0	When HIGH, disables sync word insertion for MUX1.
		MUX0_SYNC_ W_DISABLE	0:0	RW	0	When HIGH, disables sync word insertion for MUX0.
0014	RSVD	RSVD	15:0	RW	FF	Reserved. Do not change.
0015	RSVD	RSVD	15:0	RW	1	Reserved. Do not change.
0016	RSVD	RSVD	15:0	RW	5	Reserved. Do not change.
0017	RSVD	RSVD	15:0	RW	0	Reserved. Do not change.
0018	RSVD	RSVD	15:0	RW	F	Reserved. Do not change.
0019 [2]	VID_STREAM_ INTERLEAVE	RSVD	15:8	RW	0	Reserved. Do not change.
		VID_STREAM_ INTERLEAVE_STAT	7:0	RO	0	When HIGH, data in the video stream is interleaved. One bit per Input data stream. See CH<n>_DS<m> in Figure 3-9 for data stream definition. It maps as: bit0 - DDI0_DS1 bit7 - DDI3_DS2
001A	RSVD	RSVD	15:0	RO	0	Reserved.
001B	CRC_ERROR	RSVD	15:9	RO	0	Reserved.
		CRC_ERROR_MASK	8:5	RW	F	Mask for CRC_ERROR_COMB. 1 at bit (n) includes CRC_ERROR_CH (n) in logical OR.
		CRC_ERROR_COMB	4:4	ROCW	0	CRC errors from Ch0-Ch3 logical ORed
		CRC_ERROR_CH3	3:3	ROCW	0	CRC error input3/ch3
		CRC_ERROR_CH2	2:2	ROCW	0	CRC error input2/ch2
		CRC_ERROR_CH1	1:1	ROCW	0	CRC error input1/ch1
		CRC_ERROR_CH0	0:0	ROCW	0	CRC error input0/ch0
001C [1]		RSVD	15:8	RO	0	Reserved.
	DISABLE_CRC_ INS	DISABLE_CRC_ INS	7:0	RW	0	Disable insertion of recalculated CRC words at the inputs. Disable is per channel.

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Vasit Lin
DIVA Laboratories, Ltd.
09/08/2026

001D [2]	PID_DET_CH0A_DS1_BYTE_12	PID_DET_CH0A_DS1_BYTE_2	15:8	RO	0	Detected PID byte2 for video stream CH0A DS1.
		PID_DET_CH0A_DS1_BYTE_1	7:0	RO	0	Detected PID byte1 for video stream CH0A DS1.
001E [2]	PID_DET_CH0A_DS1_BYTE_34	PID_DET_CH0A_DS1_BYTE_4	15:8	RO	0	Detected PID byte4 for video stream CH0A DS1.
		PID_DET_CH0A_DS1_BYTE_3	7:0	RO	0	Detected PID byte3 for video stream CH0A DS1.
001F [2]	PID_DET_CH0A_DS2_BYTE_12	PID_DET_CH0A_DS2_BYTE_2	15:8	RO	0	Detected PID byte2 for video stream CH0A DS2.
		PID_DET_CH0A_DS2_BYTE_1	7:0	RO	0	Detected PID byte1 for video stream CH0A DS2.
0020 [2]	PID_DET_CH0A_DS2_BYTE_34	PID_DET_CH0A_DS2_BYTE_4	15:8	RO	0	Detected PID byte4 for video stream CH0A DS2.
		PID_DET_CH0A_DS2_BYTE_3	7:0	RO	0	Detected PID byte3 for video stream CH0A DS2.
0021 [2]	PID_DET_CH0B_DS1_BYTE_12	PID_DET_CH0B_DS1_BYTE_2	15:8	RO	0	Detected PID byte2 for video stream CH0B DS1.
		PID_DET_CH0B_DS1_BYTE_1	7:0	RO	0	Detected PID byte1 for video stream CH0B DS1.
0022 [2]	PID_DET_CH0B_DS1_BYTE_34	PID_DET_CH0B_DS1_BYTE_4	15:8	RO	0	Detected PID byte4 for video stream CH0B DS1.
		PID_DET_CH0B_DS1_BYTE_3	7:0	RO	0	Detected PID byte3 for video stream CH0B DS1.
0023 [2]	PID_DET_CH0B_DS2_BYTE_12	PID_DET_CH0B_DS2_BYTE_2	15:8	RO	0	Detected PID byte2 for video stream CH0B DS2.
		PID_DET_CH0B_DS2_BYTE_1	7:0	RO	0	Detected PID byte1 for video stream CH0B DS2.
0024 [2]	PID_DET_CH0B_DS2_BYTE_34	PID_DET_CH0B_DS2_BYTE_4	15:8	RO	0	Detected PID byte4 for video stream CH0B DS2.
		PID_DET_CH0B_DS2_BYTE_3	7:0	RO	0	Detected PID byte3 for video stream CH0B DS2.
0025 [2]	PID_DET_CH1A_DS1_BYTE_12	PID_DET_CH1A_DS1_BYTE_2	15:8	RO	0	Detected PID byte2 for video stream CH1A DS1.
		PID_DET_CH1A_DS1_BYTE_1	7:0	RO	0	Detected PID byte1 for video stream CH1A DS1.
0026 [2]	PID_DET_CH1A_DS1_BYTE_34	PID_DET_CH1A_DS1_BYTE_4	15:8	RO	0	Detected PID byte4 for video stream CH1A DS1.
		PID_DET_CH1A_DS1_BYTE_3	7:0	RO	0	Detected PID byte3 for video stream CH1A DS1.
0027 [2]	PID_DET_CH1A_DS2_BYTE_12	PID_DET_CH1A_DS2_BYTE_2	15:8	RO	0	Detected PID byte2 for video stream CH1A DS2.
		PID_DET_CH1A_DS2_BYTE_1	7:0	RO	0	Detected PID byte1 for video stream CH1A DS2.
0028	PID_DET_CH1A_DS2_BYTE_34	PID_DET_CH1A_DS2_BYTE_4	15:8	RO	0	Detected PID byte4 for video stream CH1A DS2.
		PID_DET_CH1A_DS2_BYTE_4	7:0	RO	0	Detected PID byte3 for video stream CH1A DS2
0029 [2]	PID_DET_CH1B_DS1_BYTE_12	PID_DET_CH1B_DS1_BYTE_2	15:8	RO	0	Detected PID byte2 for video stream CH1B DS1.
		PID_DET_CH1B_DS1_BYTE_1	7:0	RO	0	Detected PID byte1 for video stream CH1B DS1.
002A [2]	PID_DET_CH1B_DS1_BYTE_34	PID_DET_CH1B_DS1_BYTE_4	15:8	RO	0	Detected PID byte4 for video stream CH1B DS1.
		PID_DET_CH1B_DS1_BYTE_3	7:0	RO	0	Detected PID byte3 for video stream CH1B DS1.

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Kent Lin
DIV1 Laboratories Ltd.
09/08/2026

002B [2]	PID_DET_CH1B_DS2_BYTE_12	PID_DET_CH1B_DS2_BYTE_2	15:8	RO	0	Detected PID byte2 for video stream CH1B DS2.
		PID_DET_CH1B_DS2_BYTE_1	7:0	RO	0	Detected PID byte1 for video stream CH1B DS2.
002C [2]	PID_DET_CH1B_DS2_BYTE_34	PID_DET_CH1B_DS2_BYTE_4	15:8	RO	0	Detected PID byte4 for video stream CH1B DS2.
		PID_DET_CH1B_DS2_BYTE_3	7:0	RO	0	Detected PID byte3 for video stream CH1B DS2.
002D [2]	PID_DET_CH2A_DS1_BYTE_12	PID_DET_CH2A_DS1_BYTE_2	15:8	RO	0	Detected PID byte2 for video stream CH2A DS1.
		PID_DET_CH2A_DS1_BYTE_1	7:0	RO	0	Detected PID byte1 for video stream CH2A DS1.
002E [2]	PID_DET_CH2A_DS1_BYTE_34	PID_DET_CH2A_DS1_BYTE_4	15:8	RO	0	Detected PID byte4 for video stream CH2A DS1.
		PID_DET_CH2A_DS1_BYTE_3	7:0	RO	0	Detected PID byte3 for video stream CH2A DS1.
002F [2]	PID_DET_CH2A_DS2_BYTE_12	PID_DET_CH2A_DS2_BYTE_2	15:8	RO	0	Detected PID byte2 for video stream CH2A DS2.
		PID_DET_CH2A_DS2_BYTE_1	7:0	RO	0	Detected PID byte1 for video stream CH2A DS2.
0030 [2]	PID_DET_CH2A_DS2_BYTE_34	PID_DET_CH2A_DS2_BYTE_4	15:8	RO	0	Detected PID byte4 for video stream CH2A DS2.
		PID_DET_CH2A_DS2_BYTE_3	7:0	RO	0	Detected PID byte3 for video stream CH2A DS2.
0031	PID_DET_CH2B_DS1_BYTE_12	PID_DET_CH2B_DS1_BYTE_2	15:8	RO	0	Detected PID byte2 for video stream CH2B DS1.
		PID_DET_CH2B_DS1_BYTE_1	7:0	RO	0	Detected PID byte1 for video stream CH2B DS1
0032 [2]	PID_DET_CH2B_DS1_BYTE_34	PID_DET_CH2B_DS1_BYTE_4	15:8	RO	0	Detected PID byte4 for video stream CH2B DS1.
		PID_DET_CH2B_DS1_BYTE_3	7:0	RO	0	Detected PID byte3 for video stream CH2B DS1.
0033 [2]	PID_DET_CH2B_DS2_BYTE_12	PID_DET_CH2B_DS2_BYTE_2	15:8	RO	0	Detected PID byte2 for video stream CH2B DS2.
		PID_DET_CH2B_DS2_BYTE_1	7:0	RO	0	Detected PID byte1 for video stream CH2B DS2.
0034 [2]	PID_DET_CH2B_DS2_BYTE_34	PID_DET_CH2B_DS2_BYTE_4	15:8	RO	0	Detected PID byte4 for video stream CH2B DS2.
		PID_DET_CH2B_DS2_BYTE_3	7:0	RO	0	Detected PID byte3 for video stream CH2B DS2.
0035 [2]	PID_DET_CH3A_DS1_BYTE_12	PID_DET_CH3A_DS1_BYTE_2	15:8	RO	0	Detected PID byte2 for video stream CH3A DS1.
		PID_DET_CH3A_DS1_BYTE_1	7:0	RO	0	Detected PID byte1 for video stream CH3A DS1.
0036 [2]	PID_DET_CH3A_DS1_BYTE_34	PID_DET_CH3A_DS1_BYTE_4	15:8	RO	0	Detected PID byte4 for video stream CH3A DS1.
		PID_DET_CH3A_DS1_BYTE_3	7:0	RO	0	Detected PID byte3 for video stream CH3A DS1.
0037 [2]	PID_DET_CH3A_DS2_BYTE_12	PID_DET_CH3A_DS2_BYTE_2	15:8	RO	0	Detected PID byte2 for video stream CH3A DS2.
		PID_DET_CH3A_DS2_BYTE_1	7:0	RO	0	Detected PID byte1 for video stream CH3A DS2.
0038 [2]	PID_DET_CH3A_DS2_BYTE_34	PID_DET_CH3A_DS2_BYTE_4	15:8	RO	0	Detected PID byte4 for video stream CH3A DS2.
		PID_DET_CH3A_DS2_BYTE_3	7:0	RO	0	Detected PID byte3 for video stream CH3A DS2.

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Kent Lin
DIV4 Laboratories Ltd.
09/08/2026

0039 [2]	PID_DET_CH3B_DS1_BYTE_12	PID_DET_CH3B_DS1_BYTE_2	15:8	RO	0	Detected PID byte2 for video stream CH3B DS1.
		PID_DET_CH3B_DS1_BYTE_1	7:0	RO	0	Detected PID byte1 for video stream CH3B DS1.
003A [2]	PID_DET_CH3B_DS2_BYTE_34	PID_DET_CH3B_DS1_BYTE_4	15:8	RO	0	Detected PID byte3 for video stream CH3B DS1.
		PID_DET_CH3B_DS1_BYTE_3	7:0	RO	0	Detected PID byte2 for video stream CH3B DS1

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
0000	HOST_CONFIG	RSVD	15:15	RW	0	Reserved. Do not change.
		GSPI_LINK_DISABLE	14:14	RW	0	GSPI loop-through disable.
		GSPI_BUS_THROUGH_ENABLE	13:13	RW	0	Enables bus-through operation.
		RSVD	12:5	RW	0	Reserved. Do not change.
		DEVICE_UNIT_ADDRESS	4:0	RW	0	Sets the unit address for the device.
0001 [1]	OPERATING_MODE_SEL_REG	SEC_LINK_EN_REG_SEL	15:15	RW	0	If set to HIGH the SEC_LINK_EN_REG value is used instead of the SEC_LINK_EN pin.
		SEC_LINK_EN_REG	14:14	RW	0	Overrides SEC_LINK_EN pin if SEC_LINK_EN_REG_SEL set HIGH.
		PG_REF_INT_EXTB	13:13	RW	0	If set to HIGH the reference for pg is generated from the external clock reference, if set to LOW reference and all time in is derived from the video stream connected to input 0.
		SEL_PG	12:12	RW	0	Enables pattern generator. 1 = PG enabled. 0 = PG disabled.
		RSVD	11:9	RW	0	Reserved. Do not change.

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09/08/2026

		REG_CTRL_ MODE_SEL_EN	8:8	RW	0	Overrides MODE_SEL pins with values in the MODE_SEL register.
		MODE_SEL	7:5	RW	7	Selects operating mode, if REG_CTRL_MODE_SEL is set HIGH. 111 = QL 3Gb/s to SL 12Gb/s 110 = QL 1.5Gb/s to SL 6Gb/s 101 = QL 6Gb/s to DL 12Gb/s 100 = QL 3Gb/s to DL 6Gb/s 011 = DL 6Gb/s to SL 12Gb/s 010 = DL 3Gb/s to SL 6Gb/s 001 = DL 1.5Gb/s to SL 3Gb/s 000 = RSVD
		REG_CTRL_OP_ MODE_EN	4:4	RW	0	When HIGH, MUX_DEMUX_REG, PID_MODE_REG and BYPASS_REG will set operating mode instead of the associated pins.
		PID_MODE_REG	3:2	RW	0	Enabled by REG_CTRL_OP_MODE_EN. 00 = Automatic PID insertion 11 = No PID insertion
		BYPASS_REG	1:1	RW	0	When HIGH, sets the part in the BYPASS. Enabled by REG_CTRL_OP_MODE_EN.
		MUX_DEMUX_REG	0:0	RW	0	When HIGH, sets MUX operation mode. When LOW, sets DeMUX operation mode. Enabled by REG_CTRL_OP_MODE_EN.
0002 [1]	SD_BYPASS_ SEL_REG	RSVD	15:10	RO	0	Reserved.
		SD_BYPASS_ RATE_6G_3Gb	9:9	RW	0	When HIGH, oversampling rate in SD_BYPASS mode is set to 6G data rate. When LOW, it is set to 3G data rate.
		REG_CTRL_ SD_BYPASS	8:8	RW	0	When HIGH, SD_BYPASS control from registers.
		SD_BYPASS_PIN	7:4	RO	0	SD_BYPASS pin status.

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Kent Lin
DIVA Laboratories Ltd.
09/08/2026

		SD_BYPASS_SEL	3:0	RW	0	When HIGH, input Rx will be set to SD_BYPASS mode. Only active when REG_CTRL_SD_BYPASS is set HIGH. One bit per input.
0003 [2]	INPUT_LOCK_ REG	RSVD	15:12	RO	0	Reserved.
		REG_CTRL_ INPUT_LOCK	11:8	RW	0	When HIGH, control of lock signal is taken from INPUT_LOCK_REG.
		INPUT_LOCK_REG	7:4	RW	0	Overrides video lock signal if REG_CTRL_ INPUT_LOCK register is set HIGH. One bit per input.
		INPUT_LOCK	3:0	RO	0	Indicates video lock of the input 0 to 3. One bit per input.
0004	RSVD	RSVD	15:0	RW	0	Reserved. Do not change.
0005 [2]	ISP_REG	ISP_POLARITY	15:12	RW	0	When HIGH inverts ISP polarity. One bit per input.
		ISP_REG_SEL	11:8	RW	0	When HIGH, overrides ISP pin with the value from the ISP_REG_SEL parameter. One bit per input.
		ISP_REG	7:4	RW	0	Sets value of ISP signal, if REG_CTRL_ISP_SEL_EN is set HIGH. One bit per input.
		ISP_PIN	3:0	RO	0	Reports signal level (HIGH or LOW) applied to the ISP pin. One bit per input.
0006 [2]	MANUAL_ RATE	RSVD	15:15	RO	0	Reserved.
		SDI_AUTO_MODE_ FORCE_DLHD_3G	14:14	RW	0	Selects DLHD ® 3G instead of QLHD ® 6G when input data rate is HD.

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DIVA Laboratories. Ltd.
09/08/2026

		SDI_AUTO_ MODE_OUT_INTERF	13:13	RW	0	Selects the output interface when in SDI_AUTO_MODE 0 = QL output when DEMUX (6G&12G in); SL output when MUX 1 = DL output when DEMUX (6G&12G in); DL output when MUX
		SDI_AUTO_ MODE_EN	12:12	RW	0	Selects the auto rate/mode detection for SDI-SDI configuration.
		MANUAL_RATE_RX3	11:10	RW	0	Manual rate control of Rx3. 00 = HD 01 = 3G 10 = 6G 11 = 12G Only active when REG_CTRL_MANUAL_RATE[3] is set HIGH.
		MANUAL_RATE_RX2	9:8	RW	0	Manual rate control of Rx2. See MANUAL_RATE_RX3 for selection values.
		MANUAL_RATE_RX1	7:6	RW	0	Manual rate control of Rx1. See MANUAL_RATE_RX3 for selection values.
		MANUAL_RATE_RX0	5:4	RW	0	Manual rate control of Rx0. See MANUAL_RATE_RX3 for selection values.
		REG_CTRL_ MANUAL_RATE	3:0	RW	0	Manual rate control override. One bit per input.
0007 [2]	DATA_RATE_ REPORT	AUTO_MODE_DET	15:12	RO	0	Detected operational mode when in the auto mode
		INTERLEAVED_ INPUT_DET	11:8	RO	0	Interleaved stream detected at input (n)

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09/08/2026

		DATA_RATE_RX3	7:6	RO	3	Indicates data rate of Rx3. 11 = 12G 10 = 6G 01 = 3G 00 = HD **Note:** If the input is not locked, the value reported by this parameter is not valid. If the device is in the DeMUX or MUX mode, the value reported is always the same as the input data rate given by the selected gearbox mode.
		DATA_RATE_RX2	5:4	RO	3	Indicates data rate of Rx2. See DATA_RATE_RX3 for selection values.
		DATA_RATE_RX1	3:2	RO	3	Indicates data rate of Rx1. See DATA_RATE_RX3 for selection values.
		DATA_RATE_RX0	1:0	RO	3	Indicates data rate of Rx0. See DATA_RATE_RX3 for selection values.
0008	RSVD	RSVD	15:0	RW	F	Reserved. Do not change.
0009	DDI_PWR_DOWN	RSVD	15:12	RO	0	Reserved.
		DDI_PWR_DOWN_REG_SEL	11:8	RW	0	Selects the reg settings for power down for corresponding receiver One bit per input.
		DDI3_PWR_DOWN_REG	7:7	RW	0	Power-down for DDI3, if DDI_PWR_DOWN_REG_SEL is set HIGH.
		RSVD	6:6	RW	0	Reserved. Do not change.
		DDI2_PWR_DOWN_REG	5:5	RW	0	Power-down for DDI2, if DDI_PWR_DOWN_REG_SEL is set HIGH.
		RSVD	4:4	RW	0	Reserved. Do not change.
		DDI1_PWR_DOWN_REG	3:3	RW	0	Power-down for DDI1, if DDI_PWR_DOWN_REG_SEL is set HIGH.

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09/08/2026

		RSVD	2:2	RW	0	Reserved. Do not change.
		DDI0_PWR_DOWN_REG	1:1	RW	0	Power-down for DDI0, if DDI_PWR_DOWN_REG_SEL is set HIGH.
		RSVD	0:0	RW	0	Reserved. Do not change.
000A	DDO_IDLE	RSVD	15:12	RO	0	Reserved.
		DDO_IDLE_OW_EN	11:8	RW	0	Manual transmitter idle override enable. 0 = DDO idle controlled by the GS12270 operation mode 1 = DDO Idle controlled by the DDO[3:0]_IDLE_REG setting One bit per output.
		DDI3_IDLE_REG	7:6	RW	0	Idle for DDO3, if DDO_IDLE_OW_EN is set HIGH.
		DDO2_IDLE_REG	5:4	RW	0	Idle for DDO2, if DDO_IDLE_OW_EN is set HIGH.
		DDO1_IDLE_REG	3:2	RW	0	Idle for DDO1, if DDO_IDLE_OW_EN is set HIGH.
		DDO0_IDLE_REG	1:0	RW	0	Idle for DDO0, if DDO_IDLE_OW_EN is set HIGH.
000B [1]	REG_CTRL_OUTPUT_ASGMT_EN	RSVD	15:4	RO	0	Reserved.
		REG_CTRL_OUTPUT_ASGMT_EN	3:0	RW	0	When the corresponding bit <n> is asserted, the assignment of the DDO<n>serial output is controlled by the settings of the OUTPUT_ASGMT_DDO<n> parameter: DDO0 = Bit 0 DDO1 = Bit 1 DDO2 = Bit 2 DDO3 = Bit 3
		RSVD	15:15	RO	0	Reserved.

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09/08/2026

000C [1]	CHAN_ASGMT_ DDO<n>	OUTPUT_ ASGMT_DDO3	14:12	RW	2	Selects the source of the DDO3 output if REG_CTRL_OUTPUT_ASGMT_EN is set HIGH. 000 = M0 Processed Output 001 = M1 Processed Output 010 = DM0 Processed Output 011 = DM1 Processed Output 100 = DDI0 101 = DDI1 110 = DDI2 111 = DDI3
		RSVD	11:11	RO	0	Reserved.
		OUTPUT_ ASGMT_DDO2	10:8	RW	2	Selects the source of the DDO2 output if REG_CTRL_OUTPUT_ASGMT_EN is set HIGH. See OUTPUT_ASGMT_DDO3 for selection values.
		RSVD	7:7	RO	0	Reserved.
		OUTPUT_ ASGMT_DDO1	6:4	RW	2	Selects the source of the DDO1 output if REG_CTRL_OUTPUT_ASGMT_EN is set HIGH. See OUTPUT_ASGMT_DDO3 for selection values.
		RSVD	3:3	RO	0	Reserved.
		OUTPUT_ ASGMT_DDO0	2:0	RW	2	Selects the source of the DDO0 output if REG_CTRL_OUTPUT_ASGMT_EN is set HIGH. See OUTPUT_ASGMT_DDO3 for selection values.
000D	RSVD	RSVD	15:0	RW	0	Reserved. Do not change.
000E [3]	SEL_DM0_VIRT	RSVD	15:14	RO	0	Reserved.
		REG_CTRL_DM0_ LINES_2_4B	13:13	RW	0	If set to HIGH, DM0_LINES_2_4B_REG selects between 1to2 and 1to4 demuxing in DM0 virtual interface.
		DM0_LINES_ 2_4B_REG	12:12	RW	0	Selects between 1to2 and 1to4 demuxing in DM0 virtual interface when REG_CTRL_DM0_LINES_2_4B set HIGH.

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DIVA Laboratories Ltd.
09/08/2026

		SEL_DM0_VIRT3	11:10	RW	0	Manual assignment of the data stream on the Tx3, if REG_CTRL_SEL_DM0_VIRT[3] is set HIGH. 00 = Data stream 8/7 01 = Data stream 6/5 10 = Data stream 4/3 11 = Data stream 2/1
		SEL_DM0_VIRT2	9:8	RW	1	Manual assignment of the data stream on the Tx2, if REG_CTRL_SEL_DM0_VIRT[2] is set HIGH. See SEL_DM0_VIRT3 for selection values.
		SEL_DM0_VIRT1	7:6	RW	2	Manual assignment of the data stream on the Tx1, if REG_CTRL_SEL_DM0_VIRT[1] is set HIGH. See SEL_DM0_VIRT3 for selection values.
		SEL_DM0_VIRT0	5:4	RW	3	Manual assignment of the data stream on the Tx0, if REG_CTRL_SEL_DM0_VIRT[0] is set HIGH. See SEL_DM0_VIRT3 for selection values.
		REG_CTRL_ SEL_DM0_VIRT	3:0	RW	0	When HIGH, the control of the DM0 virtual interface output is from register SEL_DM0_VIRT[3:0]. One bit per output channel.
000F [1]	SEL_DM1_VIRT	RSVD	15:5	RO	0	Reserved.
		REG_CTRL_SEL_ DM1_VIRT	4:4	RW	0	When HIGH, enables SEL_DM1_VIRT control.
		SEL_DM1_VIRT	3:0	RW	5	When HIGH, swaps data stream on DM1. One bit per output channel.
0010	RSVD	RSVD	15:0	RW	0	Reserved. Do not change.
0011 [2]	SDI_IN_SEL	RSVD	15:5	RO	0	Reserved.
		UNUSED_0_2_ IN_RESET_EN	4:4	RW	0	if set HIGH input channel which is not selected is reset (doesn't apply on SDI auto modes).

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09/08/2026

		RSVD	3:2	RO	0	Reserved.
		REG_CTRL_ SDI_IN_SEL	1:1	RW	0	When HIGH, enables selection of the active input, when input is single or dual link case, through the register DEMUX_IN_0_2_SEL.
		SDI_IN_0_2_SEL	0:0	RW	0	Select the active input, when input is single or dual link case, if REG_CTRL_SDI_IN_SEL is set HIGH. 0 = DDI0 (SL case), DDI0 & DDI1 (DL case) 1 = DDI2 (SL case), DDI2 & DDI3 (DL case) In SDI-SDI mode, DL ® SL MUX mode or SL-DL DeMUX mode it selects input for M0/DM0 path (ANC, audio and TC extraction/insertion).
0012	RSVD	RSVD	15:0	RO	1DE6	Reserved.
0013 [1]	SYNC_W_ DISABLE	RSVD	15:4	RO	0	Reserved.
		DEMUX1_SYNC_ W_DISABLE	3:3	RW	0	When HIGH, disables sync word insertion for DEMUX1. Only applies to dual 6G output mode.
		DEMUX0_SYNC_ W_DISABLE	2:2	RW	0	When HIGH, disables sync word insertion for DEMUX0. Only applies to dual and quad 6G output mode.
		MUX1_SYNC_ W_DISABLE	1:1	RW	0	When HIGH, disables sync word insertion for MUX1.
		MUX0_SYNC_ W_DISABLE	0:0	RW	0	When HIGH, disables sync word insertion for MUX0.
0014	RSVD	RSVD	15:0	RW	FF	Reserved. Do not change.
0015	RSVD	RSVD	15:0	RW	1	Reserved. Do not change.
0016	RSVD	RSVD	15:0	RW	5	Reserved. Do not change.
0017	RSVD	RSVD	15:0	RW	0	Reserved. Do not change.

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DIVA Laboratories, Ltd.
09/08/2026

0018	RSVD	RSVD	15:0	RW	F	Reserved. Do not change.
0019 [2]	VID_STREAM_ INTERLEAVE	RSVD	15:8	RW	0	Reserved. Do not change.
		VID_STREAM_ INTERLEAVE_STAT	7:0	RO	0	When HIGH, data in the video stream is interleaved. One bit per Input data stream. See CH<n>_DS<m> in **Error! Reference source not found.** for data stream definition. It maps as: bit0 - DDI0_DS1 bit7 - DDI3_DS2
001A	RSVD	RSVD	15:0	RO	0	Reserved.
001B	CRC_ERROR	RSVD	15:9	RO	0	Reserved.
		CRC_ERROR_MASK	8:5	RW	F	Mask for CRC_ERROR_COMB. 1 at bit (n) includes CRC_ERROR_CH (n) in logical OR.
		CRC_ERROR_COMB	4:4	ROCW	0	CRC errors from Ch0-Ch3 logical ORed
		CRC_ERROR_CH3	3:3	ROCW	0	CRC error input3/ch3
		CRC_ERROR_CH2	2:2	ROCW	0	CRC error input2/ch2
		CRC_ERROR_CH1	1:1	ROCW	0	CRC error input1/ch1
		CRC_ERROR_CH0	0:0	ROCW	0	CRC error input0/ch0
001C [1]	DISABLE_CRC_ INS	RSVD	15:8	RO	0	Reserved.
		DISABLE_CRC_ INS	7:0	RW	0	Disable insertion of recalculated CRC words at the inputs. Disable is per channel.
001D [2]	PID_DET_CH0A_ DS1_BYTE_1_2	PID_DET_CH0A_ DS1_BYTE_2	15:8	RO	0	Detected PID byte2 for video stream CH0A DS1.
		PID_DET_CH0A_ DS1_BYTE_1	7:0	RO	0	Detected PID byte1 for video stream CH0A DS1.
001E [2]	PID_DET_CH0A_ DS1_BYTE_34	PID_DET_CH0A_ DS1_BYTE_4	15:8	RO	0	Detected PID byte4 for video stream CH0A DS1.

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Kent Lin
DIVA Laboratories, Ltd.
09/08/2026

		PID_DET_CH0A_DS1_BYTE_3	7:0	RO	0	Detected PID byte3 for video stream CH0A DS1.
001F [2]	PID_DET_CH0A_DS2_BYTE_12	PID_DET_CH0A_DS2_BYTE_2	15:8	RO	0	Detected PID byte2 for video stream CH0A DS2.
		PID_DET_CH0A_DS2_BYTE_1	7:0	RO	0	Detected PID byte1 for video stream CH0A DS2.
0020 [2]	PID_DET_CH0A_DS2_BYTE_34	PID_DET_CH0A_DS2_BYTE_4	15:8	RO	0	Detected PID byte4 for video stream CH0A DS2.
		PID_DET_CH0A_DS2_BYTE_3	7:0	RO	0	Detected PID byte3 for video stream CH0A DS2.
0021 [2]	PID_DET_CH0B_DS1_BYTE_12	PID_DET_CH0B_DS1_BYTE_2	15:8	RO	0	Detected PID byte2 for video stream CH0B DS1.
		PID_DET_CH0B_DS1_BYTE_1	7:0	RO	0	Detected PID byte1 for video stream CH0B DS1.
0022 [2]	PID_DET_CH0B_DS1_BYTE_34	PID_DET_CH0B_DS1_BYTE_4	15:8	RO	0	Detected PID byte4 for video stream CH0B DS1.
		PID_DET_CH0B_DS1_BYTE_3	7:0	RO	0	Detected PID byte3 for video stream CH0B DS1.
0023 [2]	PID_DET_CH0B_DS2_BYTE_12	PID_DET_CH0B_DS2_BYTE_2	15:8	RO	0	Detected PID byte2 for video stream CH0B DS2.
		PID_DET_CH0B_DS2_BYTE_1	7:0	RO	0	Detected PID byte1 for video stream CH0B DS2.
0024 [2]	PID_DET_CH0B_DS2_BYTE_34	PID_DET_CH0B_DS2_BYTE_4	15:8	RO	0	Detected PID byte4 for video stream CH0B DS2.
		PID_DET_CH0B_DS2_BYTE_3	7:0	RO	0	Detected PID byte3 for video stream CH0B DS2.
0025 [2]	PID_DET_CH1A_DS1_BYTE_12	PID_DET_CH1A_DS1_BYTE_2	15:8	RO	0	Detected PID byte2 for video stream CH1A DS1.
		PID_DET_CH1A_DS1_BYTE_1	7:0	RO	0	Detected PID byte1 for video stream CH1A DS1.

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DIVA Laboratories Ltd.
09/08/2026

0026 [2]	PID_DET_CH1A_ DS1_BYTE_34	PID_DET_CH1A_ DS1_BYTE_4	15:8	RO	0	Detected PID byte4 for video stream CH1A DS1.
		PID_DET_CH1A_ DS1_BYTE_3	7:0	RO	0	Detected PID byte3 for video stream CH1A DS1.
0027 [2]	PID_DET_CH1A_ DS2_BYTE_12	PID_DET_CH1A_ DS2_BYTE_2	15:8	RO	0	Detected PID byte2 for video stream CH1A DS2.
		PID_DET_CH1A_ DS2_BYTE_1	7:0	RO	0	Detected PID byte1 for video stream CH1A DS2.
0028 [2]	PID_DET_CH1A_ DS2_BYTE_34	PID_DET_CH1A_ DS2_BYTE_4	15:8	RO	0	Detected PID byte4 for video stream CH1A DS2.
		PID_DET_CH1A_ DS2_BYTE_3	7:0	RO	0	Detected PID byte3 for video stream CH1A DS2.
0029 [2]	PID_DET_CH1B_ DS1_BYTE_12	PID_DET_CH1B_ DS1_BYTE_2	15:8	RO	0	Detected PID byte2 for video stream CH1B DS1.
		PID_DET_CH1B_ DS1_BYTE_1	7:0	RO	0	Detected PID byte1 for video stream CH1B DS1.
002A [2]	PID_DET_CH1B_ DS1_BYTE_34	PID_DET_CH1B_ DS1_BYTE_4	15:8	RO	0	Detected PID byte4 for video stream CH1B DS1.
		PID_DET_CH1B_ DS1_BYTE_3	7:0	RO	0	Detected PID byte3 for video stream CH1B DS1.
002B [2]	PID_DET_CH1B_ DS2_BYTE_12	PID_DET_CH1B_ DS2_BYTE_2	15:8	RO	0	Detected PID byte2 for video stream CH1B DS2.
		PID_DET_CH1B_ DS2_BYTE_1	7:0	RO	0	Detected PID byte1 for video stream CH1B DS2.
002C [2]	PID_DET_CH1B_ DS2_BYTE_34	PID_DET_CH1B_ DS2_BYTE_4	15:8	RO	0	Detected PID byte4 for video stream CH1B DS2.
		PID_DET_CH1B_ DS2_BYTE_3	7:0	RO	0	Detected PID byte3 for video stream CH1B DS2.
002D [2]	PID_DET_CH2A_ DS1_BYTE_12	PID_DET_CH2A_ DS1_BYTE_2	15:8	RO	0	Detected PID byte2 for video stream CH2A DS1.

Semtech Confidential Information
Kent Lin
DIVA Laboratories Ltd.
09/08/2026

		PID_DET_CH2A_DS1_BYTE_1	7:0	RO	0	Detected PID byte1 for video stream CH2A DS1.
002E [2]	PID_DET_CH2A_DS1_BYTE_34	PID_DET_CH2A_DS1_BYTE_4	15:8	RO	0	Detected PID byte4 for video stream CH2A DS1.
		PID_DET_CH2A_DS1_BYTE_3	7:0	RO	0	Detected PID byte3 for video stream CH2A DS1.
002F [2]	PID_DET_CH2A_DS2_BYTE_12	PID_DET_CH2A_DS2_BYTE_2	15:8	RO	0	Detected PID byte2 for video stream CH2A DS2.
		PID_DET_CH2A_DS2_BYTE_1	7:0	RO	0	Detected PID byte1 for video stream CH2A DS2.
0030 [2]	PID_DET_CH2A_DS2_BYTE_34	PID_DET_CH2A_DS2_BYTE_4	15:8	RO	0	Detected PID byte4 for video stream CH2A DS2.
		PID_DET_CH2A_DS2_BYTE_3	7:0	RO	0	Detected PID byte3 for video stream CH2A DS2.
0031 [2]	PID_DET_CH2B_DS1_BYTE_12	PID_DET_CH2B_DS1_BYTE_2	15:8	RO	0	Detected PID byte2 for video stream CH2B DS1.
		PID_DET_CH2B_DS1_BYTE_1	7:0	RO	0	Detected PID byte1 for video stream CH2B DS1.
0032 [2]	PID_DET_CH2B_DS1_BYTE_34	PID_DET_CH2B_DS1_BYTE_4	15:8	RO	0	Detected PID byte4 for video stream CH2B DS1.
		PID_DET_CH2B_DS1_BYTE_3	7:0	RO	0	Detected PID byte3 for video stream CH2B DS1.
0033 [2]	PID_DET_CH2B_DS2_BYTE_12	PID_DET_CH2B_DS2_BYTE_2	15:8	RO	0	Detected PID byte2 for video stream CH2B DS2.
		PID_DET_CH2B_DS2_BYTE_1	7:0	RO	0	Detected PID byte1 for video stream CH2B DS2.
0034 [2]	PID_DET_CH2B_DS2_BYTE_34	PID_DET_CH2B_DS2_BYTE_4	15:8	RO	0	Detected PID byte4 for video stream CH2B DS2.
		PID_DET_CH2B_DS2_BYTE_3	7:0	RO	0	Detected PID byte3 for video stream CH2B DS2.

Semtech Confidential Information
Kent Lin
DIVA Laboratories Ltd.
09/08/2026

0035 [2]	PID_DET_CH3A_ DS1_BYTE_12	PID_DET_CH3A_ DS1_BYTE_2	15:8	RO	0	Detected PID byte2 for video stream CH3A DS1.
		PID_DET_CH3A_ DS1_BYTE_1	7:0	RO	0	Detected PID byte1 for video stream CH3A DS1.
0036 [2]	PID_DET_CH3A_ DS1_BYTE_34	PID_DET_CH3A_ DS1_BYTE_4	15:8	RO	0	Detected PID byte4 for video stream CH3A DS1.
		PID_DET_CH3A_ DS1_BYTE_3	7:0	RO	0	Detected PID byte3 for video stream CH3A DS1.
0037 [2]	PID_DET_CH3A_ DS2_BYTE_12	PID_DET_CH3A_ DS2_BYTE_2	15:8	RO	0	Detected PID byte2 for video stream CH3A DS2.
		PID_DET_CH3A_ DS2_BYTE_1	7:0	RO	0	Detected PID byte1 for video stream CH3A DS2.
0038 [2]	PID_DET_CH3A_ DS2_BYTE_34	PID_DET_CH3A_ DS2_BYTE_4	15:8	RO	0	Detected PID byte4 for video stream CH3A DS2.
		PID_DET_CH3A_ DS2_BYTE_3	7:0	RO	0	Detected PID byte3 for video stream CH3A DS2.
0039 [2]	PID_DET_CH3B_ DS1_BYTE_12	PID_DET_CH3B_ DS1_BYTE_2	15:8	RO	0	Detected PID byte2 for video stream CH3B DS1.
		PID_DET_CH3B_ DS1_BYTE_1	7:0	RO	0	Detected PID byte1 for video stream CH3B DS1.
003A [2]	PID_DET_CH3B_ DS1_BYTE_34	PID_DET_CH3B_ DS1_BYTE_4	15:8	RO	0	Detected PID byte3 for video stream CH3B DS1.
		PID_DET_CH3B_ DS1_BYTE_3	7:0	RO	0	Detected PID byte2 for video stream CH3B DS1.
003B [2]	PID_DET_CH3B_ DS2_BYTE_12	PID_DET_CH3B_ DS2_BYTE_2	15:8	RO	0	Detected PID byte2 for video stream CH3B DS2.
		PID_DET_CH3B_ DS2_BYTE_1	7:0	RO	0	Detected PID byte1 for video stream CH3B DS2.
003C [2]	PID_DET_CH3B_ DS2_BYTE_3_4	PID_DET_CH3B_ DS2_BYTE_4	15:8	RO	0	Detected PID byte4 for video stream CH3B DS2.

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Kent Lin
DIVA Laboratories Ltd.
09/08/2026

		PID_DET_CH3B_DS2_BYTE_3	7:0	RO	0	Detected PID byte3 for video stream CH3B DS2.
003D [3]	OVERRIDE_STREAM_NUMBER	OVERRIDE_STREAM_NUMBER_SEL	15:0	RW	0	When HIGH, selects the stream to override the link number. When LOW, link numbers are not modifiable.
003E [3]	LINK_N_TO_INSERT_STR_0_7	LINK_N_0_7	15:0	RW	0	PID word link number for streams 0-7 to be embedded, if the corresponding stream is selected through OVERRIDE_STREAM_NUMBER_SEL register. Two bits per data stream. Refer to **Error! Reference source not found.** to **Error! Reference source not found.** in data sheet for definition of the streams.
003F [1]	LINK_N_TO_INSERT_STR_8_15	LINK_N_8_15	15:0	RW	0	PID word link number for streams 8-15 to be embedded, if the corresponding stream is selected through OVERRIDE_STREAM_NUMBER_SEL register. Two bits per data stream. Refer to **Error! Reference source not found.** to **Error! Reference source not found.** in data sheet for definition of the streams.
0040 [3]	PID_PROGRAM_CTRL	RSVD	15:8	RO	0	Reserved.
		PID_BYTE_OVERRIDE	7:4	RW	F	When in manual PID replacement mode, set bit HIGH to select PID byte override. Bit 7 of PID_BYTE_OVERRIDE corresponds to PID byte 4. Bit 4 of PID_BYTE_OVERRIDE corresponds to PID byte 1. **Note:** Byte selection applies to all 16 streams.
		RSVD	3:3	RO	0	Reserved.
		REPLACE_EXISTING_PID	2:2	RW	0	When HIGH enables the PID insertion to replace only the 4 user data words in an existing packet, which does not have to reside immediately after EAV. When LOW, inserts a new PID packet immediately after EAV.

Semtech Confidential Information
Kent Lin
DIVA Laboratories. Ltd.
09/08/2026

						Note: Not used in HDMI-SDI mode.
		PID_WR_FAST_MODE	1:1	RW	0	When HIGH, enables fast mode PID replacement. In fast mode, PIDs from the PID_INS_CH0A_DS1_BYTE_1_2 and PID_INS_CH0A_DS1_BYTE_3_4 registers are written to all streams selected by PID_PROGRAM_STREAM_MASK. **Note:** Not used in HDMI-SDI mode.
		PID_OVERRIDE	0:0	RW	0	When HIGH, enables manual PID insertion in streams selected by PID_PROGRAM_STREAM_MASK.
0041 [3]	PID_PROGRAM_STREAM_MASK	PID_PROGRAM_VID_STREAM_MASK	15:0	RW	0	When HIGH, the PID will be overridden for the corresponding video stream. One bit per data stream. Refer to Table 3-29 to Table 3-32 in data sheet for definition of the streams. In the HDMI-SDI mode the register is split into two 8-bit vectors: PID_FROM_CSR_SEL = PID_PROGRAM_VID_STREAM_MASK[7:0] PID_VALUE_DS2_DS1B = PID_PROGRAM_VID_STREAM_MASK[15:8] Each bit in PID_FROM_CSR_SEL enables PID replacement from CSR in one of up to eight video streams (if PID_OVERRIDE is set HIGH and for BYTE for which PID_BYTE_OVERRIDE is set HIGH). Each bit in PID_VALUE_DS2_DS1B which SCR values will be used for PID replacement in corresponding video streams. 0 = selects values from PID_INS_CH0A_DS1_BYTE_*_* registers. 1 = selects values from PID_INS_CH0A_DS2_BYTE_*_* registers.

Semtech Confidential Information
Kent Lin
DIVA Laboratories, Ltd.
09/08/2026

0042 [1]	PID_ERROR	PID_ERROR	15:0	RO	0	When HIGH, PID error is detected. One bit per data stream. Refer to **Error! Reference source not found.** to **Error! Reference source not found.** in data sheet for definition of the streams.
0043 [2]	PID_DETECTED	PID_DETECTED	15:0	RO	0	When HIGH, reports that PID is detected. One bit per data stream. Refer to **Error! Reference source not found.** to **Error! Reference source not found.** in data sheet for definition of the streams.
0044 [3]	PID_INS_CH0A_ DS1_BYTE_1_2	PID_INS_CH0A_ DS1_BYTE_2	15:8	RW	0	PID byte 2 to be inserted in the video stream CH0A DS1.
		PID_INS_CH0A_ DS1_BYTE_1	7:0	RW	0	PID byte 1 to be inserted in the video stream CH0A DS1.
0045 [3]	PID_INS_CH0A_ DS1_BYTE_34	PID_INS_CH0A_ DS1_BYTE_4	15:8	RW	0	PID byte 4 to be inserted in the video stream CH0A DS1.
		PID_INS_CH0A_ DS1_BYTE_3	7:0	RW	0	PID byte 3 to be inserted in the video stream CH0A DS1.
0046 [3]	PID_INS_CH0A_ DS2_BYTE_12	PID_INS_CH0A_ DS2_BYTE_2	15:8	RW	0	PID byte 2 to be inserted in the video stream CH0A DS2.
		PID_INS_CH0A_ DS2_BYTE_1	7:0	RW	0	PID byte 1 to be inserted in the video stream CH0A DS2.
0047 [3]	PID_INS_CH0A_ DS2_BYTE_34	PID_INS_CH0A_ DS2_BYTE_4	15:8	RW	0	PID byte 4 to be inserted in the video stream CH0A DS2.
		PID_INS_CH0A_ DS2_BYTE_3	7:0	RW	0	PID byte 3 to be inserted in the video stream CH0A DS2.
0048 [1]	PID_INS_CH0B_ DS1_BYTE_12	PID_INS_CH0B_ DS1_BYTE_2	15:8	RW	0	PID byte 2 to be inserted in the video stream CH0B DS1.
		PID_INS_CH0B_ DS1_BYTE_1	7:0	RW	0	PID byte 1 to be inserted in the video stream CH0B DS1.
0049 [1]	PID_INS_CH0B_ DS1_BYTE_34	PID_INS_CH0B_ DS1_BYTE_4	15:8	RW	0	PID byte 4 to be inserted in the video stream CH0B DS1.

Semtech Confidential Information
Kent Lin
DIVA Laboratories, Ltd.
09/08/2026

		PID_INS_CH0B_DS1_BYTE_3	7:0	RW	0	PID byte 3 to be inserted in the video stream CH0B DS1.
004A [1]	PID_INS_CH0B_DS2_BYTE_12	PID_INS_CH0B_DS2_BYTE_2	15:8	RW	0	PID byte 2 to be inserted in the video stream CH0B DS2.
		PID_INS_CH0B_DS2_BYTE_1	7:0	RW	0	PID byte 1 to be inserted in the video stream CH0B DS2.
004B [1]	PID_INS_CH0B_DS2_BYTE_34	PID_INS_CH0B_DS2_BYTE_4	15:8	RW	0	PID byte 4 to be inserted in the video stream CH0B DS2.
		PID_INS_CH0B_DS2_BYTE_3	7:0	RW	0	PID byte 3 to be inserted in the video stream CH0B DS2.
004C [1]	PID_INS_CH1A_DS1_BYTE_12	PID_INS_CH1A_DS1_BYTE_2	15:8	RW	0	PID byte 2 to be inserted in the video stream CH1A DS1.
		PID_INS_CH1A_DS1_BYTE_1	7:0	RW	0	PID byte 1 to be inserted in the video stream CH1A DS1.
004D [1]	PID_INS_CH1A_DS1_BYTE_34	PID_INS_CH1A_DS1_BYTE_4	15:8	RW	0	PID byte 4 to be inserted in the video stream CH1A DS1.
		PID_INS_CH1A_DS1_BYTE_3	7:0	RW	0	PID byte 3 to be inserted in the video stream CH1A DS1.
004E [1]	PID_INS_CH1A_DS2_BYTE_12	PID_INS_CH1A_DS2_BYTE_2	15:8	RW	0	PID byte 2 to be inserted in the video stream CH1A DS2.
		PID_INS_CH1A_DS2_BYTE_1	7:0	RW	0	PID byte 1 to be inserted in the video stream CH1A DS2.
004F [1]	PID_INS_CH1A_DS2_BYTE_34	PID_INS_CH1A_DS2_BYTE_4	15:8	RW	0	PID byte 4 to be inserted in the video stream CH1A DS2.
		PID_INS_CH1A_DS2_BYTE_3	7:0	RW	0	PID byte 3 to be inserted in the video stream CH1A DS2.
0050	PID_INS_CH1B_DS1_BYTE_12	PID_INS_CH1B_DS1_BYTE_2	15:8	RW	0	PID byte 2 to be inserted in the video stream CH1B DS1.
		PID_INS_CH1B_DS1_BYTE_1	7:0	RW	0	PID byte 1 to be inserted in the video stream CH1B DS1.

Semtech Confidential Information
Kent Lin
DIVA Laboratories Ltd.
09/08/2026

0051 [1]	PID_INS_CH1B_ DS1_BYTE_34	PID_INS_CH1B_ DS1_BYTE_4	15:8	RW	0	PID byte 4 to be inserted in the video stream CH1B DS1.
		PID_INS_CH1B_ DS1_BYTE_3	7:0	RW	0	PID byte 3 to be inserted in the video stream CH1B DS1.
0052 [1]	PID_INS_CH1B_ DS2_BYTE_12	PID_INS_CH1B_ DS2_BYTE_2	15:8	RW	0	PID byte 2 to be inserted in the video stream CH1B DS2.
		PID_INS_CH1B_ DS2_BYTE_1	7:0	RW	0	PID byte 1 to be inserted in the video stream CH1B DS2.
0053 [1]	PID_INS_CH1B_ DS2_BYTE_34	PID_INS_CH1B_ DS2_BYTE_4	15:8	RW	0	PID byte 4 to be inserted in the video stream CH1B DS2.
		PID_INS_CH1B_ DS2_BYTE_3	7:0	RW	0	PID byte 3 to be inserted in the video stream CH1B DS2.
0054 [1]	PID_INS_CH2A_ DS1_BYTE_12	PID_INS_CH2A_ DS1_BYTE_2	15:8	RW	0	PID byte 2 to be inserted in the video stream CH2A DS1.
		PID_INS_CH2A_ DS1_BYTE_1	7:0	RW	0	PID byte 1 to be inserted in the video stream CH2A DS1.
0055 [1]	PID_INS_CH2A_ DS1_BYTE_34	PID_INS_CH2A_ DS1_BYTE_4	15:8	RW	0	PID byte 4 to be inserted in the video stream CH2A DS1.
		PID_INS_CH2A_ DS1_BYTE_3	7:0	RW	0	PID byte 3 to be inserted in the video stream CH2A DS1.
0056 [1]	PID_INS_CH2A_ DS2_BYTE_12	PID_INS_CH2A_ DS2_BYTE_2	15:8	RW	0	PID byte 2 to be inserted in the video stream CH2A DS2.
		PID_INS_CH2A_ DS2_BYTE_1	7:0	RW	0	PID byte 1 to be inserted in the video stream CH2A DS2.
0057 [1]	PID_INS_CH2A_ DS2_BYTE_34	PID_INS_CH2A_ DS2_BYTE_4	15:8	RW	0	PID byte 4 to be inserted in the video stream CH2A DS2.
		PID_INS_CH2A_ DS2_BYTE_3	7:0	RW	0	PID byte 3 to be inserted in the video stream CH2A DS2.
0058 [1]	PID_INS_CH2B_ DS1_BYTE_12	PID_INS_CH2B_ DS1_BYTE_2	15:8	RW	0	PID byte 2 to be inserted in the video stream CH2B DS1.

Semtech Confidential Information
Kent Lin
DIVA Laboratories Ltd.
09/08/2026

		PID_INS_CH2B_DS1_BYTE_1	7:0	RW	0	PID byte 1 to be inserted in the video stream CH2B DS1.
0059 [1]	PID_INS_CH2B_DS1_BYTE_34	PID_INS_CH2B_DS1_BYTE_4	15:8	RW	0	PID byte 4 to be inserted in the video stream CH2B DS1.
		PID_INS_CH2B_DS1_BYTE_3	7:0	RW	0	PID byte 3 to be inserted in the video stream CH2B DS1.
005A [1]	PID_INS_CH2B_DS2_BYTE_12	PID_INS_CH2B_DS2_BYTE_2	15:8	RW	0	PID byte 2 to be inserted in the video stream CH2B DS2.
		PID_INS_CH2B_DS2_BYTE_1	7:0	RW	0	PID byte 1 to be inserted in the video stream CH2B DS2.
005B [1]	PID_INS_CH2B_DS2_BYTE_34	PID_INS_CH2B_DS2_BYTE_4	15:8	RW	0	PID byte 4 to be inserted in the video stream CH2B DS2.
		PID_INS_CH2B_DS2_BYTE_3	7:0	RW	0	PID byte 3 to be inserted in the video stream CH2B DS2.
005C [1]	PID_INS_CH3A_DS1_BYTE_12	PID_INS_CH3A_DS1_BYTE_2	15:8	RW	0	PID byte 2 to be inserted in the video stream CH3A DS1.
		PID_INS_CH3A_DS1_BYTE_1	7:0	RW	0	PID byte 1 to be inserted in the video stream CH3A DS1.
005D [1]	PID_INS_CH3A_DS1_BYTE_34	PID_INS_CH3A_DS1_BYTE_4	15:8	RW	0	PID byte 4 to be inserted in the video stream CH3A DS1.
		PID_INS_CH3A_DS1_BYTE_3	7:0	RW	0	PID byte 3 to be inserted in the video stream CH3A DS1.
005E [1]	PID_INS_CH3A_DS2_BYTE_12	PID_INS_CH3A_DS2_BYTE_2	15:8	RW	0	PID byte 2 to be inserted in the video stream CH3A DS2.
		PID_INS_CH3A_DS2_BYTE_1	7:0	RW	0	PID byte 1 to be inserted in the video stream CH3A DS2.
005F [1]	PID_INS_CH3A_DS2_BYTE_34	PID_INS_CH3A_DS2_BYTE_4	15:8	RW	0	PID byte 4 to be inserted in the video stream CH3A DS2.
		PID_INS_CH3A_DS2_BYTE_3	7:0	RW	0	PID byte 3 to be inserted in the video stream CH3A DS2.

Semtech Confidential Information
Kent Lin
DIVA Laboratories Ltd.
09/08/2026

0060 [1]	PID_INS_CH3B_ DS1_BYTE_12	PID_INS_CH3B_ DS1_BYTE_2	15:8	RW	0	PID byte 2 to be inserted in the video stream CH3B DS1.
		PID_INS_CH3B_ DS1_BYTE_1	7:0	RW	0	PID byte 1 to be inserted in the video stream CH3B DS1.
0061 [1]	PID_INS_CH3B_ DS1_BYTE_34	PID_INS_CH3B_ DS1_BYTE_4	15:8	RW	0	PID byte 4 to be inserted in the video stream CH3B DS1.
		PID_INS_CH3B_ DS1_BYTE_3	7:0	RW	0	PID byte 3 to be inserted in the video stream CH3B DS1.
0062 [1]	PID_INS_CH3B_ DS2_BYTE_12	PID_INS_CH3B_ DS2_BYTE_2	15:8	RW	0	PID byte 2 to be inserted in the video stream CH3B DS2.
		PID_INS_CH3B_ DS2_BYTE_1	7:0	RW	0	PID byte 1 to be inserted in the video stream CH3B DS2.
0063 [1]	PID_INS_CH3B_ DS2_BYTE_3_4	PID_INS_CH3B_ DS2_BYTE_4	15:8	RW	0	PID byte 4 to be inserted in the video stream CH3B DS2.
		PID_INS_CH3B_ DS2_BYTE_3	7:0	RW	0	PID byte 3 to be inserted in the video stream CH3B DS2.
0064 [3]	VI_ASGMT_0	RSVD	15:14	RO	0	Reserved.
		VI1_CH1_SEL	13:13	RW	1	Select the input channel for the virtual output stream 1, VI1. Refer to output link assignment **Error! Reference source not found.** in data sheet. **Note:** Only in SDI-SDI mode.
		VI1_CH0_SEL	12:12	RW	0	Select the input channel for the virtual output stream 0, VI1. Refer to output link assignment **Error! Reference source not found.** in data sheet. **Note:** Only in SDI-SDI mode.
		VI0_CH3_SEL	11:10	RW	3	Select the input channel for the virtual output stream 3, VI0. Refer to output link assignment **Error! Reference source not found.** in data sheet.

Semtech Confidential Information
Kent Lin
DIVA Laboratories Ltd.
09/08/2026

		VI0_CH2_SEL	9:8	RW	2	Select the input channel for the virtual output stream 2, VI0. Refer to output link assignment **Error! Reference source not found.** in data sheet.
		VI0_CH1_SEL	7:6	RW	1	Select the input channel for the virtual output stream 1, VI0. Refer to output link assignment **Error! Reference source not found.** in data sheet.
		VI0_CH0_SEL	5:4	RW	0	Select the input channel for the virtual output stream 0, VI0. Refer to output link assignment **Error! Reference source not found.** in data sheet.
		MANUAL_CTRL_ LNK_ASGMT	3:3	RW	0	When HIGH, the virtual link assignment is manually selected based on the registers VIx_CHx_SEL.
		RSVD	2:2	RO	0	Reserved.
		REG_CTRL_LNK_ ASGMT_SEL	1:1	RW	0	When HIGH, the value in register LNK_ASGMT_SEL_REG is used instead of the LNK_ASGMT pin setting.
		LNK_ASGMT_ SEL_REG	0:0	RW	0	Overrides LNK_ASGMT pin setting, if REG_CTRL_LNK_ASGMT_SEL is set HIGH.
0065 [3]	DM_DL12_VIR	RSVD	15:8	RO	0	Reserved.
		REG_CTRL_VI_ L1_PAR	7:7	RW	0	When HIGH MSTRAM_SEL and MUX_DL_OUT values are taken from registers instead of the internally set ones.
		VI_L1_MUX_DL_OUT	6:6	RW	1	When in MUX mode selects if the output is dual link i.e. (QL3 ® DL6 or QL6 ® DL12) if REG_CTRL_VI_L1_PAR set HIGH.
		VI_L1_MSTREAM_ SEL	5:4	RW	1	Selects the mapping of the vi_l1 output data streams if REG_CTRL_VI_L1_MSTREAM_SEL set HIGH.
		RSVD	3:3	RO	0	Reserved.

Semtech Confidential Information
Kent Lin
DIVA Laboratories. Ltd.
09/08/2026

		MAN_CTRL_SEL_DM_DL12_VIR	2:2	RW	0	When HIGH, the DL12G stream assignment is manually selected based on the parameter SEL_DM_DL12_VIR.
		SEL_DM_DL12_VIR	1:0	RW	2	Selects between DL12G streams: SEL_DM_DL12_VIR[0] controls DDO0 and DDO1 selection. When '1', DDI0 stream demuxed to DDO0 & DDO1. When '0', DDI2 stream demuxed to DDO0 & DDO1. SEL_DM_DL12_VIR[1] controls DDO2 & DDO3 selection. When '1', DDI0 stream demuxed to DDO2& DDO3. When '0', DDI2 stream demuxed to DDO2 & DDO3.
0066 [1]	LOST_INPUT_IGNORE_CTRL	RSVD	15:9	RO	0	Reserved.
		M1_PRIM_CH	8:8	RW	1	Selects the primary channel for MUX M1.
		RSVD	7:6	RO	0	Reserved.
		M0_PRIM_CH	5:4	RW	0	Selects the primary input for MUX M0. 00 = DDI0 01 = DDI1 10 = DDI2 11 = DDI3
		IGNORE_LOST_INPUT	3:0	RW	E	When the appropriate bit is asserted, the selected input is replaced with the selected primary input. By Default, all non-primary inputs are selected to be replaced. To disable this feature, write '0' all bits. One bit per channel. Bit 3 controls input 3 Bit 2 controls input 2 Bit 1 controls input 1 Bit 0 controls input 0 **Note:** Ignore lost input is disabled when semi-auto mode is selected.
0067	RSVD	RSVD	15:0	RW	1111	Reserved. Do not change.
0068	RSVD	RSVD	15:0	RW	0F00	Reserved. Do not change.

Semtech Confidential Information
Kent Lin
DIVA Laboratories Ltd.
09/08/2026

0069 [1]	TX_REF_CLK_ SEL	RSVD	15:12	RO	0	Reserved.
		TX_REF_CLK_ CTLR	11:8	RW	0	When HIGH, the reference clock is selected from TX<n>_REF_CLK_SEL. One bit per output.
		TX3_REF_CLK_SEL	7:6	RW	0	Selects the reference clock for Tx3 if bit TX_REF_CLK_CTLR[3] set HIGH. 00 = DDI0 extracted clock 01 = DDI1 extracted clock 10 = DDI2 extracted clock 11 = DDI3 extracted clock
		TX2_REF_CLK_SEL	5:4	RW	0	Selects the reference clock for Tx2 if bit TX_REF_CLK_CTLR[2] set HIGH. See TX3_REF_CLK_SEL for selection values.
		TX1_REF_CLK_SEL	3:2	RW	0	Selects the reference clock for Tx1 if bit TX_REF_CLK_CTLR[1] set HIGH. See TX3_REF_CLK_SEL for selection values.
		TX0_REF_CLK_SEL	1:0	RW	0	Selects the reference clock for Tx0 if bit TX_REF_CLK_CTLR[0] set HIGH. See TX3_REF_CLK_SEL for selection values.
006A [1]	TX_ EXTERNAL_REF_ CLK_SEL	TX_REF_CLK_ EN_OVR	15:12	RW	0	Enables override of Tx pi reference clock enable signal. One bit per channel.
		TX_REF_CLK_EN	11:8	RW	F	Enables Tx PI reference clock when corresponding override enable bit TX_REF_CLK_EN_OVR (n) is set to '1'. One bit per channel.
		TX3_EXTREF_ CLK_SEL	7:6	RW	0	Selects between the external clocks for the Tx3 reference clock if TX3_EXT_REF_CLK_EN is set HIGH. 0 = clock from TX_PI_EXT pin 1 = clock from CLK_EXT_PLL diff. pins

Semtech Confidential Information
Kent Lin
DIVAL Laboratories Ltd.
09/08/2026

		TX2_EXTREF_CLK_SEL	5:4	RW	0	Selects between the external clocks for the Tx2 reference clock if TX2_EXT_REF_CLK_EN is set HIGH.
		TX1_EXTREF_CLK_SEL	3:2	RW	0	Selects between the external clocks for the Tx1 reference clock if TX1_EXT_REF_CLK_EN is set HIGH.
		TX0_EXTREF_CLK_SEL	1:0	RW	0	Selects between the external clocks for the Tx0 reference clock if TX0_EXT_REF_CLK_EN is set HIGH.
006B	M_CLK_CTRL	RSVD	15:14	RO	0	Reserved.
		FPLL_M0_CLK_DIV_SEL_OVR	13:13	RW	0	Enables override of M0_CLK divider settings, if set HIGH value from FPLL_M0_CLK_DIV_SEL register is used instead of an internal value.
		FPLL_M0_CLK_DIV_SEL	12:12	RW	0	Selects value of divider for M0_PLL_CLK when FPLL_M0_CLK_DIV_SEL_OVR is set HIGH. 0 = 148.5MHz 1 = 74.25 MHz
		RSVD	11:10	RO	0	Reserved.
		M0_CLK_FROM_PLL_SEL_OVR	9:9			When HIGH enables override of internal selection for the source of M0_CLK.
		M0_CLK_FROM_PLL_SEL	8:8	RW	0	When HIGH selects M0_CLK from the internal PLL if BITM0_CLK_FROM_PLL_SEL_OVR is set HIGH.
		M1_CLK_CTRL_REG	7:7	RW	0	When HIGH internal M1 clock selection and disable signals are overwritten with values from M1_CLK_SEL_REG and M1_CLK_DIS_REG.
		M1_CLK_DIS_REG	6:6	RW	0	When HIGH disables M1 clock if bit M1_CLK_CTRL_REG set HIGH.

Semtech Confidential Information
Kent Lin
DIVA Laboratories, Ltd.
09/08/2026

		M1_CLK_SEL_REG	5:4	RW	0	Selects clock for M1 if bit M1_CLK_CTRL_REG set HIGH. 00 = from Ch0 01 = from Ch1 10 = from Ch2 11 = from Ch3
		M0_CLK_CTRL_REG	3:3	RW	0	When HIGH internal M0 clock selection and disable signals are overwritten with values from M0_CLK_SEL_REG and M0_CLK_DIS_REG.
		M0_CLK_DIS_REG	2:2	RW	0	When HIGH disables M0 clock if bit M0_CLK_CTRL_REG set HIGH.
		M0_CLK_SEL_REG	1:0	RW	0	Selects clock for M0 if bit M0_CLK_CTRL_REG set HIGH. 00 = from Ch0 01 = from Ch1 10 = from Ch2 11 = fromCh3
006C [2]	CH_CLK_DIS	RSVD	15:8	RO	0	Reserved.
		CH_CLK_DIS_ CTRL_REG	7:4	RW	0	When n bit set HIGH internal Ch (n) clock disable signal is overwritten by value from CH_CLK_DIS_REG (n).
		CH_CLK_DIS_REG	3:0	RW	0	When n bit set HIGH disables Ch (n) clock if bit CH_CLK_DIS_CTRL_REG (n) is set HIGH.
006D	TIM_ OUTPUT_ ENABLE	RSVD	15:9	RO	0	Reserved.
		AUDIO_AMCLK_OEN	8:8	RW	0	When AUDIO_CLK_OUT_EN_OVRD is HIGH, enables the AMCLK_OUT output when HIGH; sets it to high-impedance when LOW.
		AUDIO_CLK_OEN	7:7	RW	0	When AUDIO_CLK_OUT_EN_OVRD is HIGH, enables the ACLK_OUT, WCLK_OUT_1 and WCLK_OUT_2 outputs when HIGH; sets them to high-impedance when LOW.

Semtech Confidential Information
Kent Lin
DIVA Laboratories. Ltd.
09/08/2026

		AUDIO_CLK_OUT_EN_OVRD	6:6	RW	0	When HIGH, ACLK_OUT, WCLK_OUT_1, WCLK_OUT_2 and AMCLK output enables are controlled by AUDIO_CLK_OEN CSR and AUDIO_AMCLK_OEN CSR.
		AUDIO_DATA_9TO16_OEN	5:5	RW	0	When AUDIO_DATA_OUT_EN_OVRD is HIGH, enables the AOUT_9_10, AOUT_11_12, AOUT_13_14 and AOUT_15_16 audio outputs when HIGH; puts them in high-impedance when LOW.
		AUDIO_DATA_1TO8_OEN	4:4	RW	0	When AUDIO_DATA_OUT_EN_OVRD is HIGH, enables the AOUT_1_2, AOUT_3_4, AOUT_5_6 and AOUT_7_8 audio outputs when HIGH; puts them in high-impedance when LOW.
		AUDIO_DATA_OUT_EN_OVR	3:3	RW	0	When HIGH, AUDIO_DATA_1TO8_OEN and AUDIO_DATA_9TO16_OEN control the output enables for all of the audio data outputs (AOUT_1_2 through AOUT_15_16).
		CLK_27_OUT_EN	2:2	RW	0	Enables buffer output of the 27MHz ref clk.
		RX_CLK_OEN	1:0	RW	0	Enables extracted clock on the output on pins B14, C14. Bit 1 enables C14 (RX_CLK_1). Bit 0 enables B14 (RX_CLK_0). One bit per pin. Only applicable in SDI-SDI and SDI-HDMI configurations.
006E	STAT_SEL_A	STAT_1_SEL	15:8	RW	1	See **Error! Reference source not found.** for explanation.
		STAT_0_SEL	7:0	RW	0	See **Error! Reference source not found.** for explanation.
006F	STAT_SEL_B	STAT_3_SEL	15:8	RW	3	See **Error! Reference source not found.** for explanation.
		STAT_2_SEL	7:0	RW	2	See **Error! Reference source not found.** for explanation.
0070	STAT_SEL_C	STAT_5_SEL	15:8	RW	1	See **Error! Reference source not found.** for explanation.

Semtech Confidential Information
Kent Lin
DIVA Laboratories. Ltd.
09/08/2026

		STAT_4_SEL	7:0	RW	0	See **Error! Reference source not found.** for explanation.
0071	STAT_SEL_D	STAT_7_SEL	15:8	RW	3	See **Error! Reference source not found.** for explanation.
		STAT_6_SEL	7:0	RW	2	See **Error! Reference source not found.** for explanation.
0072	STAT_OUTPUT_ ENABLE	RSVD	15:8	RO	0	Reserved.
		STAT_EN	7:0	RW	0	When bit<n> HIGH, enables STAT<n> output buffer. One bit per ball.
0073	SEL_CH_ HVF_GPIO	RSVD	15:14	RO	0	Reserved.
		SEL_HVF_OUT_2	13:12	RW	0	See **Error! Reference source not found.** for explanation.
		SEL_HVF_OUT_1	11:10	RW	0	See **Error! Reference source not found.** for explanation.
		SEL_HVF_OUT_0	9:8	RW	0	See **Error! Reference source not found.** for explanation.
		SEL_HVF_IN_3	7:6	RW	0	See **Error! Reference source not found.** for explanation.
		SEL_HVF_IN_2	5:4	RW	0	See **Error! Reference source not found.** for explanation.
		SEL_HVF_IN_1	3:2	RW	0	See **Error! Reference source not found.** for explanation.
		SEL_HVF_IN_0	1:0	RW	0	See **Error! Reference source not found.** for explanation.
0074	PLL_LOCK_ INVERT	RSVD	15:2	RO	0	Reserved.
		PLL_LOCK_ INVERT	1:0	RW	0	bit(0) = EXT_PLL_LOCK_INVERT bit(1) = FPLL_LOCK_GPIO_INVERT
	CRC_DISABLE	RSVD	15:4	RO	0	Reserved.

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09/08/2026

0075 [3]		CRC_DISABLE	3:0	RW	0	bit(0) = CRC_DS_1_2_DISABLE bit(1) = CRC_DS_3_4_DISABLE bit(2) = CRC_DS_5_6_DISABLE bit(3) = CRC_DS_7_8_DISABLE
0076	RSVD	RSVD	15:0	RW	0	Reserved. Do not change.
0077	RESET_CSR_ HDMI	RSVD	15:7	RW	0	Reserved. Do not change.
		RST_CSR_TMDS_ CONN_CLK	6:6	RW	0	Resets HDMI Rx logic on CONN_CLK.
		RST_CSR_ HDMIRX_ATDM_CLK	5:5	RW	0	Resets HDMI Rx logic on ATDM_CLK.
		RST_CSR_ HDMITX_ATDM_CLK	4:4	RW	0	Resets audio block in HDMI Tx.
		RSVD	3:1	RW	0	Reserved. Do not change.
		RST_CSR_HDMITX_ MAPP_CLK	0:0	RW	0	Resets HDMI Tx logic.
0078	RESET_0	RSVD	15:13	RO	0	Reserved.
		RESET_CH_ TO_M_CLK	12:9	RW	0	Resets interlink delay adjustment block. **Note:** For all reset parameters, toggle the parameter HIGH to LOW to perform reset.
		RESET_DEL_ADJ	8:8	RW	0	Resets video processing block. One bit per channel.
		RESET_CH_BLOCK	7:4	RW	0	Resets input block. One bit per input block.
		RESET_IN_BLOCK	3:0	RW	0	Resets input blocks In0-3
0079	RESET_1	RSVD	15:11	RO	0	Reserved.
		RESET_CSR_FPLL2	10:10	RW	0	Resets internal PLL2 block.

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Kent Lin
DIVA Laboratories. Ltd.
09/08/2026

		RESET_CSR_FPLL	9:9	RW	0	Resets internal PLL block.
		RESET_CSR_ HDMI_RX	8:8	RW	0	Resets HDMI Rx block.
		RESET_ CSR_ANC_EXT_RD	7:7	RW	0	Resets ANC extraction block.
		CORE_RESET	6:6	RW	0	Resets entire GS12270 digital core, except the CSRs.
		RESET_M1	5:5	RW	0	Resets MUX M1 and DEMUX DM1 blocks.
		RESET_M0	4:4	RW	0	Resets MUX M0, DEMUX DM0, and programmable delay blocks.
		RESET_CHAN_ ASGMT	3:0	RW	0	Resets crosspoint. One bit per output channel.
007A	RSVD	RSVD	15:0	RW	F	Reserved. Do not change.
007B [2]	V_LOCK_PAR_1	LENGTH_COUNT_6G	15:8	RW	55	Length of the window in which we search for two TRS word for 6G standards.
		LENGTH_COUNT_ 12G	7:0	RW	AA	Length of the window in which we search for two TRS word for 12G standards.
007C [2]	V_LOCK_PAR_2	LENGTH_COUNT_HD	15:8	RW	34	Length of the window in which we search for two TRS word for HDstandards.
		LENGTH_COUNT_3G	7:0	RW	55	Length of the window in which we search for two TRS word for 3G standards.
007D [2]	V_LOCK_PAR_3	RSVD	15:14	RO	0	Reserved.
		TRS_LOCKED_ COUNT_LIM	13:11	RW	3	The consecutive errors till unlocked.
		TRS_SEARCH_ COUNT_LIM	10:8	RW	3	Maximum number of searches.
		LOCKED_ERROR_ TOL	7:5	RW	1	The number of consecutive search windows in which the number of detected TRS is less then TRS_LOCKED_COUNT_LIM.

Semtech Confidential Information
Kent Lin
DIVA Laboratories. Ltd.
09/08/2026

		MAX_SEARCH_ COUNT	4:0	RW	1	Length of the window in which we search for two TRS word for 3G standards. The window is (MAX_SEARCH_COUNT +1)* LENGTH_COUNT_DR.
007E to 0080	RSVD	RSVD	15:0	—	N/A	Reserved.
0081	STANDBY_REG	RSVD	15:2	RO	0	Reserved.
		STANDBY	1:1	RW	0	When STANDBY_REG_PINB is HIGH, puts the device in standby mode when HIGH.
		STANDBY_REG_PINB	0:0	RW	0	Selects the standby input from pin when LOW and from standby CSR when HIGH.
0082 to 008B	RSVD	RSVD	15:0	—	N/A	Reserved. Do not change.
008C [2]	CRC_ERROR_ CH0_COUNTER	RSVD	15:13	RO	0	Reserved.
		CRC_ERROR_ CH0_COUNT_RST	12:12	RW	0	Resets the DDI0 CRC error count.
		CRC_ERROR_ CH0_COUNT	11:0	RO	0	CRC error count at DDI0.
008D [2]	CRC_ERROR_ CH1_COUNTER	RSVD	15:13	RO	0	Reserved.
		CRC_ERROR_ CH1_COUNT_RST	12:12	RW	0	Resets the DDI1 CRC error count.
		CRC_ERROR_ CH1_COUNT	11:0	RO	0	CRC error count at DDI1.
008E [2]	CRC_ERROR_ CH2_COUNTER	RSVD	15:13	RO	0	Reserved.
		CRC_ERROR_ CH2_COUNT_RST	12:12	RW	0	Resets the DDI2 CRC error count.
		CRC_ERROR_ CH2_COUNT	11:0	RO	0	CRC error count at DDI2.
		RSVD	15:13	RO	0	Reserved.

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Kent Lin
DIVA Laboratories, Ltd.
09/08/2026

008F [2]	CRC_ERROR_ CH3_COUNTER	CRC_ERROR_ CH3_COUNT_RST	12:12	RW	0	Resets the DDI3 CRC error count.
		CRC_ERROR_ CH3_COUNT	11:0	RO	0	CRC error count at DDI3.
0090 [2]	CH01_DELAY	CH1_DELAY	15:8	RO	0	Reports the delay added to DDI1 input in order to compensate inter channel skew.
		CH0_DELAY	7:0	RO	0	Reports the delay added to DDI0 input in order to compensate inter channel skew.
0091 [2]	CH23_DELAY	CH3_DELAY	15:8	RO	0	Reports the delay added to DDI3 input in order to compensate inter channel skew.
		CH2_DELAY	7:0	RO	0	Reports the delay added to DDI2 input in order to compensate inter channel skew.
0092 to 0093	RSVD	RSVD	15:0	RW	0	Reserved. Do not change.
0094	SDI_AUDIO_ ENABLE	RSVD	15:8	RO	0	Reserved.
		AUD_INS_2_EN_ GRP2	7:7	RW	0	Set to HIGH to enable the second group in the second SDI audio insertion block.
		AUD_INS_2_EN_ GRP1	6:6	RW	0	Set to HIGH to enable the first group in the second SDI audio insertion block.
		AUD_INS_1_EN_ GRP2	5:5	RW	0	Set to HIGH to enable the second group in the first SDI audio insertion block.
		AUD_INS_1_EN_ GRP1	4:4	RW	0	Set to HIGH to enable the first group in the first SDI audio insertion block.
		AUD_INS_EN_ OVRD_EN	3:3	RW	0	When HIGH, AUD_INS_1_EN_GRP1, AUD_INS_1_EN_GRP2, AUD_INS_2_EN_GRP1 and AUD_INS_2_EN_GRP2 are used to enable the first and second audio insertion cores. When LOW, AUD_INS_1_EN_GRP1 is enabled by default when in HDMI-SDI mode and disabled in all other modes. When LOW, AUD_INS_1_EN_GRP2, AUD_INS_2_EN_GRP1 and AUD_INS_2_EN_GRP2 are disabled.

Semtech Confidential Information
Kent Lin
DIVA Laboratories Ltd.
09/08/2026

		AUD_EXT_2_EN	2:2	RW	0	Set to HIGH to enable the second SDI audio extraction block.
		AUD_EXT_1_EN	1:1	RW	0	Set to HIGH to enable the first SDI audio extraction block.
		AUD_EXT_EN_OVRD_EN	0:0	RW	0	When HIGH, aud_ext_1_en and AUD_EXT_2_EN are used to enable the first and second audio extraction cores. When low, AUD_EXT_1_EN is enabled in SDI-HDMI mode and disabled in all other modes. When low, AUD_EXT_2_EN is disabled in all modes.
0095	SDI_AUD_EXT_SYNC	RSVD	15:1	RO	0	Reserved.
		SYNC_AUDIO_OUTPUTS	0:0	RW	0	Set HIGH to sync the first 8 audio channel outputs with the second 8.
0096	AUD_INS_CONFIG	RSVD	15:12	RO	0	Reserved.
		SDI_AUDIO_SEL_9TO16_1TO8B	11:11	RW	0	When the SDI audio input is set to pins only and the sampling rate is 96kHz or when the SDI audio input is set to a combination of pins and HDMI and the sampling rate is 48kHz; selects the 8 channels of audio to come from pins AIN_1_2 through AIN_7_8 when LOW and pins AIN_9_10 through AIN_15_16 when HIGH.
		AUDIO_SEL_EXT_HDMI_OVRD_EN	10:10	RW	0	When HIGH, uses the AUDIO_SEL_EXT_HDMI CSR instead of the internal value.
		AUDIO_SEL_EXT_HDMI	9:8	RW	1	Select source for SDI audio insertion when AUDIO_SEL_EXT_HDMI_OVRD_EN is HIGH: 00 = All audio to be embedded in SDI comes from pins 01 = Up to 8 channels of audio to be embedded in SDI come from HDMI 10 or 11 = Only for 48kHz mode; up to 8 channels of audio from HDMI and up to 8 channels from pins
		AUD_INS_96KHZ_OVRD_EN	7:7	RW	0	Overrides the internal value for audio sampling frequency when HIGH with the value in AUDIO_INS_96KHZ_OVRD.

Semtech Confidential Information
Kent Lin
DIVA Laboratories, Ltd.
09/08/2026

		AUD_INS_96KHZ_OVRD	6:6	RW	0	When AUDIO_INS_96KHZ_OVRD_EN is HIGH, this signal sets AUDIO_INS_96KHZ as follows: 0 = Incoming audio is 48kHz 1 = Incoming audio is 96kHz
		AUD_INS_2_CH_SEL	5:3	RW	0	Selects stream to insert audio data into for the second SDI audio insertion block.
		AUD_INS_1_CH_SEL	2:0	RW	0	Selects stream to insert audio data into for the first SDI audio insertion block.
0097	AUDIO_EXT_CONFIG	RSVD	15:9	RO	0	Reserved.
		AUDIO_EXT_96KHZ_OVRD_EN	8:8	RW	0	Overrides the internal value for audio sampling frequency when HIGH with the value in AUDIO_EXT_96KHZ_OVRD.
		AUDIO_EXT_96KHZ_OVRD	7:7	RW	0	When AUDIO_EXT_96KHZ_OVRD_EN is HIGH, this signal sets AUDIO_EXT_96KHZ as follows: 0 = Embedded audio is 48kHz 1 = Embedded audio is 96kHz
		SEL_AUD_REF_CLK_2_1B	6:6	RW	0	0 = Use the reference clock from the first SDI SDI audio extraction block. 1 = Use the reference clock from the second SDI audio extraction block.
		AUD_EXT_2_CH_SEL	5:3	RW	0	Selects stream to extract audio data from for the second SDI audio extraction block.
		AUD_EXT_1_CH_SEL	2:0	RW	0	Selects stream to extract audio data from for the first SDI audio extraction block.
0098 [2]	SDI_STR_DELAY_CONF	RSVD	15:5	RO	0	Reserved.
		AUDIO_AND_DELAY_BYPASS	4:4	RW	0	When HIGH, bypasses the audio insertion and delay blocks. When LOW, audio and latency blocks controlled independently with their own enables.

Semtech Confidential Information
Kent Lin
DIVA Laboratories, Ltd.
09/08/2026

		DELAY_DS4_EN	3:3	RW	0	When HIGH, DS4 shall be delayed by the amount in DELAY_DS4. When LOW, delay is set internally to balance delay through audio insertion.
		DELAY_DS3_EN	2:2	RW	0	When HIGH, DS3 shall be delayed by the amount in DELAY_DS3. When LOW, delay is set internally to balance delay through audio insertion.
		DELAY_DS2_EN	1:1	RW	0	When HIGH, DS2 shall be delayed by the amount in DELAY_DS2. When LOW, delay is set internally to balance delay through audio insertion.
		DELAY_DS1_EN	0:0	RW	0	When HIGH, DS1 shall be delayed by the amount in DELAY_DS1. When LOW, delay is set internally to balance delay through audio insertion.
0099	DELAY_ DS1_REG	RSVD	15:12	RO	0	Reserved.
		DELAY_DS1	11:0	RW	0	Number of video pixel clock cycles to delay DS1 up to a maximum of 2060 cycles.
009A	DELAY_ DS2_REG	RSVD	15:12	RO	0	Reserved.
		DELAY_DS2	11:0	RW	0	Number of video pixel clock cycles to delay DS2 up to a maximum of 2060 cycles.
009B	DELAY_ DS3_REG	RSVD	15:12	RO	0	Reserved.
		DELAY_DS3	11:0	RW	0	Number of video pixel clock cycles to delay DS3 up to a maximum of 2060 cycles.
009C	DELAY_ DS4_REG	RSVD	15:12	RO	0	Reserved.
		DELAY_DS4	11:0	RW	0	Number of video pixel clock cycles to delay DS4 up to a maximum of 2060 cycles.
009D	AUD_STATUS	RSVD	15:2	RO	0	Reserved.

Semtech Confidential Information
Kent Lin
DIVA Laboratories. Ltd.
09/08/2026

		AUDIO_INS_ 96KHZ	1:1	RO	0	Reports the audio sampling frequency being used for SDI audio insertion before overrides. 0 = 48kHz 1 = 96kHz
		AUDIO_EXT_ 96KHZ	0:0	RO	0	Reports the audio sampling frequency being used for SDI audio extraction before overrides. 0 = 48kHz 1 = 96kHz
009E	ACG_CTRL	RSVD	15:2	RW	0	Reserved. Do not change.
		AUDIO_ CLK_OUT_SEL	1:0	RW	0	Audio Master Clock (AMCLK) Output Frequency Select: 0 = 128 fs 1 = 256 fs 2 = 512 fs
009F to 00B0	RSVD	RSVD	15:0	—	N/A	Reserved. Do not change.
00B1	AUDIO_DIGITAL_ PLL_LOCK_REG	RSVD	15:1	RO	0	Reserved.
		AUDIO_DIGITAL_ PLL_LOCK	0:0	RO	0	When HIGH, indicates that the SDI AUDIO_DIGITAL_PLL block is locked to the incoming REF_CLK.
00B2	AUDIO_DIGITAL_ PLL_LOCK_ STICKY_REG	RSVD	15:2	RO	0	Reserved.
		AUDIO_DIGITAL_ PLL_UNLOCK_ STICKY	1:1	ROCW	0	When HIGH, indicates that the SDI AUDIO_DIGITAL_PLL lost lock.
		AUDIO_DIGITAL_ PLL_LOCK_STICKY	0:0	ROCW	0	When HIGH, indicates that the SDI AUDIO_DIGITAL_PLL block is locked to the incoming REF_CLK.
00B3 to 00BD	RSVD	RSVD	15:0	—	N/A	Reserved. Do not change.
00BD		RSVD	15:3	RO	0	Reserved.

Semtech Confidential Information
Kent Lin
DIVA Laboratories, Ltd.
09/08/2026

	SDI_VIDEO_ ERROR_STATUS	RASTER_VALID	4:4	ROCW	0	When HIGH, indicates that the raster structure values are valid. Sticky. Clear on write.
		RSVD	3:0	RO	0	Reserved.
00BE	SDI_VIDEO_ STATUS	RSVD	15:9	RO	0	Reserved.
		NUMBER_OF_ SAMPLES	8:6	RO	0	Specifies the number of samples per audio channel per line for SDI audio.
		RATE_DETECT_M	5:5	RO	0	Specifies M value 0 = 1.000 1 = 1.001
		INTERLACED	4:4	RO	0	1 = interlaced 0 = progressive
		FRAMERATE_60_30	3:3	RO	0	When HIGH, indicates that the frame rate is 60Hz, 59.94Hz, 30Hz or 29.97Hz. LOW for all other frame rates.
		MAPPING234_LVLA	2:2	RO	0	When HIGH, indicates that the input is a 3G level A mapping 2, 3 or 4 format.
		V_LOCK	1:1	RO	0	Vertical lock indication.
		H_LOCK	0:0	RO	0	Horizontal lock indication.
00BF	RASTER_ STRUC_1	RSVD	15:11	RO	0	Reserved.
		ACTLINE_PER_ FIELD	10:0	RO	0	Active lines per field for current input on Rx0.
00C0	RASTER_ STRUC_2	RSVD	15:14	RO	0	Reserved.
		WORDS_PER_ LINE	13:0	RO	0	Total number of words per line for current input on Rx0.
00C1	RASTER_ STRUC_3	RSVD	15:11	RO	0	Reserved.
		LINES_PER_ FRAME	10:0	RO	0	Total number of lines per frame for current input on Rx0.

Semtech Confidential Information
Kent Lin
DIVA Laboratories Ltd.
09/08/2026

00C2	RASTER_ STRUC_4	RSVD	15:14	RO	0	Reserved.
		WORDS_PER_ ACTLINE	13:0	RO	0	Words per active line for current input on Rx0.
00C3 to 00D1	RSVD	RSVD	15:0	—	N/A	Reserved. Do not change.
00D2	FPLL_REG_0	RSVD	15:9	RW	8	Reserved. Do not change.
		FPLL_NARROW_ LBW_SEL	8:8	RW	0	Selects narrower LBW for FPLL.
		RSVD	7:7	RO	0	Reserved.
		FPLL_RX_CLK_ SEL_OVR_EN	6:6	RW	0	Enables override of FPLL Rx clock selection.
		FPLL_RX_CLK_ SEL_REG	5:4	RW	0	Select RX clock (Rx0-Rx3) for the FPLL reference when FPLL_RX_CLK_SEL_OVR_EN is set to '1'. 00 = Rx0 01 = Rx1 10 = Rx2 11 = Rx3
		RSVD	3:2	RO	0	Reserved.
		FPLL_REFCLK_ SEL_OVR_EN	1:1	RW	0	Enables override of FPLL reference clock selection.
		FPLL_REFCLK_ SEL_REG	0:0	RW	0	Selects the FPLL reference clock when FPLL_REFCLK_SEL_OVR_EN is set to '1'. 0 = HDMI clock from the dedicated pins 1 = Rx extracted clock (Rx0-Rx3 selectable)
00D3 to 00EA	RSVD	RSVD	15:0	RW	N/A	Reserved. Do not change.
00EB	REF_CLK_MUX_ REG_0	RSVD	15:13	RO	0	Reserved.
		COMPLL_REFCLK_ BUF_EN	12:12	RW	1	Enables internal COM_PLL reference clock buffer.

Semtech Confidential Information
Kent Lin
DIVA Laboratories Ltd.
09/08/2026

		RSVD	11:10	RO	0	Reserved.
		EXT_PLL_REF_OEN	9:9	RW	1	Enables EXT_PLL_REF_CLK, differential output buffer.
		EXT_PLL_REF_ CLK_DIV2_SEL	8:8	RW	0	Enables division by 2 of external PLL reference clock (EXT_PLL_REF_CLK, pins L4&M4).
		RSVD	7:6	RO	0	Reserved.
		COMPLL_PI_ REFCLK_SEL_ OVR_EN	5:5	RW	0	Enables override of COM_PLL clock selection.
		COMPLL_PI_ REFCLK_SEL_REG	4:4	RW	0	TBD.
		RSVD	3:2	RO	0	Reserved.
		EXT_PLL_REF_ SEL_OVR_EN	1:1	RW	0	Enables override of external PLL clock selection.
		EXT_PLL_REF_ SEL_REG	0:0	RW	0	TBD
00EC	PLLS_LOCK_ OVERRIDE	RSVD	15:6	—	1	Reserved. Do not change.
		EXT_PLL_LOCK_OVR	5:5	RW	0	Enables of EXT_FPLL lock override.
		EXT_PLL_LOCK	4:4	RW	1	Used instead of EXT_FPLL lock pin when EXT_FPLL_LOCK_OVR set to 1.
		RSVD	3:0	RW	5	Reserved. Do not change.
00ED to 00F0	RSVD	RSVD	15:0	—	N/A	Reserved. Do not change.
00F1	FVH_IN_SELECT_ STAT_OUT	RSVD	15:2	RO	0	Reserved.
		FVH_IN_STAT_SEL	1:0	RW	0	Selects FVH from different points in the input path. Default is earliest. See **Error! Reference source not found.** for more info.

Semtech Confidential Information
Kent Lin
DIVA Laboratories Ltd.
09/08/2026

00F2	FVH_OUT_SELECT_STAT_OUT	RSVD	15:2	RO	0	Reserved.
		FVH_OUT_STAT_SEL	1:0	RW	0	Selects FVH from different points in the output path. Default is latest. See **Error! Reference source not found.** for more info.
00F3	TCEXT_RESET_REG	RSVD	15:1	RO	0	Reserved.
		TC_EXT_CSR_RESET	0:0	RW	0	CSR reset for the time code extraction logic. Active HIGH.
00F4 [2]	TCEXT_CONFIG_REG	RSVD	15:4	RO	0	Reserved.
		TC_EXT_ENABLE	3:3	RW	1	Enables capture of ATC_HFRTC packets (when frame-synchronized TC_EXT_ENABLE is also HIGH), must be configured while TC_EXT_ENABLE is LOW.
		TC_EXT_LTC_EN	2:2	RW	1	Enables capture of ATC_VITC packets (when frame-synchronized TC_EXT_ENABLE is also HIGH), must be configured while TC_EXT_ENABLE is LOW.
		TC_EXT_VITC_EN	1:1	RW	1	Enables capture of ATC_LTC packets (when frame-synchronized TC_EXT_ENABLE is also HIGH), must be configured while TC_EXT_ENABLE is LOW.
		TC_EXT_HFRTC_EN	0:0	RW	0	Enables time code packet extraction when HIGH, changes take effect at start of vertical blanking of selected data stream.
00F5 [2]	TCEXT_CONFIG2_REG	RSVD	15:13	RO	0	Reserved.
		TC_EXT_FRAME_RATE_OVR_EN	12:12	RW	0	Enables override of frame rate obtained from PID with value in TC_EXT_FRAME_RATE_OVR.
		RSVD	11:10	RO	0	Reserved.

Semtech Confidential Information
Kent Lin
DIVA Laboratories Ltd.
09/08/2026

		TC_EXT_FRAME_RATE_OVR	9:8	RW	2	Override value for frame rate of current video format, used to decode field positions in ATC packets 00 = 24 frames (max frames/super-frames value 23) 01 = 25 frames (max frames/super-frames value 24) 10 = 30 frames (max frames/super-frames value 29) 11 = unused
		RSVD	7:5	RO	0	Reserved.
		TC_EXT_CHK_PARITY	4:4	RW	1	Enables checking for correct parity bits in time code UDW samples.
		RSVD	3:3	RO	0	Reserved.
		TC_EXT_DS_SELECT	2:0	RW	0	Selects data stream for time code extraction. Default selects DS0_IN which is expected to be Y stream of master channel.
00F6 [2]	TCEXT_STATUS_REG	TC_EXT_MISSING_HFRTC_ERR_FLAG	15:15	ROCW	0	Set HIGH at end of a frame/field when, while TC_EXT_ENABLE and TC_EXT_HFRTC_EN are HIGH, ATC_HFRTC packet was not found in the frame/field.
		TC_EXT_MISSING_VITC_ERR_FLAG	14:14	ROCW	0	Set HIGH at end of a frame/field when, while TC_EXT_ENABLE and TC_EXT_VITC_EN are HIGH, ATC_VITC packet was not found in the frame/field.
		TC_EXT_MISSING_LTC_ERR_FLAG	13:13	ROCW	0	Set HIGH at end of frame when, while TC_EXT_ENABLE and TC_EXT_LTC_EN are HIGH, ATC_LTC packet was not found in the frame.
		TC_EXT_MISSING_ERR_FLAG	12:12	ROCW	0	Set HIGH at end of frame when, while TC_EXT_ENABLE is HIGH, none of the expected (ATC_LTC, ATC_VITC1, ATC_VITC2, ATC_HFRTC) packets were found.
		TC_EXT_HFRTC_DATA_ERR_FLAG	11:11	ROCW	0	Sticky flag for TC_EXT_HFRTC_DATA_ERR.

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09/08/2026

		TC_EXT_HFRTC_DATA_ERR	10:10	RO	0	HIGH when parity or checksum errors were detected in last ATC_HFRTC packet.
		TC_EXT_HFRTC_CAPTURED_FLAG	9:9	ROCW	0	Asserted when new ATC_HFRTC packet is captured, cleared on write of 1.
		TC_EXT_HFRTC_PRESENT	8:8	RO	0	HIGH when ATC_HFRTC packed was captured in current or previous frame/field.
		TC_EXT_VITC_DATA_ERR_FLAG	7:7	ROCW	0	Sticky flag for TC_EXT_VITC_DATA_ERR.
		TC_EXT_VITC_DATA_ERR	6:6	RO	0	HIGH when parity or checksum errors were detected in last ATC_VITC# packet.
		TC_EXT_VITC_CAPTURED_FLAG	5:5	ROCW	0	Asserted when new ATC_VITC packet is captured, cleared on write of 1.
		TC_EXT_VITC_PRESENT	4:4	RO	0	HIGH when ATC_VITC# packed was captured in current or previous field.
		TC_EXT_LTC_DATA_ERR_FLAG	3:3	ROCW	0	Sticky flag for TC_EXT_LTC_DATA_ERR.
		TC_EXT_LTC_DATA_ERR	2:2	RO	0	HIGH when parity or checksum errors were detected in last ATC_LTC packet.
		TC_EXT_LTC_CAPTURED_FLAG	1:1	ROCW	0	Asserted when new ATC_LTC packet is captured, cleared on write of 1.
		TC_EXT_LTC_PRESENT	0:0	RO	0	HIGH when ATC_LTC packed was captured in current or previous frame (a frame may span two fields in for ex. interlaced video).
00F7 [2]	TCEXT_LTC_UDW4TO1_REG	TC_EXT_LTC_UDW4	15:12	RO	0	Extracted User Data Word 4 time code field (4 bits per ANC User Data Word) for last ATC_LTC packet.
		TC_EXT_LTC_UDW3	11:8	RO	0	Extracted User Data Word 3 time code field (4 bits per ANC User Data Word) for last ATC_LTC packet.
		TC_EXT_LTC_UDW2	7:4	RO	0	Extracted User Data Word 2 time code field (4 bits per ANC User Data Word) for last ATC_LTC packet.

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DIVA Laboratories Ltd.
09/08/2026

		TC_EXT_LTC_UDW1	3:0	RO	0	Extracted User Data Word 1 time code field (4 bits per ANC User Data Word) for last ATC_LTC packet.
00F8 [2]	TCEXT_LTC_ UDW8TO5_REG	TC_EXT_LTC_UDW8	15:12	RO	0	Extracted User Data Word 8 time code field (4 bits per ANC User Data Word) for last ATC_LTC packet.
		TC_EXT_LTC_UDW7	11:8	RO	0	Extracted User Data Word 7 time code field (4 bits per ANC User Data Word) for last ATC_LTC packet.
		TC_EXT_LTC_UDW6	7:4	RO	0	Extracted User Data Word 6 time code field (4 bits per ANC User Data Word) for last ATC_LTC packet.
		TC_EXT_LTC_UDW5	3:0	RO	0	Extracted User Data Word 5 time code field (4 bits per ANC User Data Word) for last ATC_LTC packet.
00F9 [2]	TCEXT_LTC_ UDW12TO9_REG	TC_EXT_ LTC_UDW12	15:12	RO	0	Extracted User Data Word 12 time code field (4 bits per ANC User Data Word) for last ATC_LTC packet.
		TC_EXT_ LTC_UDW11	11:8	RO	0	Extracted User Data Word 11 time code field (4 bits per ANC User Data Word) for last ATC_LTC packet.
		TC_EXT_ LTC_UDW10	7:4	RO	0	Extracted User Data Word 10 time code field (4 bits per ANC User Data Word) for last ATC_LTC packet.
		TC_EXT_LTC_UDW9	3:0	RO	0	Extracted User Data Word 9 time code field (4 bits per ANC User Data Word) for last ATC_LTC packet.
00FA [2]	TCEXT_LTC_ UDW16TO13_REG	TC_EXT_ LTC_UDW16	15:12	RO	0	Extracted User Data Word 16 time code field (4 bits per ANC User Data Word) for last ATC_LTC packet.
		TC_EXT_ LTC_UDW15	11:8	RO	0	Extracted User Data Word 15 time code field (4 bits per ANC User Data Word) for last ATC_LTC packet.

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DIVA Laboratories, Ltd.
09/08/2026

		TC_EXT_ LTC_UDW14	7:4	RO	0	Extracted User Data Word 14 time code field (4 bits per ANC User Data Word) for last ATC_LTC packet.
		TC_EXT_ LTC_UDW13	3:0	RO	0	Extracted User Data Word 13 time code field (4 bits per ANC User Data Word) for last ATC_LTC packet.
00FB [2]	TCEXT_LTC_DBB_REG	TC_EXT_LTC_DBB2	15:8	RO	0	DBB2 byte extracted from last ATC_LTC packet. **Note**: DBB1= 00_h for ATC_LTC (this is positioned so that the register can be assumed to contain DBB2 and DBB1 for a total of 16 bits).
		RSVD	7:0	RO	0	Reserved.
00FC [2]	TCEXT_VITC_ UDW4TO1_REG	TC_EXT_ VITC_UDW4	15:12	RO	0	Extracted User Data Word 4 time code field (4 bits per ANC User Data Word) for last ATC_VITC1 or ATC_VITC2 packet.
		TC_EXT_ VITC_UDW3	11:8	RO	0	Extracted User Data Word 3 time code field (4 bits per ANC User Data Word) for last ATC_VITC1 or ATC_VITC2 packet.
		TC_EXT_ VITC_UDW2	7:4	RO	0	Extracted User Data Word 2 time code field (4 bits per ANC User Data Word) for last ATC_VITC1 or ATC_VITC2 packet.
		TC_EXT_ VITC_UDW1	3:0	RO	0	Extracted User Data Word 1 time code field (4 bits per ANC User Data Word) for last ATC_VITC1 or ATC_VITC2 packet.
00FD [2]	TCEXT_VITC_ UDW8TO5_REG	TC_EXT_ VITC_UDW8	15:12	RO	0	Extracted User Data Word 8 time code field (4 bits per ANC User Data Word) for last ATC_VITC1 or ATC_VITC2 packet.
		TC_EXT_ VITC_UDW7	11:8	RO	0	Extracted User Data Word 7 time code field (4 bits per ANC User Data Word) for last ATC_VITC1 or ATC_VITC2 packet.
		TC_EXT_ VITC_UDW6	7:4	RO	0	Extracted User Data Word 6 time code field (4 bits per ANC User Data Word) for last ATC_VITC1 or ATC_VITC2 packet.

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09/08/2026

		TC_EXT_ VITC_UDW5	3:0	RO	0	Extracted User Data Word 5 time code field (4 bits per ANC User Data Word) for last ATC_VITC1 or ATC_VITC2 packet.
00FE [2]	TCEXT_VITC_ UDW12TO9_REG	TC_EXT_ VITC_UDW12	15:12	RO	0	Extracted User Data Word 12 time code field (4 bits per ANC User Data Word) for last ATC_VITC1 or ATC_VITC2 packet.
		TC_EXT_ VITC_UDW11	11:8	RO	0	Extracted User Data Word 11 time code field (4 bits per ANC User Data Word) for last ATC_VITC1 or ATC_VITC2 packet.
		TC_EXT_ VITC_UDW10	7:4	RO	0	Extracted User Data Word 10 time code field (4 bits per ANC User Data Word) for last ATC_VITC1 or ATC_VITC2 packet.
		TC_EXT_ VITC_UDW9	3:0	RO	0	Extracted User Data Word 9 time code field (4 bits per ANC User Data Word) for last ATC_VITC1 or ATC_VITC2 packet.
00FF [2]	TCEXT_VITC_ UDW16TO13_REG	TC_EXT_ VITC_UDW16	15:12	RO	0	Extracted User Data Word 16 time code field (4 bits per ANC User Data Word) for last ATC_VITC1 or ATC_VITC2 packet.
		TC_EXT_ VITC_UDW15	11:8	RO	0	Extracted User Data Word 15 time code field (4 bits per ANC User Data Word) for last ATC_VITC1 or ATC_VITC2 packet.
		TC_EXT_ VITC_UDW14	7:4	RO	0	Extracted User Data Word 14 time code field (4 bits per ANC User Data Word) for last ATC_VITC1 or ATC_VITC2 packet.
		TC_EXT_ VITC_UDW13	3:0	RO	0	Extracted User Data Word 13 time code field (4 bits per ANC User Data Word) for last ATC_VITC1 or ATC_VITC2 packet.
0100 [2]	TCEXT_VITC_DBB_ REG	TC_EXT_VITC_DBB2	15:8	RO	0	DBB2 byte extracted from last ATC_VITC1 or ATC_VITC2 packet (this is positioned so that the register can be assumed to contain DBB2 and DBB1 for a total of 16 bits).
		RSVD	7:2	RO	0	Reserved.

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09/08/2026

		TC_EXT_VITC_DBB1_2LSBS	1:0	RO	0	Two LSBs of DBB1 byte extracted from last ATC_VITC1 or ATC_VITC2 packet. **Note**: this is to distinguish between ATC_VITC1 and ATC_VITC2. DBB1 values are: 01_h – ATC_VITC1 => TC_EXT_VITC_DBB1_2LSBS[1:0] = 01_b 02_h – ATC_VITC2 => TC_EXT_VITC_DBB1_2LSBS[1:0] = 10_b
0101 [2]	TCEXT_HFRTC_UDW4TO1_REG	TC_EXT_HFRTC_UDW4	15:12	RO	0	Extracted User Data Word 4 time code field (4 bits per ANC User Data Word) for last ATC_HFRTC packet.
		TC_EXT_HFRTC_UDW3	11:8	RO	0	Extracted User Data Word 3 time code field (4 bits per ANC User Data Word) for last ATC_HFRTC packet.
		TC_EXT_HFRTC_UDW2	7:4	RO	0	Extracted User Data Word 2 time code field (4 bits per ANC User Data Word) for last ATC_HFRTC packet.
		TC_EXT_HFRTC_UDW1	3:0	RO	0	Extracted User Data Word 1 time code field (4 bits per ANC User Data Word) for last ATC_HFRTC packet.
0102 [2]	TCEXT_HFRTC_UDW8TO5_REG	TC_EXT_HFRTC_UDW8	15:12	RO	0	Extracted User Data Word 8 time code field (4 bits per ANC User Data Word) for last ATC_HFRTC packet.
		TC_EXT_HFRTC_UDW7	11:8	RO	0	Extracted User Data Word 7 time code field (4 bits per ANC User Data Word) for last ATC_HFRTC packet.
		TC_EXT_HFRTC_UDW6	7:4	RO	0	Extracted User Data Word 6 time code field (4 bits per ANC User Data Word) for last ATC_HFRTC packet.
		TC_EXT_HFRTC_UDW5	3:0	RO	0	Extracted User Data Word 5 time code field (4 bits per ANC User Data Word) for last ATC_HFRTC packet.
0103 [2]	TCEXT_HFRTC_UDW12TO9_REG	TC_EXT_HFRTC_UDW12	15:12	RO	0	Extracted User Data Word 12 time code field (4 bits per ANC User Data Word) for last ATC_HFRTC packet.

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DIVA Laboratories. Ltd.
09/08/2026

		TC_EXT_ HFRTC_UDW11	11:8	RO	0	Extracted User Data Word11 time code field (4 bits per ANC User Data Word) for last ATC_HFRTC packet.
		TC_EXT_ HFRTC_UDW10	7:4	RO	0	Extracted User Data Word 10 time code field (4 bits per ANC User Data Word) for last ATC_HFRTC packet.
		TC_EXT_ HFRTC_UDW9	3:0	RO	0	Extracted User Data Word 9 time code field (4 bits per ANC User Data Word) for last ATC_HFRTC packet.
0104 [2]	TCEXT_HFRTC_ UDW16TO13_REG	TC_EXT_ HFRTC_UDW16	15:12	RO	0	Extracted User Data Word 16 time code field (4 bits per ANC User Data Word) for last ATC_HFRTC packet.
		TC_EXT_ HFRTC_UDW15	11:8	RO	0	Extracted User Data Word 15 time code field (4 bits per ANC User Data Word) for last ATC_HFRTC packet.
		TC_EXT_ HFRTC_UDW14	7:4	RO	0	Extracted User Data Word 14 time code field (4 bits per ANC User Data Word) for last ATC_HFRTC packet.
		TC_EXT_ HFRTC_UDW13	3:0	RO	0	Extracted User Data Word 13 time code field (4 bits per ANC User Data Word) for last ATC_HFRTC packet.
0105 [2]	TCEXT_HFRTC_ DBB_REG	TC_EXT_ HFRTC_DBB1	15:8	RO	0	DBB1 byte extracted from last ATC_HFRTC packet.
		TC_EXT_ HFRTC_DBB2	7:0	RO	0	DBB2 byte extracted from last ATC_HFRTC packet.
0106 [2]	TCEXT_LTC_HH_ MM_REG	RSVD	15:14	RO	0	Reserved.
		TC_EXT_LTC_HH	13:8	RO	0	LTC packet field: HH - hours in Binary Coded Decimal format, 2 bits of 'tens' and 4 bits for 'units'.
		RSVD	7:7	RO	0	Reserved.
		TC_EXT_LTC_MM	6:0	RO	0	LTC packet field: MM - minutes in Binary Coded Decimal format, 3 bits of 'tens' and 4 bits for 'units'.

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DIVA Laboratories, Ltd.
09/08/2026

0107 [2]	TCEXT_LTC_SS_ FF_REG	RSVD	15:15	RO	0	Reserved.
		TC_EXT_LTC_SS	14:8	RO	0	LTC packet field: FF - frames in Binary Coded Decimal format, 2 bits of 'tens' and 4 bits for 'units'.
		RSVD	7:6	RO	0	Reserved.
		TC_EXT_LTC_FF	5:0	RO	0	LTC packet field: SS - seconds in Binary Coded Decimal format, 3 bits of 'tens' and 4 bits for 'units'.
0108 [2]	TCEXT_LTC_ FLAGS	RSVD	15:15	RO	0	Reserved.
		TC_EXT_LTC_BGF	14:12	RO	0	LTC packet field: binary groups flag.
		RSVD	11:9	RO	0	Reserved.
		TC_EXT_LTC_ BI_POL_CORR_FLAG	8:8	RO	0	LTC packet field: biphase polarity correction flag.
		RSVD	7:5	RO	0	Reserved.
		TC_EXT_LTC_ COLOR_FRAME_ FLAG	4:4	RO	0	LTC packet field: colour frame flag.
		RSVD	3:1	RO	0	Reserved.
		TC_EXT_LTC_DROP_ FRAME_FLAG	0:0	RO	0	LTC packet field: drop frame flag.
0109 [2]	TCEXT_VITC_HH_ MM_REG	RSVD	15:14	RO	0	Reserved.
		TC_EXT_VITC_HH	13:8	RO	0	VITC packet field: HH - hours in Binary Coded Decimal format, 2 bits of 'tens' and 4 bits for 'units'.
		RSVD	7:7	RO	0	Reserved.
		TC_EXT_VITC_MM	6:0	RO	0	VITC packet field: MM - minutes in Binary Coded Decimal format, 3 bits of 'tens' and 4 bits for 'units'.

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DIVA Laboratories, Ltd.
09/08/2026

010A [2]	TCEXT_VITC_ SS_FF_REG	RSVD	15:15	RO	0	Reserved.
		TC_EXT_VITC_SS	14:8	RO	0	VITC packet field: FF - frames in Binary Coded Decimal format, 2 bits of 'tens' and 4 bits for 'units'.
		RSVD	7:6	RO	0	Reserved.
		TC_EXT_VITC_FF	5:0	RO	0	VITC packet field: SS - seconds in Binary Coded Decimal format, 3 bits of 'tens' and 4 bits for 'units'.
010B [2]	TCEXT_VITC_ FLAGS	RSVD	15:15	RO	0	Reserved.
		TC_EXT_VITC_BGF	14:12	RO	0	VITC packet field: binary groups flag.
		RSVD	11:9	RO	0	Reserved.
		TC_EXT_VITC_ FIELD_FLAG	8:8	RO	0	VITC packet field: field identification flag.
		RSVD	7:5	RO	0	Reserved.
		TC_EXT_VITC_ COLOR_FRAME_ FLAG	4:4	RO	0	VITC packet field: colour frame flag.
		RSVD	3:1	RO	0	Reserved.
		TC_EXT_VITC_ DROP_FRAME_FLAG	0:0	RO	0	VITC packet field: drop frame flag.
010C [2]	TCEXT_HFRTC_ HH_MM_REG	RSVD	15:14	RO	0	Reserved.
		TC_EXT_HFRTC_MM	13:8	RO	0	HFRTC packet field: HH - hours in Binary Coded Decimal format, 2 bits of 'tens' and 4 bits for 'units'.
		RSVD	7:7	RO	0	Reserved.
		TC_EXT_HFRTC_HH	6:0	RO	0	HFRTC packet field: MM - minutes in Binary Coded Decimal format, 3 bits of 'tens' and 4 bits for 'units'.

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DIVA Laboratories, Ltd.
09/08/2026

010D [2]	TCEXT_HFRTC_ SS_FF_REG	RSVD	15:15	RO	0	Reserved.
		TC_EXT_HFRTC_SS	14:8	RO	0	HFRTC packet field: SS- hours in Binary Coded Decimal format, 2 bits of 'tens' and 4 bits for 'units'.
		RSVD	7:6	RO	0	Reserved.
		TC_EXT_HFRTC_FF	5:0	RO	0	HFRTC packet field: FF- minutes in Binary Coded Decimal format, 3 bits of 'tens' and 4 bits for 'units'.
010E [2]	TCEXT_HFRTC_ SUBF_REG	RSVD	15:11	RO	0	Reserved.
		TC_EXT_HFRTC_ SUBF	10:8	RO	0	HFRTC packet field: sub-frame - interpreted sub-frame count.
		RSVD	7:5	RO	0	Reserved.
		TC_EXT_HFRTC_ SUBF_BITS	4:0	RO	0	HFRTC packet field: raw sub-frame bits “SUB-FRAME_5” down to “SUB-FRAME_1”.
010F [2]	TCEXT_HFRTC_ FLAGS_REG	RSVD	15:15	RO	0	Reserved.
		TC_EXT_HFRTC_ SUBFRAMES	14:12	RO	0	HFRTC packet field: subframes, extracted from DBB2.
		RSVD	11:10	RO	0	Reserved.
		TC_EXT_HFRTC_ FRAMES	9:8	RO	0	HFRTC packet field: frames, extracted from DBB2.
		TC_EXT_HFRTC_ BITSTREAM_ NUMBER	7:4	RO	0	HFRTC packet field: bit-stream number, extracted from DBB1.
		RSVD	3:1	RO	0	Reserved.
		TC_EXT_HFRTC_ DROP_FRAME_FLAG	0:0	RO	0	HFRTC packet field: drop frame flag.
	TCINS_EN_REG	RSVD	15:1	RO	0	Reserved.

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09/08/2026

0110 [3]		TC_INS_EN	0:0	RW	0	When asserted (HIGH) time code insertion is enabled. When de-asserted no data is inserted. Takes effect on frame boundary. All configuration parameters must be modified with TC_INS_EN LOW.
0111 [3]	TCINS_CONFIG_ REG	RSVD	15:13	RO	0	Reserved.
		TC_INS_FLAG_ COLORFRAME	12:12	RW	0	Value to insert as colourframe flag. For digital TC should always be 0. Providing for flexibility.
		TC_INS_ REPLACE_DELETED	11:11	RW	1	Enables Time Code insertion by replacing, in selected line and region, of ANC packets marked deleted when they match size. Note: this facilitates replacing deleted ATC packets.
		TC_INS_CRC_INS_EN	10:10	RW	0	Enables recalculation of per-line CRC checksum. Only needed (and recommend) enabled when inserting in VANC region.
		TC_INS_ANC_ REGION	9:9	RW	0	Selects whether Time Code packet is inserted into the HANC region (0) or the VANC region (1). HANC region is recommended for LTC and VITC Time Code packets. VANC should be used for HFRTC packets.
		TC_INS_ATC_TYPE	8:7	RW	3	Selects the ATC time code packet type: 0 = ATC_LTC 1 = ATC_VITC1/2 2 = ATC_HFRTC 3 = Auto select between ATC_VITC and ATC_HFRTC
		TC_INS_FVH_SEL	6:5	RW	0	F, V, H selection. The block will then use the selected set of F, V and H to figure out HANC and VANC regions of the video signal. 00 = F1_I, V1_I, H1_I will be selected. 00 = F3_I, V3_I, H3_I will be selected. 00 = F5_I, V5_I, H5_I will be selected. 00 = F7_I, V7_I, H7_I will be selected. Must be modified with both TC_INS_EN and TC_INS_TIME_COUNT_EN LOW.

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09/08/2026

		TC_INS_LINE_NUM_EXTR_DS_SEL	4:3	RW	0	Data stream selection. The block will then use the selected data stream to extract the line numbers from: 00 = DS1_I will be selected 01 = DS3_I will be selected 10 = DS5_I will be selected 11 = DS7_I will be selected
		TC_INS_DS_SEL	2:0	RW	0	Data stream selection for time code insertion. 000 = DS1_I will be selected for ANC data insertion. 001 = DS2_I will be selected for ANC data insertion. 010 = DS3_I will be selected for ANC data insertion. 011 = DS4_I will be selected for ANC data insertion. 100 = DS5_I will be selected for ANC data insertion. 101 = DS6_I will be selected for ANC data insertion. 110 = DS7_I will be selected for ANC data insertion. 111 = DS8_I will be selected for ANC data insertion.
0112 [3]	TCINS_AUTO_STAT_REG	RSVD	15:13	RO	0	Reserved.
		TC_INS_DROP_FRAME_EN	13:13	RO	0	Current configuration whether drop frame counting is enabled.
		TC_INS_FRACTIONAL	12:12	RO	0	Current configuration whether frame rate is fractional (1/1.001).
		TC_INS_USE_SUBF_FOR_FIELDFLAG	11:11	RO	0	1 selects sub-frame count bit 0 for field flag in ATC and to select VITC1 vs VITC2 format. When 0, F#_IN field signal input is used. Set to 1 for progressive frame rates >30 up to 60 and whenever 2-frame, frame count increment is required and the F#_IN input will not distinguish the frames.

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DIVA Laboratories. Ltd.
09/08/2026

		TC_INS_SUBFRAMES	10:8	RO	1	For HFRTC indicates the number of subframes to count ('N' value from SMPTE 12-3:2016). For LTC/VITC set to 2 for frame rates over 30 and interlaced/segmented formats, otherwise set to 1. Valid values are 1-5.
		TC_INS_FRAMES	7:6	RO	0	Current frame rate used to insert time code packets, sampled post-override 00 = 24 frames (max frames/super-frames value 23) 01 = 25 frames (max frames/super-frames value 24) 10 = 30 frames (max frames/super-frames value 29) 11 = unused
		TC_INS_ANC_ TYPE_USED	5:4	RO	1	Current ATC time code packet type used by TC Insert block.
		TC_INS_PID_ PICTURE_RATE	3:0	RO	0	Current “Picture Rate” PID field value used for auto-configuration of TC_INSERT block, post overrides. See TC_INS_PID_PICURE_RATE_OVR for encoding.
0113 [3]	TCINS_AUTO_ OVR1_REG	TC_INS_ SUBFRAMES_ OVR_EN	15:15	RW	0	Enables override of 'subframes' auto configured value with TC_INS_SUBFRAMES_OVR (Must be modified with TC_INS_TIME_COUNT_EN LOW).
		TC_INS_ SUBFRAMES_OVR	14:12	RW	0	Override value for 'subframes' configuration of Time Address counter. See TC_INS_SUBFRAMES parameter for details. (Must be modified with TC_INS_TIME_COUNT_EN LOW).
		RSVD	11:11	RO	0	Reserved.
		TC_INS_ FRAMES_OVR_EN	10:10	RW	0	Enables override of 'frames' auto configuration value with TC_INS_FRAMES_OVR. (Must be modified with TC_INS_TIME_COUNT_EN LOW).

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09/03/2026

		TC_INS_ FRAMES_OVR	9:8	RW	0	Override value for 'frames' configuration of Time Address counter, see TC_INS_FRAMES parameter for encoding (Must be modified with TC_INS_TIME_COUNT_EN LOW).
		RSVD	7:5	RO	0	Reserved.
		TC_INS_PID_ PICTURE_RATE_ OVR_EN	4:4	RW	0	Enables override of PID picture rate from Rx system.
		TC_INS_PID_ PICTURE_RATE_OVR	3:0	RW	2	Override value used as PID picture rate (for auto-configuration) when TC_INS_PID_PICTURE_RATE_OVR_EN is HIGH. Encoding per SMPTE-352-2013 and ST2082-10:2015: 4'h2 - 24/1.001 4'h3 - 24 4'h4 - 48/1.001 4'h5 - 25 4'h6 - 30/1.001 4'h7 - 30 4'h8 - 48 4'h9 - 50 4'hA - 60/1.001 4'hB - 60 4'hC - 96 4'hD - 100 4'hE - 120/1.001 4'hF - 120
0114 [3]	TCINS_AUTO_ OVR2_REG	RSVD	15:10	RO	0	Reserved.
		TC_INS_DROP_ FRAME_EN_OVR_EN	9:9	RW	0	Enables override of auto-configured drop frame counting setting with TC_INS_DROP_FRAME_EN_OVR.
		TC_INS_DROP_ FRAME_EN_OVR	8:8	RW	0	Override value used to enable Time Address drop frame counting.
		RSVD	7:6	RO	0	Reserved.
		TC_INS_ FRACTIONAL_ OVR_EN	5:5	RW	0	Enables override of auto-configured fractional frame rate setting with TC_INS_FRACTIONAL_OVR.

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09/08/2026

		TC_INS_ FRACTIONAL_OVR	4:4	RW	0	Override value used to configure fractional (1/1.001) frame rate.
		RSVD	3:2	RO	0	Reserved.
		TC_INS_USE_SUBF_ FOR_FFLAG_ OVR_EN	1:1	RW	0	Enables override of auto-configured 'use subframe for field flag' parameter with TC_INS_USE_SUBF_FOR_FFLAG_OVR.
		TC_INS_USE_SUBF_ FOR_FFLAG_OVR	0:0	RW	0	'Use subframe for field flag' override value, in effect when override enabled.
0115 [3]	TC_INS_FIRST_ LINE_REG	RSVD	15:12	RO	0	Reserved.
		TC_INS_FIRST_ LINE_OVR_EN	11:11	RW	0	When HIGH, TC_INS_FIRST_LINE_OVR[] value is used to determine “first line” for Time Code packet insertion.
		TC_INS_FIRST_ LINE_OVR	10:0	RW	A	Value used to override “first line”, defines the line number used for field 1 Time Code packet insertion.
0116 [3]	TC_INS_SECOND_L INE_REG	RSVD	15:11	RO	0	Reserved.
		TC_INS_SECOND_ LINE_NUMBER	10:0	RW	23B	Defines the line number used for field 2 Time Code packet insertion for interlaced and fragmented video formats. This line is video format dependent and must be programmed for specific video format. Ignored for progressive formats.
0117 [3]	TC_INS_ BITSTREAM_ NUMBER_REG	RSVD	15:4	RO	0	Reserved.
		TC_INS_BITSTREAM_ NUMBER	3:0	RW	0	HFRTC only: Bit-stream number to use in DBB1 LSBs.
0118 [3]	TC_INS_TIME_ COUNT_EN_REG	RSVD	15:1	RO	0	Reserved.
		TC_INS_ TIME_COUNT_EN	0:0	RW	0	Enables Time Address increment starting with next vertical interval.
		RSVD	15:14	RO	0	Reserved.

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Kent Lin
DIVA Laboratories Ltd.
09/03/2026

0119 [3]	TCINS_NEW_ TIME_REG1	TC_INS_NEW_ TIME_HH	13:8	RW	0	New value of the hours component of Time Address (in Binary Coded Decimal format), used for writing and checking Time Address values under TC_INS_TIME_WR_REQ[] parameter's control.
		RSVD	7:7	RO	0	Reserved.
		TC_INS_NEW_ TIME_MM	6:0	RW	0	New value of the minutes component of Time Address (in Binary Coded Decimal format), used for writing and checking Time Address values under TC_INS_TIME_WR_REQ[] parameter's control.
011A [3]	TCINS_NEW_ TIME_REG2	RSVD	15:15	RO	0	Reserved.
		TC_INS_NEW_ TIME_SS	14:8	RW	0	New value of the seconds component of Time Address (in Binary Coded Decimal format), used for writing and checking Time Address values under TC_INS_TIME_WR_REQ[] parameter's control.
		RSVD	7:6	RO	0	Reserved.
		TC_INS_NEW_ TIME_FF	5:0	RW	0	New value of the frames component of Time Address (in Binary Coded Decimal format), used for writing and checking Time Address values under TC_INS_TIME_WR_REQ[] parameter's control.
011B [3]	TCINS_NEW_ TIME_REG3	RSVD	15:3	RO	0	Reserved.
		TC_INS_NEW_ TIME_SUBF	2:0	RW	0	New value of the sub-frame component of Time Address, used for writing and checking Time Address values under TC_INS_TIME_WR_REQ[] parameter's control. For HFR: ({SUB_FRAME_1, SUB_FRAME_2, SUB_FRAME_3} for N=5, else {n/a, SUB_FRAME_1,SUB_FRAME_2}). For progressive rates >30 and <=60, set to 0 or 1 to indicate position within the 2-frame sequence. For interlaced and fragmented must set to 0.

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09/08/2026

011C [3]	TCINS_WR_ REQ_REG	RSVD	15:13	RO	0	Reserved.
		TC_INS_BIN_GRP_ CONT_WR_EN	12:12	RW	0	Enables writing of the binary groups continuously, in every packet inserted, change takes effect on frame/field boundary.
		RSVD	11:9	RO	0	Reserved.
		TC_INS_BIN_ GRP_WR_REQ	8:8	RWPT	0	Writing 1 requests write of provided binary groups and binary group flag bits with next field/frame's time code packet, cleared when complete to provide 'done' status.
		RSVD	7:5	RO	0	Reserved.
		TC_INS_TIME_WR_ IMMEDIATE	4:4	RW	0	When HIGH operations requested by TC_INS_TIME_WR_REQ[] are immediate. When LOW, these operations will take effect on next frame interval, after Time Address increments (if increment enabled).
		RSVD	3:2	RO	0	Reserved.
		TC_INS_ TIME_WR_REQ	1:0	RWPT	0	Request check/write of time code values - bits will be cleared when operation completes: bit 1 = request check of Time Address value, raising TC_INS_NEW_TIME_MISMATCH_ERR_O on mismatch. bit 0 = request write of new Time Address NOTE: multiple bits can be set simultaneously. Example: to write new Time Address value "and" check on write, set bits 2 and 1.
011D [3]	TCINS_BIN_ GRP4321_REG	TC_INS_BIN_GRP4	15:12	RW	0	Value to be inserted into packet's binary group (custom group) 4.
		TC_INS_BIN_GRP3	11:8	RW	0	Value to be inserted into packet's binary group (custom group) 3.
		TC_INS_BIN_GRP2	7:4	RW	0	Value to be inserted into packet's binary group (custom group) 2.

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Kent Lin
DIVA Laboratories. Ltd.
09/08/2026

		TC_INS_BIN_GRP1	3:0	RW	0	Value to be inserted into packet's binary group (custom group) 1.
011E [3]	TCINS_BIN_ GRP8765_REG	TC_INS_BIN_GRP8	15:12	RW	0	Value to be inserted into packet's binary group (custom group) 8.
		TC_INS_BIN_GRP7	11:8	RW	0	Value to be inserted into packet's binary group (custom group) 7.
		TC_INS_BIN_GRP6	7:4	RW	0	Value to be inserted into packet's binary group (custom group) 6.
		TC_INS_BIN_GRP5	3:0	RW	0	Value to be inserted into packet's binary group (custom group) 5.
011F [3]	TCINS_BIN_ BFG_REG	RSVD	15:3	RO	0	Reserved.
		TC_INS_BGF	2:0	RW	0	Value to be inserted into packet's binary group flag bits BGF2. BGF0. Ignored in HFRTC.
0120 [3]	TCINS_ERRORS_ REG	RSVD	15:2	RO	0	Reserved.
		TC_INS_ PACKET_MISSED_ ERR	1:1	ROCW	0	Error raised when the insertion block runs out of ancillary data space and can’t complete insertion of Time Code packet.
		TC_INS_NEW_ TIME_MISMATCH_ ERR	0:0	ROCW	0	Error raised when new Time Address check operation does not match internally sequenced value.
0121 [3]	TCINS_CURRENT_ TIME_REG1	RSVD	15:14	RO	0	Reserved.
		TC_INS_TIME_HH	13:8	RO	0	Current value of the hours component of Time Address.
		RSVD	7:7	RO	0	Reserved.
		TC_INS_TIME_MM	6:0	RO	0	Current value of the minutes component of Time Address.
		RSVD	15:15	RO	0	Reserved.

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DIVA Laboratories. Ltd.
09/08/2026

0122 [3]	TCINS_CURRENT_ TIME_REG2	TC_INS_TIME_SS	14:8	RO	0	Current value of the seconds component of Time Address.
		RSVD	7:6	RO	0	Reserved.
		TC_INS_TIME_FF	5:0	RO	0	Current value of the frames component of Time Address.
0123 [3]	TCINS_CURRENT_ TIME_REG3	RSVD	15:3	RO	0	Reserved.
		TC_INS_TIME_SUBF	2:0	RO	0	Current value of the seconds component of Time Address.
0124 [1]	RX_AUTO_ MODE_1	PID_BYTE1_6G	15:8	RW	C2	Custom 6G PID byte1 for SDI semi-auto mode. It can be adjust to accommodate any future/custom 6G PIDs.
		PID_BYTE1_12G	7:0	RW	CE	Custom 12G PID byte1 for SDI semi-auto mode. It can be adjust to accommodate any future/custom 12G PIDs.
0125 [2]	RX_AUTO_ MODE_2	PID_BYTE1_HD	15:8	RW	85	Custom 1.5G byte1 PID for SDI semi-auto mode. It can be adjust to accommodate any future/custom 1.5G PIDs.
		PID_BYTE1_3G	7:0	RW	89	Custom 3G byte1 PID for SDI semi-auto mode. It can be adjust to accommodate any future/custom 3G PIDs.
0126 [1]	RX_AUTO_ MODE_3	OP_MODE_HD	15:12	RW	0	Gearbox OP mode selected when input PID byte1 matches PID_BYTE1_HD.
		OP_MODE_3G	11:8	RW	0	Gearbox OP mode selected when input PID byte1 matches PID_BYTE1_3G.
		OP_MODE_6G	7:4	RW	0	Gearbox OP mode selected when input PID byte1 matches PID_BYTE1_6G.
		OP_MODE_12G	3:0	RW	7	Gearbox OP mode selected when input PID byte1 matches PID_BYTE1_12G.
0127	RSVD	RSVD	15:0	RO	N/A	Reserved.
		RSVD	15:6	RO	0	Reserved.

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DIVA Laboratories, Ltd.
09/08/2026

0128 [2]	RX_RCLK_ SEL_REG	PORT2_RX_CLK_SEL	5:3	RW	1	Selects the RX_CLK to output on RX_RCLK0 pin as follows: Bit 0 = 1: RX2_DIV2_CLK Bit 0 = 0: Bit 1 = 0: PORT2_RX_RCLK Bit 0 = 0: Bit 1 = 1: Bit 2 = 0: PORT3_RX_RCLK Bit 0 = 0: Bit 1 = 1: Bit 2 = 1: PORT1_RX_RCLK
		PORT0_RX_CLK_SEL	2:0	RW	0	Selects the RX_CLK to output on RX_RCLK0 pin as follows: Bit 0 = 1: RX0_DIV2_CLK Bit 0 = 0: Bit 1 = 0: PORT0_RX_RCLK Bit 0 = 0: Bit 1 = 1: Bit 2 = 0: PORT3_RX_RCLK Bit 0 = 0: Bit 1 = 1: Bit 2 = 1: PORT1_RX_RCLK
0129	VERSION_ID_REG	RSVD	15:8	RO	0	Reserved.
		VERSION_ID	7:0	RO	0	Silicon version identifier. First version is 0.
012A to 012C	RSVD	RSVD	15:0	RW	N/A	Reserved. Do not change.
012D	AUDIO_INS_ BLANK_OVRD_ EN_REG	RSVD	15:1	RO	0	Reserved.
		AUDIO_INS_ BLANK_OVRD_EN	0:0	RW	0	When HIGH, audio insertion block uses AUDIO_INS_Y/C_BLANK_0/1_OVRD_VAL instead of value from BLANK_CODE block.
012E	AUDIO_INS_Y_ BLANK_0_OVRD_V AL_REG	RSVD	15:10	RO	0	Reserved.
		AUDIO_INS_ Y_BLANK_0_OVRD_V AL	9:0	RW	0	Override value for Y_BLANK_0 for audio insertion block to be used when AUDIO_INS_BLANK_OVRD_EN is HIGH.
012F	AUDIO_INS_Y_ BLANK_1_OVRD_V AL_REG	RSVD	15:10	RO	0	Reserved.
		AUDIO_INS_ Y_BLANK_1_OVRD_V AL	9:0	RW	0	Override value for Y_BLANK_1 for audio insertion block to be used when AUDIO_INS_BLANK_OVRD_EN is HIGH.
0130	AUDIO_INS_C_ BLANK_0_OVRD_V AL_REG	RSVD	15:10	RO	0	Reserved.
		AUDIO_INS_ C_BLANK_0_OVRD_V AL	9:0	RW	0	Override value for C_BLANK_0 for audio insertion block to be used when AUDIO_INS_BLANK_OVRD_EN is HIGH.

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DIVA Laboratories, Ltd.
09/08/2026

0131	AUDIO_INS_C_BLANK_1_OVRD_VAL_REG	RSVD	15:10	RO	0	Reserved.
		AUDIO_INS_C_BLANK_1_OVRD_VAL	9:0	RW	0	Override value for C_BLANK_1 for audio insertion block to be used when AUDIO_INS_BLANK_OVRD_EN is HIGH.
0132 to 0135	RSVD	RSVD	15:0	—	N/A	Reserved. Do not change.
0136 [2]	TCEXT_FRAME_RATE_STAT_REG	RSVD	15:2	RO	0	Reserved.
		TC_EXT_FRAME_RATE	1:0	RO	0	The effective frame rate used to parse time code packets, sampled post-override 00 = 24 frames (max frames/super-frames value 23) 01 = 25 frames (max frames/super-frames value 24) 10 = 30 frames (max frames/super-frames value 29) 11 = unused
0137	RSVD	RSVD	15:0	RO	0	Reserved.
0138	ENABLE_FIFO_BASED_RESET	RSVD	15:13	RW	0	Reserved. Do not change.
		SEL_FIFO1_CTRL	12:12	RW	0	Selects a FIFO1 controller.
		RSVD	11:5	RW	0	Reserved. Do not change.
		FIFO_BASED_RESET_EN	4:0	RW	10	Enables FIFO based reset 0:1 Ch0-Ch3; bit 4 M0/PLL.
0139	SEMI_AUTO_MODE_PID_TEST	RSVD	15:9	RO	0	Reserved.
		PID_BYTE1_AUTO_OVR	8:8	RW	0	Enables override of PID detected byte1 used in the auto mode.
		PID_BYTE1_AUTO	7:0	RW	0	Used instead of detected PID byte1 in auto mode when PID_BYTE1_AUTO_OVR is set HIGH.
013A	RSVD	RSVD	15:0	RW	23C	Reserved. Do not change.

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09/08/2026

4.2.2. Rx Control and Status Registers

Table 4-7 Rx Control and Status Registers

1. Can be used only in SDI-SDI mode.
2. Can be used in SDI-SDI and SDI-HDMI modes.
3. Can be used in SDI-SDI and HDMI-SDI modes.

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
1000 [2]	PMA_RX_REG_0	RSVD	15:1	RW	57	Reserved. Do not change.
		CDR_ALT_METHOD	0:0	RW	0	Selects the alternate CDR configuration. 0 = the recommended CDR configuration is used. 1 = the alternate CDR configuration. After the selection change, the soft RX PMA reset is required. **Note:** CDR configuration setting is only applicable when in SDI-SDI or SDI-HDMI mode.
1001 to 101A	RSVD	RSVD	15:0	RW	N/A	Reserved. Do not change.
101B	DDI_CDR_LBW	DDI3_UPDATE_CDR_LBW	15:15	ROSW	0	Write 1 to upload bandwidth settings from DDI3_CDR_LBW. The register will be automatically set back to 0 when the CDR bandwidth is updated. **Note:** The DDI3_UPDATE_CDR_LBW bit is not updated until DDI3 is enabled (powered up in the selected mode and ISP is LOW).
		DDI3_CDR_LBW	14:13	RW	1	Loop bandwidth settings: 00 = LOW 01 = Default 10 = HIGH 11 = Default See **Error! Reference source not found.** for bandwidth values.
		DDI2_UPDATE_CDR_LBW	12:12	ROSW	0	See DDI3_UPDATE_CDR_LBW.

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09/08/2026

		DDI2_CDR_LBW	11:10	RW	1	See DDI3_CDR_LBW for settings.
		DDI1_UPDATE_CDR_LBW	9:9	ROSW	0	See DDI3_UPDATE_CDR_LBW.
		DDI1_CDR_LBW	8:7	RW	1	See DDI3_CDR_LBW for settings.
		DDI0_UPDATE_CDR_LBW	6:6	ROSW	0	See DDI3_UPDATE_CDR_LBW.
		DDI0_CDR_LBW	5:4	RW	1	See DDI3_CDR_LBW for settings.
		RSVD	3:0	RW	F	Reserved. Do not change.
101C to 1022	RSVD	RSVD	15:0	RW	N/A	Reserved. Do not change.
1023	DDI0_EQ_UPDT	PORT0_RERUN_RXEQ_SEQ	15:15	ROSW	0	Lane 0 parameter. When set PMA-RX reruns RXEQ (by running the RXEQ_0 sequence).
		PORT0_UPDATE_RXEQ_SETTINGS	14:14	ROSW	0	Lane 0 parameter. When set PMA-RX updates RXEQ settings (by running the RXEQ_CHNG_0 sequence).
		PORT0_RX_FEQ2_OVR_EN	13:13	RW	0	Overwrite enable signal. When HIGH, the PORT0_RX_FEQ2 signal will be used. When LOW, internal computed value will be used.
		PORT0_RX_FEQ2	12:7	RW	12	Lane 0 parameter. Used only when PORT0_RX_FEQ2_OVR_EN is HIGH. RX CTLE #2 setting.
		PORT0_RX_FEQ1_OVR_EN	6:6	RW	0	Overwrite enable signal. When HIGH, the PORT0_RX_FEQ1 signal will be used. When LOW, internal computed value will be used.
		PORT0_RX_FEQ1	5:0	RW	8	Lane 0 parameter. Used only when PORT0_RX_FEQ1_OVR_EN is HIGH. RX CTLE #1 setting.
1024	DDI1_EQ_UPDT	PORT1_RERUN_RXEQ_SEQ	15:15	ROSW	0	Lane 1 parameter. When set PMA-RX reruns RXEQ. (by running the RXEQ_0 sequence).
		PORT1_UPDATE_RXEQ_SETTINGS	14:14	ROSW	0	Lane 1 parameter. When set PMA-RX updates RXEQ settings (by running the RXEQ_CHNG_0 sequence).

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09/08/2026

		PORT1_RX_FEQ2_OVR_EN	13:13	RW	0	Overwrite enable signal. When HIGH, the PORT1_RX_FEQ2 signal will be used. When LOW, internal computed value will be used.
		PORT1_RX_FEQ2	12:7	RW	12	Lane 1 parameter. Used only when PORT1_RX_FEQ2_OVR_EN is HIGH. RX CTLE #2 setting.
		PORT1_RX_FEQ1_OVR_EN	6:6	RW	0	Overwrite enable signal. When HIGH, the PORT1_RX_FEQ1 signal will be used. When LOW, internal computed value will be used.
		PORT1_RX_FEQ1	5:0	RW	8	Lane 1 parameter. Used only when PORT1_RX_FEQ1_OVR_EN is HIGH. Rx CTLE #1 setting.
1025	DDI2_EQ_UPDT	PORT2_RERUN_RXEQ_SEQ	15:15	ROSW	0	Lane 2 parameter. When set PMA-RX reruns RXEQ. (by running the RXEQ_0 sequence).
		PORT2_UPDATE_RXEQ_SETTINGS	14:14	ROSW	0	Lane 2 parameter. When set PMA-RX updates RXEQ settings (by running the RXEQ_CHNG_0 sequence).
		PORT2_RX_FEQ2_OVR_EN	13:13	RW	0	Overwrite enable signal. When HIGH, the PORT2_RX_FEQ2 signal will be used. When LOW, internal computed value will be used.
		PORT2_RX_FEQ2	12:7	RW	12	Lane 2 parameter. Used only when PORT2_RX_FEQ2_OVR_EN is HIGH. RX CTLE #2 setting.
		PORT2_RX_FEQ1_OVR_EN	6:6	RW	0	Overwrite enable signal. When HIGH, the PORT2_RX_FEQ1 signal will be used. When LOW, internal computed value will be used.
		PORT2_RX_FEQ1	5:0	RW	8	Lane 2 parameter. Used only when PORT2_RX_FEQ1_OVR_EN is HIGH. RX CTLE #1 setting.
1026	DDI3_EQ_UPDT	PORT3_RERUN_RXEQ_SEQ	15:15	ROSW	0	Lane 3 parameter. When set PMA-RX reruns RXEQ (by running the RXEQ_0 sequence).
		PORT3_UPDATE_RXEQ_SETTINGS	14:14	ROSW	0	Lane 3 parameter. When set PMA-RX updates RXEQ settings (by running the RXEQ_CHNG_0 sequence).
		PORT3_RX_FEQ2_OVR_EN	13:13	RW	0	Overwrite enable signal. When HIGH, the PORT3_RX_FEQ2 signal will be used. When LOW, internal computed value will be used.

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		PORT3_RX_FEQ2	12:7	RW	12	Lane 3 parameter. Used only when PORT3_RX_FEQ2_OVR_EN is HIGH. RX CTLE #2 setting.
		PORT3_RX_FEQ1_OVR_EN	6:6	RW	0	Overwrite enable signal. When HIGH, the PORT3_RX_FEQ1 signal will be used. When LOW, internal computed value will be used.
		PORT3_RX_FEQ1	5:0	RW	8	Lane 3 parameter. Used only when PORT3_RX_FEQ1_OVR_EN is HIGH. RX CTLE #1 setting.
1027 to 1046	RSVD	RSVD	15:0	RW	N/A	Reserved. Do not change.
1047	PMA_RX_REG_71	RSVD	15:4	RO	0	Reserved.
		PORT3_RX_POLARITY	3:3	RW	0	Lane 3 RX data polarity inversion. This is for the RX_DATA[159:120] signal. 0 = normal 1 = inverted
		PORT2_RX_POLARITY	2:2	RW	0	Lane 2 RX data polarity inversion. This is for the RX_DATA[119:80] signal. 0 = normal 1 = inverted
		PORT1_RX_POLARITY	1:1	RW	0	Lane 1 RX data polarity inversion. This is for the RX_DATA[79:40] signal. 0 = normal 1 = inverted
		PORT0_RX_POLARITY	0:0	RW	0	Lane 0 RX data polarity inversion. This is for the RX_DATA[39:0] signal. 0 = normal 1 = inverted
1048 to 1064	RSVD	RSVD	15:0	RW	N/A	Reserved. Do not change.
1065	PMA_CTRL_REG_101	RSVD	15:1	RW	3	Reserved. Do not change.
		PMA_CTRL_SOFT_RESET	0:0	RW	0	When HIGH, will reset the PMA_RX_CTRL FSM of the 4 lanes.
1066 to 1108	RSVD	RSVD	15:0	RW	N/A	Reserved. Do not change.

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09/08/2026

4.2.3. Tx Control and Status Registers

Table 4-8 Tx Control and Status Registers

1. Can be used only in SDI-SDI mode.
2. Can be used in SDI-SDI and SDI-HDMI modes.
3. Can be used in SDI-SDI and HDMI-SDI modes.

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
2000 to 2009	RSVD	RSVD	15:0	RW	N/A	Reserved. Do not change.
2010	PMA_TX_ REG_16	RSVD	15:15	RO	0	Reserved.
		PORT1_TX_POST_ CUR_OVR_EN	14:14	RW	0	Overwrite enable signal. When HIGH, the PORT1_TX_POST_CUR signal will be used. When LOW, internal computed value will be used.
		PORT1_TX_POST_ CUR	13:8	RW	8	Used only when PORT1_TX_POST_CUR_OVR_EN is HIGH. Tx 3-tap equalizer post-cursor setting.
		PORT0_TX_POST_ CUR_OVR_EN	7:7	RW	0	Overwrite enable signal. When HIGH, the PORT0_TX_POST_CUR signal will be used. When LOW, internal computed value will be used.
		PORT0_TX_POST_ CUR	6:1	RW	8	Used only when PORT0_TX_POST_CUR_OVR_EN is HIGH. Tx 3-tap equalizer post-cursor setting.
		PORT3_TX_PICTL_ EN_OVR_EN	0:0	RW	0	Overwrite enable signal. When HIGH, the PORT3_TX_PICTL_EN signal will be used. When LOW, internal computed value will be used.
2011	PMA_TX_REG_ 17	RSVD	15:14	RO	0	Reserved.
		PORT3_TX_POST_ CUR_OVR_EN	13:13	RW	0	Overwrite enable signal. When HIGH, the PORT3_TX_POST_CUR signal will be used. When LOW, internal computed value will be used.
		PORT3_TX_POST_ CUR	12:7	RW	8	Used only when PORT3_TX_POST_CUR_OVR_EN is HIGH. Tx 3-tap equalizer post-cursor setting.

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09/08/2026

		PORT2_TX_POST_CUR_OVR_EN	6:6	RW	0	Overwrite enable signal. When HIGH, the PORT2_TX_POST_CUR signal will be used. When LOW, internal computed value will be used.
		PORT2_TX_POST_CUR	5:0	RW	8	Used only when PORT2_TX_POST_CUR_OVR_EN is HIGH. Tx 3-tap equalizer post-cursor setting.
2012	PMA_TX_REG_18	RSVD	15:12	RO	0	Reserved.
		PORT1_TX_PRE_CUR	11:6	RW	0	Lane 0 parameter. TX 3-tap equalizer pre-cursor setting.
		PORT0_TX_PRE_CUR	5:0	RW	0	Lane 1 parameter. TX 3-tap equalizer pre-cursor setting.
2013	PMA_TX_REG_19	RSVD	15:12	RO	0	Reserved.
		PORT3_TX_PRE_CUR	11:6	RW	0	Lane 3 parameter. TX 3-tap equalizer pre-cursor setting.
		PORT2_TX_PRE_CUR	5:0	RW	0	Lane 2 parameter. TX 3-tap equalizer pre-cursor setting.
2014	DDO_DRV_AMP	RSVD	15:12	RO	0	Reserved.
		DDO0_AMP	11:9	RW	4	DDO0 output Driver Amplitude settings.

DDO0_AMP	Differential Amplitude (mV_{ppd})
0	400
1	500
2	600
3	700
4	800
5	900
6	1000
7	400

Note: This value will be loaded into the GS12270 once the DDO0_DRV_AMP_UPDATE parameter is set HIGH.

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09/08/2026

		DDO1_AMP	8:6	RW	0	See DDO0_AMP for DDO1 Driver Amplitude settings.
		DDO2_AMP	5:3	RW	0	See DDO0_AMP for DDO2 Driver Amplitude settings.
		DDO3_AMP	2:0	RW	0	See DDO0_AMP for DDO3 Driver Amplitude settings.
2015 to 2019	RSVD	RSVD	15:0	RW	N/A	Reserved. Do not change.
201A [1]	DDO_LBW	DDO0_LBW	15:12	RW	0	See **Error! Reference source not found.**. **Note:** This value will be loaded into the GS12270 once the PORT3_UPDATE_PI_LBW_SETTINGS parameter is set HIGH. Only applies in SDI-SDI mode.
		DDO1_LBW	11:8	RW	0	See **Error! Reference source not found.**.
		DDO2_LBW	7:4	RW	0	See **Error! Reference source not found.**.
		DDO3_LBW	3:0	RW	0	See **Error! Reference source not found.**.
201B [1]	DDO_LBW_UPDT	RSVD	15:4	RO	0	Reserved.
		DDO0_UPDATE_LBW	3:3	ROSW	0	Write 1 to upload DDO loop bandwidth settings from DDO0_LBW. The register will be automatically set back to 0 when the DDO loop bandwidth is updated. **Note:** Bits are not updated if DDO0 is idle (**Error! Reference source not found.**) or manually powered down.
		DDO1_UPDATE_LBW	2:2	ROSW	0	See DDO0_UPDATE_LBW.
		DDO2_UPDATE_LBW	1:1	ROSW	0	See DDO0_UPDATE_LBW.
		DDO3_UPDATE_LBW	0:0	ROSW	0	See DDO0_UPDATE_LBW.
201C	DDO_DRV_UPDT	RSVD	15:4	RO	0	Reserved.

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09/08/2026

		DDO0_DRV_AMP_UPDATE	3:3	ROSW	0	Write 1 to update DDO driver amplitude settings from DDO0_AMP parameter. The register will be automatically set back to 0 when the amplitude is updated.
		DDO1_DRV_AMP_UPDATE	2:2	ROSW	0	See DDO0_DRV_AMP_UPDATE.
		DDO2_DRV_AMP_UPDATE	1:1	ROSW	0	See DDO0_DRV_AMP_UPDATE.
		DDO3_DRV_AMP_UPDATE	0:0	ROSW	0	See DDO0_DRV_AMP_UPDATE.
201D	PMA_TX_REG_29	RSVD	15:4	RO	0	Reserved.
		PORT3_TX_IDLE	3:3	RW	0	Used only when PORT3_TX_IDLE_OVR_EN is HIGH. When HIGH, set the TX differential outputs in electrical idle state.
		PORT2_TX_IDLE	2:2	RW	0	Used only when PORT2_TX_IDLE_OVR_EN is HIGH. When HIGH, set the TX differential outputs in electrical idle state.
		PORT1_TX_IDLE	1:1	RW	0	Used only when PORT1_TX_IDLE_OVR_EN is HIGH. When HIGH, set the TX differential outputs in electrical idle state.
		PORT0_TX_IDLE	0:0	RW	0	Used only when PORT0_TX_IDLE_OVR_EN is HIGH. When HIGH, set the TX differential outputs in electrical idle state.
201E	PMA_TX_REG_30	RSVD	15:4	RW	0	Reserved. Do not change.
		PORT3_TX_IDLE_OVR_EN	3:3	RW	0	Overwrite enable signal. When HIGH, the PORT3_TX_IDLE signal will be used. When LOW, internal computed value will be used.
		PORT2_TX_IDLE_OVR_EN	2:2	RW	0	Overwrite enable signal. When HIGH, the PORT2_TX_IDLE signal will be used. When LOW, internal computed value will be used.
		PORT1_TX_IDLE_OVR_EN	1:1	RW	0	Overwrite enable signal. When HIGH, the PORT1_TX_IDLE signal will be used. When LOW, internal computed value will be used.

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09/08/2026

		PORT0_TX_IDLE_OVR_EN	0:0	RW	0	Overwrite enable signal. When HIGH, the PORT0_TX_IDLE signal will be used. When LOW, internal computed value will be used.
201F to 2036	RSVD	RSVD	15:0	RW	N/A	Reserved. Do not change.
2037	OUTPUT_PWR_DOWN	TX_PD_OVR_EN	15:12	RW	0	Bit 12 is related to lane 0, bit 13 is related to lane 1, bit 14 is related to lane 2, bit 15 is related to lane 3. When one particular bit is HIGH, the corresponding TX_PD bit will be used, otherwise internal signals will be used.
		TX_PD	11:8	RW	0	TX power down mode select. Bit 8 is for lane 0, bit 9 is for lane 1, bit 10 is for lane 2 and bit 11 is for lane 3. Only used when the corresponding TX_PD_OVR_EN bit is HIGH.
		TX_RESET_OVR_EN	7:4	RW	0	Bit 4 is related to lane 0, bit 5 is related to lane 1, bit 6 is related to lane 2, bit 7 is related to lane 3. When one particular bit is HIGH, the corresponding TX_RESET bit will be used, otherwise internal signals will be used.
		TX_RESET	3:0	RW	0	TX total reset including clock dividers, mainly used for lane-to-lane synchronization 1:reset, 0:normal operation. Bit 0 is for lane 0, bit 1 is for lane 1, bit 2 is for lane 2 and bit 3 is for lane 3. Used only when the corresponding TX_RESET_OVR_EN bit is HIGH.
2038	DDO_DRIVER_DISABLE	RSVD	15:8	RO	0	Reserved.
		DDO_DISABLE_OW_EN	7:4	RW	0	Enables the DDO_DISABLE register setting – one bit per DDO output. Bit 7 = DDO0 Bit 6 = DDO1 Bit 5 = DDO2 Bit 4 = DDO3 **Note:** Only select bits that are related to the desired output to be manually disabled.
		DDO_DISABLE	3:0	RW	0	'1' Disables the DDO output – one bit per DDO output. Bit 3 = DDO0 Bit 2 = DDO1 Bit 1 = DDO2 Bit 0 = DDO3

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09/08/2026

2039	RSVD	RSVD	15:0	RW	0B6D	Reserved. Do not change.
203A	PMA_TX_REG_58	RSVD	15:8	RW	0	Reserved. Do not change.
		PORT3_TX_ POLARITY_OVR_EN	7:7	RW	0	Overwrite enable signal. When HIGH, the PORT3_TX_POLARITY signal will be used. When LOW, internal computed value will be used.
		PORT2_TX_ POLARITY_OVR_EN	6:6	RW	0	Overwrite enable signal. When HIGH, the PORT2_TX_POLARITY signal will be used. When LOW, internal computed value will be used.
		PORT1_TX_ POLARITY_OVR_EN	5:5	RW	0	Overwrite enable signal. When HIGH, the PORT1_TX_POLARITY signal will be used. When LOW, internal computed value will be used.
		PORT0_TX_ POLARITY_OVR_EN	4:4	RW	0	Overwrite enable signal. When HIGH, the PORT0_TX_POLARITY signal will be used. When LOW, internal computed value will be used.
		PORT3_TX_ POLARITY	3:3	RW	0	Lane 3 parameter. Used only when PORT3_TX_POLARITY_OVR_EN is HIGH. TX data polarity inversion. 0 = normal, 1 = inverted.
		PORT2_TX_ POLARITY	2:2	RW	0	Lane 2 parameter. Used only when PORT2_TX_POLARITY_OVR_EN is HIGH. TX data polarity inversion. 0 = normal, 1 = inverted
		PORT1_TX_ POLARITY	1:1	RW	0	Lane 1 parameter. Used only when PORT1_TX_POLARITY_OVR_EN is HIGH. TX data polarity inversion. 0 = normal, 1 = inverted.
		PORT0_TX_ POLARITY	0:0	RW	0	Lane 0 parameter. Used only when PORT0_TX_POLARITY_OVR_EN is HIGH. TX data polarity inversion. 0 = normal, 1 = inverted.
203B to 2064	RSVD	RSVD	15:0	RW	N/A	Reserved. Do not change.
2065		RSVD	15:1	RO	0	Reserved.

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09/08/2026

	PMA_CTRL_ REG_101	PMA_CTRL_ SOFT_RESET	0:0	RW	0	When HIGH, will reset the PMA_TX_CTRL FSM of the 4 lanes.
2066 to 2102	RSVD	RSVD	15:0	RW	N/A	Reserved. Do not change.

4.2.4. Pattern Generator Control Registers

Table 4-9 Pattern Generator Control and Status Registers

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
3000	PG_MODE	YC_RAMP_LIMIT_SEL	13:12	RW	0	Selects Luma (Y)/Chroma (C) limits: 00 = SMPTE 10 = Full X1 = Custom limit and step for Y ramp
		YC_RAMP_SEL	11:8	RW	0	Selects Luma (Y)/Chroma (C) ramp type.
		PG_MODE_0	7:7	RW	1	TBD.
		PG_LINE_SEL	6:4	RW	0	Set: 1 = for 2048 line standards 0 = for 1920 line standards
		PG_PATTERN_ SEL	3:0	RW	0	Selects a pattern. See **Error! Reference source not found.**.
3001	PG_REG_0	RSVD	15:6	RO	0	Reserved.
		REPETIT_PATT_SEL	5:4	RW	1	Selects a repetitive pattern instead of the selected pattern by PG_PATTERN_SEL. The repeated values are define by registers Y_SI0_REPET_VAL to Y_SI7_REPET_VAL. 00 = one word repeating pattern (Y_SI0) 01 = two words repeating pattern (Y_SI0-Y_SI1) 10 = four words repeating pattern (Y_SI0-Y_SI3) 11 = eight words repeating pattern (Y_SI0-Y_SI7)
		RSVD	3:1	RO	0	Reserved.

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		BOX_EN	0:0	RW	0	Enables insertion of the Luma box (ramp if selected) region whose boundaries are defined by REPLACE_*_START and REPLACE_*_STOP parameters.
3002	H_REGION_0	RSVD	15:12	RO	0	Reserved.
		H_REGION_0	11:0	RW	FFF	Selects horizontal region for custom pattern.
3003	H_REGION_1	RSVD	15:12	RO	0	Reserved.
		H_REGION_1	11:0	RW	0	Selects horizontal region for custom pattern.
3004	V_REGION_0	RSVD	15:12	RO	0	Reserved.
		V_REGION_0	11:0	RW	438	Selects vertical region for custom pattern.
3005	V_REGION_1	RSVD	15:12	RO	0	Reserved.
		V_REGION_1	11:0	RW	870	Selects vertical region for custom pattern.
3006	REPLACE_H_START	RSVD	15:12	RO	0	Reserved.
		REPLACE_H_START	11:0	RW	0	Defines horizontal start of the box insertion region.
3007	REPLACE_H_STOP	RSVD	15:12	RO	0	Reserved.
		REPLACE_H_STOP	11:0	RW	0	Defines horizontal stop of the box insertion region.
3008	REPLACE_V_START	RSVD	15:12	RO	0	Reserved.
		REPLACE_V_START	11:0	RW	0	Defines vertical start of the box insertion region.
3009	REPLACE_V_STOP	RSVD	15:12	RO	0	Reserved.
		REPLACE_V_STOP	11:0	RW	0	Defines vertical stop of the box insertion region.
300A	YRAMP_H_START_VALUE	YRAMP_H_START	15:0	RW	0	Start Y/C value of the ramp.

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09/08/2026

300B	YRAMP_H_ STEP_VALUE	YRAMP_H_STEP	15:0	RW	0	H step Y/C value of the ramp.
300C	YRAMP_V_ STEP_VALUE	YRAMP_V_STEP	15:0	RW	0	V step Y/C value of the ramp.
300D	Y_BLANKING	RSVD	15:10	RO	0	Reserved.
		Y_BLANKING	9:0	RW	40	Y value in the blanking region.
300E	C_BLANKING	RSVD	15:10	RO	0	Reserved.
		C_BLANKING	9:0	RW	200	C value in the blanking region.
300F	RSVD	RSVD	15:0	RO	0	Reserved. Do not change.
3010	Y_SI0_REPET_ VAL	RSVD	15:10	RO	0	Reserved.
		Y_SI0_REPET_VAL	9:0	RW	1FF	Colour value for repeating pattern.
3011	Y_SI1_REPET_ VAL	RSVD	15:10	RO	0	Reserved.
		Y_SI1_REPET_VAL	9:0	RW	2EF	Colour value for repeating pattern.
3012	Y_SI2_REPET_ VAL	RSVD	15:10	RO	0	Reserved.
		Y_SI2_REPET_VAL	9:0	RW	0	Colour value for repeating pattern.
3013	Y_SI3_REPET_ VAL	RSVD	15:10	RO	0	Reserved.
		Y_SI3_REPET_VAL	9:0	RW	0	Colour value for repeating pattern.
3014	Y_SI4_REPET_ VAL	RSVD	15:10	RO	0	Reserved.
		Y_SI4_REPET_VAL	9:0	RW	0	Colour value for repeating pattern.
3015	Y_SI5_REPET_ VAL	RSVD	15:10	RO	0	Reserved.
		Y_SI5_REPET_VAL	9:0	RW	0	Colour value for repeating pattern.
3016	Y_SI6_REPET_ VAL	RSVD	15:10	RO	0	Reserved.
		Y_SI6_REPET_VAL	9:0	RW	0	Colour value for repeating pattern.

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3017	Y_SI7_REPET_VAL	RSVD	15:10	RO	0	Reserved.
		Y_SI7_REPET_VAL	9:0	RW	0	Colour value for repeating pattern.

4.2.5. SDI Audio De-Embedding Control Registers

Table 4-10 SDI Audio De-Embedding Control and Status Register

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
4*00	RSVD	RSVD	15:1	RW	0	Reserved. Do not change.
4*01	CFG_AUD	RSVD	15:14	RO	0	Reserved.
		AUD_EXT_*_ASWLB	13:12	RW	0	Group B output word length. 00_b = 24 bits 01_b = 20 bits 10_b = 16 bits 11_b= Invalid
		AUD_EXT_*_ASWLA	11:10	RW	0	Group A output word length. 00_b = 24 bits 01_b = 20 bits 10_b = 16 bits 11_b= Invalid
		AUD_EXT_*_AMB	9:8	RW	3	Group B output format selector. 00_b = AES/EBU audio output 01_b = Serial audio output: left justified 10_b = Serial audio output: right justified 11_b = I²S serial audio output
		AUD_EXT_*_AMA	7:6	RW	3	Group A output format selector. 00_b = AES/EBU audio output 01_b = Serial audio output: left justified 10_b = Serial audio output: right justified 11_b = I²S serial audio output

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09/03/2026

		AUD_EXT_*_ EXTEND_IDB	5:5	RW	0	0 = Group B will extract SMPTE audio groups 1, 2, 3, or 4 1 = Group B will extract SMPTE audio groups 5, 6, 7, or 8
		AUD_EXT_*_IDB	4:3	RW	1	Along with EXTEND_IDB, specifies the SMPTE audio group to extract for Group B. 00_b = Audio group #1 or #5 01_b = Audio group #2 or #6 10_b = Audio group #3 or #7 11_b = Audio group #4 or #8 Note: Should IDA & EXTEND_IDA and IDB & EXTEND_IDB be set to the same audio group, IDA and IDB automatically revert to their default values.
		AUD_EXT_*_ EXTEND_IDA	2:2	RW	0	0 = Group A will extract SMPTE audio groups 1, 2, 3 or 4. 1 = Group A will extract SMPTE audio groups 5, 6, 7 or 8.
		AUD_EXT_*_IDA	1:0	RW	0, 2	Along with EXTEND_IDA, specifies the SMPTE audio group to extract for Group A. 00_b = Audio group #1 or #5 01_b = Audio group #2 or #6 10_b = Audio group #3 or #7 11_b = Audio group #4 or #8 Note: Should IDA & EXTEND_IDA and IDB & EXTEND_IDB be set to the same audio group, IDA and IDB automatically revert to their default values.
4*02	CFG_AUD2	RSVD	15:2	RO	0	Reserved.
		AUD_EXT_*_ MUTE_ALL	1:1	RW	0	Mute all output channels: 0 = Normal 1 = Muted
		AUD_EXT_*_ACS_ USE_SECOND	0:0	RW	0	Extract Audio Channel Status from second channel pair.
4*03	ACS_DET	RSVD	15:8	RO	0	Reserved.
		AUD_EXT_*_ DBNB_ERR	7:7	ROCW	0	Set when Group B audio Data Block Number sequence is discontinuous.
		AUD_EXT_*_ DBNA_ERR	6:6	ROCW	0	Set when Group A audio Data Block Number sequence is discontinuous.

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		AUD_EXT_*_ CTRB_DET	5:5	ROCW	0	Set when Group B audio control packet is detected.
		AUD_EXT_*_ CTRA_DET	4:4	ROCW	0	Set when Group A audio control packet is detected.
		AUD_EXT_*_ ACS_DET3_4B	3:3	ROCW	0	Group B audio status detected for channels 3 and 4.
		AUD_EXT_*_ ACS_DET1_2B	2:2	ROCW	0	Group B audio status detected for channels 1 and 2.
		AUD_EXT_*_ ACS_DET3_4A	1:1	ROCW	0	Group A audio status detected for channels 3 and 4.
		AUD_EXT_*_ ACS_DET1_2A	0:0	ROCW	0	Group A audio status detected for channels 1 and 2.
4*04	AUD_DET1	RSVD	15:13	RO	0	Reserved.
		AUD_EXT_*_ IDB_READBACK	12:11	RO	1	Actual value of IDB in the hardware.
		AUD_EXT_*_ IDA_READBACK	10:9	RO	0	Actual value of IDA in the hardware.
		AUD_EXT_*_ ADPG8_DET	8:8	RO	0	Set to 1 and remains set while SMPTE Group 8 audio data packets are detected. Goes to 0 if none are detected for more than 1 frame.
		AUD_EXT_*_ ADPG7_DET	7:7	RO	0	Set to 1 and remains set while SMPTE Group 7 audio data packets are detected. Goes to 0 if none are detected for more than 1 frame.
		AUD_EXT_*_ ADPG6_DET	6:6	RO	0	Set to 1 and remains set while SMPTE Group 6 audio data packets are detected. Goes to 0 if none are detected for more than 1 frame.
		AUD_EXT_*_ ADPG5_DET	5:5	RO	0	Set to 1 and remains set while SMPTE Group 5 audio data packets are detected. Goes to 0 if none are detected for more than 1 frame.
		AUD_EXT_*_ ADPG4_DET	4:4	RO	0	Set to 1 and remains set while SMPTE Group 4 audio data packets are detected. Goes to 0 if none are detected for more than 1 frame.

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		AUD_EXT_*_ ADPG3_DET	3:3	RO	0	Set to 1 and remains set while SMPTE Group 3 audio data packets are detected. Goes to 0 if none are detected for more than 1 frame.
		AUD_EXT_*_ ADPG2_DET	2:2	RO	0	Set to 1 and remains set while SMPTE Group 2 audio data packets are detected. Goes to 0 if none are detected for more than 1 frame.
		AUD_EXT_*_ ADPG1_DET	1:1	RO	0	Set to 1 and remains set while SMPTE Group 1 audio data packets are detected. Goes to 0 if none are detected for more than 1 frame.
		AUD_EXT_*_ ACS_APPLY_ WAIT	0:0	RO	0	Set while output channels 1 and 2 are waiting for a status boundary to apply the ACSR[183:0] data.
4*05	AUD_DET2	RSVD	15:2	RO	0	Reserved.
		AUD_EXT_*_ ECCA_ERROR	1:1	ROCW	0	Group A audio data packet error detected.
		AUD_EXT_*_ ECCB_ERROR	0:0	ROCW	0	Group B audio data packet error detected.
4*06	REGEN	RSVD	15:2	RO	0	Reserved.
		AUD_EXT_*_ ACS_APPLY	1:1	RW	0	When set to 1, this causes channel status data in ACSR[183:0] (ACSR_BYTE_* registers) to be transferred to the channel status replacement mechanism. The transfer shall not occur until the next status boundary.
		AUD_EXT_*_ ACS_REGEN	0:0	RW	0	Specifies that Audio Channel Status of all channels should be replaced with ACSR[183:0] field (ACSR_BYTE_* registers). 0 = Do not replace Channel Status 1 = Replace Channel Status of all channels
4*07	CH_MUTE	RSVD	15:8	RO	0	Reserved.
		AUD_EXT_*_ MUTEB	7:4	RW	0	Mute Group B output channels 4 to 1; bits 7:4 = channel 4:1 0 = Normal 1 = Muted

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09/03/2026

		AUD_EXT_*_ MUTEA	3:0	RW	0	Mute Group A output channels 4 to 1; bits 3:0 = channel 4:1 0 = Normal 1 = Muted
4*08	CH_VALID	RSVD	15:8	RO	0	Reserved.
		AUD_EXT_*_ CH4_VALIDB	7:7	RO	0	Group B channel 4 sample validity flag.
		AUD_EXT_*_ CH3_VALIDB	6:6	RO	0	Group B channel 3 sample validity flag.
		AUD_EXT_*_ CH2_VALIDB	5:5	RO	0	Group B channel 2 sample validity flag.
		AUD_EXT_*_ CH1_VALIDB	4:4	RO	0	Group B channel 1 sample validity flag.
		AUD_EXT_*_ CH4_VALIDA	3:3	RO	0	Group A channel 4 sample validity flag.
		AUD_EXT_*_ CH3_VALIDA	2:2	RO	0	Group A channel 3 sample validity flag.
		AUD_EXT_*_ CH2_VALIDA	1:1	RO	0	Group A channel 2 sample validity flag.
		AUD_EXT_*_ CH1_VALIDA	0:0	RO	0	Group A channel 1 sample validity flag.
4*09	INT_ENABLE	RSVD	15:8	RO	0	Reserved.
		AUD_EXT_*_ EN_ADPG8_DET	7:7	RW	0	When enabled, interrupt will assert when ADPG8_DET is set.
		AUD_EXT_*_ EN_ADPG7_DET	6:6	RW	0	When enabled, interrupt will assert when ADPG7_DET is set.
		AUD_EXT_*_ EN_ADPG6_DET	5:5	RW	0	When enabled, interrupt will assert when ADPG6_DET is set.
		AUD_EXT_*_ EN_ADPG5_DET	4:4	RW	0	When enabled, interrupt will assert when ADPG5_DET is set.
		AUD_EXT_*_ EN_ADPG4_DET	3:3	RW	0	When enabled, interrupt will assert when ADPG4_DET is set.

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09/08/2026

		AUD_EXT_*_EN_ADPG3_DET	2:2	RW	0	When enabled, interrupt will assert when ADPG3_DET is set.
		AUD_EXT_*_EN_ADPG2_DET	1:1	RW	0	When enabled, interrupt will assert when ADPG2_DET is set.
		AUD_EXT_*_EN_ADPG1_DET	0:0	RW	0	When enabled, interrupt will assert when ADPG1_DET is set.
4*0A	INT_ENABLE2	RSVD	15:11	RO	0	Reserved.
		AUD_EXT_*_EN_MISSING_PHASE	10:10	RW	0	When enabled, interrupt will assert when chosen group's phase data is missing or invalid.
		AUD_EXT_*_EN_ACS_DET3_4B	9:9	RW	0	When enabled, interrupt will assert when ACS_DET3_4B is set.
		AUD_EXT_*_EN_ACS_DET1_2B	8:8	RW	0	When enabled, interrupt will assert when ACS_DET1_2B is set.
		AUD_EXT_*_EN_ACS_DET3_4A	7:7	RW	0	When enabled, interrupt will assert when ACS_DET3_4A is set.
		AUD_EXT_*_EN_ACS_DET1_2A	6:6	RW	0	When enabled, interrupt will assert when ACS_DET1_2A is set.
		AUD_EXT_*_EN_CTRB_DET	5:5	RW	0	When enabled, interrupt will assert when CTRB_DET is set.
		AUD_EXT_*_EN_CTRA_DET	4:4	RW	0	When enabled, interrupt will assert when CTRA_DET is set.
		AUD_EXT_*_EN_DBNB_ERR	3:3	RW	0	When enabled, interrupt will assert when DBNB_ERR is set.
		AUD_EXT_*_EN_DBNA_ERR	2:2	RW	0	When enabled, interrupt will assert when DBNA_ERR is set.
		AUD_EXT_*_EN_ECCB_ERR	1:1	RW	0	When enabled, interrupt will assert when ECCB_ERROR is set.
		AUD_EXT_*_EN_ECCA_ERR	0:0	RW	0	When enabled, interrupt will assert when ECCA_ERROR is set.
4*0B	CFG_AUD_2	RSVD	15:13	RO	0	Reserved.

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AUD_EXT_*_ CHANNEL_ STATUS_EXT_ NO_MOD	12:12	RW	0	By default, the channel status extracted for HDMI will be converted to consumer. Set this bit HIGH to keep it as professional.
AUD_EXT_*_ SEL_PHASE_SRC	11:11	RW	0	Selects between the Group A and Group B embedded phase info when FORCE_PHASE_SRC set to 1. 0 = Use Group A phase information 1 = Use Group B phase information
AUD_EXT_*_ FORCE_PHASE_SRC	10:10	RW	0	Phase source override: 0 = Auto phase source selection 1 = Manually set the phase source using SEL_PHASE_SRC
RSVD	9:8	RW	0	Reserved. Do not change.
AUD_EXT_*_ FORCE_M	7:7	RW	0	Disables auto-detection of M value and forces it to the state specified by the FORCE_MEQ1001 signal.
AUD_EXT_*_ FORCE_ MEQ1001	6:6	RW	0	Specifies M value when FORCE_M is set: 0 = M is 1.000 1 = M is 1.001
AUD_EXT_*_ IGNORE_PHASE	5:5	RW	0	When HIGH, ignores the embedded clock info in both Group A and Group B audio data packets. Clock is generated based on the video format and M value.
AUD_EXT_*_ FORCE_ACLK128	4:4	RW	0	When HIGH, ignores embedded clock info and derives phase information from ACLK128.
AUD_EXT_*_EN_ NOT_LOCKED	3:3	RW	0	When enabled, interrupt will assert when locked is not asserted.
RSVD	2:2	RW	0	Reserved. Do not change.
AUD_EXT_*_EN_ INVALID_ EMBEDDED_ PHASE_B	1:1	RW	0	When enabled, interrupt will assert when INVALID_EMBEDDED_PHASE_B is set.
AUD_EXT_*_EN_ INVALID_ EMBEDDED_ PHASE_A	0:0	RW	0	When enabled, interrupt will assert when INVALID_EMBEDDED_PHASE_A is set.

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4*0C	CFG_AUD_3	RSVD	15:6	RO	0	Reserved.
		AUD_EXT_*_ SELECTED_ PHASE_SRC	5:5	RO	0	Indicates the source audio group for the embedded phase information: 0 = Using Group A phase information 1 = Using Group B phase information
		AUD_EXT_*_ MISSING_PHASE	4:4	RO	0	When HIGH, either INVALID_EMBEDDED_PHASE_A or INVALID_EMBEDDED_PHASE_B is asserted based on SELECTED_PHASE_SRC.
		AUD_EXT_*_ INVALID_ EMBEDDED_ PHASE_B	3:3	RO	0	When HIGH, Group B audio data packets have invalid embedded phase data.
		AUD_EXT_*_ INVALID_ EMBEDDED_ PHASE_A	2:2	RO	0	When HIGH, Group A audio data packets have invalid embedded phase data.
		AUD_EXT_*_ EMBEDDED_ PHASE_ IGNORED_B	1:1	RO	0	When HIGH, Group B audio data packets have invalid embedded phase data or when IGNORE_PHASE or FORCE_ACLK128 are asserted.
		AUD_EXT_*_ EMBEDDED_ PHASE_ IGNORED_A	0:0	RO	0	When HIGH, Group A audio data packets have invalid embedded phase data or when IGNORE_PHASE or FORCE_ACLK128 are asserted.
4*0D	OUTPUT_SEL_1	RSVD	15:12	RO	0	Reserved.
		AUD_EXT_*_ OP4_SRC	11:9	RW	3	Output channel 4 source selector: 000_b = Group A channel 1 001_b = Group A channel 2 010_b = Group A channel 3 011_b = Group A channel 4 100_b = Group B channel 1 101_b = Group B channel 2 110_b = Group B channel 3 111_b = Group B channel 4
		AUD_EXT_*_ OP3_SRC	8:6	RW	2	Output channel 3 source selector. See OP4_SRC for decoding.
		AUD_EXT_*_ OP2_SRC	5:3	RW	1	Output channel 2 source selector. See OP4_SRC for decoding.

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Kent Lin
DIVA Laboratories, Ltd.
09/08/2026

		AUD_EXT_*_OP1_SRC	2:0	RW	0	Output channel 1 source selected. See OP4_SRC for decoding.
4*0E	OUTPUT_SEL_2	RSVD	15:12	RO	0	Reserved.
		AUD_EXT_*_OP8_SRC	11:9	RW	7	Output channel 8 source selector. See OP4_SRC for decoding.
		AUD_EXT_*_OP7_SRC	8:6	RW	6	Output channel 7 source selector. See OP4_SRC for decoding.
		AUD_EXT_*_OP6_SRC	5:3	RW	5	Output channel 6 source selector. See OP4_SRC for decoding.
		AUD_EXT_*_OP5_SRC	2:0	RW	4	Output channel 5 source selector. See OP4_SRC for decoding.
4*0F to 4*1F	RSVD	RSVD	15:0	RO	0	Reserved.
4*20	AFNA	RSVD	15:9	RO	0	Reserved.
		AUD_EXT_*_AFNA	8:0	RO	0	Group A audio frame number.
4*21	RATEA	RSVD	15:4	RO	0	Reserved.
		AUD_EXT_*_RATEA	3:1	RO	0	Group A sampling frequency for channels 1 and 2.
		AUD_EXT_*_ASXA	0:0	RO	0	Group A asynchronous mode for channels 1 and 2.
4*22	ACTA	RSVD	15:4	RO	0	Reserved.
		AUD_EXT_*_ACTA	3:0	RO	0	Group A active channels.
4*23	PRIM_AUD_DELAY_1	RSVD	15:9	RO	0	Reserved.
		AUD_EXT_*_DEL1_2A_1	8:1	RO	0	Group A delay data for channels 1 and 2 [7:0].
		AUD_EXT_*_EBIT1_2A	0:0	RO	0	Group A delay data valid flag for channels 1 and 2.

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DIVA Laboratories, Ltd.
09/08/2026

4*24	PRIM_AUD_DELAY_2	RSVD	15:9	RO	0	Reserved.
		AUD_EXT_*_DEL1_2A_2	8:0	RO	0	Group A delay data for channels 1 and 2 [16:8].
4*25	PRIM_AUD_DELAY_3	RSVD	15:9	RO	0	Reserved.
		AUD_EXT_*_DEL1_2A_3	8:0	RO	0	Group A delay data for channels 1 and 2 [25:17].
4*26	PRIM_AUD_DELAY_4	RSVD	15:9	RO	0	Reserved.
		AUD_EXT_*_DEL3_4A_4	8:1	RO	0	Group A delay data for channels 3 and 4 [7:0].
		AUD_EXT_*_EBIT3_4A	0:0	RO	0	Group A delay data valid flag for channels 3 and 4.
4*27	PRIM_AUD_DELAY_5	RSVD	15:9	RO	0	Reserved.
		AUD_EXT_*_DEL3_4A_5	8:0	RO	0	Group A delay data for channels 3 and 4 [16:8].
4*28	PRIM_AUD_DELAY_6	RSVD	15:9	RO	0	Reserved.
		AUD_EXT_*_DEL3_4A_6	8:0	RO	0	Group A delay data for channels 3 and 4 [25:17].
4*30	AFNB	RSVD	15:9	RO	0	Reserved.
		AUD_EXT_*_AFNB	8:0	RO	0	Group B audio frame number.
4*31	RATEB	RSVD	15:4	RO	0	Reserved.
		AUD_EXT_*_RATEB	3:1	RO	0	Group B sampling frequency for channels 1 and 2.
		AUD_EXT_*_ASXB	0:0	RO	0	Group B asynchronous mode for channels 1 and 2.
4*32	ACTB	RSVD	15:4	RO	0	Reserved.
		AUD_EXT_*_ACTB	3:0	RO	0	Group B active channels.

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Kent Lin
DIVA Laboratories, Ltd.
09/08/2026

4*33	SEC_AUD_ DELAY_1	RSVD	15:9	RO	0	Reserved.
		AUD_EXT_*_ DEL1_2B_1	8:1	RO	0	Group B delay data for channels 1 and 2 [7:0].
		AUD_EXT_*_ EBIT1_2B	0:0	RO	0	Group B delay data valid flag for channels 1 and 2.
4*34	SEC_AUD_ DELAY_2	RSVD	15:9	RO	0	Reserved.
		AUD_EXT_*_ DEL1_2B_2	8:0	RO	0	Group B delay data for channels 1 and 2 [16:8].
4*35	SEC_AUD_ DELAY_3	RSVD	15:9	RO	0	Reserved.
		AUD_EXT_*_ DEL1_2B_3	8:0	RO	0	Group B delay data for channels 1 and 2 [25:17].
4*36	SEC_AUD_ DELAY_4	RSVD	15:9	RO	0	Reserved.
		AUD_EXT_*_ DEL3_4B_4	8:1	RO	0	Group B delay data for channels 3 and 4 [7:0].
		AUD_EXT_*_ EBIT3_4B	0:0	RO	0	Group B delay data valid flag for channels 3 and 4.
4*37	SEC_AUD_ DELAY_5	RSVD	15:9	RO	0	Reserved.
		AUD_EXT_*_ DEL3_4B_5	8:0	RO	0	Group B delay data for channels 3 and 4 [16:8].
4*38	SEC_AUD_ DELAY_6	RSVD	15:9	RO	0	Reserved.
		AUD_EXT_*_ DEL3_4B_6	8:0	RO	0	Group B delay data for channels 3 and 4 [25:17].
4*40	ACSR1_2A_ BYTE0_1	AUD_EXT_*_ ACSR1_2A_0	15:0	RO	0	Bytes 0 and 1 of audio Group A channel status for channels 1 and 2.
4*41	ACSR1_2A_ BYTE2_3	AUD_EXT_*_ ACSR1_2A_2	15:0	RO	0	Bytes 2 and 3 of audio Group A channel status for channels 1 and 2.
4*42	ACSR1_2A_ BYTE4_5	AUD_EXT_*_ ACSR1_2A_4	15:0	RO	0	Bytes 4 and 5 of audio Group A channel status for channels 1 and 2.

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DIVA Laboratories, Ltd.
09/08/2026

4*43	ACSR1_2A_BYTE6_7	AUD_EXT_*_ACSR1_2A_6	15:0	RO	0	Bytes 6 and 7 of audio Group A channel status for channels 1 and 2.
4*44	ACSR1_2A_BYTE8_9	AUD_EXT_*_ACSR1_2A_8	15:0	RO	0	Bytes 8 and 9 of audio Group A channel status for channels 1 and 2.
4*45	ACSR1_2A_BYTE10_11	AUD_EXT_*_ACSR1_2A_10	15:0	RO	0	Bytes 10 and 11 of audio Group A channel status for channels 1 and 2.
4*46	ACSR1_2A_BYTE12_13	AUD_EXT_*_ACSR1_2A_12	15:0	RO	0	Bytes 12 and 13 of audio Group A channel status for channels 1 and 2.
4*47	ACSR1_2A_BYTE14_15	AUD_EXT_*_ACSR1_2A_14	15:0	RO	0	Bytes 14 and 15 of audio Group A channel status for channels 1 and 2.
4*48	ACSR1_2A_BYTE16_17	AUD_EXT_*_ACSR1_2A_16	15:0	RO	0	Bytes 16 and 17 of audio Group A channel status for channels 1 and 2.
4*49	ACSR1_2A_BYTE18_19	AUD_EXT_*_ACSR1_2A_18	15:0	RO	0	Bytes 18 and 19 of audio Group A channel status for channels 1 and 2.
4*4A	ACSR1_2A_BYTE20_21	AUD_EXT_*_ACSR1_2A_20	15:0	RO	0	Bytes 20 and 21 of audio Group A channel status for channels 1 and 2.
4*4B	ACSR1_2A_BYTE22	RSVD	15:8	RO	0	Reserved.
		AUD_EXT_*_ACSR1_2A_22	7:0	RO	0	Bytes 22 of audio Group A channel status for channels 1 and 2.
4*4C to 4*4F	RSVD	RSVD	15:0	RO	0	Reserved.
4*50	ACSR3_4A_BYTE0_1	AUD_EXT_*_ACSR3_4A_0	15:0	RO	0	Bytes 0 and 1 of audio Group A channel status for channels 3 and 4.
4*51	ACSR3_4A_BYTE2_3	AUD_EXT_*_ACSR3_4A_2	15:0	RO	0	Bytes 2 and 3 of audio Group A channel status for channels 3 and 4.
4*52	ACSR3_4A_BYTE4_5	AUD_EXT_*_ACSR3_4A_4	15:0	RO	0	Bytes 4 and 5 of audio Group A channel status for channels 3 and 4.
4*53	ACSR3_4A_BYTE6_7	AUD_EXT_*_ACSR3_4A_6	15:0	RO	0	Bytes 6 and 7 of audio Group A channel status for channels 3 and 4.

Semtech Confidential Information
Kent Lin
DIVA Laboratories, Ltd.
09/08/2026

4*54	ACSR3_4A_ BYTE8_9	AUD_EXT_*_ ACSR3_4A_8	15:0	RO	0	Bytes 8 and 9 of audio Group A channel status for channels 3 and 4.
4*55	ACSR3_4A_ BYTE10_11	AUD_EXT_*_ ACSR3_4A_10	15:0	RO	0	Bytes 10 and 11 of audio Group A channel status for channels 3 and 4.
4*56	ACSR3_4A_ BYTE12_13	AUD_EXT_*_ ACSR3_4A_12	15:0	RO	0	Bytes 12 and 13 of audio Group A channel status for channels 3 and 4.
4*57	ACSR3_4A_ BYTE14_15	AUD_EXT_*_ ACSR3_4A_14	15:0	RO	0	Bytes 14 and 15 of audio Group A channel status for channels 3 and 4.
4*58	ACSR3_4A_ BYTE16_17	AUD_EXT_*_ ACSR3_4A_16	15:0	RO	0	Bytes 16 and 17 of audio Group A channel status for channels 3 and 4.
4*59	ACSR3_4A_ BYTE18_19	AUD_EXT_*_ ACSR3_4A_18	15:0	RO	0	Bytes 18 and 19 of audio Group A channel status for channels 3 and 4.
4*5A	ACSR3_4A_ BYTE20_21	AUD_EXT_*_ ACSR3_4A_20	15:0	RO	0	Bytes 20 and 21 of audio Group A channel status for channels 3 and 4.
4*5B	ACSR3_4A_ BYTE22	RSVD	15:8	RO	0	Reserved.
		AUD_EXT_*_ ACSR3_4A_22	7:0	RO	0	Bytes 22 of audio Group A channel status for channels 3 and 4.
4*5C to 4*5F	RSVD	RSVD	15:0	RO	0	Reserved.
4*60	ACSR1_2B_ BYTE0_1	AUD_EXT_*_ ACSR1_2B_0	15:0	RO	0	Bytes 0 and 1 of audio Group B channel status for channels 1 and 2.
4*61	ACSR1_2B_ BYTE2_3	AUD_EXT_*_ ACSR1_2B_2	15:0	RO	0	Bytes 2 and 3 of audio Group B channel status for channels 1 and 2.
4*62	ACSR1_2B_ BYTE4_5	AUD_EXT_*_ ACSR1_2B_4	15:0	RO	0	Bytes 4 and 5 of audio Group B channel status for channels 1 and 2.
4*63	ACSR1_2B_ BYTE6_7	AUD_EXT_*_ ACSR1_2B_6	15:0	RO	0	Bytes 6 and 7 of audio Group B channel status for channels 1 and 2.
4*64	ACSR1_2B_ BYTE8_9	AUD_EXT_*_ ACSR1_2B_8	15:0	RO	0	Bytes 8 and 9 of audio Group B channel status for channels 1 and 2.

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Kent Lin
DIVA Laboratories, Ltd.
09/08/2026

4*65	ACSR1_2B_ BYTE10_11	AUD_EXT_*_ ACSR1_2B_10	15:0	RO	0	Bytes 10 and 11 of audio Group B channel status for channels 1 and 2.
4*66	ACSR1_2B_ BYTE12_13	AUD_EXT_*_ ACSR1_2B_12	15:0	RO	0	Bytes 12 and 13 of audio Group B channel status for channels 1 and 2.
4*67	ACSR1_2B_ BYTE14_15	AUD_EXT_*_ ACSR1_2B_14	15:0	RO	0	Bytes 14 and 15 of audio Group B channel status for channels 1 and 2.
4*68	ACSR1_2B_ BYTE16_17	AUD_EXT_*_ ACSR1_2B_16	15:0	RO	0	Bytes 16 and 17 of audio Group B channel status for channels 1 and 2.
4*69	ACSR1_2B_ BYTE18_19	AUD_EXT_*_ ACSR1_2B_18	15:0	RO	0	Bytes 18 and 19 of audio Group B channel status for channels 1 and 2.
4*6A	ACSR1_2B_ BYTE20_21	AUD_EXT_*_ ACSR1_2B_20	15:0	RO	0	Bytes 20 and 21 of audio Group B channel status for channels 1 and 2.
4*6B	ACSR1_2B_ BYTE22	RSVD	15:8	RO	0	Reserved.
		AUD_EXT_*_ ACSR1_2B_22	7:0	RO	0	Bytes 22 of audio Group B channel status for channels 1 and 2.
4*6C to 4*6F	RSVD	RSVD	15:0	RO	0	Reserved.
4*70	ACSR3_4B_ BYTE0_1	AUD_EXT_*_ ACSR3_4B_0	15:0	RO	0	Bytes 0 and 1 of audio Group B channel status for channels 3 and 4.
4*71	ACSR3_4B_ BYTE2_3	AUD_EXT_*_ ACSR3_4B_2	15:0	RO	0	Bytes 2 and 3 of audio Group B channel status for channels 3 and 4.
4*72	ACSR3_4B_ BYTE4_5	AUD_EXT_*_ ACSR3_4B_4	15:0	RO	0	Bytes 4 and 5 of audio Group B channel status for channels 3 and 4.
4*73	ACSR3_4B_ BYTE6_7	AUD_EXT_*_ ACSR3_4B_6	15:0	RO	0	Bytes 6 and 7 of audio Group B channel status for channels 3 and 4.
4*74	ACSR3_4B_ BYTE8_9	AUD_EXT_*_ ACSR3_4B_8	15:0	RO	0	Bytes 8 and 9 of audio Group B channel status for channels 3 and 4.
4*75	ACSR3_4B_ BYTE10_11	AUD_EXT_*_ ACSR3_4B_10	15:0	RO	0	Bytes 10 and 11 of audio Group B channel status for channels 3 and 4.

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DIVA Laboratories Ltd.
09/08/2026

4*76	ACSR3_4B_BYTE12_13	AUD_EXT_*_ACSR3_4B_12	15:0	RO	0	Bytes 12 and 13 of audio Group B channel status for channels 3 and 4.
4*77	ACSR3_4B_BYTE14_15	AUD_EXT_*_ACSR3_4B_14	15:0	RO	0	Bytes 14 and 15 of audio Group B channel status for channels 3 and 4.
4*78	ACSR3_4B_BYTE16_17	AUD_EXT_*_ACSR3_4B_16	15:0	RO	0	Bytes 16 and 17 of audio Group B channel status for channels 3 and 4.
4*79	ACSR3_4B_BYTE18_19	AUD_EXT_*_ACSR3_4B_18	15:0	RO	0	Bytes 18 and 19 of audio Group B channel status for channels 3 and 4.
4*7A	ACSR3_4B_BYTE20_21	AUD_EXT_*_ACSR3_4B_20	15:0	RO	0	Bytes 20 and 21 of audio Group B channel status for channels 3 and 4.
4*7B	ACSR3_4B_BYTE22	RSVD	15:8	RO	0	Reserved.
		AUD_EXT_*_ACSR3_4B_22	7:0	RO	0	Bytes 22 of audio Group B channel status for channels 3 and 4.
4*7C to 4*7F	RSVD	RSVD	15:0	RO	0	Reserved.
4*80 to 4*96	ACSR_BYTE_0 to ACSR_BYTE_22	RSVD	15:8	RO	0	Reserved.
		AUD_EXT_*_ACSR0 to AUD_EXT_*_ACSR22	7:0	WO	0	Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. 8 bits per register for 23 registers.
4*97 to 4*99	RSVD	RSVD	15:0	RO	0	Reserved.

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09/08/2026

4.2.6. SDI Audio Embedding Control Registers

Table 4-11 SDI Audio Embedding Control and Status Registers

Address$_h$	**Register Name**	**Parameter Name**	**Bit Slice**	**R/W**	**Reset Value$_h$**	**Description**

5*00	CFG_AUD	AUD_INS_*_CHANNEL_STATUS_INS_NO_MOD	15:15	RW	0	By default, channel status coming from HDMI will be converted from consumer to professional, or left as professional if it comes in as professional. Set this bit to keep the channel status as consumer if it comes in as consumer.
		AUD_INS_*_CTRB_ON	14:14	RW	1	Specifies the embedding of the Group B audio control packets. Active HIGH.
		AUD_INS_*_ASXB	13:13	RW	0	Group B asynchronous mode. Active HIGH.
		AUD_INS_*_AFNB_AUTO	12:12	RW	1	Enables Group B audio frame number generation. Active HIGH.
		AUD_INS_*_CTRA_ON	11:11	RW	1	Specifies the embedding of Group A audio control packets. Active HIGH.
		AUD_INS_*_ASXA	10:10	RW	0	Group A asynchronous mode.
		AUD_INS_*_AFNA_AUTO	9:9	RW	1	Enables Group A audio frame number generation.
		AUD_INS_*_AFN_OFS	8:6	RW	0	Offset to add to generated Audio Frame Number. Must be in the range of 0 to 4.
		AUD_INS_*_C_EXTEND_IDB	5:5	RW	0	When set to 0, Group B will embed audio groups 1, 2, 3 or 4. When set to 1, Group B will embed audio groups 5, 6, 7 or 8.
		AUD_INS_*_IDB	4:3	RW	1, 3	Specifies the Group B SMPTE audio group to embed. 00_b = Audio group #1or #5 01_b = Audio group #2 or #6 10_b = Audio group #3 or #7 11_b = Audio group #4 or #8
		AUD_INS_*_C_EXTEND_IDA	2:2	RW	0	When set to 0, Group A will embed audio groups 1, 2, 3 or 4. When set to 1, Group A will embed audio groups 5, 6, 7 or 8.

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09/03/2026

		AUD_INS_*_IDA	1:0	RW	0, 2	Specifies the Group A SMPTE audio group to embed. 00_b = Audio group #1 or #5 01_b = Audio group #2 or #6 10_b = Audio group #3 or #7 11_b = Audio group #4 or #8
5*01	GROUP_REPL	RSVD	15:3	RO	0	Reserved.
		AUD_INS_*_ ONE_AGR	2:2	RW	0	Specifies the replacement of just Group A 0 = Replace both Group A and Group B. 1 = Replace only Group A.
		AUD_INS_*_ CTR_AGR	1:1	RW	0	Selects replacement of audio control packets. 0 = Do not replace audio control packets. 1 = Replace all audio control packets.
		AUD_INS_*_AGR	0:0	RW	0	Selects replacement of audio control packets. 0 = Do not replace audio control packets. 1 = Replace all audio control packets.
5*02	CHANNEL_ STAT_REGEN	RSVD	15:1	RWPT	0	Reserved. Do not change.
		AUD_INS_*_ ACS_REGEN	0:0	RWPT	0	Specifies that Audio Channel Status of all channels should be replaced with ACSR[183:0] field. LOW = Do not replace Channel Status HIGH = Replace Channel Status of all channels
5*03	HD_STATUS_1	RSVD	15:2	RO	0	Reserved.
		AUD_INS_*_ACS_ APPLY_WAITB	1:1	RO	0	Set while the multiplexer is waiting for a status boundary in Group B before applying the ACSR[183:0] data to that group.
		AUD_INS_*_ACS_ APPLY_WAITA	0:0	RO	0	ACS_APPLY: Cause channel status data in ACSR[183:0] to be transferred to the channel status replacement mechanism. The transfer shall not occur until the next status boundary. ACS_APPLY_WAITA: Set while the multiplexer is waiting for a status boundary in Group A before applying the ACSR[183:0] data.

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09/08/2026

5*04	HD_STATUS_2	AUD_INS_*_ACPG8_DET	15:15	RO	0	Set while SMPTE Group 8 audio control packets are detected.
		AUD_INS_*_ACPG7_DET	14:14	RO	0	Set while SMPTE Group 7 audio control packets are detected.
		AUD_INS_*_ACPG6_DET	13:13	RO	0	Set while SMPTE Group 6 audio control packets are detected.
		AUD_INS_*_ACPG5_DET	12:12	RO	0	Set while SMPTE Group 5 audio control packets are detected.
		AUD_INS_*_ACPG4_DET	11:11	RO	0	Set while SMPTE Group 4 audio control packets are detected.
		AUD_INS_*_ACPG3_DET	10:10	RO	0	Set while SMPTE Group 3 audio control packets are detected.
		AUD_INS_*_ACPG2_DET	9:9	RO	0	Set while SMPTE Group 2 audio control packets are detected.
		AUD_INS_*_ACPG1_DET	8:8	RO	0	Set while SMPTE Group 1 audio control packets are detected.
		AUD_INS_*_ADPG8_DET	7:7	RO	0	Set while SMPTE Group 8 audio data packets are detected.
		AUD_INS_*_ADPG7_DET	6:6	RO	0	Set while SMPTE Group 7 audio data packets are detected.
		AUD_INS_*_ADPG6_DET	5:5	RO	0	Set while SMPTE Group 6 audio data packets are detected.
		AUD_INS_*_ADPG5_DET	4:4	RO	0	Set while SMPTE Group 5 audio data packets are detected.
		AUD_INS_*_ADPG4_DET	3:3	RO	0	Set while SMPTE Group 4 audio data packets are detected.
		AUD_INS_*_ADPG3_DET	2:2	RO	0	Set while SMPTE Group 3 audio data packets are detected.
		AUD_INS_*_ADPG2_DET	1:1	RO	0	Set while SMPTE Group 2 audio data packets are detected.
		AUD_INS_*_ADPG1_DET	0:0	RO	0	Set while SMPTE Group 1 audio data packets are detected.

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09/08/2026

5*05	HD_STATUS_3	RSVD	15:12	RO	0	Reserved.
		AUD_INS_*_HELD_AES_ERR	11:8	RO	0	AES received errors for the 4 audio channel pairs.
		AUD_INS_*_INTERRUPT	7:7	RO	0	Asserted when any audio insertion interrupts are pending.
		RSVD	6:4	RO	0	Reserved.
		AUD_INS_*_AES_ERRD	3:3	RO	0	Stereo Pair D audio input parity error when using AES format. Automatically cleared when read.
		AUD_INS_*_AES_ERRC	2:2	RO	0	Stereo Pair C audio input parity error when using AES format. Automatically cleared when read.
		AUD_INS_*_AES_ERRB	1:1	RO	0	Stereo Pair B audio input parity error when using AES format. Automatically cleared when read.
		AUD_INS_*_AES_ERRA	0:0	RO	0	Stereo Pair A audio input parity error when using AES format. Automatically cleared when read.
5*06	CASCADE	RSVD	15:1	RO	0	Reserved.
		AUD_INS_*_EN_CASCADE	0:0	RW	0, 1	If HIGH, puts the audio insertion into cascade mode. This bit is only effective if the AGR bit is LOW.
5*07	SERIAL_AUDIO_FORMAT	AUD_INS_*_AMD	15:14	RW	3	Audio input format selector for Stereo Pair D input channels 7 and 8. 00 = AES/EBU 01 = Serial Left Justified 10 = Serial Right Justified 11 = I^2S
		AUD_INS_*_AMC	13:12	RW	3	Audio input format selector for Stereo Pair C input channels 5 and 6 (see above for decoding).
		AUD_INS_*_AMB	11:10	RW	3	Audio input format selector for Stereo Pair B input channels 3 and 4 (see above for decoding).

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09/08/2026

		AUD_INS_*_AMA	9:8	RW	3	Audio input format selector for Stereo Pair A input channels 1 and 2 (see above for decoding).
		AUD_INS_*_MUTE8	7:7	RW	0	Audio input channel 8 mute enable.
		AUD_INS_*_MUTE7	6:6	RW	0	Audio input channel 7 mute enable.
		AUD_INS_*_MUTE6	5:5	RW	0	Audio input channel 6 mute enable.
		AUD_INS_*_MUTE5	4:4	RW	0	Audio input channel 5 mute enable.
		AUD_INS_*_MUTE4	3:3	RW	0	Audio input channel 4 mute enable.
		AUD_INS_*_MUTE3	2:2	RW	0	Audio input channel 3 mute enable.
		AUD_INS_*_MUTE2	1:1	RW	0	Audio input channel 2 mute enable.
		AUD_INS_*_MUTE1	0:0	RW	0	Audio input channel 1 mute enable.
5*08	CHANNEL_XP_GRPA	RSVD	15:15	RO	0	Reserved.
		AUD_INS_*_GPA_WCLK_SRC	14:12	RW	0	Group A word clock source selector.
		AUD_INS_*_GPA_CH4_SRC	11:9	RW	3	Group A channel 4 source selector.
		AUD_INS_*_GPA_CH3_SRC	8:6	RW	2	Group A channel 3 source selector.
		AUD_INS_*_GPA_CH2_SRC	5:3	RW	1	Group A channel 2 source selector.
		AUD_INS_*_GPA_CH1_SRC	2:0	RW	0	Group A channel 1 source selector.
5*09	CHANNEL_XP_GRPB	RSVD	15:15	RO	0	Reserved.
		AUD_INS_*_GPB_WCLK_SRC	14:12	RW	4	Group B word clock source selector.
		AUD_INS_*_GPB_CH4_SRC	11:9	RW	7	Group B channel 4 source selector.
		AUD_INS_*_GPB_CH3_SRC	8:6	RW	6	Group B channel 3 source selector.

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09/08/2026

		AUD_INS_*_GPB_CH2_SRC	5:3	RW	5	Group B channel 2 source selector.
		AUD_INS_*_GPB_CH1_SRC	2:0	RW	4	Group B channel 1 source selector.
5*0A	INTERRUPT_MASK_1	EN_ACPG8_DET	15:15	RW	0	Asserts interrupt when ACPG8_DET flag is set.
		EN_ACPG7_DET	14:14	RW	0	Asserts interrupt when ACPG7_DET flag is set.
		EN_ACPG6_DET	13:13	RW	0	Asserts interrupt when ACPG6_DET flag is set.
		EN_ACPG5_DET	12:12	RW	0	Asserts interrupt when ACPG5_DET flag is set.
		EN_ACPG4_DET	11:11	RW	0	Asserts interrupt when ACPG4_DET flag is set.
		EN_ACPG3_DET	10:10	RW	0	Asserts interrupt when ACPG3_DET flag is set.
		EN_ACPG2_DET	9:9	RW	0	Asserts interrupt when ACPG2_DET flag is set.
		EN_ACPG1_DET	8:8	RW	0	Asserts interrupt when ACPG1_DET flag is set.
		EN_ADPG8_DET	7:7	RW	0	Asserts interrupt when ADPG8_DET flag is set.
		EN_ADPG7_DET	6:6	RW	0	Asserts interrupt when ADPG7_DET flag is set.
		EN_ADPG6_DET	5:5	RW	0	Asserts interrupt when ADPG6_DET flag is set.
		EN_ADPG5_DET	4:4	RW	0	Asserts interrupt when ADPG5_DET flag is set.
		EN_ADPG4_DET	3:3	RW	0	Asserts interrupt when ADPG4_DET flag is set.
		EN_ADPG3_DET	2:2	RW	0	Asserts interrupt when ADPG3_DET flag is set.
		EN_ADPG2_DET	1:1	RW	0	Asserts interrupt when ADPG2_DET flag is set.
		EN_ADPG1_DET	0:0	RW	0	Asserts interrupt when ADPG1_DET flag is set.
5*0B	INTERRUPT_MASK_2	RSVD	15:6	RO	0	Reserved.
		AUD_INS_*_EN_MUX_ERRB	5:5	RW	0	Asserts AUDIO_INT when the MUX_ERRB flag is set.

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09/08/2026

		AUD_INS_*_EN_MUX_ERRA	4:4	RW	0	Asserts AUDIO_INT when the MUX_ERRA flag is set.
		AUD_INS_*_EN_AES_ERRD	3:3	RW	0	Asserts AUDIO_INT when the AES_ERRD flag is set.
		AUD_INS_*_EN_AES_ERRC	2:2	RW	0	Asserts AUDIO_INT when the AES_ERRC flag is set.
		AUD_INS_*_EN_AES_ERRB	1:1	RW	0	Asserts AUDIO_INT when the AES_ERRB flag is set.
		AUD_INS_*_EN_AES_ERRA	0:0	RW	0	Asserts AUDIO_INT when the AES_ERRA flag is set.
5*0C	ACTIVE_CHANNEL	RSVD	15:13	RO	0	Reserved.
		AUD_INS_*_MUTE_ALL	12:12	RW	0	Mutes all input audio channels.
		AUD_INS_*_LSB_FIRSTD	11:11	RW	0	Causes the fourth stereo pair serial input formats to use LSB first.
		AUD_INS_*_LSB_FIRSTC	10:10	RW	0	Causes the third stereo pair serial input formats to use LSB first.
		AUD_INS_*_LSB_FIRSTB	9:9	RW	0	Causes the second stereo pair serial input formats to use LSB first.
		AUD_INS_*_LSB_FIRSTA	8:8	RW	0	Causes the first stereo pair serial input formats to use LSB first.
		AUD_INS_*_ACT8	7:7	RW	1	Specifies embedding of Group B channel 8. Active HIGH.
		AUD_INS_*_ACT7	6:6	RW	1	Specifies embedding of Group B channel 7. Active HIGH.
		AUD_INS_*_ACT6	5:5	RW	1	Specifies embedding of Group B channel 6. Active HIGH.
		AUD_INS_*_ACT5	4:4	RW	1	Specifies embedding of Group B channel 5. Active HIGH.
		AUD_INS_*_ACT4	3:3	RW	1	Specifies embedding of Group B channel 4. Active HIGH.

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09/03/2026

		AUD_INS_*_ACT3	2:2	RW	1	Specifies embedding of Group B channel 3. Active HIGH.
		AUD_INS_*_ACT2	1:1	RW	1	Specifies embedding of Group B channel 2. Active HIGH.
		AUD_INS_*_ACT1	0:0	RW	1	Specifies embedding of Group B channel 1. Active HIGH.
5*0D	XPOINT_ERROR	RSVD	15:3	RO	0	Reserved.
		AUD_INS_*_ MUX_ERRB	2:2	RO	0	Set in Cascade mode when the incoming video contains packets with the same group number as Group B.
		AUD_INS_*_ MUX_ERRA	1:1	RO	0	Set in Cascade mode when the incoming video contains packets with the same group number as Group A.
		AUD_INS_*_ XPOINT_ERROR	0:0	RO	0	Set when the crosspoint switch is configured to put the same audio channel in both Group A and Group B.
5*0E	CHANNEL_ STATUS_REG_1	AUD_INS_*_ ACSR_BYTE_2	15:8	RW	8	Audio channel status block byte 2.
		AUD_INS_*_ ACSR_BYTE_1	7:0	RW	85	Audio channel status block byte 1.
5*0F	CHANNEL_ STATUS_REG_2	AUD_INS_*_ ACSR_BYTE_4	15:8	RW	0	Audio channel status block byte 4.
		AUD_INS_*_ ACSR_BYTE_3	7:0	RW	2C	Audio channel status block byte 3.
5*10	CHANNEL_ STATUS_REG_3	AUD_INS_*_ ACSR_BYTE_6	15:8	RW	0	Audio channel status block byte 6.
		AUD_INS_*_ ACSR_BYTE_5	7:0	RW	0	Audio channel status block byte 5.
5*11	CHANNEL_ STATUS_REG_4	AUD_INS_*_ ACSR_BYTE_8	15:8	RW	0	Audio channel status block byte 8.
		AUD_INS_*_ ACSR_BYTE_7	7:0	RW	0	Audio channel status block byte 7.
5*12	CHANNEL_ STATUS_REG_5	AUD_INS_*_ ACSR_BYTE_10	15:8	RW	0	Audio channel status block byte 10.

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09/08/2026

		AUD_INS_*_ ACSR_BYTE_9	7:0	RW	0	Audio channel status block byte 9.
5*13	CHANNEL_ STATUS_REG_6	AUD_INS_*_ ACSR_BYTE_12	15:8	RW	0	Audio channel status block byte 12.
		AUD_INS_*_ ACSR_BYTE_11	7:0	RW	0	Audio channel status block byte 11.
5*14	CHANNEL_ STATUS_REG_7	AUD_INS_*_ ACSR_BYTE_14	15:8	RW	0	Audio channel status block byte 14.
		AUD_INS_*_ ACSR_BYTE_13	7:0	RW	0	Audio channel status block byte 13.
5*15	CHANNEL_ STATUS_REG_8	AUD_INS_*_ ACSR_BYTE_16	15:8	RW	0	Audio channel status block byte 16.
		AUD_INS_*_ ACSR_BYTE_15	7:0	RW	0	Audio channel status block byte 15.
5*16	CHANNEL_ STATUS_REG_9	AUD_INS_*_ ACSR_BYTE_18	15:8	RW	0	Audio channel status block byte 18.
		AUD_INS_*_ ACSR_BYTE_17	7:0	RW	0	Audio channel status block byte 17.
5*17	CHANNEL_ STATUS_REG_10	AUD_INS_*_ ACSR_BYTE_20	15:8	RW	0	Audio channel status block byte 20.
		AUD_INS_*_ ACSR_BYTE_19	7:0	RW	0	Audio channel status block byte 19.
5*18	CHANNEL_ STATUS_REG_11	AUD_INS_*_ ACSR_BYTE_22	15:8	RW	0	Audio channel status block byte 22.
		AUD_INS_*_ ACSR_BYTE_21	7:0	RW	0	Audio channel status block byte 21.
5*19	CHANNEL_ STATUS_REG_12	RSVD	15:8	RO	0	Reserved.
		AUD_INS_*_ ACSR_BYTE_23	7:0	RW	0	Audio channel status block byte 23.
5*1A	AUDIO_CTRL_ GRPA_GRPB_ REG_0	RSVD	15:1	RO	0	Reserved.
		AUD_INS_*_ AUDIO_RATE	0:0	RW	0	Indicates audio sampling rate. Set to 0 for 48kHz audio. Set to 1 for 96kHz audio.

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09/08/2026

5*1B	AUDIO_CTRL_GRPA_REG_1	RSVD	15:9	RO	0	Reserved.
		AUD_INS_*_DEL1_2A_BYTE_1	8:1	RW	0	Group A delay data for channel 1 & 2.
		AUD_INS_*_EBIT1_2A	0:0	RW	0	Group A delay data valid flag for channel 1 & 2.
5*1C	AUDIO_CTRL_GRPA_REG_2	RSVD	15:9	RO	0	Reserved.
		AUD_INS_*_DEL1_2A_BYTE_2	8:0	RW	0	Group A delay data for channel 1 & 2.
5*1D	AUDIO_CTRL_GRPA_REG_3	RSVD	15:9	RO	0	Reserved.
		AUD_INS_*_DEL1_2A_BYTE_3	8:0	RW	0	Group A delay data for channel 1 & 2.
5*1E	AUDIO_CTRL_GRPA_REG_4	RSVD	15:9	RO	0	Reserved.
		AUD_INS_*_DEL3_4A_BYTE_1	8:1	RW	0	Group A delay data for channel 3 & 4.
		AUD_INS_*_EBIT3_4A	0:0	RW	0	Group A delay data valid flag for channel 3 & 4.
5*1F	AUDIO_CTRL_GRPA_REG_5	RSVD	15:9	RO	0	Reserved.
		AUD_INS_*_DEL3_4A_BYTE_2	8:0	RW	0	Group A delay data for channel 3 & 4.
5*20	AUDIO_CTRL_GRPA_REG_6	RSVD	15:9	RO	0	Reserved.
		AUD_INS_*_DEL3_4A_BYTE_3	8:0	RW	0	Group A delay data for channel 3 & 4.
5*21	AUDIO_CTRL_GRPB_REG_1	RSVD	15:9	RO	0	Reserved.
		AUD_INS_*_DEL1_2B_BYTE_1	8:1	RW	0	Group B delay data for channel 1 & 2.
		AUD_INS_*_EBIT1_2B	0:0	RW	0	Group B delay data valid flag for channel 1 & 2.
5*22		RSVD	15:9	RO	0	Reserved.

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	AUDIO_CTRL_ GRPB_REG_2	AUD_INS_*_ DEL1_2B_BYTE_2	8:0	RW	0	Group B delay data for channel 1 & 2.
5*23	AUDIO_CTRL_ GRPB_REG_3	RSVD	15:9	RO	0	Reserved.
		AUD_INS_*_ DEL1_2B_BYTE_3	8:0	RW	0	Group B delay data for channel 1 & 2.
5*24	AUDIO_CTRL_ GRPB_REG_4	RSVD	15:9	RO	0	Reserved.
		AUD_INS_*_ DEL3_4B_BYTE_1	8:1	RW	0	Group B delay data for channel 3 & 4.
		AUD_INS_*_ EBIT3_4B	0:0	RW	0	Group B delay data for channel 3 & 4.
5*25	AUDIO_CTRL_ GRPB_REG_5	RSVD	15:9	RO	0	Reserved.
		AUD_INS_*_ DEL3_4B_BYTE_2	8:0	RW	0	Group B delay data for channel 3 & 4.
5*26	AUDIO_CTRL_ GRPB_REG_6	RSVD	15:9	RO	0	Reserved.
		AUD_INS_*_ DEL3_4B_BYTE_3	8:0	RW	0	Group B delay data for channel 3 & 4.
5*27	RSVD	RSVD	15:0	RW	0	Reserved. Do not change.
5*28	CHANNEL_ STATUS_CFG_REG	RSVD	15:1	RO	0	Reserved.
		AUD_INS_*_ OVERRIDE_ HDMI_CH_STAT	0:0	RW	0	When in HDMI ® SDI mode, takes channel status from HDMI when LOW, from CSRs when HIGH.
5*29 to 5*2C	RSVD	RSVD	15:0	RO	0	Reserved.
5*2D	AUDIO_BLANKING	RSVD	15:1	RW	0	Reserved. Do not change.
		AUD_INS_*_ DISABLE_ANC_ BLANKING	0:0	RW	0	When HIGH, overrides the blanking in the audio insertion such that blanking values will not be updated. Can be set HIGH when no audio is being deleted.

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4.2.7. HDMI Rx Control Registers

Table 4-12 HDMI Rx Control and Status Register

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
6000	HDMI_RX_CTRL	RSVD	15:13	RW	0	Reserved. Do not change.
		HPD_CSR_OVR	12:12	RW	0	Enables override of the HPD signal.
		HPD_CSR	11:11	RW	1	Overrides internally generated HPD signal when HPD_CSR_OVR is set to '1'
		CLK_CHANGE_EN	10:10	RW	1	Set to '0' to disable clock change strobe used to reset PLL and Rx PMA.
		LINE_STABLE_OVR	9:9	RW	0	Enables override of the LINE_STABLE signal.
		LINE_STABLE_REG	8:8	RW	0	Overrides internally GENERATEDLINE_STABLE signal when LINE_STABLE_OVR is set to '1'.
		CLOCK_STABLE_OVR	7:7	RW	0	Enables override of the CLOCK_STABLE signal.
		CLOCK_STABLE	6:6	RW	1	Overrides internally generated CLOCK_STABLE signal when CLOCK_STABLE_OVR is set to '1'.
		CLOCK_RATIO_OVR	5:5	RW	0	Enables override of the CLOCK_RATIO signal.
		CLOCK_RATIO	4:4	RW	0	Overrides the internally generated clock ratio signal (high for rates >3G) when CLOCK_RATIO_OVR is set to '1'.
		HDMI_SCRAMBLER_EN_OVR	3:3	RW	0	Enables override of the scrambler enable signal.
		HDMI_SCRAMBLER_EN	2:2	RW	0	Overrides the internal scrambler enable value (high for rates >3G) if HDMI_SCRAMBLER_EN_OVR is set to '1'.
		HDMI_RX_CABLE_DETECT_OVR	1:1	RW	0	Enable cable detect pin override.

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09/08/2026

		HDMI_RX_ CABLE_DETECT	0:0	RW	0	Overrides cable detect (5V) from pin (N10) if HDMI_RX_CABLE_DETECT_OVR is set to '1'.
6001	HDMI_REC_ STATUS	RSVD	15:14	RO	0	Reserved.
		HDMI_REC_ STATUS	13:13	RO	0	Sync polarity (1 = positive sync, 0 = negative sync).
		DATAPATH_RESET	12:12	RO	0	TBD.
		LINK_CTRL_RESYNC	11:11	RO	0	TBD.
		LINK_CTRL_RST	10:10	RO	0	TBD.
		CRG_HDMI_RX_ TMDS_ASYNC_ RST_D2	9:9	RO	0	TBD.
		HDMI_CTRL_RST	8:8	RO	0	TBD.
		PMA_READY_I	7:7	RO	0	TBD.
		LINE_STABLE	6:6	RO	0	TBD.
		HDMI_REC_STAT_ CH_ALIGNED	5:5	RO	0	TBD.
		HDMI_REC_STAT_ WRD_ALIGNED	4:4	RO	0	TBD.
		HDMI_REC_STAT_ DEC_ERR	3:3	RO	0	TBD.
		HDMI_REC_STAT_ SYNC_FIFO_OVFL	2:2	RO	0	TBD.
		HDMI_REC_STAT_ CH_ALIGN_ERR	1:1	RO	0	TBD.

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09/08/2026

		HDMI_REC_STAT_WRD_ALIGN_ERR	0:0	RO	0	TBD.
6002	HDMI_MISC_STATUS	VIDEO_STABLE	15:15	RO	0	TBD.
		FORMAT	14:14	RO	0	TBD.
		VIDEO_STABLE	13:13	RO	0	TBD.
		SCDC_SCRAMBLING_STATUS	12:12	RO	0	TBD.
		SCDC_STATUS_UPDATE	11:11	RO	0	TBD.
		SCDC_ERR_DET_CHECKUM	10:10	RO	0	TBD.
		SCDC_CH2_ERR_DET_VALID	9:9	RO	0	TBD.
		SCDC_CH1_ERR_DET_VALID	8:8	RO	0	TBD.
		SCDC_CH0_ERR_DET_VALID	7:7	RO	0	TBD.
		SCDC_CLOCK_DETECTED	6:6	RO	0	TBD.
		SCDC_CH2_LOCKED	5:5	RO	0	TBD.
		SCDC_CH1_LOCKED	4:4	RO	0	TBD.
		SCDC_CH0_LOCKED	3:3	RO	0	TBD.
		CLOCK_RATIO	2:2	RO	0	TBD.
		SCRAMBLER_EN	1:1	RO	0	TBD.
		CABLE_DETECTED	0:0	RO	0	TBD.

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6003	HDMI_MISC_STATUS2	HDMI_REC_TEST_LOST_SYNC	15:13	RO	0	TBD.
		HDMI_REC_AUX_ERR_CH2	12:12	RO	0	TBD.
		HDMI_REC_AUX_ERR_CH1	11:11	RO	0	TBD.
		HDMI_REC_AUX_ERR_CH0	10:10	RO	0	TBD.
		HDMI_REC_CH_ALIGN_OVERFLOW	9:9	RO	0	TBD.
		HDMI_REC_CH_ALIGN_ERR_CH2	8:8	RO	0	TBD.
		HDMI_REC_CH_ALIGN_ERR_CH1	7:7	RO	0	TBD.
		HDMI_REC_CH_ALIGN_ERR_CH0	6:6	RO	0	TBD.
		HDMI_REC_WRD_ALIGN_ERR_CH2	5:5	RO	0	TBD.
		HDMI_REC_WRD_ALIGN_ERR_CH1	4:4	RO	0	TBD.
		HDMI_REC_WRD_ALIGN_ERR_CH0	3:3	RO	0	TBD.
		HDMI_REC_LOST_SYNC_CH2	2:2	RO	0	TBD.
		HDMI_REC_LOST_SYNC_CH1	1:1	RO	0	TBD.
		HDMI_REC_LOST_SYNC_CH0	0:0	RO	0	TBD.
6004	STREAM_SEL	RSVD	15:8	RO	0	Reserved.
		FORMAT_DETECT_REG	7:6	RW	1	0x0 = default 0x1 = Enable format detection on Video Guard Band 0x2 = Enable format detection on Data Guard Band

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09/08/2026

		CH2_RX_SRC_SEL	5:4	RW	2	Selects TMDS input stream to ch2.
		CH1_RX_SRC_SEL	3:2	RW	1	Selects TMDS input stream to ch1.
		CH0_RX_SRC_SEL	1:0	RW	0	Selects TMDS input stream to ch0.
6005 to 6013	RSVD_REG	RSVD	15:0	RW	N/A	Reserved. Do not change.
6014	HVF_STAT_SEL	RSVD	15:12	RO	0	Reserved.
		HVF2_SEL	11:8	RW	0	Select H, V and F from HDMI_RX to send to GPIO selection block H, V, F_IN[2].
		HVF1_SEL	7:4	RW	0	Select H, V and F from HDMI_RX to send to GPIO selection block H, V, F_IN[1].
		HVF0_SEL	3:0	RW	0	Select H, V and F from HDMI_RX to send to GPIO selection block H, V, F_IN[0].
6015	VIDEO_STABLE	RSVD	15:2	RO	0	Reserved.
		VIDEO_STABLE_OVR	1:1	RW	0	VIDEO_STABLE overwrite enable.
		VIDEO_STABLE_REG	0:0	RW	0	VIDEO_STABLE.
6016	HDMI_RX_CH_STATUS_SELECT	RSVD	15:1	RO	0	Reserved.
		HDMI_RX_CH_STATUS_SELECT	0:0	RW	0	When HIGH, the HDMI Rx audio extraction block will output 4 audio channels status values that correspond to audio channel 2, 4, 6 and 8 (second channel in stereo pair). When LOW, the HDMI Rx block will output 4 audio channel status values that correspond to audio channels 1, 3, 5 and 7.
6017	HDMI_RX_PACKET_DETECT	RSVD	15:8	RO	0	Reserved.
		HDMI_RX_PGR_PKT_DETECT	7:7	ROCW	0	When HIGH, indicates that a generic packet with the 8 LSBs of its header matching the HDMI_RX_PGR_HEADER has been received. When LOW, such a packet has not been received.

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09/03/2026

		HDMI_RX_DR_INFOFRAME_PKT_DETECT	6:6	ROCW	0	When HIGH, indicates that a Dynamic Range and Mastering InfoFrame packet has been received. When LOW, no Dynamic Range and Mastering InfoFrame packet has been received.
		HDMI_RX_AVI_INFOFRAME_PKT DETECT	5:5	ROCW	0	When HIGH, indicates that an AVI InfoFrame packet has been received. When LOW, no AVI InfoFrame packet has been received.
		HDMI_RX_VENDOR_INFOFRAME_PKT_DETECT	4:4	ROCW	0	When HIGH, indicates that a vendor specific InfoFrame packet has been received. When LOW, no vendor specific InfoFrame packet has been received.
		HDMI_RX_GENERAL_CTRL_PKT_DETECT	3:3	ROCW	0	When HIGH, indicates that a general control packet has been received. When LOW, no general control packet has been received.
		HDMI_RX_AUDIO_CLK_REGEN_PKT_DETECT	2:2	ROCW	0	When HIGH, indicates that an audio clock regeneration packet has been received. When LOW, no audio clock regeneration packet has been received.
		HDMI_RX_AUDIO_INFOFRAME_PKT_DETECT	1:1	ROCW	0	When HIGH, indicates that an audio InfoFrame packet has been received. When LOW, no audio InfoFrame packet has been received.
		HDMI_RX_AUDIO_SAMPLE_PKT_DETECT	0:0	ROCW	0	When HIGH, indicates that an audio sample packet has been received. When LOW, no audio sample packet has been received.
6018	HDMI_RX_AUDIO_SMPL_PKT_FIELDS	RSVD	15:9	RO	0	Reserved.
		HDMI_RX_AUDIO_SAMPLE_FLAT	8:5	RO	0	Audio sample packet field. When a particular bit is HIGH it indicates that the corresponding sub-packet carries no useful audio data. When a particular bit is LOW it indicates that the corresponding sub-packet carries actual audio data.

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		HDMI_RX_ AUDIO_ SAMPLE_PRESENT	4:1	RO	0	Audio sample packet field: 0000 = No sub-packet contain audio samples 0001 = Only sub-packet 0 contains audio samples 0011 = sub-packet 0 and 1 contain audio samples 0111 = sub-packet 0, 1 and 2 contain audio samples 1111 = All sub-packet contain audio samples
		HDMI_RX_ AUDIO_LAYOUT_BIT	0:0	RO	0	Audio sample packet field. When LOW, indicates that audio sample packets carry only samples of channels 1 and 2. When HIGH, indicates that audio sample packets carry samples of channels 1 to 8.
6019	HDMI_RX_ AUDIO_SMPL_ PKT_FIELDS_2	HDMI_RX_ AUDIO_SAMPLE_ PKT_TYPE	15:8	RO	0	Audio sample packet field. Lower byte of an audio sample packet header.
		HDMI_RX_ AUDIO_ CHANNEL_VALID	7:0	RO	0	Audio sample packet field. Validity bits of the 8 audio channels of an audio sample packet: Bit 0 = channel 1 Bit 1 = channel 2 ... Bit 7 = channel 8
601A	HDMI_RX_ AUDIO_ INFOFRAME_ PKT_FIELDS	RSVD	15:15	RO	0	Reserved.
		HDMI_RX_AUD_ INFO_CHN_ALLOC	14:9	RO	0	Audio InfoFrame packet field. Channel/Speaker Allocation. See CEA-861-D section 6.6.2 for details.
		HDMI_RX_AUD_ INFO_CODING_TYPE	6:3	RO	0	Audio InfoFrame packet field. Coding Type. These bits should always be set to 0 according to the HDMI Specification 1.4b.
		HDMI_RX_AUD_ INFO_ CHANNEL_COUNT	2:0	RO	0	Audio InfoFrame packet field. Channel count: 000 = Refer to Stream Header 001 = 2ch 010 = 3ch 011 = 4ch 100 = 5ch 101 = 6ch 110 = 7ch 111 = 8ch
601B		RSVD	15:10	RO	0	Reserved.

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	HDMI_RX_AUDIO_INFOFRAME_PKT_FIELDS_2	HDMI_RX_AUD_INFO_SAMPLING_FREQ	9:7	RO	0	Audio InfoFrame packet field: 000 = Refer to Stream Header 001 = 32kHz 010 = 44.1kHz (CD) 011 = 48kHz 100 = 88.2kHz 101 = 96kHz 110 = 176.4kHz 111 = 192kHz
		HDMI_RX_AUD_INFO_LFE_PLAY	6:5	RO	0	Audio InfoFrame packet field. LFE playback level information: 00 = No information 01 = 0dB playback 10 = +10dB playback 11 = Reserved
		HDMI_RX_AUD_INFO_DM_INH	4:4	RO	0	Audio InfoFrame packet field. Describes whether the down mixed stereo output is permitted or not: 0 = Permitted or no information about any assertion of this 1 = Prohibited
		HDMI_RX_AUD_INFO_LEVEL_SHIFT	3:0	RO	0	Audio InfoFrame packet field. Level Shift Values: 0000 = 0dB 0001 = 1dB ... 1110 = 14dB 1111 = 15dB
601C	HDMI_RX_VENDOR_INFOFRAME_IEEE_REG_ID	HDMI_RX_IEEE_REG_ID_15_0	15:0	RO	0	HDMI Vendor Specific InfoFrame packet field. 24-bit IEEE Registration Identifier. Bits 15 down to 0.
601D	HDMI_RX_VENDOR_INFOFRAME_IEEE_REG_ID_2	RSVD	15:8	RO	0	Reserved.
		HDMI_RX_IEEE_REG_ID_23_16	7:0	RO	0	HDMI Vendor Specific InfoFrame packet field. 24-bit IEEE Registration Identifier. Bits 23 down to 16.
601E		RSVD	15:11	RO	0	Reserved.

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09/08/2026

	HDMI_RX_VENDOR_INFOFRAME_PKT_FIELDS	HDMI_RX_VDR_INFO_HDMI_VIC	10:3	RO	0	HDMI Vendor Specific InfoFrame packet field. HDMI proprietary Video Format Identification Code: 0x00 = Reserved 0x01 = 4K x 2K 29.97, 30 Hz 0x02 = 4K x 2K 25 Hz 0x03 = 4K x 2K 23.98, 24 Hz 0x04 = 4K x 2K 24 Hz (SMPTE) 0x05 to 0xFF = Reserved
		HDMI_RX_VDR_INFO_VIDEO_FORMAT	2:0	RO	0	HDMI Vendor Specific InfoFrame packet field. HDMI Video Format: 000 = No additional HDMI video format is presented in this packet 001 = Extended resolution format (e.g. used for 4K x 2K video) present. 1 byte of HDMI_VIC parameter value follows 010 = 3D format indication present 011 ~ 111 = Reserved for future use
601F	HDMI_RX_AVI_INFOFRAME_PKT_FIELDS	HDMI_RX_AVI_INFO_ITC	15:15	RO	0	AVI InfoFrame packet field. IT content: 0 = No data 1 = IT content
		HDMI_RX_AVI_INFO_FMT_ASPECT_RATIO	14:11	RO	0	AVI InfoFrame packet field. Active Format Aspect Ratio: 1000 = Same as picture aspect ratio 1001 = 4:3 (Centre) 1010 = 16:9 (Centre) 1011 = 14:9 (Centre, other values = Per DVB AFD ACTIVE_FORMAT field in ETSI)
		HDMI_RX_AVI_INFO_PIC_ASPECT_RATIO	10:9	RO	0	AVI InfoFrame packet field. Picture Aspect Ratio: 00 = No Data 01 = 4:3 10 = 16:9 11 = Future use
		HDMI_RX_AVI_INFO_COLORIMETRY	8:7	RO	0	AVI InfoFrame packet field. Colorimetry: 00 = No Data 01 = SMPTE 170M/ITU601 10 = ITU709 11 = Extended Colorimetry Information Valid

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DIVA Laboratories Ltd.
09/08/2026

		HDMI_RX_AVI_INFO_SCAN_INFO	6:5	RO	0	AVI InfoFrame packet field. Scan Information: 00 = No Data 01 = Composed for an over-scanned display, where some active pixels and lines at the edges are not displayed 10 = Composed for an under-scanned display, where all active pixels are displayed with or without a border 11 = Future use
		HDMI_RX_AVI_INFO_BAR_INFO_VLD	4:3	RO	0	AVI InfoFrame packet field. Bar Info: 00 = Bar Data not valid 01 = Vertical Bar Info valid 10 = Horizontal Bar Info valid 11 = Vertical and Horizontal Bar Info valid
		HDMI_RX_AVI_INFO_ACTIVE_INFO	2:2	RO	0	AVI InfoFrame packet field. Active Format Information Present: 0 = No Data 1 = Active Format
		HDMI_RX_AVI_INFO_COLOR_SPACE	1:0	RO	0	AVI InfoFrame packet field. Colour space: 00 = RGB, 01 = YC_bC_r 4:2:2, 10 = YC_bC_r 4:4:4, 11 = Future use
6020	HDMI_RX_AVI_INFOFRAME_PKT_FIELDS_2	HDMI_RX_AVI_INFO_YCC_QUANTIZATION	15:14	RO	0	AVI InfoFrame packet field. YCC Quantization: 00 = Limited Range 01 = Full Range 1X = Reserved
		HDMI_RX_AVI_INFO_VIC	13:7	RO	0	AVI InfoFrame packet field. Video Identification Code. See CEA-861-D for details.
		HDMI_RX_AVI_INFO_SCALING	6:5	RO	0	AVI InfoFrame packet field. Non-Uniform Picture Scaling: 00 = No Known non-uniform Scaling 01 = Picture has been scaled horizontally 10 = Picture has been scaled vertically 11 = Picture has been scaled horizontally and vertically
		HDMI_RX_AVI_INFO_QUANTIZATION	4:3	RO	0	AVI InfoFrame packet field. RGB Quantization Range: 00 = depends on video format 01 = Limited Range 10 = Full Range 11 = Reserved

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DIVA Laboratories, Ltd.
09/08/2026

		HDMI_RX_AVI_INFO_EXT_COLORIMETRY	2:0	RO	0	AVI InfoFrame packet field. Extended Colorimetry: 000 = xvYCC601 001 = xvYCC709 All other values reserved
6021	HDMI_RX_AVI_INFOFRAME_PKT_FIELDS_3	RSVD	15:6	RO	0	Reserved.
		HDMI_RX_AVI_INFO_PIX_REP	5:2	RO	0	AVI InfoFrame packet field. Pixel Repetition Factor: 0000 = No repetition 0001 = pixel sent 2 times 0010 = pixel sent 3 times ... 1001 = pixel sent 10 times Other values = Reserved
		HDMI_RX_AVI_INFO_CONTENT_TYPE	1:0	RO	0	AVI InfoFrame packet field. Content Type: 00 = Graphics 01 = Photo 10 = Cinema 11 = Game
6022	HDMI_RX_GEN_CTRL_PKT_FIELDS	RSVD	15:11	RO	0	Reserved.
		HDMI_RX_GEN_CTRL_DEFAULT_PHASE	10:10	RO	0	General Control packet field. Default Phase. See HDMI Specification 1.4b.
		HDMI_RX_GEN_CTRL_SET_AVMUTE	9:9	RO	0	General Control packet field. Sets the AVMUTE flag.
		HDMI_RX_GEN_CTRL_CLEAR_AVMUTE	8:8	RO	0	General Control packet field. Clears the AVMUTE flag.
		HDMI_RX_GEN_CTRL_COLOR_DEPTH	7:4	RO	0	General Control packet field. Colour Depth: 0000 = Colour Depth not indicated 0100 = 24 bits per pixel 0101 = 30 bits per pixel 0110 = 36 bits per pixel 0111 = 48 bits per pixel Other values = Reserved
		HDMI_RX_GEN_CTRL_PIXEL_PACKING	3:0	RO	0	General Control packet field. Pixel Packing Phase: 0000 = Phase 4 (10P4) 0001 = Phase 1 (10P1, 12P1, 16P1) 0010 = Phase 2 (10P2, 12P2) 0011 Phase 3 (10P3) All other values = Reserved

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DIVA Laboratories. Ltd.
09/08/2026

6023	HDMI_RX_DR_INFOFRAME_PKT_FIELDS	RSVD	15:6	RO	0	Reserved.
		HDMI_RX_DR_INFO_SMDI	5:3	RO	0	Dynamic Range and Mastering InfoFrame packet field. STATIC_METADATA_DESCRIPTOR_ID: 000 = Static Meta data Type 1 Others = Reserved for future use
		HDMI_RX_DR_INFO_EOTF	2:0	RO	0	Dynamic Range and Mastering InfoFrame packet field. Electro-Optical Transfer Function: 000 = Traditional gamma – SDR Luminance Range 001 = Traditional gamma – HDR Luminance Range 010 = SMPTE ST 2084 011 = Hybrid Log-Gamma (HLG) based on ITU-R BT.2100-0 1xx = Reserved for future use
6024	HDMI_RX_DR_BYTE_3_4	HDMI_RX_DR_DISP_PRIM_X0_MSB	15:8	RO	0	Dynamic Range and Mastering InfoFrame byte 4.
		HDMI_RX_DR_DISP_PRIM_X0_LSB	7:0	RO	0	Dynamic Range and Mastering InfoFrame byte 3.
6025	HDMI_RX_DR_BYTE_5_6	HDMI_RX_DR_DISP_PRIM_Y0_MSB	15:8	RO	0	Dynamic Range and Mastering InfoFrame byte 6.
		HDMI_RX_DR_DISP_PRIM_Y0_LSB	7:0	RO	0	Dynamic Range and Mastering InfoFrame byte 5.
6026	HDMI_RX_DR_BYTE_7_8	HDMI_RX_DR_DISP_PRIM_X1_MSB	15:8	RO	0	Dynamic Range and Mastering InfoFrame byte 8.
		HDMI_RX_DR_DISP_PRIM_X1_LSB	7:0	RO	0	Dynamic Range and Mastering InfoFrame byte 7.
6027	HDMI_RX_DR_BYTE_9_10	HDMI_RX_DR_DISP_PRIM_Y1_MSB	15:8	RO	0	Dynamic Range and Mastering InfoFrame byte 10.
		HDMI_RX_DR_DISP_PRIM_Y1_LSB	7:0	RO	0	Dynamic Range and Mastering InfoFrame byte 9.
6028	HDMI_RX_DR_BYTE_11_12	HDMI_RX_DR_DISP_PRIM_X2_MSB	15:8	RO	0	Dynamic Range and Mastering InfoFrame byte 12.

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09/08/2026

		HDMI_RX_DR_DISP_PRIM_X2_LSB	7:0	RO	0	Dynamic Range and Mastering InfoFrame byte 11.
6029	HDMI_RX_DR_BYTE_13_14	HDMI_RX_DR_DISP_PRIM_Y2_MSB	15:8	RO	0	Dynamic Range and Mastering InfoFrame byte 14.
		HDMI_RX_DR_DISP_PRIM_Y2_LSB	7:0	RO	0	Dynamic Range and Mastering InfoFrame byte 13.
602A	HDMI_RX_DR_BYTE_15_16	HDMI_RX_DR_WHITE_P_X_MSB	15:8	RO	0	Dynamic Range and Mastering InfoFrame byte 16.
		HDMI_RX_DR_WHITE_P_X_LSB	7:0	RO	0	Dynamic Range and Mastering InfoFrame byte 15.
602B	HDMI_RX_DR_BYTE_17_18	HDMI_RX_DR_WHITE_P_Y_MSB	15:8	RO	0	Dynamic Range and Mastering InfoFrame byte 18.
		HDMI_RX_DR_WHITE_P_Y_LSB	7:0	RO	0	Dynamic Range and Mastering InfoFrame byte 17.
602C	HDMI_RX_DR_BYTE_19_20	HDMI_RX_DR_MAX_DIS_M_LUM_MSB	15:8	RO	0	Dynamic Range and Mastering InfoFrame byte 20.
		HDMI_RX_DR_MAX_DIS_M_LUM_LSB	7:0	RO	0	Dynamic Range and Mastering InfoFrame byte 19.
602D	HDMI_RX_DR_BYTE_21_22	HDMI_RX_DR_MIN_DIS_M_LUM_MSB	15:8	RO	0	Dynamic Range and Mastering InfoFrame byte 22.
		HDMI_RX_DR_MIN_DIS_M_LUM_LSB	7:0	RO	0	Dynamic Range and Mastering InfoFrame byte 21.
602E	HDMI_RX_DR_BYTE_23_24	HDMI_RX_DR_MAX_CONT_L_LEV_MSB	15:8	RO	0	Dynamic Range and Mastering InfoFrame byte 24.
		HDMI_RX_DR_MAX_CONT_L_LEV_LSB	7:0	RO	0	Dynamic Range and Mastering InfoFrame byte 23.
602F	HDMI_RX_DR_BYTE_25_26	HDMI_RX_DR_MAX_F_AVRL_LEV_MSB	15:8	RO	0	Dynamic Range and Mastering InfoFrame byte 26.

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DIVA Laboratories, Ltd.
09/08/2026

		HDMI_RX_DR_MAX_F_AVRL_LEV_LSB	7:0	RO	0	Dynamic Range and Mastering InfoFrame byte 25.
6030	HDMI_RX_AUD_CLK_REGEN_PKT_FIELDS	HDMI_RX_AUD_CLK_REGEN_N_15_0	15:0	RO	0	Audio Clock Regeneration packet field. Value of audio clock regeneration N bits 15 down to 0.
6031	HDMI_RX_AUD_CLK_REGEN_PKT_FIELDS_2	RSVD	15:4	RO	0	Reserved.
		HDMI_RX_AUD_CLK_REGEN_N_19_16	3:0	RO	0	Audio Clock Regeneration packet field. Value of audio clock regeneration N bits 19 down to 16.
6032	HDMI_RX_AUD_CLK_REGEN_PKT_FIELDS_3	HDMI_RX_AUD_CLK_REGEN_CTS_15_0	15:0	RO	0	Audio Clock Regeneration packet field. Cycle Time Stamp. Bits 15 down to 0.
6033	HDMI_RX_AUD_CLK_REGEN_PKT_FIELDS_4	RSVD	15:4	RO	0	Reserved.
		HDMI_RX_AUD_CLK_REGEN_CTS_19_16	3:0	RO	0	Audio Clock Regeneration packet field. Cycle Time Stamp. Bits 19 down to 16.
6034	HDMI_RX_AUD_CH_STATUS_SELECT	RSVD	15:3	RO	0	Reserved.
		HDMI_RX_AUD_CH_STATUS_SELECT	2:0	RW	0	Audio Channel status selection parameter for HDMI_RX_AUDIO_CH_STAT_BYTE_*. Allows the selection of 1 out of 8 channel status word to be routed to CSR for observability: 000 = audio channel status for channel 1 001 = audio channel status for channel 2 010 = audio channel status for channel 3 011 = audio channel status for channel 4 100 = audio channel status for channel 5 101 = audio channel status for channel 6 110 = audio channel status for channel 7 111 = audio channel status for channel 8
6035	HDMI_RX_AUDIO_CH_STAT_BYTE_0_1	HDMI_RX_AUDIO_CH_STAT_BYTE_1	15:8	RO	0	Audio channel status byte 1 (as per AES3-1992 standard definition).
		HDMI_RX_AUDIO_CH_STAT_BYTE_0	7:0	RO	0	Audio channel status byte 0 (as per AES3-1992 standard definition).

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Kent Lin
DIVA Laboratories Ltd.
09/08/2026

6036	HDMI_RX_AUDIO_CH_STAT_BYTE_2_3	HDMI_RX_AUDIO_CH_STAT_BYTE_3	15:8	RO	0	Audio channel status byte 3 (as per AES3-1992 standard definition).
		HDMI_RX_AUDIO_CH_STAT_BYTE_2	7:0	RO	0	Audio channel status byte 2 (as per AES3-1992 standard definition).
6037	HDMI_RX_AUDIO_CH_STAT_BYTE_4_5	HDMI_RX_AUDIO_CH_STAT_BYTE_5	15:8	RO	0	Audio channel status byte 5 (as per AES3-1992 standard definition).
		HDMI_RX_AUDIO_CH_STAT_BYTE_4	7:0	RO	0	Audio channel status byte 4 (as per AES3-1992 standard definition).
6038	HDMI_RX_AUDIO_CH_STAT_BYTE_6_7	HDMI_RX_AUDIO_CH_STAT_BYTE_7	15:8	RO	0	Audio channel status byte 7 (as per AES3-1992 standard definition).
		HDMI_RX_AUDIO_CH_STAT_BYTE_6	7:0	RO	0	Audio channel status byte 6 (as per AES3-1992 standard definition).
6039	HDMI_RX_AUDIO_CH_STAT_BYTE_8_9	HDMI_RX_AUDIO_CH_STAT_BYTE_9	15:8	RO	0	Audio channel status byte 9 (as per AES3-1992 standard definition).
		HDMI_RX_AUDIO_CH_STAT_BYTE_8	7:0	RO	0	Audio channel status byte 8 (as per AES3-1992 standard definition).
603A	HDMI_RX_AUDIO_CH_STAT_BYTE_10_11	HDMI_RX_AUDIO_CH_STAT_BYTE_11	15:8	RO	0	Audio channel status byte 11 (as per AES3-1992 standard definition).
		HDMI_RX_AUDIO_CH_STAT_BYTE_10	7:0	RO	0	Audio channel status byte 10 (as per AES3-1992 standard definition).
603B	HDMI_RX_AUDIO_CH_STAT_BYTE_12_13	HDMI_RX_AUDIO_CH_STAT_BYTE_13	15:8	RO	0	Audio channel status byte 13 (as per AES3-1992 standard definition).
		HDMI_RX_AUDIO_CH_STAT_BYTE_12	7:0	RO	0	Audio channel status byte 12 (as per AES3-1992 standard definition).
603C	HDMI_RX_AUDIO_CH_	HDMI_RX_AUDIO_CH_STAT_BYTE_15	15:8	RO	0	Audio channel status byte 15 (as per AES3-1992 standard definition).

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09/08/2026

	STAT_BYTE_14_15	HDMI_RX_AUDIO_CH_STAT_BYTE_14	7:0	RO	0	Audio channel status byte 14 (as per AES3-1992 standard definition).
603D	HDMI_RX_AUDIO_CH_STAT_BYTE_16_17	HDMI_RX_AUDIO_CH_STAT_BYTE_17	15:8	RO	0	Audio channel status byte 17 (as per AES3-1992 standard definition).
		HDMI_RX_AUDIO_CH_STAT_BYTE_16	7:0	RO	0	Audio channel status byte 16 (as per AES3-1992 standard definition).
603E	HDMI_RX_AUDIO_CH_STAT_BYTE_18_19	HDMI_RX_AUDIO_CH_STAT_BYTE_19	15:8	RO	0	Audio channel status byte 19 (as per AES3-1992 standard definition).
		HDMI_RX_AUDIO_CH_STAT_BYTE_18	7:0	RO	0	Audio channel status byte 18 (as per AES3-1992 standard definition).
603F	HDMI_RX_AUDIO_CH_STAT_BYTE_20_21	HDMI_RX_AUDIO_CH_STAT_BYTE_21	15:8	RO	0	Audio channel status byte 21 (as per AES3-1992 standard definition).
		HDMI_RX_AUDIO_CH_STAT_BYTE_20	7:0	RO	0	Audio channel status byte 20 (as per AES3-1992 standard definition).
6040	HDMI_RX_AUDIO_CH_STAT_BYTE_22_23	HDMI_RX_AUDIO_CH_STAT_BYTE_23	15:8	RO	0	Audio channel status byte 23 (as per AES3-1992 standard definition).
		HDMI_RX_AUDIO_CH_STAT_BYTE_22	7:0	RO	0	Audio channel status byte 22 (as per AES3-1992 standard definition).
6041 to 6043	RSVD_REG	RSVD	15:0	RW	N/A	Reserved. Do not change.
6044	HDMI_RX_MCLK_LOCK_STATUS	RSVD	15:1	RO	0	Reserved.
		HDMI_RX_MCLK_LOCK	0:0	RO	0	When HIGH, indicates that the digital PLL generating the audio clock is locked, using the audio CLK regeneration N and CTS values. When LOW, indicates that the digital PLL generating the audio clock is not locked.
6045	HDMI_RX_AUDIO_STICKY_STATUS	RSVD	15:5	RO	0	Reserved.
		HDMI_RX_PDS_FIFO_UNDERFLOW_STICKY	4:4	ROCW	0	Packet Down Shift block FIFO underflow. When HIGH, the block FIFO under-flowed. When LOW, no underflow happened.

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Kent Lin
DIVA Laboratories. Ltd.
09/08/2026

		HDMI_RX_PDS_FIFO_OVERFLOW_STICKY	3:3	ROCW	0	Packet Down Shift block FIFO overflow. When HIGH, the block FIFO overflowed. When LOW, no overflow happened.
		HDMI_RX_ATDM_FIFO_FULL_STICKY	2:2	ROCW	0	ATDM FIFO underflow. When HIGH, the block FIFO under-flowed. When LOW, no underflow happened.
		HDMI_RX_ATDM_FIFO_EMPTY_STICKY	1:1	ROCW	0	ATDM block FIFO overflow. When HIGH, the block FIFO overflowed. When LOW, no overflow happened.
		HDMI_RX_MCLK_LOCK_STICKY	0:0	ROCW	0	When HIGH, indicates that the digital PLL generating the audio clock is locked, using the audio CLK regeneration N and CTS values. When LOW, indicates that the digital PLL generating the audio clock is not locked.
6046	HDMI_RX_AUDIO_DIG_PLL_ERROR_STATUS	HDMI_RX_HCR_ERROR_CNT_VAL_D2	15:0	RO	0	NLPCM_FLOW_STABILIZER_GB2_E/HDMI_CLK_REGEN_GB2_E/SV_ERROR_CNT_VAL_D2. Error signal of the HDMI RX audio digital PLL. This is a 2's complement number. Should be around 0 when the PLL is locked.
6047	HDMI_RX_PGR_PKT_HEADER	RSVD	15:8	RO	0	Reserved.
		HDMI_RX_GEN_PKT_HEADER	7:0	RW	0	User defined Packet Type Value for InfoFrame header (HB0) (Generic InfoFrame user programmable). The data island extraction block will look for the value to extract a Generic (user defined) InfoFrame.
6048	HDMI_RX_PGR_PKT_HEADER_0	HDMI_RX_GEN_PKT_HEADER_WORD_0	15:8	RO	0	Packet header HB1.
			7:0	RO	0	Packet header HB0.
6049	HDMI_RX_PGR_PKT_HEADER_1	HDMI_RX_GEN_PKT_HEADER_WORD_1	15:8	RO	0	Packer Header parity bits.
			7:0	RO	0	Packet header HB2.
604A	HDMI_RX_PGR_PKT_SUBPKT_0_BYTES_0	HDMI_RX_GEN_PKT_PB1	15:8	RO	0	Generic InfoFrame PB1
		HDMI_RX_GEN_PKT_PB0	7:0	RO	0	Generic InfoFrame Packet Byte 0 (PB0), usually checksum.

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Kent Lin
DIVA Laboratories. Ltd.
09/03/2026

604B	HDMI_RX_PGR_PKT_SUBPKT_0_BYTES_1	HDMI_RX_GEN_PKT_PB3	15:8	RO	0	Generic InfoFrame PB3.
		HDMI_RX_GEN_PKT_PB2	7:0	RO	0	Generic InfoFrame PB2.
604C	HDMI_RX_PGR_PKT_SUBPKT_0_BYTES_2	HDMI_RX_GEN_PKT_PB5	15:8	RO	0	Generic InfoFrame PB5.
		HDMI_RX_GEN_PKT_PB4	7:0	RO	0	Generic InfoFrame PB4.
604D	HDMI_RX_PGR_PKT_SUBPKT_0_BYTES_3	HDMI_RX_GEN_PKT_BCH_PAR0	15:8	RO	0	Generic InfoFrame BCH block 0 Parity bits (for PB0-PB6).
		HDMI_RX_GEN_PKT_PB6	7:0	RO	0	Generic InfoFrame PB6.
604E	HDMI_RX_PGR_PKT_SUBPKT_1_BYTES_0	HDMI_RX_GEN_PKT_PB8	15:8	RO	0	Generic InfoFrame PB8.
		HDMI_RX_GEN_PKT_PB7	7:0	RO	0	Generic InfoFrame PB7.
604F	HDMI_RX_PGR_PKT_SUBPKT_1_BYTES_1	HDMI_RX_GEN_PKT_PB10	15:8	RO	0	Generic InfoFrame PB10.
		HDMI_RX_GEN_PKT_PB9	7:0	RO	0	Generic InfoFrame PB9.
6050	HDMI_RX_PGR_PKT_SUBPKT_1_BYTES_2	HDMI_RX_GEN_PKT_PB12	15:8	RO	0	Generic InfoFrame PB12.
		HDMI_RX_GEN_PKT_PB11	7:0	RO	0	Generic InfoFrame PB11.
6051	HDMI_RX_PGR_PKT_SUBPKT_1_BYTES_3	HDMI_RX_GEN_PKT_BCH_PAR1	15:8	RO	0	Generic InfoFrame BCH block 1 Parity bits (for PB7-PB13).
		HDMI_RX_GEN_PKT_PB13	7:0	RO	0	Generic InfoFrame PB13.
6052	HDMI_RX_PGR_PKT_SUBPKT_2_BYTES_0	HDMI_RX_GEN_PKT_PB15	15:8	RO	0	Generic InfoFrame PB15.
		HDMI_RX_GEN_PKT_PB14	7:0	RO	0	Generic InfoFrame PB14.

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Kent Lin
DIVA Laboratories, Ltd.
09/08/2026

6053	HDMI_RX_PGR_PKT_SUBPKT_2_BYTES_1	HDMI_RX_GEN_PKT_PB17	15:8	RO	0	Generic InfoFrame PB17.
		HDMI_RX_GEN_PKT_PB16	7:0	RO	0	Generic InfoFrame PB16.
6054	HDMI_RX_PGR_PKT_SUBPKT_2_BYTES_2	HDMI_RX_GEN_PKT_PB19	15:8	RO	0	Generic InfoFrame PB19.
		HDMI_RX_GEN_PKT_PB18	7:0	RO	0	Generic InfoFrame PB18.
6055	HDMI_RX_PGR_PKT_SUBPKT_2_BYTES_3	HDMI_RX_GEN_PKT_BCH_PAR2	15:8	RO	0	Generic InfoFrame BCH block 2 Parity bits (for PB14-PB20).
		HDMI_RX_GEN_PKT_PB20	7:0	RO	0	Generic InfoFrame PB20.
6056	HDMI_RX_PGR_PKT_SUBPKT_3_BYTES_0	HDMI_RX_GEN_PKT_PB22	15:8	RO	0	Generic InfoFrame PB22.
		HDMI_RX_GEN_PKT_PB21	7:0	RO	0	Generic InfoFrame PB21.
6057	HDMI_RX_PGR_PKT_SUBPKT_3_BYTES_1	HDMI_RX_GEN_PKT_PB24	15:8	RO	0	Generic InfoFrame PB24.
		HDMI_RX_GEN_PKT_PB23	7:0	RO	0	Generic InfoFrame PB23.
6058	HDMI_RX_PGR_PKT_SUBPKT_3_BYTES_2	HDMI_RX_GEN_PKT_PB26	15:8	RO	0	Generic InfoFrame PB26.
		HDMI_RX_GEN_PKT_PB25	7:0	RO	0	Generic InfoFrame PB25.
6059	HDMI_RX_PGR_PKT_SUBPKT_3_BYTES_3	HDMI_RX_GEN_PKT_BCH_PAR3	15:8	RO	0	Generic InfoFrame BCH block 3 Parity bits (for PB21-PB27).
		HDMI_RX_GEN_PKT_PB27	7:0	RO	0	Generic InfoFrame PB27.
605A	FVH_SYNC_ADJUST	RSVD	15:3	RW	0	Reserved. Do not change.
		HSYNC_INVERT_REG	2:2	RW	0	Inverts the detected polarity of the input HSYNC when asserted (in the eia861b_to_fvh block).

Semtech Confidential Information
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DIVA Laboratories, Ltd.
09/08/2026

		VSYNC_INVERT_REG	1:1	RW	0	Inverts the detected polarity of the input VSYNC when asserted (in the EIA861B_TO_FVH block).
		FSYNC_INVERT_REG	0:0	RW	0	Inverts the polarity of the detected field when asserted (in the EIA861B_TO_FVH block).
605B	CLKS_PER_LINE_861	RSVD	15:13	RO	0	Reserved.
		CLKS_PER_LINE_861_REG	12:0	RO	0	Reports line length selected by the EIA861B_TO_FVH block.
605C	LINES_PER_FRAME_861	RSVD	15:14	RO	0	Reserved.
		INTERLACED_DET	13:13	RO	0	Reports if interlaced timing has been detected.
		H_CONFIG_DET	12:12	RO	0	Reports H_CONFIG detected
		LINES_PER_FRAME_861_REG	11:0	RO	0	Reports number of lines per frame selected by the EIA861B_TO_FVH block.
605D	CEA_861_PARAM_0	RSVD	15:13	RO	0	Reserved.
		CEA_861_INTERLACED_MEAS_DET_B_SEL	12:12	RW	0	When set to 1, detected format forced as interlaced, when 0 interlaced/progressive decision is taken from VIC.
		RSVD	11:9	RO	0	Reserved.
		CEA_861_PARAM_FBLANK_OVR	8:8	RW	0	When set to 1, parameters from reg 6064-6065 are used by the EIA861B_TO_FVH block instead of detected ones.
		CEA_861_PARAM_VBLANK_OVR	7:7	RW	0	When set to 1, parameters from reg 6060-6063 are used by the EIA861B_TO_FVH block instead of detected ones.
		CEA_861_PARAM_HBLANK_OVR	6:6	RW	0	When set to 1, parameters from reg 605F are used by the EIA861B_TO_FVH block instead of detected ones.
		RSVD	5:0	RW	1	Reserved. Do not change.
605E		RSVD	15:13	RO	0	Reserved.

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Kent Lin
DIVA Laboratories, Ltd.
09/03/2026

	CEA_861_PARAM_1	CEA_861_RESET_PIXEL_REG	12:0	RW	58	CEA_861_RESET_PIXEL parameter.
605F	CEA_861_PARAM_2	RSVD	15:13	RO	0	Reserved.
		CEA_861_HBLANK_STOP_PIXEL_REG	12:0	RW	118	CEA_861_HBLANK_STOP_PIXEL parameter.
6060	CEA_861_PARAM_3	RSVD	15:12	RO	0	Reserved.
		CEA_861_VBLANK1_START_LINE_REG	11:0	RW	462	CEA_861_VBLANK1_START_LINE parameter.
6061	CEA_861_PARAM_4	RSVD	15:12	RO	0	Reserved.
		CEA_861_VBLANK1_STOP_LINE_REG	11:0	RW	2A	CEA_861_VBLANK1_STOP_LINE parameter.
6062	CEA_861_PARAM_5	RSVD	15:12	RO	0	Reserved.
		CEA_861_VBLANK2_START_LINE_REG	11:0	RW	462	CEA_861_VBLANK2_START_LINE parameter.
6063	CEA_861_PARAM_6	RSVD	15:12	RO	0	Reserved.
		CEA_861_VBLANK2_STOP_LINE_REG	11:0	RW	2A	CEA_861_VBLANK2_STOP_LINE parameter.
6064	CEA_861_PARAM_7	RSVD	15:12	RO	0	Reserved.
		CEA_861_FBLANK_START_LINE_REG	11:0	RW	0	CEA_861_FBLANK_START_LINE parameter.
6065	CEA_861_PARAM_8	RSVD	15:12	RO	0	Reserved.
		CEA_861_FBLANK_STOP_LINE_REG	11:0	RW	0	CEA_861_FBLANK_STOP_LINE parameter.
6066	VIC_CEA_861	RSVD	15:8	RO	0	Reserved.
		VIC_CEA_861_OVR	7:7	RW	0	Enables overwrite of the detected VIC number. When set HIGH, the VIC_CES_861_REG value is used instead of the detected VIC value for all internal processing.

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DIVA Laboratories, Ltd.
09/08/2026

		VIC_CEA_861_REG	6:0	RW	10	Overwrites detected VIC number.
6067	HDMI_RX_ OVR_0_REG	RSVD	15:9	RO	0	Reserved.
		INFFRAME_ DETECTED_OVR	8:8	RW	0	Enables register override of INFFRAME_DETECTED signal.
		INFFRAME_ DETECTED_REG	7:7	RW	1	Overrides internal signal indicating InfoFrame detection.
		INTERLACED_ INFFRAME_OVR	6:6	RW	0	Enables register override of INTERLACED_INFFRAME_REG.
		INTERLACED_ INFFRAME_REG	5:5	RW	1	Overrides internal signal indicating interlaced video.
		FRAME_RASTER_ SEL_OVR	4:4	RW	0	Enables register override of FRAME_RASTER_SEL_REG.
		FRAME_RASTER_ SEL_REG	3:0	RW	6	Overwrites internal FRAME_RASTER_SEL signal if FRAME_RASTER_SEL_OVR is set HIGH. 0000 = 1280x720@25 0001 = 1280x720@30 0010 = 1280x720@50 0011 = 1280x720@60 0100 = 1920x1080@24, 48 0101 = 1920x1080@25, 50 1010 = 1920x1080@100 0110 = 1920x1080@30, 60 0100 = 3840x2160@24, 48 0101 = 3840x2160@25, 50 0110 = 3840x2160@30, 60 0111 = 4096x2160@24, 48 1000 = 4096x2160@25, 50 1001 = 4096x2160@30, 60 1011 = 1920x1080@120 Others = RSVD
6068	RSVD_REG	RSVD	15:0	RW	0	Reserved. Do not change.
6069	HDMI_RX_ STATUS_0_REG	RSVD	15:8	RO	1	Reserved.
		GB_COLOR_SPACE	7:4	RO	0	From the VIDEO_PHASE_ALIGN, block. 0000 = RGB 0001 = 422 0010 = 444 0011 = 420 Other = N/A

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DIVA Laboratories, Ltd.
09/08/2026

		TMDS_DC_ COLOR_DEPTH	3:0	RO	0	From the TMDS_PHASE_CALC block. 0000 = N/A 0100 = 24 0101 = 30 0110 = 36 0111 = 48
606A	HDMI_RX_ STATUS_1_REG	BIT_DEPTH_DET	15:14	RO	0	Bit depth detected from VIC: 00 = 24 01 = 30 10 = 36 11 = 48
		COLOR_SMPL_DET	13:12	RO	0	Colour sampling detected from VIC for debug: 00 = RGB 01 = 422 10 = 444 11 = 420
		FRAME_RATE_DET	11:8	RO	0	Frame rate detected from VIC for debug: 0000 = 24 0001 = 25 0010 = 30 0011 = 48 0100 = 50 0101 = 60 0110 = 96 0111 = 100 1000 = 120
		FRAME_RASTER_ SEL_DET	7:4	RO	0	Frame raster selected: 0000 = 1280x720@25 0001 = 1280x720@30 0010 = 1280x720@50 0011 = 1280x720@60 0100 = 1920x1080@24, 48 0101 = 1920x1080@25, 50 1010 = 1920x1080@100 0110 = 1920x1080@30, 60 0100 = 3840x2160@24, 48 0101 = 3840x2160@25, 50 0110 = 3840x2160@30, 60 0111 = 4096x2160@24, 48 1000 = 4096x2160@25, 50 1001 = 4096x2160@30, 60 1011 = 1920x1080@120 1111 = 1920x1080@60 (non defined VIC detected)

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09/08/2026

		HDMI_RX_ DATA_RATE_DET	3:0	RO	0	Detected HDMI data rate: 0000 = 0.74Gb/s 0001 = 0.93Gb/s 0010 = 1.11Gb/s 0011 = 1.49Gb/s 0100 = 1.86Gb/s 0101 = 2.23Gb/s 0110 = 2.97Gb/s 0111 = 3.71Gb/s 1000 = 4.46Gb/s 1001 = 5.94Gb/s
606B	SDI_OUTPUT_ INTERFACE	RSVD	15:2	RO	0	Reserved.
		SDI_OUTPUT_ INTERFACE_REG	1:0	RW	0	Selects output interface as SL, DL or QL for 12G and 6G image data rates: 00 or 01 = SL 11 = DL 10 = QL
606C	RSVD_REG	RSVD	15:0	RW	0	Reserved. Do not change.
606D	VIC_CSPACE_ CDEPTH	RSVD	15:15	RO	0	Reserved.
		CDEPTH_OVR	14:14	RW	0	Enables overwrite of the colour depth, detected from the InfoFrame.
		CSPACE_OVR	13:13	RW	0	Enables overwrite of the colour space, detected from the InfoFrame.
		VIC_OVR	12:12	RW	0	Enables overwrite of the VIC, detected from the InfoFrame.
606D	VIC_CSPACE_ CDEPTH	COLOR_SPACE_REG	11:10	RW	1	Overwrites detected colour space from the InfoFrame if CSPACE_OVR =1: 00 = RGB 01 = YC_bC_r 4:2:2 10 = YC_bC_r 4:4:4 11 = YC_bC_r 4:2:0
		COLOR_DEPTH_REG	9:7	RW	5	Overwrites detected colour depth from the InfoFrame if DEPTH_OVR = 1: 000 = N/A 100 = 24 101 = 30 110 = 36 111 = 48 (not supported)

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DIVA Laboratories Ltd.
09/08/2026

		VIC_REG	6:0	RW	61	Overwrites detected VIC number from the InfoFrame if VIC_OVR =1.
606E	HV_SYNC_ POLARITY	RSVD	15:2	RO	0	Reserved.
		HV_SYNC_INV	1:1	RW	0	If 1 inverts sync polarity.
		POS_SYNC_INV_EN	0:0	RW	1	Enables auto inversion of sync signal with positive polarity.
606F	RSVD_REG	RSVD	15:0	RW	0	Reserved. Do not change.
6070	SDI_ FORMATTING	RSVD	15:14	RO	0	Reserved.
		ASPECT_RATIO_REG	13:13	RW	1	Default value for Aspect ratio in PIDs (16:9 (1) or Unknown (0)).
		CRC_INS_REG	12:12	RW	1	Enable SCRC_INSERTION in the SDI_FORMAT block.
		LNUM_INS_REG	11:11	RW	1	Enables line number insertion in the SDI_FORMAT block.
		TRS_INS_REG	10:10	RW	1	Enables TRS insertion in the SDI_FORMAT block.
		WORD_REMAP_REG	9:9	RW	1	Enables 8-bit word remapping in the SDI_FORMAT block.
		PID_STREAM_EN_ OVR	8:8	RW	0	Enables PID insertion override.
		PID_STREAM_EN_ REG	7:0	RW	FF	Overrides PID insertion enable bits in the SDI_FORMAT block, one bit per stream.
6071	RSVD_REG	RSVD	15:0	RW	465	Reserved. Do not change.
6072	DEFAULT_ ALPHA_VALUE	RSVD	15:10	RO	0	Reserved.
		DEFAULT_ ALPHA_VALUE_REG	9:0	RW	40	Default value used to insert instead of the missing alpha channel for formats which support alpha channel.
6073		RSVD	15:8	RO	0	Reserved.

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09/08/2026

	PID_ COLORIMETRY_ OVR	TRANSFER_ CHAR_OVR	7:7	RW	0	Enables override of TRANSFER_CHAR.
		TRANSFER_ CHAR_REG	6:5	RW	0	Overrides detected Transfer characteristics value to be inserted in PID if TRANSFER_CHAR_OVR is set to '1'.
		ICTCP_YCBCR_OVR	4:4	RW	0	Enables override of ICTCP_YCBCR.
		ICTCP_YCBCR_REG	3:3	RW	0	Overrides detected Luminance and colour difference signal value to be inserted in PID if ICTCP_YCBCR_OVR is set to '1'.
		PID_ COLORIMETRY_OVR	2:2	RW	0	Enables override of PID_COLORIMETRY.
		PID_ COLORIMETRY_REG	1:0	RW	0	Overrides detected colorimetry value to be inserted in PID if PID_COLORIMETRY_OVR is set to '1'.
6074	PID_B4_ AUDIO_COPY	RSVD	15:8	RO	0	Reserved.
		AUDIO_COPY_ STATUS	7:0	RW	0	Audio copy status to be inserted in the PID (one bit per stream).
6075	RSVD_REG	RSVD	15:0	RW	0	Reserved. Do not change.
6076	DEBUG_ HSYNC_FALL_ POS	HSYNC_FALL_POS	15:0	RO	0	Detected HSYNC falling edge position.
6077	DEBUG_VEN_ RISE_POS	VEN_RISE_POS	15:0	RO	0	Detected VEN rising edge position.
6078	DEBUG_VEN_ FALL_POS	VEN_FALL_POS	15:0	RO	0	Detected VEN falling edge position.
6079	DEBUG_ HTOTAL	HTOTAL	15:0	RO	0	Detected HSYNC length.
607A	ACTIVE_LINE_ DETECTED	RSVD	15:1	RO	0	Reserved.
		AV_2048_1920B	0:0	RO	0	0 = Indicates detected 1920 active pixels 1= Indicates detected 2048 active pixels
607B		RSVD	15:2	RO	0	Reserved.

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DIVA Laboratories Ltd.
09/08/2026

	EXTERNAL_ EDID_SEL	SEL_EXT_EDID_OVR	1:1	RW	0	Enable override of the SEL_EXT_EDID pin (N11, dual function pin).
		SEL_EXT_EDID	0:0	RW	0	If SEL_EXT_EDID_OVR set to 1, controls selection between external EDID (an external EPROM) when set to ‘1’ or internal EDID when set to ‘0’.
607C	HDMI_RX_DS1_ BLANK_1	RSVD	15:10	RO	0	Reserved.
		HDMI_RX_DS1_ BLANK_0	9:0	RW	40	Blanking value 1 DS1, used for SDI formatting when BLANK_EN(0) is set to '1'.
607D	HDMI_RX_DS1_ BLANK_2	RSVD	15:10	RO	0	Reserved.
		HDMI_RX_DS1_ BLANK_1	9:0	RW	40	Blanking value 2 DS1, used for SDI formatting when BLANK_EN(0) is set to '1'.
607E	HDMI_RX_DS2_ BLANK_1	RSVD	15:10	RO	0	Reserved.
		HDMI_RX_DS2_ BLANK_0	9:0	RW	200	Blanking value 1 DS2, used for SDI formatting when BLANK_EN(0) is set to '1'.
607F	HDMI_RX_DS2_ BLANK_2	RSVD	15:10	RO	0	Reserved.
		HDMI_RX_DS2_ BLANK_1	9:0	RW	40	Blanking value 2 DS2, used for SDI formatting when BLANK_EN(0) is set to '1'.
6080	HDMI_RX_DS3_ BLANK_1	RSVD	15:10	RO	0	Reserved.
		HDMI_RX_DS3_ BLANK_0	9:0	RW	200	Blanking value 1 DS3, used for SDI formatting when BLANK_EN(1) is set to '1'.
6081	HDMI_RX_DS3_ BLANK_2	RSVD	15:10	RO	0	Reserved.
		HDMI_RX_DS3_ BLANK_1	9:0	RW	40	Blanking value 2 DS3, used for SDI formatting when BLANK_EN(1) is set to '1'.
6082	HDMI_RX_DS4_ BLANK_1	RSVD	15:10	RO	0	Reserved.
		HDMI_RX_DS4_ BLANK_0	9:0	RW	200	Blanking value 1 DS4, used for SDI formatting when BLANK_EN(1) is set to '1'.
6083		RSVD	15:10	RO	0	Reserved.

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DIVA Laboratories, Ltd.
09/08/2026

	HDMI_RX_DS4_BLANK_2	HDMI_RX_DS4_BLANK_1	9:0	RW	200	Blanking value 2 DS4, used for SDI formatting when BLANK_EN(1) is set to '1'.
6084	HDMI_RX_DS5_BLANK_1	RSVD	15:10	RO	0	Reserved.
		HDMI_RX_DS5_BLANK_0	9:0	RW	40	Blanking value 1 DS5, used for SDI formatting when BLANK_EN(2) is set to '1'.
6085	HDMI_RX_DS5_BLANK_2	RSVD	15:10	RO	0	Reserved.
		HDMI_RX_DS5_BLANK_1	9:0	RW	40	Blanking value 2 DS5, used for SDI formatting when BLANK_EN(2) is set to '1'.
6086	HDMI_RX_DS6_BLANK_1	RSVD	15:10	RO	0	Reserved.
		HDMI_RX_DS6_BLANK_0	9:0	RW	200	Blanking value 1 DS6, used for SDI formatting when BLANK_EN(2) is set to '1'.
6087	HDMI_RX_DS6_BLANK_2	RSVD	15:10	RO	0	Reserved.
		HDMI_RX_DS6_BLANK_1	9:0	RW	200	Blanking value 2 DS6, used for SDI formatting when BLANK_EN(2) is set to '1'.
6088	HDMI_RX_DS7_BLANK_1	RSVD	15:10	RO	0	Reserved.
		HDMI_RX_DS7_BLANK_0	9:0	RW	40	Blanking value 1 DS7, used for SDI formatting when BLANK_EN(3) is set to '1'.
6089	HDMI_RX_DS7_BLANK_2	RSVD	15:10	RO	0	Reserved.
		HDMI_RX_DS7_BLANK_1	9:0	RW	40	Blanking value 2 DS7, used for SDI formatting when BLANK_EN(3) is set to '1'.
608A	HDMI_RX_DS8_BLANK_1	RSVD	15:10	RO	0	Reserved.
		HDMI_RX_DS8_BLANK_0	9:0	RW	200	Blanking value 1 DS8, used for SDI formatting when BLANK_EN(3) is set to '1'.
608B	HDMI_RX_DS8_BLANK_2	RSVD	15:10	RO	0	Reserved.
		HDMI_RX_DS8_BLANK_1	9:0	RW	200	Blanking value 2 DS8, used for SDI formatting when BLANK_EN(3) is set to '1'.
608C		RSVD	15:4	RO	0	Reserved.

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DIVA Laboratories Ltd.
09/08/2026

	HDMI_RX_ BLANK_EN	BLANK_EN	3:0	RW	0	Enables override of default blanking values with values entered in registers 607C-608D.
608D	BLANK_ DEFAULT_1	RSVD	15:10	RO	0	Reserved.
		BLANK_Y_RGB	9:0	RW	40	Default blanking value for Y_RGB.
608E	BLANK_ DEFAULT_2	RSVD	15:10	RO	0	Reserved.
		BLANK_Y_RGB_FULL	9:0	RW	4	Default blanking value for Y_RGB full range.
608F	BLANK_ DEFAULT_3	RSVD	15:10	RO	0	Reserved.
		BLANK_CB_CR	9:0	RW	200	Default blanking value for CB_CR.
6090	BLANK_ DEFAULT_4	RSVD	15:10	RO	0	Reserved.
		BLANK_CB_CR_FULL	9:0	RW	200	Default blanking value for CB_CR full range.
6091	BLANK_ DEFAULT	RSVD	15:2	RO	0	Reserved.
		FULL_RANGE_OVR	1:1	RW	0	Enables FULL_RANGE override.
		FULL_RANGE	0:0	RW	0	Replaces detected value when FULL_RANGE_OVR is set to 1.
6092	LINES_1125	RSVD	15:12	RO	0	Reserved.
		LINES_1125	11:0	RW	465	Line length 1125.
6093	LINES_750	RSVD	15:12	RO	0	Reserved.
		LINES_750	11:0	RW	2EE	Line length 750.
6094 to 61FF	RSVD_REG	RSVD	15:0	RO	0	Reserved.
6200 to 627F	EDID_BASE_ BLOCK_[1:128]	RSVD	15:8	RO	0	Reserved.
		EDID_BASE_ BLOCK_BYTE_[1:128]	7:0	RW	TBA.	EDID base block. 8 LSBs are used.
6280 to 62FF	RSVD_REG	RSVD	15:0	RO	0	Reserved.

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DIVA Laboratories, Ltd.
09/08/2026

6300 to 637F	EDID_CTA_ BLOCK_[1:128]	RSVD	15:8	RO	0	Reserved.
		EDID_CTA_BLOCK_ BYTE_[1:128]	7:0	RW	TBA.	EDID CTA block. 8 LSBs are used.

4.2.8. HDMI Tx Control Registers

Table 4-13 HDMI Tx Control and Status Register

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
7000	MISC_CTRL	RSVD	15:6	RO	0	Reserved.
		TX_HDMI_ FLW_VLOCK_ RST_EN	5:5	RW	0	Enables reset of the HDMI Tx path based on the flywheel V lock signal.
		TX_HDMI_ FLW_DIST_RST_DIS	4:4	RW	0	Disables reset of the HDMI Tx path based on the flywheel disturbance signal.
		SCRAMBLER_OVR	3:3	RW	0	Enables override of the scrambler enable signal.
		SCRAMBLER_EN	2:2	RW	1	Overrides the internal scrambler enable value (for high rates >3G) if SCRAMBLER_OVR is set to '1'. Applies only for encoder setting. The SCDC value will not be changed.
		RSVD	1:0	RW	0	Reserved. Do not change.
7001	STREAM_SEL	RSVD	15:14	RO	0	Reserved.
		DDO3_TX_SRC_SEL	13:12	RW	2	Selects output at DDO03 (DATA0-2/clock).
		RSVD	11:10	RO	0	Reserved.
		DDO2_TX_SRC_SEL	9:8	RW	1	Selects output at DDO2 (DATA0-2/clock).
		RSVD	7:6	RO	0	Reserved.
		DDO1_TX_SRC_SEL	5:4	RW	0	Selects output at DDO1 (DATA0-2/clock).

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09/08/2026

		RSVD	3:2	RO	0	Reserved.
		DDO0_TX_SRC_SEL	1:0	RW	3	Selects output at DDO0 (DATA0-2/clock): 00 = TMDS_DATA0 01 = TMDS_DATA1 10 = TMDS_DATA2 11 = CLOCK
7002	REG2	RSVD	15:6	RO	0	Reserved.
		HDMI_5V_EN_OVR	5:5	RW	0	Enables override of the output 5V EN signal.
		HDMI_5V_EN_REG	4:4	RW	0	Sets 5VEN signal when HDMI_5V_EN_OVR is set to 1.
		RSVD	3:2	RO	0	Reserved.
		HDMI_HPD_OVR	1:1	RW	0	Enables override of the input HPD signal.
		HDMI_HPD_REG	0:0	RW	0	Override HPD input signal value when HDMI_HPD_OVR is set to 1.
7003	REG3	RSVD	15:1	RO	0	Reserved.
		FORCE_RGB_8B	0:0	RW	0	Forces RGB 24-bit colour depth (Valid only if the video colour depth is 10-bit. If set to 1, the 2LSB will be truncated).
7004	REG4	RSVD	15:6	RW	0	Reserved. Do not change.
		SCDC_ SCRAMBL_EN_OVR	5:5	RW	0	Enables override of the SCDC_SCRAMBL_EN signal.
		SCDC_SCRAMBL_ EN_REG	4:4	RW	0	Overrides the internal scrambler enable value (HIGH for rates >3G) if SCDC_SCRAMBL_EN_OVR is set to '1'. Applies only for SCDC value.
		TMDS_BIT_CLK_ RATIO_OVR	3:3	RW	0	Enables override of the TMDS_BIT_CLK_RATIO signal.
		TMDS_BIT_CLK_ RATIO_REG	2:2	RW	0	Overrides the internal scrambler enable value (HIGH for rates >3G) if SCDC_SCRAMBL_EN_OVR is set to '1'. Applies only for SCDC value.

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09/08/2026

		RSVD	1:0	RW	0	Reserved. Do not change.
7005	REG5	RSVD	15:1	RO	0	Reserved.
		EDID_UPDATE_REG	0:0	ROSW	0	Write '1' to manually re-read the HDMI sink's EDID.
7006	REG6	RSVD	15:5	RO	0	Reserved.
		SCDC_READ_ WRITE_N_REG	4:4	RW	0	When 1, selects SCDC read when 0 selects SCDC write.
		RSVD	3:1	RO	0	Reserved.
		SCDC_UPDATE_REG	0:0	ROSW	0	Write '1' to manually re-read/write the HDMI sink's SCDC registers.
7007	REG7	RSVD	15:8	RO	0	Reserved.
		SCDC_UPDATE_ REG_ADDRESS	7:0	RW	0	SCDC register address to write or read data to/from.
7008	REG8	RSVD	15:8	RO	0	Reserved.
		SCDC_UPDATE_ REG_WDATA	7:0	RW	0	Data to write to the selected SCDC address.
7009	REG9	RSVD	15:8	RO	0	Reserved.
		SCDC_UPDATE_ REG_RDATA	7:0	RO	0	Read data from the selected SCDC address.
700A	REG10	RSVD	15:14	RO	0	Reserved.
		HPD_STATE	13:13	RO	0	Indicates HPD on the pin.
		RSVD	12:11	RO	0	Reserved.
		EDID_NO_ACK	10:10	RO	0	Indicates no acknowledge when EDID read.
		EDID_DONE	9:9	RO	0	Indicates that EDID read has been done.
		RSVD	8:6	RO	0	Reserved.

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09/03/2026

		SCDC_NO_ACK	5:5	RO	0	Indicates no acknowledge when SCDC write/read.
		SCDC_DONE	4:4	RO	0	Indicates that SCDC W/R has been done.
		RSVD	3:1	RO	0	Reserved.
		DDC_DONE	0:0	RO	0	Indicates that DDC W/R has been done (EDID and SCDC).
700B	REG11	DYN_RANGE_ INFOFRAME_ DATA_OVR	15:15	RW	0	Enables register overwrite of info frame insertion enable.
		HDMI_V_S_ INFOFRAME_ DATA_OVR	14:14	RW	0	Enables register overwrite of info frame insertion enable.
		AUDIO_ INFOFRAME_ DATA_OVR	13:13	RW	0	Enables register overwrite of info frame insertion enable.
		AVI_INFOFRAME_ DATA_OVR	12:12	RW	0	Enables register overwrite of info frame insertion enable.
		RSVD	11:9	RO	0	Reserved.
		INFO_FRAME_ EN_OVR	8:8	RW	0	Enables register overwrite of info frame insertion enable.
		INFO_FRAME_EN	7:0	RW	F	Bit wise enable of InfoFrame insertion: Bit 0 = General Control Packet Bit 1 = AVI InfoFrame Bit 2 = Audio InfoFrame Bit 3 = HDMI Vendor Specific InfoFrame Bit 4 = Dynamic Range and Mastering InfoFrame Bit 5 = Generic InfoFrame Valid if corresponding bit in INFO_FRAME_EN_OVR is set to HIGH. Valid settings of this parameter are the following ONLY: 00000001 or 00000011 or 00000111 or 00001111 or 00011111 or 00111111.
700C	REG12	AVI_INFOFRAME_ HEADER_HB1	15:8	RW	2	AVI InfoFrame header HB1, Version = 0x02.

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09/08/2026

		AVI_INFOFRAME_HEADER_HB0	7:0	RW	82	AVI InfoFrame header HB0, Packet Type = 0x82.
700D	REG13	RSVD	15:8	RO	0	Reserved.
		AVI_INFOFRAME_HEADER_HB2	7:0	RW	D	AVI InfoFrame header HB2, Length = 13 (0x0D).
700E	REG14	AVI_INFOFRAME_PB2	15:8	RW	0	AVI InfoFrame PB2.
		AVI_INFOFRAME_PB1	7:0	RW	0	AVI InfoFrame PB1. Checksum (PB0) is calculated automatically.
700F	REG15	AVI_INFOFRAME_PB4	15:8	RW	0	AVI InfoFrame PB4.
		AVI_INFOFRAME_PB3	7:0	RW	0	AVI InfoFrame PB3.
7010	REG16	AVI_INFOFRAME_PB6	15:8	RW	0	AVI InfoFrame PB6.
		AVI_INFOFRAME_PB5	7:0	RW	0	AVI InfoFrame PB5.
7011	REG17	AVI_INFOFRAME_PB8	15:8	RW	0	AVI InfoFrame PB8.
		AVI_INFOFRAME_PB7	7:0	RW	0	AVI InfoFrame PB7.
7012	REG18	AVI_INFOFRAME_PB10	15:8	RW	0	AVI InfoFrame PB10.
		AVI_INFOFRAME_PB9	7:0	RW	0	AVI InfoFrame PB9.
7013	REG19	AVI_INFOFRAME_PB12	15:8	RW	0	AVI InfoFrame PB12.
		AVI_INFOFRAME_PB11	7:0	RW	0	AVI InfoFrame PB11.
7014	REG20	RSVD	15:8	RO	0	Reserved.
		AVI_INFOFRAME_PB13	7:0	RW	0	AVI InfoFrame PB13.

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DIVA Laboratories, Ltd.
09/09/2026

7015	REG21	AUDIO_ INFOFRAME_ HEADER_HB1	15:8	RW	1	Audio InfoFrame header HB1, Version = 0x01.
		AUDIO_ INFOFRAME_ HEADER_HB0	7:0	RW	84	Audio InfoFrame header HB0, Packet Type = 0x84.
7016	REG22	RSVD	15:8	RO	0	Reserved.
		AUDIO_ INFOFRAME_ HEADER_HB2	7:0	RW	A	Audio InfoFrame header HB2, Length = 10 (0x0A).
7017	REG23	AUDIO_ INFOFRAME_PB2	15:8	RW	0	AUDIO_INFOFRAME_PB2.
		AUDIO_ INFOFRAME_PB1	7:0	RW	0	AUDIO_INFOFRAME_PB1. Checksum (PB0) is calculated automatically.
7018	REG24	AUDIO_ INFOFRAME_PB4	15:8	RW	0	AUDIO_INFOFRAME_PB4.
		AUDIO_ INFOFRAME_PB3	7:0	RW	0	AUDIO_INFOFRAME_PB3.
7019	REG25	RSVD	15:8	RO	0	Reserved.
		AUDIO_ INFOFRAME_PB5	7:0	RW	0	AUDIO_INFOFRAME_PB5.
701A	REG26	HDMI_V_S_ INFOFRAME_ HEADER_HB1	15:8	RW	1	HDMI Vendor Specific InfoFrame header HB1, Version = 0x01.
		HDMI_V_S_ INFOFRAME_ HEADER_HB0	7:0	RW	81	HDMI Vendor Specific InfoFrame header HB0, Packet Type = 0x81.
701B	REG27	RSVD	15:8	RO	0	Reserved.
		HDMI_V_S_ INFOFRAME_ HEADER_HB2	7:0	RW	5	HDMI Vendor Specific InfoFrame header HB2, Length = 5 (0x05).
701C	REG28	HDMI_V_S_ INFOFRAME_PB2	15:8	RW	0	HDMI Vendor Specific InfoFrame PB2.

Semtech Confidential Information
Kent Lin
DIVA Laboratories Ltd.
09/08/2026

		HDMI_V_S_ INFOFRAME_PB1	7:0	RW	0	HDMI Vendor Specific InfoFrame PB1. Checksum (PB0) is calculated automatically.
701D	REG29	HDMI_V_S_ INFOFRAME_PB4	15:8	RW	0	HDMI Vendor Specific InfoFrame PB4.
		HDMI_V_S_ INFOFRAME_PB3	7:0	RW	0	HDMI Vendor Specific InfoFrame PB3.
701E	REG30	HDMI_V_S_ INFOFRAME_PB6	15:8	RW	0	HDMI Vendor Specific InfoFrame PB6.
		HDMI_V_S_ INFOFRAME_PB5	7:0	RW	0	HDMI Vendor Specific InfoFrame PB5.
701F	REG31	HDMI_V_S_ INFOFRAME_PB8	15:8	RW	0	HDMI Vendor Specific InfoFrame PB8.
		HDMI_V_S_ INFOFRAME_PB7	7:0	RW	0	HDMI Vendor Specific InfoFrame PB7.
7020	REG32	HDMI_V_S_ INFOFRAME_PB10	15:8	RW	0	HDMI Vendor Specific InfoFrame PB10.
		HDMI_V_S_ INFOFRAME_PB9	7:0	RW	0	HDMI Vendor Specific InfoFrame PB9.
7021	REG33	HDMI_V_S_ INFOFRAME_PB12	15:8	RW	0	HDMI Vendor Specific InfoFrame PB12.
		HDMI_V_S_ INFOFRAME_PB11	7:0	RW	0	HDMI Vendor Specific InfoFrame PB11.
7022	REG34	HDMI_V_S_ INFOFRAME_PB14	15:8	RW	0	HDMI Vendor Specific InfoFrame PB14.
		HDMI_V_S_ INFOFRAME_PB13	7:0	RW	0	HDMI Vendor Specific InfoFrame PB13.
7023	REG35	HDMI_V_S_ INFOFRAME_PB16	15:8	RW	0	HDMI Vendor Specific InfoFrame PB16.
		HDMI_V_S_ INFOFRAME_PB15	7:0	RW	0	HDMI Vendor Specific InfoFrame PB15.
7024	REG36	HDMI_V_S_ INFOFRAME_PB18	15:8	RW	0	HDMI Vendor Specific InfoFrame PB18.

Semtech Confidential Information
Kent Lin
DIVA Laboratories, Ltd.
09/08/2026

		HDMI_V_S_ INFOFRAME_PB17	7:0	RW	0	HDMI Vendor Specific InfoFrame PB17.
7025	REG37	HDMI_V_S_ INFOFRAME_PB20	15:8	RW	0	HDMI Vendor Specific InfoFrame PB20.
		HDMI_V_S_ INFOFRAME_PB19	7:0	RW	0	HDMI Vendor Specific InfoFrame PB19.
7026	REG38	HDMI_V_S_ INFOFRAME_PB22	15:8	RW	0	HDMI Vendor Specific InfoFrame PB22.
		HDMI_V_S_ INFOFRAME_PB21	7:0	RW	0	HDMI Vendor Specific InfoFrame PB21.
7027	REG39	HDMI_V_S_ INFOFRAME_PB24	15:8	RW	0	HDMI Vendor Specific InfoFrame PB24.
		HDMI_V_S_ INFOFRAME_PB23	7:0	RW	0	HDMI Vendor Specific InfoFrame PB23.
7028	REG40	HDMI_V_S_ INFOFRAME_PB26	15:8	RW	0	HDMI Vendor Specific InfoFrame PB26.
		HDMI_V_S_ INFOFRAME_PB25	7:0	RW	0	HDMI Vendor Specific InfoFrame PB25.
7029	REG41	RSVD	15:8	RO	0	Reserved.
		HDMI_V_S_ INFOFRAME_PB27	7:0	RW	0	HDMI Vendor Specific InfoFrame PB27.
702A	REG42	RSVD	15:14	RO	0	Reserved.
		HDMI_AUDIO_ INS_IS_96KHZ_ OVRD	13:13	RW	0	Enables override of the internal value for audio sampling frequency.
		HDMI_AUDIO_ INS_IS_96KHZ	12:12	RW	0	Overrides internal signal when HDMI_AUDIO_INS_IS_96KHZ_OVRD = 1: 0 = Audio is 48kHz 1 = Audio is 96kHz
		A_IN_STREAM_ 7_8_SEL	11:10	RW	3	Selects audio which will be inserted as stream 7_8.
		A_IN_STREAM_ 5_6_SEL	9:8	RW	2	Selects audio which will be inserted as stream 5_6.

Semtech Confidential Information
Kent Lin
DIVA Laboratories, Ltd.
09/08/2026

		A_IN_STREAM_3_4_SEL	7:6	RW	1	Selects audio which will be inserted as stream 3_4.
		A_IN_STREAM_1_2_SEL	5:4	RW	0	Selects audio which will be inserted as stream 1_2: 00 = Audio selected at channels 1-2 (9-10) 01 = Audio selected at channels 3-4 10 = Audio selected at channels 5-6 11 = Audio selected at channels 7-8 (15-19)
		RSVD	3:2	RO	0	Reserved.
		AUDIO_SEL_9TO16_1TO8B	1:1	RW	0	Selects eight audio channels, out of 16 possible, to be embedded into HDMI video stream. 1 = Selects channels 9-16 0 = selects channels 1-8
		AUDIO_SEL_EXT_SDI	0:0	RW	0	Selects audio to be embedded into HDMI stream from audio extracted from SDI video input stream or audio fed from external pins: 0 = SDI audio 1 = External audio
702B	RSVD_REG	RSVD	15:0	RO	0	Reserved.
702C	REG44	RSVD	15:6	RO	0	Reserved.
		CTS_CNT_INCR_OVR	5:5	RW	0	Enables CTS_CNT_INCR override.
		CTS_CNT_INCR	4:4	RW	0	Debug. Configuration for the increment step of the CTS counter. When LOW, the counter increments by 1. When HIGH, the counter increments by 4.
		RSVD	3:3	RO	0	Reserved.
		HDMI_TX_AUDIO_SCLK_POLARITY	2:2	RW	0	HDMI Tx audio SCLK polarity: 0 = audio data to be captured by the rising edge of SCLK 1 = audio data to be captured by the falling edge of SCLK

Semtech Confidential Information
Kent Lin
DIVA Laboratories. Ltd.
09/08/2026

		HDMI_TX_AUDIO_WCLK_POLARITY	1:1	RW	1	HDMI Tx audio WCLK polarity: 0 = Sample left channel on WCLK falling and right channel on WCLK rising 1 = Sample left channel on WCLK rising and right channel on WCLK falling
		HDMI_TX_AUDIO_SERIAL_MODE	0:0	RW	1	HDMI Tx audio serial mode: 0 = Left justify 1 = I²S mode (first bit delayed by one SCLK)
702D	REG45	HDMI_AUDIO_N_VALUE_LSB	15:0	RW	1800	16 LSBs of the audio N value, used to override internal signal.
702E	REG46	RSVD	15:5	RO	0	Reserved.
		HDMI_AUDIO_N_VALUE_OVR	4:4	RW	0	Enables AUDIO_N_VALUE override.
		HDMI_AUDIO_N_VALUE_MSB	3:0	RW	0	4 MSBs of the audio N value, used to override internal signal. Default N = 6144.
702F	REG47	RSVD	15:2	RO	0	Reserved.
		HDMI_TX_AUDIO_SERIAL_IS_96KHZ	1:1	RO	0	HDMI Tx audio is 96kHz. When HIGH indicates that the block detects 96kHz audio present on the I²S serial lines. When LOW, 48kHz audio is set.
		HDMI_TX_AUDIO_SERIAL_PRESENT	0:0	RO	0	HDMI Tx audio detected. When HIGH indicates that the block detects the audio WCLK toggling and therefore declares audio present on the I²S serial lines (audio to be embedded in the HDMI stream). When LOW, no audio is detected.
7030	REG48	RSVD	15:3	RO	0	Reserved.
		HDMI_TX_AUDIO_CLK_REGEN_PKT_ENABLE	2:2	RW	1	When HIGH, enables audio clock regeneration packets insertion. When LOW, disables audio clock regeneration packets insertion.
		HDMI_TX_AUDIO_SAMPLE_PKT_ENABLE	1:1	RW	1	When HIGH, enables audio sample packets insertion. When LOW, disables audio sample packets insertion.

Semtech Confidential Information
Kent Lin
DIVA Laboratories. Ltd.
09/08/2026

		HDMI_TX_AUX_ ENABLE	0:0	RW	1	When HIGH, enables the block to perform auxiliary packets (InfoFrame, audio sample, audio clock regeneration) insertion. When LOW, the packet insertion functionality is disabled and the block simply retransmit what came to it.
7031	REG49	RSVD	15:8	RO	0	Reserved.
		HDMI_TX_AUDIO_ PKT_TYPE	7:0	RW	2	Bits related to audio sample packets. Header parameter. A value of 2 indicates Audio Sample (L-PCM and IEC 61937 compressed formats). A value of 9 indicates a High Bit Rate (HBR) Audio Stream Packet (IEC 61937). Any other values do not indicate an audio packet and are not valid configurations.
7032	REG50	RSVD	15:9	RO	0	Reserved.
		HDMI_TX_AUDIO_ SAMPLE_FLAT	8:5	RW	0	Bits related to audio sample packets, one bit per channel pair. It indicates if audio samples are mute samples (value of 1) or actual audio (value of 0). Bit 0 = Channels 1&2 Bit 1 = Channels 3&4 Bit 2 = Channels 5&6 Bit 3 = Channels 7&8
		HDMI_TX_AUDIO_ SAMPLE_PRESENT	4:1	RW	F	Bits related to audio sample packets, one bit per channel pair. It indicates if there are valid audio samples. Bit 0 = Channels 1&2 Bit 1 = Channels 3&4 Bit 2 = Channels 5&6 Bit 3 = Channels 7&8 Valid configurations of this parameter are 0001, 0011, 0111, and 1111.
		HDMI_TX_AUDIO_ PKT_LAYOUT_BIT	0:0	RW	1	Bit related to audio sample packets. When LOW, indicates that the audio sample packet carries a maximum of 2 audio channels and therefore 4 samples of each channel. When HIGH, indicates that the audio sample packet carries a maximum of 8 audio channels and therefore 1 sample of each channel.
7033	REG51	RSVD	15:1	RO	0	Reserved.

Semtech Confidential Information
Kent Lin
DIVA Laboratories, Ltd.
09/08/2026

		HDMI_TX_AUDIO_CH_STAT_OVR_EN	0:0	RW	0	When HIGH, the HDMI_TX_AUDIO_CH_STAT_*_*_BYTE*_OVR (register addresses 7034 to 7063) CSR bits will be used to construct the audio channel status fields of the audio sample packets. When LOW, the channel status extracted in the audio packets of the SDI signal will be used.
7034	REG52	HDMI_TX_AUDIO_CH_STAT_1_2_BYTE_1_OVR	15:8	RW	0	Audio channel status override for audio channels 1 and 2, byte 1 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_1_2_BYTE_0_OVR	7:0	RW	0	Audio channel status override for audio channels 1 and 2, byte 0 (as per AES3-1992 standard definition).
7035	REG53	HDMI_TX_AUDIO_CH_STAT_1_2_BYTE_3_OVR	15:8	RW	0	Audio channel status override for audio channels 1 and 2, byte 3 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_1_2_BYTE_2_OVR	7:0	RW	0	Audio channel status override for audio channels 1 and 2, byte 2 (as per AES3-1992 standard definition).
7036	REG54	HDMI_TX_AUDIO_CH_STAT_1_2_BYTE_5_OVR	15:8	RW	0	Audio channel status override for audio channels 1 and 2, byte 5 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_1_2_BYTE_4_OVR	7:0	RW	0	Audio channel status override for audio channels 1 and 2, byte 4 (as per AES3-1992 standard definition).
7037	REG55	HDMI_TX_AUDIO_CH_STAT_1_2_BYTE_7_OVR	15:8	RW	0	Audio channel status override for audio channels 1 and 2, byte 7 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_1_2_BYTE_6_OVR	7:0	RW	0	Audio channel status override for audio channels 1 and 2, byte 6 (as per AES3-1992 standard definition).
7038	REG56	HDMI_TX_AUDIO_CH_STAT_1_2_BYTE_9_OVR	15:8	RW	0	Audio channel status override for audio channels 1 and 2, byte 9 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_1_2_BYTE_8_OVR	7:0	RW	0	Audio channel status override for audio channels 1 and 2, byte 8 (as per AES3-1992 standard definition).

Semtech Confidential Information
Keat Lin
DIVA Laboratories, Ltd.
09/08/2026

7039	REG57	HDMI_TX_AUDIO_CH_STAT_1_2_BYTE_11_OVR	15:8	RW	0	Audio channel status override for audio channels 1 and 2, byte 11 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_1_2_BYTE_10_OVR	7:0	RW	0	Audio channel status override for audio channels 1 and 2, byte 10 (as per AES3-1992 standard definition).
703A	REG58	HDMI_TX_AUDIO_CH_STAT_1_2_BYTE_13_OVR	15:8	RW	0	Audio channel status override for audio channels 1 and 2, byte 13 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_1_2_BYTE_12_OVR	7:0	RW	0	Audio channel status override for audio channels 1 and 2, byte 12 (as per AES3-1992 standard definition).
703B	REG59	HDMI_TX_AUDIO_CH_STAT_1_2_BYTE_15_OVR	15:8	RW	0	Audio channel status override for audio channels 1 and 2, byte 15 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_1_2_BYTE_14_OVR	7:0	RW	0	Audio channel status override for audio channels 1 and 2, byte 14 (as per AES3-1992 standard definition).
703C	REG60	HDMI_TX_AUDIO_CH_STAT_1_2_BYTE_17_OVR	15:8	RW	0	Audio channel status override for audio channels 1 and 2, byte 17 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_1_2_BYTE_16_OVR	7:0	RW	0	Audio channel status override for audio channels 1 and 2, byte 16 (as per AES3-1992 standard definition).
703D	REG61	HDMI_TX_AUDIO_CH_STAT_1_2_BYTE_19_OVR	15:8	RW	0	Audio channel status override for audio channels 1 and 2, byte 19 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_1_2_BYTE_18_OVR	7:0	RW	0	Audio channel status override for audio channels 1 and 2, byte 18 (as per AES3-1992 standard definition).
703E	REG62	HDMI_TX_AUDIO_CH_STAT_1_2_BYTE_21_OVR	15:8	RW	0	Audio channel status override for audio channels 1 and 2, byte 21 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_1_2_BYTE_20_OVR	7:0	RW	0	Audio channel status override for audio channels 1 and 2, byte 20 (as per AES3-1992 standard definition).

Semtech Confidential Information
Kent Lin
DIVA Laboratories, Ltd.
09/08/2026

703F	REG63	HDMI_TX_AUDIO_CH_STAT_1_2_BYTE_23_OVR	15:8	RW	0	Audio channel status override for audio channels 1 and 2, byte 23 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_1_2_BYTE_22_OVR	7:0	RW	0	Audio channel status override for audio channels 1 and 2, byte 22 (as per AES3-1992 standard definition).
7040	REG64	HDMI_TX_AUDIO_CH_STAT_3_4_BYTE_1_OVR	15:8	RW	0	Audio channel status override for audio channels 3 and 4, byte 1 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_3_4_BYTE_0_OVR	7:0	RW	0	Audio channel status override for audio channels 3 and 4, byte 0 (as per AES3-1992 standard definition).
7041	REG65	HDMI_TX_AUDIO_CH_STAT_3_4_BYTE_3_OVR	15:8	RW	0	Audio channel status override for audio channels 3 and 4, byte 3 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_3_4_BYTE_2_OVR	7:0	RW	0	Audio channel status override for audio channels 3 and 4, byte 2 (as per AES3-1992 standard definition).
7042	REG66	HDMI_TX_AUDIO_CH_STAT_3_4_BYTE_5_OVR	15:8	RW	0	Audio channel status override for audio channels 3 and 4, byte 5 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_3_4_BYTE_4_OVR	7:0	RW	0	Audio channel status override for audio channels 3 and 4, byte 4 (as per AES3-1992 standard definition).
7043	REG67	HDMI_TX_AUDIO_CH_STAT_3_4_BYTE_7_OVR	15:8	RW	0	Audio channel status override for audio channels 3 and 4, byte 7 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_3_4_BYTE_6_OVR	7:0	RW	0	Audio channel status override for audio channels 3 and 4, byte 6 (as per AES3-1992 standard definition).
7044	REG68	HDMI_TX_AUDIO_CH_STAT_3_4_BYTE_9_OVR	15:8	RW	0	Audio channel status override for audio channels 3 and 4, byte 9 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_3_4_BYTE_8_OVR	7:0	RW	0	Audio channel status override for audio channels 3 and 4, byte 8 (as per AES3-1992 standard definition).

Semtech Confidential Information
Kent Lin
DIVA Laboratories, Ltd.
09/08/2026

7045	REG69	HDMI_TX_AUDIO_CH_STAT_3_4_BYTE_11_OVR	15:8	RW	0	Audio channel status override for audio channels 3 and 4, byte 11 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_3_4_BYTE_10_OVR	7:0	RW	0	Audio channel status override for audio channels 3 and 4, byte 10 (as per AES3-1992 standard definition).
7046	REG70	HDMI_TX_AUDIO_CH_STAT_3_4_BYTE_13_OVR	15:8	RW	0	Audio channel status override for audio channels 3 and 4, byte 13 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_3_4_BYTE_12_OVR	7:0	RW	0	Audio channel status override for audio channels 3 and 4, byte 12 (as per AES3-1992 standard definition).
7047	REG71	HDMI_TX_AUDIO_CH_STAT_3_4_BYTE_15_OVR	15:8	RW	0	Audio channel status override for audio channels 3 and 4, byte 15 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_3_4_BYTE_14_OVR	7:0	RW	0	Audio channel status override for audio channels 3 and 4, byte 14 (as per AES3-1992 standard definition).
7048	REG72	HDMI_TX_AUDIO_CH_STAT_3_4_BYTE_17_OVR	15:8	RW	0	Audio channel status override for audio channels 3 and 4, byte 17 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_3_4_BYTE_16_OVR	7:0	RW	0	Audio channel status override for audio channels 3 and 4, byte 16 (as per AES3-1992 standard definition).
7049	REG73	HDMI_TX_AUDIO_CH_STAT_3_4_BYTE_19_OVR	15:8	RW	0	Audio channel status override for audio channels 3 and 4, byte 19 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_3_4_BYTE_18_OVR	7:0	RW	0	Audio channel status override for audio channels 3 and 4, byte 18 (as per AES3-1992 standard definition).
704A	REG74	HDMI_TX_AUDIO_CH_STAT_3_4_BYTE_21_OVR	15:8	RW	0	Audio channel status override for audio channels 3 and 4, byte 21 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_3_4_BYTE_20_OVR	7:0	RW	0	Audio channel status override for audio channels 3 and 4, byte 20 (as per AES3-1992 standard definition).

Semtech Confidential Information
Kent Lin
DIVA Laboratories, Ltd.
09/08/2026

704B	REG75	HDMI_TX_AUDIO_CH_STAT_3_4_BYTE_23_OVR	15:8	RW	0	Audio channel status override for audio channels 3 and 4, byte 23 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_3_4_BYTE_22_OVR	7:0	RW	0	Audio channel status override for audio channels 3 and 4, byte 22 (as per AES3-1992 standard definition).
704C	REG76	HDMI_TX_AUDIO_CH_STAT_5_6_BYTE_1_OVR	15:8	RW	0	Audio channel status override for audio channels 5 and 6, byte 1 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_5_6_BYTE_0_OVR	7:0	RW	0	Audio channel status override for audio channels 5 and 6, byte 0 (as per AES3-1992 standard definition).
704D	REG77	HDMI_TX_AUDIO_CH_STAT_5_6_BYTE_3_OVR	15:8	RW	0	Audio channel status override for audio channels 5 and 6, byte 3 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_5_6_BYTE_2_OVR	7:0	RW	0	Audio channel status override for audio channels 5 and 6, byte 2 (as per AES3-1992 standard definition).
704E	REG78	HDMI_TX_AUDIO_CH_STAT_5_6_BYTE_5_OVR	15:8	RW	0	Audio channel status override for audio channels 5 and 6, byte 5 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_5_6_BYTE_4_OVR	7:0	RW	0	Audio channel status override for audio channels 5 and 6, byte 4 (as per AES3-1992 standard definition).
704F	REG79	HDMI_TX_AUDIO_CH_STAT_5_6_BYTE_7_OVR	15:8	RW	0	Audio channel status override for audio channels 5 and 6, byte 7 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_5_6_BYTE_6_OVR	7:0	RW	0	Audio channel status override for audio channels 5 and 6, byte 6 (as per AES3-1992 standard definition).
7050	REG80	HDMI_TX_AUDIO_CH_STAT_5_6_BYTE_9_OVR	15:8	RW	0	Audio channel status override for audio channels 5 and 6, byte 9 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_5_6_BYTE_8_OVR	7:0	RW	0	Audio channel status override for audio channels 5 and 6, byte 8 (as per AES3-1992 standard definition).

Semtech Confidential Information
Kent Lin
DIVA Laboratories, Ltd.
09/08/2026

7051	REG81	HDMI_TX_AUDIO_CH_STAT_5_6_BYTE_11_OVR	15:8	RW	0	Audio channel status override for audio channels 5 and 6, byte 11 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_5_6_BYTE_10_OVR	7:0	RW	0	Audio channel status override for audio channels 5 and 6, byte 10 (as per AES3-1992 standard definition).
7052	REG82	HDMI_TX_AUDIO_CH_STAT_5_6_BYTE_13_OVR	15:8	RW	0	Audio channel status override for audio channels 5 and 6, byte 13 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_5_6_BYTE_12_OVR	7:0	RW	0	Audio channel status override for audio channels 5 and 6, byte 12 (as per AES3-1992 standard definition).
7053	REG83	HDMI_TX_AUDIO_CH_STAT_5_6_BYTE_15_OVR	15:8	RW	0	Audio channel status override for audio channels 5 and 6, byte 15 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_5_6_BYTE_14_OVR	7:0	RW	0	Audio channel status override for audio channels 5 and 6, byte 14 (as per AES3-1992 standard definition).
7054	REG84	HDMI_TX_AUDIO_CH_STAT_5_6_BYTE_17_OVR	15:8	RW	0	Audio channel status override for audio channels 5 and 6, byte 17 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_5_6_BYTE_16_OVR	7:0	RW	0	Audio channel status override for audio channels 5 and 6, byte 16 (as per AES3-1992 standard definition).
7055	REG85	HDMI_TX_AUDIO_CH_STAT_5_6_BYTE_19_OVR	15:8	RW	0	Audio channel status override for audio channels 5 and 6, byte 19 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_5_6_BYTE_18_OVR	7:0	RW	0	Audio channel status override for audio channels 5 and 6, byte 18 (as per AES3-1992 standard definition).
7056	REG86	HDMI_TX_AUDIO_CH_STAT_5_6_BYTE_21_OVR	15:8	RW	0	Audio channel status override for audio channels 5 and 6, byte 21 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_5_6_BYTE_20_OVR	7:0	RW	0	Audio channel status override for audio channels 5 and 6, byte 20 (as per AES3-1992 standard definition).

Semtech Confidential Information
Kent Lin
DIVA Laboratories Ltd.
09/08/2026

7057	REG87	HDMI_TX_AUDIO_CH_STAT_5_6_BYTE_23_OVR	15:8	RW	0	Audio channel status override for audio channels 5 and 6, byte 23 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_5_6_BYTE_22_OVR	7:0	RW	0	Audio channel status override for audio channels 5 and 6, byte 22 (as per AES3-1992 standard definition).
7058	REG88	HDMI_TX_AUDIO_CH_STAT_7_8_BYTE_1_OVR	15:8	RW	0	Audio channel status override for audio channels 7 and 8, byte 1 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_7_8_BYTE_0_OVR	7:0	RW	0	Audio channel status override for audio channels 7 and 8, byte 0 (as per AES3-1992 standard definition).
7059	REG89	HDMI_TX_AUDIO_CH_STAT_7_8_BYTE_3_OVR	15:8	RW	0	Audio channel status override for audio channels 7 and 8, byte 3 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_7_8_BYTE_2_OVR	7:0	RW	0	Audio channel status override for audio channels 7 and 8, byte 2 (as per AES3-1992 standard definition).
705A	REG90	HDMI_TX_AUDIO_CH_STAT_7_8_BYTE_5_OVR	15:8	RW	0	Audio channel status override for audio channels 7 and 8, byte 5 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_7_8_BYTE_4_OVR	7:0	RW	0	Audio channel status override for audio channels 7 and 8, byte 4 (as per AES3-1992 standard definition).
705B	REG91	HDMI_TX_AUDIO_CH_STAT_7_8_BYTE_7_OVR	15:8	RW	0	Audio channel status override for audio channels 7 and 8, byte 7 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_7_8_BYTE_6_OVR	7:0	RW	0	Audio channel status override for audio channels 7 and 8, byte 6 (as per AES3-1992 standard definition).
705C	REG92	HDMI_TX_AUDIO_CH_STAT_7_8_BYTE_9_OVR	15:8	RW	0	Audio channel status override for audio channels 7 and 8, byte 9 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_7_8_BYTE_8_OVR	7:0	RW	0	Audio channel status override for audio channels 7 and 8, byte 8 (as per AES3-1992 standard definition).

Semtech Confidential Information
Kent Lin
DIVA Laboratories, Ltd.
09/08/2026

705D	REG93	HDMI_TX_AUDIO_CH_STAT_7_8_BYTE_11_OVR	15:8	RW	0	Audio channel status override for audio channels 7 and 8, byte 11 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_7_8_BYTE_10_OVR	7:0	RW	0	Audio channel status override for audio channels 7 and 8, byte 10 (as per AES3-1992 standard definition).
705E	REG94	HDMI_TX_AUDIO_CH_STAT_7_8_BYTE_13_OVR	15:8	RW	0	Audio channel status override for audio channels 7 and 8, byte 13 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_7_8_BYTE_12_OVR	7:0	RW	0	Audio channel status override for audio channels 7 and 8, byte 12 (as per AES3-1992 standard definition).
705F	REG95	HDMI_TX_AUDIO_CH_STAT_7_8_BYTE_15_OVR	15:8	RW	0	Audio channel status override for audio channels 7 and 8, byte 15 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_7_8_BYTE_14_OVR	7:0	RW	0	Audio channel status override for audio channels 7 and 8, byte 14 (as per AES3-1992 standard definition).
7060	REG96	HDMI_TX_AUDIO_CH_STAT_7_8_BYTE_17_OVR	15:8	RW	0	Audio channel status override for audio channels 7 and 8, byte 17 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_7_8_BYTE_16_OVR	7:0	RW	0	Audio channel status override for audio channels 7 and 8, byte 16 (as per AES3-1992 standard definition).
7061	REG97	HDMI_TX_AUDIO_CH_STAT_7_8_BYTE_19_OVR	15:8	RW	0	Audio channel status override for audio channels 7 and 8, byte 19 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_7_8_BYTE_18_OVR	7:0	RW	0	Audio channel status override for audio channels 7 and 8, byte 18 (as per AES3-1992 standard definition).
7062	REG98	HDMI_TX_AUDIO_CH_STAT_7_8_BYTE_21_OVR	15:8	RW	0	Audio channel status override for audio channels 7 and 8, byte 21 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_7_8_BYTE_20_OVR	7:0	RW	0	Audio channel status override for audio channels 7 and 8, byte 20 (as per AES3-1992 standard definition).

Semtech Confidential Information
Kent Lin
DIVA Laboratories, Ltd.
09/08/2026

7063	REG99	HDMI_TX_AUDIO_CH_STAT_7_8_BYTE_23_OVR	15:8	RW	0	Audio channel status override for audio channels 7 and 8, byte 23 (as per AES3-1992 standard definition).
		HDMI_TX_AUDIO_CH_STAT_7_8_BYTE_22_OVR	7:0	RW	0	Audio channel status override for audio channels 7 and 8, byte 22 (as per AES3-1992 standard definition).
7064	REG100	GEN_CTRL_PACKET_HEADER_HB1	15:8	RW	0	General Control Packet header HB1, Version = 0x00.
		GEN_CTRL_PACKET_HEADER_HB0	7:0	RW	3	General Control Packet InfoFrame header HB0, Packet Type = 0x03.
7065	REG101	RSVD	15:8	RO	0	Reserved.
		GEN_CTRL_PACKET_HEADER_HB2	7:0	RW	0	General Control Packet header HB2, Length = 0x00.
7066	REG102	RSVD	15:10	RO	0	Reserved.
		DEFAULT_PHASE_OVR	9:9	RW	0	Enables override of Default Phase in General Control Packet.
		DEFAULT_PHASE_REG	8:8	RW	0	Overrides Default Phase in General Control Packet when DEFAULT_PHASE_OVR is set to '1'.
		RSVD	7:5	RO	0	Reserved.
		GEN_CTRL_PCK_COLOR_DEPTH_OVR	4:4	RW	0	Enables override of colour depth in General Control Packet.
		GEN_CTRL_PCK_COLOR_DEPTH_REG	3:0	RW	4	Overrides selected colour depth in General Control Packet when GEN_CTRL_PCK_COLOR_DEPTH_OVR is set to '1'.
7067	REG103	RSVD	15:2	RO	0	Reserved.
		SET_AVMUTE	1:1	RW	0	SET_AVMUTE value to be embedded in General Control Packet.
		CLEAR_AVMUTE	0:0	RW	0	CLEAR_AVMUTE value to be embedded in General Control Packet.

Semtech Confidential Information
Kent Lin
DIVA Laboratories Ltd.
09/08/2026

7068	REG104	RSVD	15:1	RO	0	Reserved.
		DYN_RANGE_ INFOFRAME_ BYTE_1_2_EN_OVR	0:0	RW	0	Enables override of PB1 and PB2 in the Dynamic Range and Mastering InfoFrame. If set to 1, values from reg 706B are used, if set to 0, calculated values based on PIDs in input video stream(s) are used. **Note:** for PB3-PB26 values from registers 706C-7077 are always used, when Dynamic Range and Mastering InfoFrame embedding is enabled. If override is not used keep these registers at value 0.
7069	REG105	DYN_RANGE_ INFOFRAME_ HEADER_HB1	15:8	RW	1	Dynamic Range and Mastering InfoFrame header HB1.
		DYN_RANGE_ INFOFRAME_ HEADER_HB0	7:0	RW	7	Dynamic Range and Mastering InfoFrame header HB0. **Note:** If used, register value should be set to 87_h.
706A	REG106	RSVD	15:8	RW	0	Reserved. Do not change.
		DYN_RANGE_ INFOFRAME_ HEADER_HB2	7:0	RW	1A	Dynamic Range and Mastering InfoFrame header HB2, Length = 26.
706B	REG107	DYN_RANGE_ INFOFRAME_PB2	15:8	RW	0	Dynamic Range and Mastering InfoFrame Data Byte 2.
		DYN_RANGE_ INFOFRAME_PB1	7:0	RW	0	Dynamic Range and Mastering InfoFrame Data Byte 1.
706C	REG108	DYN_RANGE_ INFOFRAME_PB4	15:8	RW	0	Dynamic Range and Mastering InfoFrame Data Byte 4.
		DYN_RANGE_ INFOFRAME_PB3	7:0	RW	0	Dynamic Range and Mastering InfoFrame Data Byte 3.
706D	REG109	DYN_RANGE_ INFOFRAME_PB6	15:8	RW	0	Dynamic Range and Mastering InfoFrame Data Byte 6.
		DYN_RANGE_ INFOFRAME_PB5	7:0	RW	0	Dynamic Range and Mastering InfoFrame Data Byte 5.
706E	REG110	DYN_RANGE_ INFOFRAME_PB8	15:8	RW	0	Dynamic Range and Mastering InfoFrame Data Byte 8.

Semtech Confidential Information
Kent Lin
DIVA Laboratories. Ltd.
09/08/2026

		DYN_RANGE_ INFOFRAME_PB7	7:0	RW	0	Dynamic Range and Mastering InfoFrame Data Byte 7.
706F	REG111	DYN_RANGE_ INFOFRAME_PB10	15:8	RW	0	Dynamic Range and Mastering InfoFrame Data Byte 10.
		DYN_RANGE_ INFOFRAME_PB9	7:0	RW	0	Dynamic Range and Mastering InfoFrame Data Byte 9.
7070	REG112	DYN_RANGE_ INFOFRAME_PB12	15:8	RW	0	Dynamic Range and Mastering InfoFrame Data Byte 12.
		DYN_RANGE_ INFOFRAME_PB11	7:0	RW	0	Dynamic Range and Mastering InfoFrame Data Byte 11.
7071	REG113	DYN_RANGE_ INFOFRAME_PB14	15:8	RW	0	Dynamic Range and Mastering InfoFrame Data Byte 14.
		DYN_RANGE_ INFOFRAME_PB13	7:0	RW	0	Dynamic Range and Mastering InfoFrame Data Byte 13.
7072	REG114	DYN_RANGE_ INFOFRAME_PB16	15:8	RW	0	Dynamic Range and Mastering InfoFrame Data Byte 16.
		DYN_RANGE_ INFOFRAME_PB15	7:0	RW	0	Dynamic Range and Mastering InfoFrame Data Byte 15.
7073	REG115	DYN_RANGE_ INFOFRAME_PB18	15:8	RW	0	Dynamic Range and Mastering InfoFrame Data Byte 18.
		DYN_RANGE_ INFOFRAME_PB17	7:0	RW	0	Dynamic Range and Mastering InfoFrame Data Byte 17.
7074	REG116	DYN_RANGE_ INFOFRAME_PB20	15:8	RW	0	Dynamic Range and Mastering InfoFrame Data Byte 20.
		DYN_RANGE_ INFOFRAME_PB19	7:0	RW	0	Dynamic Range and Mastering InfoFrame Data Byte 19.
7075	REG117	DYN_RANGE_ INFOFRAME_PB22	15:8	RW	0	Dynamic Range and Mastering InfoFrame Data Byte 22.
		DYN_RANGE_ INFOFRAME_PB21	7:0	RW	0	Dynamic Range and Mastering InfoFrame Data Byte 21.

Semtech Confidential Information
Kent Lin
DIVA Laboratories, Ltd.
09/08/2026

7076	REG118	DYN_RANGE_ INFOFRAME_PB24	15:8	RW	0	Dynamic Range and Mastering InfoFrame Data Byte 24.
		DYN_RANGE_ INFOFRAME_PB23	7:0	RW	0	Dynamic Range and Mastering InfoFrame Data Byte 23.
7077	REG119	DYN_RANGE_ INFOFRAME_PB26	15:8	RW	0	Dynamic Range and Mastering InfoFrame Data Byte 26.
		DYN_RANGE_ INFOFRAME_PB25	7:0	RW	0	Dynamic Range and Mastering InfoFrame Data Byte 25.
7078	GENERIC_ INFOFRAME_ HEADER_1	GENERIC_ INFOFRAME_ HEADER_HB1	15:8	RW	0	Generic InfoFrame header HB1.
		GENERIC_ INFOFRAME_ HEADER_HB0	7:0	RW	0	Generic InfoFrame header HB0, user defined Packet Type Value.
7079	GENERIC_ INFOFRAME_ HEADER_2	RSVD	15:8	RO	0	Reserved.
		GENERIC_ INFOFRAME_ HEADER_HB2	7:0	RW	0	Generic InfoFrame header HB2.
707A	GENERIC_ INFOFRAME_ PAYLOAD_ BYTES_0_ AND_1_REG	GENERIC_ INFOFRAME_PB1	15:8	RW	0	Generic InfoFrame Data Byte 1.
		GENERIC_ INFOFRAME_PB0	7:0	RW	0	Generic InfoFrame Data Byte 0.
707B	GENERIC_ INFOFRAME_ PAYLOAD_ BYTES_2_ AND_3_REG	GENERIC_ INFOFRAME_PB3	15:8	RW	0	Generic InfoFrame Data Byte 3.
		GENERIC_ INFOFRAME_PB2	7:0	RW	0	Generic InfoFrame Data Byte 2.
707C	GENERIC_ INFOFRAME_ PAYLOAD_ BYTES_4_ AND_5_REG	GENERIC_ INFOFRAME_PB5	15:8	RW	0	Generic InfoFrame Data Byte 5.
		GENERIC_ INFOFRAME_PB4	7:0	RW	0	Generic InfoFrame Data Byte 4.
707D	GENERIC_ INFOFRAME_	GENERIC_ INFOFRAME_PB7	15:8	RW	0	Generic InfoFrame Data Byte 7.

Semtech Confidential Information
Kent Lin
DIVA Laboratories Ltd.
09/08/2026

	PAYLOAD_ BYTES_6_ AND_7_REG	GENERIC_ INFOFRAME_PB6	7:0	RW	0	Generic InfoFrame Data Byte 6.
707E	GENERIC_ INFOFRAME_ PAYLOAD_ BYTES_8_ AND_9_REG	GENERIC_ INFOFRAME_PB9	15:8	RW	0	Generic InfoFrame Data Byte 9.
		GENERIC_ INFOFRAME_PB8	7:0	RW	0	Generic InfoFrame Data Byte 8.
707F	GENERIC_ INFOFRAME_ PAYLOAD_ BYTES_10_ AND_11_REG	GENERIC_ INFOFRAME_PB11	15:8	RW	0	Generic InfoFrame Data Byte 11.
		GENERIC_ INFOFRAME_PB10	7:0	RW	0	Generic InfoFrame Data Byte 10.
7080	GENERIC_ INFOFRAME_ PAYLOAD_ BYTES_12_ AND_13_REG	GENERIC_ INFOFRAME_PB13	15:8	RW	0	Generic InfoFrame Data Byte 13.
		GENERIC_ INFOFRAME_PB12	7:0	RW	0	Generic InfoFrame Data Byte 12.
7081	GENERIC_ INFOFRAME_ PAYLOAD_ BYTES_14_ AND_15_REG	GENERIC_ INFOFRAME_PB15	15:8	RW	0	Generic InfoFrame Data Byte 15.
		GENERIC_ INFOFRAME_PB16	7:0	RW	0	Generic InfoFrame Data Byte 16.
7082	GENERIC_ INFOFRAME_ PAYLOAD_ BYTES_16_ AND_17_REG	GENERIC_ INFOFRAME_PB17	15:8	RW	0	Generic InfoFrame Data Byte 17.
		GENERIC_ INFOFRAME_PB16	7:0	RW	0	Generic InfoFrame Data Byte 16.
7083	GENERIC_ INFOFRAME_ PAYLOAD_ BYTES_18_ AND_19_REG	GENERIC_ INFOFRAME_PB19	15:8	RW	0	Generic InfoFrame Data Byte 19.
		GENERIC_ INFOFRAME_PB18	7:0	RW	0	Generic InfoFrame Data Byte 18.
7084	GENERIC_ INFOFRAME_ PAYLOAD_ BYTES_20_ AND_21_REG	GENERIC_ INFOFRAME_PB21	15:8	RW	0	Generic InfoFrame Data Byte 21.
		GENERIC_ INFOFRAME_PB20	7:0	RW	0	Generic InfoFrame Data Byte 20.

Semtech Confidential Information
Kent Lin
DIVA Laboratories Ltd.
09/03/2026

7085	GENERIC_ INFOFRAME_ PAYLOAD_ BYTES_22_ AND_23_REG	GENERIC_ INFOFRAME_PB23	15:8	RW	0	Generic InfoFrame Data Byte 23.
		GENERIC_ INFOFRAME_PB22	7:0	RW	0	Generic InfoFrame Data Byte 22.
7086	GENERIC_ INFOFRAME_ PAYLOAD_ BYTES_24_ AND_25_REG	GENERIC_ INFOFRAME_PB25	15:8	RW	0	Generic InfoFrame Data Byte 25.
		GENERIC_ INFOFRAME_PB24	7:0	RW	0	Generic InfoFrame Data Byte 24.
7087	GENERIC_ INFOFRAME_ PAYLOAD_ BYTES_26_ AND_27_REG	GENERIC_ INFOFRAME_PB27	15:8	RW	0	Generic InfoFrame Data Byte 27.
		GENERIC_ INFOFRAME_PB26	7:0	RW	0	Generic InfoFrame Data Byte 26.
7088	HDMI_TX_ MAPPING_ SETTINGS	RSVD	15:2	RO	0	Reserved.
		M_VALUE_OVR	14:14	RW	0	Enables HDMI_TX_SMPTE_DATA_RATE overwrite.
		M_VALUE	13:13	RW	0	Overrides detected M_VALUE when M_VALUE_OVR is set HIGH.
		M_VALUE_FROM_ FLYWHEEL	12:12	RW	0	HIGH selects the M_VALUE detected by the internal flywheel to be used instead of the one detected from PIDs.
		HDMI_TX_SMPTE_ DATA_RATE_OVR	11:11	RW	0	Enables detected HDMI_TX_SMPTE_DATA_RATE overwrite.
		HDMI_TX_SMPTE_ DATA_RATE	10:8	RW	0	Overwrites HDMI_TX_SMPTE_DATA_RATE when HDMI_TX_SMPTE_DATA_RATE_OVR is set to 1. 000 = HD 001 = 3G 010 = 6G Mode3 011 = 6G Mode 2 100 = 6G Mode 1 101 = 12G Mode2 110 = 12G Mode1
		RSVD	7:0	RW	0	Reserved. Do not change.

Semtech Confidential Information
Kent Lin
DVA Laboratories Ltd.
09/08/2026

7089	PID_DET_REG_1	PID_DET_WD2_REG	15:8	RW	0	Overwrites detected PID byte2 when DETECTED_PID_OVR (reg. 708B) is set to 1.
		PID_DET_WD1_REG	7:0	RW	0	Overwrites detected PID byte1 when DETECTED_PID_OVR is set to 1.
708A	PID_DET_REG_2	PID_DET_WD4_REG	15:8	RW	0	Overwrites detected PID byte4 when DETECTED_PID_OVR is set to 1.
		PID_DET_WD3_REG	7:0	RW	0	Overwrites detected PID byte3 when DETECTED_PID_OVR is set to 1.
708B	HDMI_TX_DIV_ SETTINGS	HDMI_TX_ CLK_DIV_OVR	15:15	RW	0	Enables overwrite of detected clock ratio dividers, MAPP_CLK_SEL and CLK_2PPC_SEL.
		CLK_2PPC_SEL	14:13	RW	0	Overwrites detected CLK_2PPC_SEL when HDMI_TX_CLK_DIV_OVR is set to 1.
		MAPP_CLK_SEL	12:12	RW	0	Overwrites detected MAPP_CLK_SEL when HDMI_TX_CLK_DIV_OVR is set to 1.
		RSVD	11:9	RO	0	Reserved.
		HDMI_TX_ DATA_RATE_OVR	8:8	RW	0	Enables overwrite of detected HDMI_TX data rate.
		HDMI_TX_ DATA_RATE	7:4	RW	0	Overwrites internal HDMI_TX_DATA_RATE signal when HDMI_TX_DATA_RATE_OVR is set to 1: 0000 = 0.7425Gb/s 0001 = 0.7425Gb/s 0010 = 0.9281Gb/s 0011 = 1.1138Gb/s 0100 = 1.485Gb/s 0101 = 1. 8563Gb/s 0110 = 2.2275Gb/s 0111 = 2.97Gb/s 1000 = 2.97Gb/s 1001 = 3.715Gb/s 1010 = 3.715Gb/s 1011 = 4.455Gb/s 1100 = 4.455Gb/s 1101 = 5.94Gb/s 1110 = 5.94Gb/s
		RSVD	3:2	RO	0	Reserved.
		DETECTED_PID_OVR	1:1	RW	0	Enables overwrite of detected PID bytes.

Semtech Confidential Information
Kent Lin
DIVA Laboratories Ltd.
09/08/2026

		PID_DETECTED	0:0	RW	0	Overwrites PID_DETECTED signal when DETECTED_PID_OVR is set to 1.
708C	HDMI_TX_ COLOR_ SETTINGS	RSVD	15:9	RO	0	Reserved.
		COLOR_SMPL_ DEPTH_OVR	8:8	RW	0	Enables overwrite of COLOR_SUBSAMPL and COLOR_DEPTH.
		COLOR_DEPTH	7:4	RW	0	Overwrites detected COLOR_DEPTH when COLOR_SMPL_DEPTH_OVR is set to 1. 0000 = N/A 0100 = 24 0101 = 30 0110 = 36 0111 = 48 (not supported)
		COLOR_SUBSAMPL	3:0	RW	0	Overwrites detected COLOR_SUBSAMPL when COLOR_SMPL_DEPTH_OVR is set to 1. 0000 = RGB 0001 = YCbCr 4:2:2 0010 = YCbCr 4:4:4 0011 = YCbCr 4:2:0
708D	VID_STD_ SETTINGS	RSVD	15:9	RO	0	Reserved.
		VID_STD_FROM_PID	8:8	RW	1	Selects which video standard number is used for 861 timing converter. When 0, VID_STD# calculated by the FRONT_END block is used. When 1, VID_STD# based on PID info is used.
		RSVD	7:7	RO	0	Reserved.
		VD_STD_OVR	6:6	RW	0	Enables overwrite of detected VD_STD.
		VD_STD	5:0	RW	2B	Overwrites detected VD_STD when VD_STD_OVR is set to 1. Debug, do not use.
708E	VD_STD_ DETECTED_FE	RSVD	15:6	RO	0	Reserved.
		VD_STD_FE_DET	5:0	RO	0	VID_STD# detected by FE.
708F	VD_STD_ DETECTED_PID	RSVD	15:6	RO	0	Reserved.
		VD_STD_PID_DET	5:0	RO	0	VID_STD# detected from PIDs.

Semtech Confidential Information
Kent Lin
DIVA Laboratories. Ltd.
09/08/2026

7090	VIC_NUM_SELECTED	RSVD	15:8	RO	0	Reserved.
		VIC_NUM_DET	7:0	RO	0	Reports internally detected/selected VIC_NUM_DET.
7091	VIC_NUM_SETTING	RSVD	15:9	RO	0	Reserved.
		VIC_NUM_OVR	8:8	RW	0	Enables overwrite of VIC_NUM.
		VIC_NUM_REG	7:0	RW	0	VIC number to insert in info frame if VIC_NUM_OVR is set to 1.
7092	HDMI_TX_MAPP_DETECTED	SMPTE_DATA_RATE_DET	15:13	RO	0	Reports detected/selected SMPTE_DATA_RATE_DET by control logic.
		MAPP_CLK_SEL_DET	12:12	RO	0	Reports detected/selected MAPP_CLK_SEL_DET by control logic.
		RSVD	11:11	RO	0	Reserved.
		SDI_MAPP_SEL_DET	10:8	RO	0	Reports detected/selected SDI_MAPP_SEL_DET by control logic.
		RSVD	7:7	RO	0	Reserved.
		M0_CLK_SELL_DET	6:6	RO	0	Reports detected/selected M0_CLK_SEL_DET by control logic.
		CLK_2PPC_SEL_DET	5:4	RO	0	Reports detected/selected CLK_2PPC_SEL_DET by control logic.
		RSVD	3:2	RO	0	Reserved.
		CONV_2SI_DET	1:0	RO	0	Reports detected/selected CONV_2SI_DET by control logic.
7093	HDMI_TX_COLOR_SETT_RAST_DETECTED	RSVD	15:14	RO	0	Reserved.
		RASTGEN_MODE_DET	13:13	RO	0	Reports detected/selected RASTGEN_MODE_DET by control logic.
		RASTGEN_EN_DET	12:12	RO	0	Reports detected/selected RASTGEN_EN_DET by control logic.

Semtech Confidential Information
Kent Lin
DIVA Laboratories Ltd.
09/08/2026

		COLOR_ SUBSAMPL_DET	11:8	RO	0	Reports detected/selected COLOR_SUBSAMPL_DET by control logic.
		COLOR_DEPTH_DET	7:4	RO	0	Reports detected/selected COLOR_DEPTH_DET by control logic.
		HDMI_TX_ DATA_RATE_DET	3:0	RO	0	Reports detected/selected HDMI_TX_DATA_RATE_DET by control logic.
7094	HDMI_TX_ RAST_GEN_ DETECTED	RSVD	15:13	RO	0	Reserved.
		RASTGEN_ VACTIVE_DET	12:0	RO	0	Reports detected/selected RASTGEN_VACTIVE_DET by control logic.
7095 to 7096	RSVD_REG	RSVD	15:0	RW	N/A	Reserved. Do not change.
7097	GPIO_HVF_ OUT_SEL	RSVD	15:4	RW	TBA	Reserved. Do not change.
		HVF_SEL	3:0	RW	0	Selects HVF from HDMI_TX for GPIO HVF_OUT[0].
7098	AVI_IF_ACTIVE_ FORMAT_ AND_BAR	RSVD	15:6	RO	0	Reserved.
		ACTIVE_FORMAT_ OVR	5:5	RW	0	Enables override of active format info, A0, in AVI InfoFrame. **Note:** This enables overwrite of active format only when no AVI InfoFrame replacement is selected, AVI_INFOFRAME_DATA_OVR = 0. If AVI_INFOFRAME_DATA_OVR is set to 1, AVI InfoFrame PB1-PB13 from registers 700E-7014 are used to override all data.
		ACTIVE_FORMAT_ INF_PRESENT	4:4	RW	0	Active info format present, A0. Overrides internal data when ACTIVE_FORMAT_OVR = 1: 1 = Present 0 = No active format information
		ACTIVE_ASPECT_ RATIO	3:0	RW	8	Active Format Aspect Ratio, R3-R0, lock data from register. Overrides internal data when ACTIVE_FORMAT_OVR = 1: 1000 = Same as a picture rate 1001 = 4:3 (centre) 1010 = 16:9 (centre) 1011 = 14:9 (centre) Other values = See CTA-861-G Annex H

Semtech Confidential Information
Kent Lin
DIVA Laboratories, Ltd.
09/08/2026

7099	FLY_WHEEL	RSVD	15:5	RO	0	Reserved.
		FLYWHEEL_DISABLE	4:4	RW	0	Disables flywheel in the HDMI Tx path.
		RSVD	3:1	RO	0	Reserved.
		USE_FLYWHEEL	0:0	RW	0	Enables use of flywheel in the HDMI Tx path.
709A	FLY_WHEEL_ LOCKED	RSVD	15:2	RO	0	Reserved.
		FLYWHEEL_LOCK	1:0	RO	0	Indicates flywheel lock: bit 0 = H lock bit 1 = V lock
709B	FIFO_297_ TMDS_ DISTURB_ RST_EN	RSVD	15:1	RO	0	Reserved.
		FIFO_297_TMDS_ DISTURB_RST_DIS	0:0	RW	0	Disables reset of logic on TMDS clock based on the FIFO overflow.
709C	HDMI_AUDIO	RSVD	15:8	RO	0	Reserved.
		HDMI_AUDIO_ CHANNEL_ COUNT_OVR	7:7	RW	0	Enables override of HDMI audio channel count.
		HDMI_AUDIO_ CHANNEL_COUNT	6:4	RW	0	HDMI audio channel count.
		RSVD	5:2	RO	0	Reserved.
		HDMI_AUDIO_ EN_OVR	1:1	RW	0	Enables override of HDMI audio enable.
		HDMI_AUDIO_EN	0:0	RW	0	Overrides internal enable value when HDMI_AUDIO_EN_OVR is set to 1.
709D	INFR_AUDIO_ SMPL_SIZE_ FREQ	HDMI_AUDIO_LVL_ SHIFT_VAL	15:12	RW	0	Default value for LSV3-LSV0 Level Shift Value (Audio InfoFrame): 0000 = 0dB ... 1111 = 15dB
		RSVD	11:10	RO	0	Reserved.

Semtech Confidential Information
Kent Lin
DIVA Laboratories. Ltd.
09/08/2026

		HDMI_AUDIO_ LFE_PLBK_LVL	9:8	RW	0	Default value for LFE Playback level information, LFEPBL1 and LFEPBL0 in Audio InfoFrame, see CTA-861-G section 6.6 for more information. 00 = No info 01 = 0dB 10 = +10dB 11 = Reserved
		RSVD	7:7	RO	0	Reserved.
		HDMI_AUDIO_ SMPL_FREQ	6:4	RW	0	Sample frequency. For L-PCM and IEC61937 compressed audio streams, the SF will always be set to 0. For One Bit Audio and DST streams, the value indicated by the SF will equal the ACR FS value. For Super Audio CD, the SF bit are set to 010 to indicate 2.8224M samples/s (64*44.1kHz).
		RSVD	3:2	RO	0	Reserved.
		HDMI_AUDIO_ SMPL_SIZE	1:0	RW	0	HDMI 1.4 Sample size. The SS bits will always be set to a value of 0 (refer to Stream header). **Note:** Values in registers 709D-709F will be embedded when audio InfoFrame is not selected for replacement, AUDIO_INFOFRAME_DATA_OVR = 0. If AUDIO_INFOFRAME_DATA_OVR is set to 1, the PB1-PB5 values from registers 7016-7019 are used to insert Audio InfoFrame.
709E	INFR_AUDIO_ FORMAT	RSVD	15:8	RO	0	Reserved.
		HDMI_AUDIO_ FORMAT	7:0	RW	0	Refer to Audio Coding Type (CT) field in Packet Byte 1.
709F	INFR_AUDIO_ CHSP_ALLOC	RSVD	15:8	RO	0	Reserved.
		HDMI_AUDIO_ CHSP_ALLOC	7:0	RW	13	Refer to CTA-861-G pg 84, Table 35.
7100 to 7EFF	RSVD_REG	RSVD	15:0	RW	N/A	Reserved. Do not change.
7F00 to 7F3F	EDID_BASE_ BLOCK	EDID_BB_ BYTE_N+1	15:8	RW	TBA.	EDID base block read from a sink and stored in memory. Byte n is Byte 0 for address 7F00 and 124 (FE) for address 7F3F.

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09/08/2026

		EDID_BB_ BYTE_N	7:0	RW	TBA.	EDID base block read from a sink and stored in memory. Byte n is Byte 0 for address 7F00 and 124 (FE) for address 7F3F.
7F40 to 7F7F	EDID_CTA_ BLOCK	EDID_CTA_ BYTE_N+1	15:8	RW	TBA.	EDID CTA block read from a sink and stored in memory. Byte n is Byte 0 for address 7F40 and 124 (FE) for address 7F7F.
		EDID_CTA_ BYTE_N	7:0	RW	TBA.	EDID CTA block read from a sink and stored in memory. Byte n is Byte 0 for address 7F40 and 124 (FE) for address 7F7F.
7F80 to 7FBF	EDID_BASE_ BLOCK2	EDID_B2_ BYTE_N+1	15:8	RW	TBA.	EDID block 2 (Segment pointer = 1) read from a sink and stored in memory. Byte n is Byte 0 for address 7F80 and 124 (FE) for address 7FBF.
		EDID_B2_ BYTE_N	7:0	RW	TBA.	EDID block 2 (Segment pointer = 1) read from a sink and stored in memory. Byte n is Byte 0 for address 7F80 and 124 (FE) for address 7FBF.
7FC0 to 7FFF	EDID_BASE_ BLOCK3	EDID_B3_ BYTE_N+1	15:8	RW	TBA.	EDID block 3 (Segment pointer = 1) read from a sink and stored in memory. Byte n is Byte 0 for address 7FC0 and 124 (FE) for address 7FFF.
		EDID_B3_ BYTE_N	7:0	RW	TBA.	EDID block 3 (Segment pointer = 1) read from a sink and stored in memory. Byte n is Byte 0 for address 7FC0 and 124 (FE) for address 7FFF.

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09/03/2026

4.2.9. ANC Insertion Control Registers

Table 4-14 ANC Insertion Control and Status Register

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
8000	ANC_INS_ EN_REG	RSVD	15:1	RO	0	Reserved.
		ANC_INS_EN	0:0	RW	1	When asserted (HIGH) ancillary data insertion is enabled. When de-asserted no data is inserted.

8001	ANC_INS_ CFG_REG	RSVD	15:5	RO	0	Reserved.
		FVH_SEL	4:3	RW	0	F, V, H selection. The block will then use the selected set of F, V and H to figure out HANC and VANC regions of the video signal: 00 = F1_I, V1_I, H1_I will be selected 00 = F3_I, V3_I, H3_I will be selected 00 = F5_I, V5_I, H5_I will be selected 00 = F7_I, V7_I, H7_I will be selected
		DS_LINE_ NUMBER_ EXTRACTION_ SEL	2:1	RW	0	Data stream selection. The block will then use the selected data stream to extract the line numbers from: 00 = DS1_I will be selected 01 = DS3_I will be selected 10 = DS5_I will be selected 11 = DS7_I will be selected
		ANC_INS_MODE	0:0	RW	0	Selects the ANC data insertion operating mode: 0 = Separate line mode 1 = Concatenated mode
8002	START_SINGLE_ INS_REG	RSVD	15:1	RO	0	Reserved.
		START_SINGLE_ INS_TOG	0:0	RW	0	A level change (toggle) on this value initiates the single frame/field ANC insertion for all lines which are set to single frame insertion mode. This applies to all lines in separate line mode or the single line in concatenated mode.
8003	FIRST_LINE_ NUMBER_REG	RSVD	15:11	RO	0	Reserved.
		FIRST_LINE_ NUMBER	10:0	RW	0	Defines the line number for ANC data insertion for the first line in separate line mode or the single line for concatenated mode. Must be different than other *LINE_NUMBER[10:0] settings.
8004		RSVD	15:6	RO	0	Reserved.

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	FIRST_LINE_CFG_REG	CONT_SING_EN_1	5:4	RW	0	Selects whether ANC data insertion happens for a single frame/field or on every frame/field 0 = Insert ANC on one frame/field (single frame insertion mode) 1 = Insert ANC on every frame/field (continuous insertion mode) 2, 3 = ANC insertion disabled This applies to the first line in separate line mode or the single line for concatenated mode.
		DATA_STREAM_INS_SEL_LINE_1	3:1	RW	0	Data stream selection for the first line insertion: 000 = DS1_I will be selected for ANC data insertion 001 = DS2_I will be selected for ANC data insertion 010 = DS3_I will be selected for ANC data insertion 011 = DS4_I will be selected for ANC data insertion 100 = DS5_I will be selected for ANC data insertion 101 = DS6_I will be selected for ANC data insertion 110 = DS7_I will be selected for ANC data insertion 111 = DS8_I will be selected for ANC data insertion
		ANC_TYPE_LINE_1	0:0	RW	0	Selects whether ancillary data for the first line in separate line mode or the single line for concatenated mode is inserted into the HANC region (0) or the VANC region (1).
8005	FIRST_LINE_NUMBER_WORDS_REG	RSVD	15:12	RO	0	Reserved.
		FIRST_LINE_NUMBER_OF_WORDS	11:0	RW	0	Defines the total number of 8-bit data words to insert on the first line in separate line mode or single line in concatenated mode.
8006		RSVD	15:11	RO	0	Reserved.

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	SECOND_LINE_NUMBER_REG	SECOND_LINE_NUMBER	10:0	RW	0	Defines the line number for ANC data insertion for the second line in separate line mode (not applicable in concatenated mode). Must be different than other *LINE_NUMBER[10:0] settings.
8007	SECOND_LINE_CFG_REG	RSVD	15:6	RO	0	Reserved.
		CONT_SING_EN_2	5:4	RW	0	Selects whether ANC data insertion happens for a single frame/field or on every frame/field. 0 = Insert ANC on one frame/field (single frame insertion mode) 1 = Insert ANC on every frame/field (continuous insertion mode) 2, 3 = ANC insertion disabled This applies to the second line in separate line mode (not applicable in concatenated mode).
		DATA_STREAM_INS_SEL_LINE_2	3:1	RW	0	Data stream selection for the second line insertion: 000 = DS1_I will be selected for ANC data insertion 001 = DS2_I will be selected for ANC data insertion 010 = DS3_I will be selected for ANC data insertion 011 = DS4_I will be selected for ANC data insertion 100 = DS5_I will be selected for ANC data insertion 101 = DS6_I will be selected for ANC data insertion 110 = DS7_I will be selected for ANC data insertion 111 = DS8_I will be selected for ANC data insertion
		ANC_TYPE_LINE_2	0:0	RW	0	Selects whether ancillary data for the second line in separate line mode is inserted into the HANC region (0) or the VANC region (1) (not applicable in concatenated mode).
8008		RSVD	15:11	RO	0	Reserved.

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	SECOND_LINE_ NUMBER_ WORDS_REG	SECOND_LINE_ NUMBER_OF_ WORDS	10:0	RW	0	Defines the total number of 8-bit data words to insert on the second line in separate line mode (not applicable in concatenated mode).
8009	THIRD_LINE_ NUMBER_REG	RSVD	15:11	RO	0	Reserved.
		THIRD_LINE_ NUMBER	10:0	RW	0	Defines the line number for ANC data insertion for the third line in separate line mode (not applicable in concatenated mode). Must be different than other *LINE_NUMBER[10:0] settings.
800A	THIRD_LINE_ CFG_REG	RSVD	15:6	RO	0	Reserved.
		CONT_SING_ EN_3	5:4	RW	0	Selects whether ANC data insertion happens for a single frame/field or on every frame/field: 0 = Insert ANC on one frame/field (single frame insertion mode) 1 = Insert ANC on every frame/field (continuous insertion mode) 2, 3 = ANC insertion disabled This applies to the third line in separate line mode (not applicable in concatenated mode).
		DATA_STREAM_ INS_SEL_LINE_3	3:1	RW	0	Data stream selection for the third line insertion: 000 = DS1_I will be selected for ANC data insertion 001 = DS2_I will be selected for ANC data insertion 010 = DS3_I will be selected for ANC data insertion 011 = DS4_I will be selected for ANC data insertion 100 = DS5_I will be selected for ANC data insertion 101 = DS6_I will be selected for ANC data insertion 110 = DS7_I will be selected for ANC data insertion 111 = DS8_I will be selected for ANC data insertion
		ANC_TYPE_ LINE_3	0:0	RW	0	Selects whether ancillary data for the third line in separate line mode is inserted into the HANC region (0) or the VANC region (1). (Not applicable in concatenated mode).

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800B	THIRD_LINE_NUMBER_WORDS_REG	RSVD	15:9	RO	0	Reserved.
		THIRD_LINE_NUMBER_OF_WORDS	8:0	RW	0	Defines the total number of 8-bit data words to insert on the third line in separate line mode (not applicable in concatenated mode).
800C	FOURTH_LINE_NUMBER_REG	RSVD	15:11	RO	0	Reserved.
		FOURTH_LINE_NUMBER	10:0	RW	0	Defines the line number for ANC data insertion for the fourth line in separate line mode (not applicable in concatenated mode). Must be different than other *LINE_NUMBER[10:0] settings.
800D	FOURTH_LINE_CFG_REG	RSVD	15:6	RO	0	Reserved.
		CONT_SING_EN_4	5:4	RW	0	Selects whether ANC data insertion happens for a single frame/field or on every frame/field: 0 = Insert ANC on one frame/field (single frame insertion mode) 1 = Insert ANC on every frame/field (continuous insertion mode) 2, 3 = ANC insertion disabled This applies to the fourth line in separate line mode (not applicable in concatenated mode).
		DATA_STREAM_INS_SEL_LINE_4	3:1	RW	0	Data stream selection for the fourth line insertion: 000 = DS1_I will be selected for ANC data insertion 001 = DS2_I will be selected for ANC data insertion 010 = DS3_I will be selected for ANC data insertion 011 = DS4_I will be selected for ANC data insertion 100 = DS5_I will be selected for ANC data insertion 101 = DS6_I will be selected for ANC data insertion 110 = DS7_I will be selected for ANC data insertion 111 = DS8_I will be selected for ANC data insertion

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		ANC_TYPE_LINE_4	0:0	RW	0	Selects whether ancillary data for the fourth line in separate line mode is inserted into the HANC region (0) or the VANC region (1). (Not applicable in concatenated mode).
800E	FOURTH_LINE_NUMBER_WORDS_REG	RSVD	15:9	RO	0	Reserved.
		FOURTH_LINE_NUMBER_OF_WORDS	8:0	RW	0	Defines the total number of 8-bit data words to insert on the fourth line in separate line mode (not applicable in concatenated mode).
800F	PACKET_MISSED_REG	RSVD	15:1	RO	0	Reserved.
		PACKET_MISSED	0:0	ROCW	0	Signal that shall be asserted HIGH when the insertion block runs out of ancillary data space and can't complete insertion of user data.
8010	INSERTION_COMPLETE_REG	RSVD	15:1	RO	0	Reserved.
		INS_COMPLETE	0:0	RO	0	Set to '1' to indicate that single frame/field ANC insertion has completed.
8011	ANC_INS_CRC_INS_ENABLE_REG	RSVD	15:1	RO	0	Reserved.
		ANC_INS_CRC_INS_ENABLE	0:0	RW	1	When HIGH, the CRCs embedded in the video (at EAV) will be computed for the data stream selected for ANC insertion. When LOW, the CRCs will not be computed and inserted.

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4.2.10. ANC Insertion Memory Control and Status Registers

Table 4-15 ANC Insertion Memory Control and Status Register

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
9000	ANC_INS_RAM_REG	ANS_INS_RAM	15:0	RW	0	TBD.

4.2.11. ANC Extraction Control and Status Registers

Table 4-16 ANC Extraction Control and Status Register

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
A000	ANC_DD_ANC_ TYPE1_DS_ 1_2_REG	ANC_DD_ANC_ TYPE1_DS_ 1_AND_2	15:0	RW	0	Programmable ancillary data detection type for video data streams 1 and 2. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A001	ANC_DD_ANC_ TYPE2_DS_ 1_2_REG	ANC_DD_ANC_ TYPE2_DS_ 1_AND_2	15:0	RW	0	Programmable ancillary data detection type for video data streams 1 and 2. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A002	ANC_DD_ANC_ TYPE3_DS_ 1_2_REG	ANC_DD_ANC_ TYPE3_DS_ 1_AND_2	15:0	RW	0	Programmable ancillary data detection type for video data streams 1 and 2. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A003	ANC_DD_ANC_ TYPE4_DS_ 1_2_REG	ANC_DD_ANC_ TYPE4_DS_ 1_AND_2	15:0	RW	0	Programmable ancillary data detection type for video data streams 1 and 2. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A004	ANC_DD_ANC_ TYPE5_DS_ 1_2_REG	ANC_DD_ANC_ TYPE5_DS_ 1_AND_2	15:0	RW	0	Programmable ancillary data detection type for video data streams 1 and 2. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A005	ANC_DD_ANC_ TYPE6_DS_ 1_2_REG	ANC_DD_ANC_ TYPE6_DS_ 1_AND_2	15:0	RW	0	Programmable ancillary data detection type for video data streams 1 and 2. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A006	ANC_DD_ANC_ TYPE7_DS_ 1_2_REG	ANC_DD_ANC_ TYPE7_DS_ 1_AND_2	15:0	RW	0	Programmable ancillary data detection type for video data streams 1 and 2. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A007	ANC_DD_ANC_ TYPE8_DS_ 1_2_REG	ANC_DD_ANC_ TYPE8_DS_ 1_AND_2	15:0	RW	0	Programmable ancillary data detection type for video data streams 1 and 2. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.

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09/08/2026

A008	ANC_DD_ANC_TYPE9_DS_1_2_REG	ANC_DD_ANC_TYPE9_DS_1_AND_2	15:0	RW	0	Programmable ancillary data detection type for video data streams 1 and 2. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A009	ANC_DD_ANC_TYPE10_DS_1_2_REG	ANC_DD_ANC_TYPE10_DS_1_AND_2	15:0	RW	0	Programmable ancillary data detection type for video data streams 1 and 2. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A00A	ANC_DD_CTRL_DS_1_2_REG	RSVD	15:2	RO	0	Reserved.
		ANC_DD_EXCLUDE_V_FROM_VANC_DS_1_AND_2	1:1	RW	0	When HIGH, indicates that the VANC indicators will be computed when the H signal is LOW only. When LOW, indicates that the VANC indicators will be computed when H signal is LOW and the V signal is HIGH.
		ANC_DD_ANC_CSUM_INS_DS_1_AND_2	0:0	RW	0	When HIGH, enables checksum error correction on packets present on data streams 1 and 2.
A00B	ANC_DD_STATS_0_DS_1_2_REG	RSVD	15:2	RO	0	Reserved.
		ANC_DD_DS2_FRAME_ANC	1:1	RO	0	When HIGH, indicates that ancillary data packet(s) selected for detection has/have been detected on DS2_I in the HANC or the VANC part of the video signal. This signal is set at the beginning of every video frame, but is based on the detection of the previous frame.
		ANC_DD_DS1_FRAME_ANC	0:0	RO	0	When HIGH, indicates that ancillary data packet(s) selected for detection has/have been detected on DS1_I in the HANC or the VANC part of the video signal. This signal is set at the beginning of every video frame, but is based on the detection of the previous frame.
A00C	ANC_DD_STATS_1_DS_1_2_REG	RSVD	15:6	RO	0	Reserved.
		ANC_DD_DS2_CS_ERR	5:5	ROCW	0	When HIGH, indicates that the calculated checksum for ANC data packet selected for detection on DS2_I channel does not match the incoming packet checksum value.

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09/08/2026

		ANC_DD_DS1_CS_ERR	4:4	ROCW	0	When HIGH, indicates that the calculated checksum for ANC data packet selected for detection on DS1_I channel does not match the incoming packet checksum value.
		ANC_DD_DS2_LIVE_VANC_ANC	3:3	ROCW	0	Signal that will be set HIGH when an ancillary data packet selected for detection is present during the VANC of the DS2_O output video signal.
		ANC_DD_DS2_LIVE_HANC_ANC	2:2	ROCW	0	Signal that will be set HIGH when an ancillary data packet selected for detection is present during the HANC of the DS2_O output video signal.
		ANC_DD_DS1_LIVE_VANC_ANC	1:1	ROCW	0	Signal that will be set HIGH when an ancillary data packet selected for detection is present during the VANC of the DS1_O output video signal.
		ANC_DD_DS1_LIVE_HANC_ANC	0:0	ROCW	0	Signal that will be set HIGH when an ancillary data packet selected for detection is present during the HANC of the DS1_O output video signal.
A00D	ANC_DD_HANC_ANC_CNT_DS_1_REG	ANC_DD_DS1_HANC_ANC_COUNT	15:0	RO	0	DS1 ancillary data packet word count. This signal gets updated at the beginning of every video frame (but is based on the detection of the previous frame) and represent the number of ancillary data words that were part of ancillary data packet(s) selected for detection and that were found in the HANC part of DS1_I.
A00E	ANC_DD_VANC_ANC_CNT_DS_1_REG	ANC_DD_DS1_VANC_ANC_COUNT	15:0	RO	0	DS1 ancillary data packet word count. This signal gets updated at the beginning of every video frame (but is based on the detection of the previous frame) and represent the number of ancillary data words that were part of ancillary data packet(s) selected for detection and that were found in the VANC part of DS1_I.
A00F	ANC_DD_HANC_ANC_PKT_CNT_DS_1_REG	ANC_DD_DS1_HANC_ANC_PKT_COUNT	15:0	RO	0	DS1 ancillary data packet count. This signal gets updated at the beginning of every video frame (but is based on the detection of the previous frame) and represent the number of ancillary data packets selected for detection and that were found in the HANC part of DS1_I.

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09/08/2026

A010	ANC_DD_VANC_ ANC_PKT_CNT_ DS_1_REG	ANC_DD_DS1_ VANC_ANC_ PKT_COUNT	15:0	RO	0	DS1 ancillary data packet count. This signal gets updated at the beginning of every video frame (but is based on the detection of the previous frame) and represent the number of ancillary data packets selected for detection and that were found in the VANC part of DS1_I.
A011	ANC_DD_HANC_A NC_CNT_ DS_2_REG	ANC_DD_DS2_ HANC_ANC_COUNT	15:0	RO	0	DS2 ancillary data packet word count. This signal gets updated at the beginning of every video frame (but is based on the detection of the previous frame) and represent the number of ancillary data words that were part of ancillary data packet(s) selected for detection and that were found in the HANC part of DS2_I.
A012	ANC_DD_VANC_ ANC_CNT_ DS_2_REG	ANC_DD_DS2_ VANC_ANC_COUNT	15:0	RO	0	DS2 ancillary data packet word count. This signal gets updated at the beginning of every video frame (but is based on the detection of the previous frame) and represent the number of ancillary data words that were part of ancillary data packet(s) selected for detection and that were found in the VANC part of DS2_I.
A013	ANC_DD_HANC_A NC_PKT_CNT_ DS_2_REG	ANC_DD_DS2_ HANC_ANC_ PKT_COUNT	15:0	RO	0	DS2 ancillary data packet count. This signal gets updated at the beginning of every video frame (but is based on the detection of the previous frame) and represent the number of ancillary data packets selected for detection and that were found in the HANC part of DS2_I.
A014	ANC_DD_VANC_ ANC_PKT_CNT_ DS_2_REG	ANC_DD_DS2_ VANC_ANC_ PKT_COUNT	15:0	RO	0	DS2 ancillary data packet count. This signal gets updated at the beginning of every video frame (but is based on the detection of the previous frame) and represent the number of ancillary data packets selected for detection and that were found in the VANC part of DS2_I.
A015	ANC_DD_ANC_ TYPE1_DS_ 3_4_REG	ANC_DD_ANC_ TYPE1_DS_3_AND_4	15:0	RW	0	Programmable ancillary data detection type for video data streams 3 and 4. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A016	ANC_DD_ANC_ TYPE2_DS_ 3_4_REG	ANC_DD_ANC_ TYPE2_DS_3_AND_4	15:0	RW	0	Programmable ancillary data detection type for video data streams 3 and 4. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.

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A017	ANC_DD_ANC_TYPE3_DS_3_4_REG	ANC_DD_ANC_TYPE3_DS_3_AND_4	15:0	RW	0	Programmable ancillary data detection type for video data streams 3 and 4. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A018	ANC_DD_ANC_TYPE4_DS_3_4_REG	ANC_DD_ANC_TYPE4_DS_3_AND_4	15:0	RW	0	Programmable ancillary data detection type for video data streams 3 and 4. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A019	ANC_DD_ANC_TYPE5_DS_3_4_REG	ANC_DD_ANC_TYPE5_DS_3_AND_4	15:0	RW	0	Programmable ancillary data detection type for video data streams 3 and 4. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A01A	ANC_DD_ANC_TYPE6_DS_3_4_REG	ANC_DD_ANC_TYPE6_DS_3_AND_4	15:0	RW	0	Programmable ancillary data detection type for video data streams 3 and 4. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A01B	ANC_DD_ANC_TYPE7_DS_3_4_REG	ANC_DD_ANC_TYPE7_DS_3_AND_4	15:0	RW	0	Programmable ancillary data detection type for video data streams 3 and 4. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A01C	ANC_DD_ANC_TYPE8_DS_3_4_REG	ANC_DD_ANC_TYPE8_DS_3_AND_4	15:0	RW	0	Programmable ancillary data detection type for video data streams 3 and 4. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A01D	ANC_DD_ANC_TYPE9_DS_3_4_REG	ANC_DD_ANC_TYPE9_DS_3_AND_4	15:0	RW	0	Programmable ancillary data detection type for video data streams 3 and 4. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A01E	ANC_DD_ANC_TYPE10_DS_3_4_REG	ANC_DD_ANC_TYPE10_DS_3_AND_4	15:0	RW	0	Programmable ancillary data detection type for video data streams 3 and 4. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A01F	ANC_DD_CTRL_DS_3_4_REG	RSVD	15:2	RO	0	Reserved.
		ANC_DD_EXCLUDE_V_FROM_VANC_DS_3_AND_4	1:1	RW	0	When HIGH, indicates that the VANC indicators will be computed when the H signal is LOW only. When LOW, indicates that the VANC indicators will be computed when H signal is LOW and the V signal is HIGH.

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		ANC_DD_ANC_CSUM_INS_DS_3_AND_4	0:0	RW	0	When HIGH, enables checksum error correction on packets present on data streams 3 and 4.
A020	ANC_DD_STATS_0_DS_3_4_REG	RSVD	15:2	RO	0	Reserved.
		ANC_DD_DS4_FRAME_ANC	1:1	RW	0	When HIGH, indicates that ancillary data packet(s) selected for detection has/have been detected on DS4_I in the HANC or the VANC part of the video signal. This signal is set at the beginning of every video frame, but is based on the detection of the previous frame.
		ANC_DD_DS3_FRAME_ANC	0:0	RW	0	When HIGH, indicates that ancillary data packet(s) selected for detection has/have been detected on DS3_I in the HANC or the VANC part of the video signal. This signal is set at the beginning of every video frame, but is based on the detection of the previous frame.
A021	ANC_DD_STATS_1_DS_3_4_REG	RSVD	15:6	RO	0	Reserved.
		ANC_DD_DS4_CS_ERR	5:5	ROCW	0	When HIGH, indicates that the calculated checksum for ANC data packet selected for detection on DS4_I channel does not match the incoming packet checksum value.
		ANC_DD_DS3_CS_ERR	4:4	ROCW	0	When HIGH, indicates that the calculated checksum for ANC data packet selected for detection on DS3_I channel does not match the incoming packet checksum value.
		ANC_DD_DS4_LIVE_VANC_ANC	3:3	ROCW	0	Signal that will be set HIGH when an ancillary data packet selected for detection is present during the VANC of the DS4_O output video signal.
		ANC_DD_DS4_LIVE_HANC_ANC	2:2	ROCW	0	Signal that will be set HIGH when an ancillary data packet selected for detection is present during the HANC of the DS4_O output video signal.
		ANC_DD_DS3_LIVE_VANC_ANC	1:1	ROCW	0	Signal that will be set HIGH when an ancillary data packet selected for detection is present during the VANC of the DS3_O output video signal.

Semtech Confidential Information
Kent Lin
DIVA Laboratories, Ltd.
09/08/2026

		ANC_DD_DS3_LIVE_HANC_ANC	0:0	ROCW	0	Signal that will be set HIGH when an ancillary data packet selected for detection is present during the HANC of the DS3_O output video signal.
A022	ANC_DD_HANC_ANC_CNT_DS_3_REG	ANC_DD_DS3_HANC_ANC_COUNT	15:0	RO	0	DS3 ancillary data packet word count. This signal gets updated at the beginning of every video frame (but is based on the detection of the previous frame) and represent the number of ancillary data words that were part of ancillary data packet(s) selected for detection and that were found in the HANC part of DS3_I.
A023	ANC_DD_VANC_ANC_CNT_DS_3_REG	ANC_DD_DS3_VANC_ANC_COUNT	15:0	RO	0	DS3 ancillary data packet word count. This signal gets updated at the beginning of every video frame (but is based on the detection of the previous frame) and represent the number of ancillary data words that were part of ancillary data packet(s) selected for detection and that were found in the VANC part of DS3_I.
A024	ANC_DD_HANC_ANC_PKT_CNT_DS_3_REG	ANC_DD_DS3_HANC_ANC_PKT_COUNT	15:0	RO	0	DS3 ancillary data packet count. This signal gets updated at the beginning of every video frame (but is based on the detection of the previous frame) and represent the number of ancillary data packets selected for detection and that were found in the HANC part of DS3_I.
A025	ANC_DD_VANC_ANC_PKT_CNT_DS_3_REG	ANC_DD_DS3_VANC_ANC_PKT_COUNT	15:0	RO	0	DS3 ancillary data packet count. This signal gets updated at the beginning of every video frame (but is based on the detection of the previous frame) and represent the number of ancillary data packets selected for detection and that were found in the VANC part of DS3_I.
A026	ANC_DD_HANC_ANC_CNT_DS_4_REG	ANC_DD_DS4_HANC_ANC_COUNT	15:0	RO	0	DS4 ancillary data packet word count. This signal gets updated at the beginning of every video frame (but is based on the detection of the previous frame) and represent the number of ancillary data words that were part of ancillary data packet(s) selected for detection and that were found in the HANC part of DS4_I.

Semtech Confidential Information
Kent Lin
DIVA Laboratories, Ltd.
09/08/2026

A027	ANC_DD_VANC_ ANC_CNT_ DS_4_REG	ANC_DD_DS4_ VANC_ANC_COUNT	15:0	RO	0	DS4 ancillary data packet word count. This signal gets updated at the beginning of every video frame (but is based on the detection of the previous frame) and represent the number of ancillary data words that were part of ancillary data packet(s) selected for detection and that were found in the VANC part of DS4_I.
A028	ANC_DD_HANC_A NC_PKT_CNT_ DS_4_REG	ANC_DD_DS4_ HANC_ANC_ PKT_COUNT	15:0	RO	0	DS4 ancillary data packet count. This signal gets updated at the beginning of every video frame (but is based on the detection of the previous frame) and represent the number of ancillary data packets selected for detection and that were found in the HANC part of DS4_I.
A029	ANC_DD_VANC_ ANC_PKT_CNT_ DS_4_REG	ANC_DD_DS4_ VANC_ANC_ PKT_COUNT	15:0	RO	0	DS4 ancillary data packet count. This signal gets updated at the beginning of every video frame (but is based on the detection of the previous frame) and represent the number of ancillary data packets selected for detection and that were found in the VANC part of DS4_I.
A02A	ANC_DD_ANC_ TYPE1_DS_ 5_6_REG	ANC_DD_ANC_ TYPE1_DS_5_AND_6	15:0	RW	0	Programmable ancillary data detection type for video data streams 5 and 6. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A02B	ANC_DD_ANC_ TYPE2_DS_ 5_6_REG	ANC_DD_ANC_ TYPE2_DS_5_AND_6	15:0	RW	0	Programmable ancillary data detection type for video data streams 5 and 6. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A02C	ANC_DD_ANC_ TYPE3_DS_ 5_6_REG	ANC_DD_ANC_ TYPE3_DS_5_AND_6	15:0	RW	0	Programmable ancillary data detection type for video data streams 5 and 6. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A02D	ANC_DD_ANC_ TYPE4_DS_ 5_6_REG	ANC_DD_ANC_ TYPE4_DS_5_AND_6	15:0	RW	0	Programmable ancillary data detection type for video data streams 5 and 6. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A02E	ANC_DD_ANC_ TYPE5_DS_ 5_6_REG	ANC_DD_ANC_ TYPE5_DS_5_AND_6	15:0	RW	0	Programmable ancillary data detection type for video data streams 5 and 6. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.

Semtech Confidential Information
Kent Lin
DIVA Laboratories. Ltd.
09/08/2026

A02F	ANC_DD_ANC_TYPE6_DS_5_6_REG	ANC_DD_ANC_TYPE6_DS_5_AND_6	15:0	RW	0	Programmable ancillary data detection type for video data streams 5 and 6. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A030	ANC_DD_ANC_TYPE7_DS_5_6_REG	ANC_DD_ANC_TYPE7_DS_5_AND_6	15:0	RW	0	Programmable ancillary data detection type for video data streams 5 and 6. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A031	ANC_DD_ANC_TYPE8_DS_5_6_REG	ANC_DD_ANC_TYPE8_DS_5_AND_6	15:0	RW	0	Programmable ancillary data detection type for video data streams 5 and 6. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A032	ANC_DD_ANC_TYPE9_DS_5_6_REG	ANC_DD_ANC_TYPE9_DS_5_AND_6	15:0	RW	0	Programmable ancillary data detection type for video data streams 5 and 6. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A033	ANC_DD_ANC_TYPE10_DS_5_6_REG	ANC_DD_ANC_TYPE10_DS_5_AND_6	15:0	RW	0	Programmable ancillary data detection type for video data streams 5 and 6. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A034	ANC_DD_CTRL_DS_5_6_REG	RSVD	15:2	RO	0	Reserved.
		ANC_DD_EXCLUDE_V_FROM_VANC_DS_5_AND_6	1:1	RW	0	When HIGH, indicates that the VANC indicators will be computed when the H signal is LOW only. When LOW, indicates that the VANC indicators will be computed when H signal is LOW and the V signal is HIGH.
		ANC_DD_ANC_CSUM_INS_DS_5_AND_6	0:0	RW	0	When HIGH, enables checksum error correction on packets present on data streams 5 and 6.
A035	ANC_DD_STATS_0_DS_5_6_REG	RSVD	15:2	RO	0	Reserved.
		ANC_DD_DS6_FRAME_ANC	1:1	RO	0	When HIGH, indicates that ancillary data packet(s) selected for detection has/have been detected on DS6_I in the HANC or the VANC part of the video signal. This signal is set at the beginning of every video frame, but is based on the detection of the previous frame.

Semtech Confidential Information
Kent Lin
DIVA Laboratories, Ltd.
09/03/2026

		ANC_DD_DS5_FRAME_ANC	0:0	RO	0	When HIGH, indicates that ancillary data packet(s) selected for detection has/have been detected on DS5_I in the HANC or the VANC part of the video signal. This signal is set at the beginning of every video frame, but is based on the detection of the previous frame.
A036	ANC_DD_STATS_1_DS_5_6_REG	RSVD	15:6	RO	0	Reserved.
		ANC_DD_DS6_CS_ERR	5:5	ROCW	0	When HIGH, indicates that the calculated checksum for ANC data packet selected for detection on DS6_I channel does not match the incoming packet checksum value.
		ANC_DD_DS5_CS_ERR	4:4	ROCW	0	When HIGH, indicates that the calculated checksum for ANC data packet selected for detection on DS5_I channel does not match the incoming packet checksum value.
		ANC_DD_DS6_LIVE_VANC_ANC	3:3	ROCW	0	Signal that will be set HIGH when an ancillary data packet selected for detection is present during the VANC of the DS6_O output video signal.
		ANC_DD_DS6_LIVE_HANC_ANC	2:2	ROCW	0	Signal that will be set HIGH when an ancillary data packet selected for detection is present during the HANC of the DS6_O output video signal.
		ANC_DD_DS5_LIVE_VANC_ANC	1:1	ROCW	0	Signal that will be set HIGH when an ancillary data packet selected for detection is present during the VANC of the DS5_O output video signal.
		ANC_DD_DS5_LIVE_HANC_ANC	0:0	ROCW	0	Signal that will be set HIGH when an ancillary data packet selected for detection is present during the HANC of the DS5_O output video signal.
A037	ANC_DD_HANC_ANC_CNT_DS_5_REG	ANC_DD_DS5_HANC_ANC_COUNT	15:0	RO	0	DS5 ancillary data packet word count. This signal gets updated at the beginning of every video frame (but is based on the detection of the previous frame) and represent the number of ancillary data words that were part of ancillary data packet(s) selected for detection and that were found in the HANC part of DS5_I.

Semtech Confidential Information
Kent Lin
DIVA Laboratories Ltd.
09/08/2026

A038	ANC_DD_VANC_ANC_CNT_DS_5_REG	ANC_DD_DS5_VANC_ANC_COUNT	15:0	RO	0	DS5 ancillary data packet word count. This signal gets updated at the beginning of every video frame (but is based on the detection of the previous frame) and represent the number of ancillary data words that were part of ancillary data packet(s) selected for detection and that were found in the VANC part of DS5_I.
A039	ANC_DD_HANC_ANC_PKT_CNT_DS_5_REG	ANC_DD_DS5_HANC_ANC_PKT_COUNT	15:0	RO	0	DS5 ancillary data packet count. This signal gets updated at the beginning of every video frame (but is based on the detection of the previous frame) and represent the number of ancillary data packets selected for detection and that were found in the HANC part of DS5_I.
A03A	ANC_DD_VANC_ANC_PKT_CNT_DS_5_REG	ANC_DD_DS5_VANC_ANC_PKT_COUNT	15:0	RO	0	DS5 ancillary data packet count. This signal gets updated at the beginning of every video frame (but is based on the detection of the previous frame) and represent the number of ancillary data packets selected for detection and that were found in the VANC part of DS5_I.
A03B	ANC_DD_HANC_ANC_CNT_DS_6_REG	ANC_DD_DS6_HANC_ANC_COUNT	15:0	RO	0	DS6 ancillary data packet word count. This signal gets updated at the beginning of every video frame (but is based on the detection of the previous frame) and represent the number of ancillary data words that were part of ancillary data packet(s) selected for detection and that were found in the HANC part of DS6_I.
A03C	ANC_DD_VANC_ANC_CNT_DS_6_REG	ANC_DD_DS6_VANC_ANC_COUNT	15:0	RO	0	DS6 ancillary data packet word count. This signal gets updated at the beginning of every video frame (but is based on the detection of the previous frame) and represent the number of ancillary data words that were part of ancillary data packet(s) selected for detection and that were found in the VANC part of DS6_I.
A03D	ANC_DD_HANC_ANC_PKT_CNT_DS_6_REG	ANC_DD_DS6_HANC_ANC_PKT_COUNT	15:0	RO	0	DS6 ancillary data packet count. This signal gets updated at the beginning of every video frame (but is based on the detection of the previous frame) and represent the number of ancillary data packets selected for detection and that were found in the HANC part of DS6_I.

Semtech Confidential Information
Kent Lin
DIVA Laboratories. Ltd.
09/08/2026

A03E	ANC_DD_VANC_ANC_PKT_CNT_DS_6_REG	ANC_DD_DS6_VANC_ANC_PKT_COUNT	15:0	RO	0	DS6 ancillary data packet count. This signal gets updated at the beginning of every video frame (but is based on the detection of the previous frame) and represent the number of ancillary data packets selected for detection and that were found in the VANC part of DS6_I.
A03F	ANC_DD_ANC_TYPE1_DS_7_8_REG	ANC_DD_ANC_TYPE1_DS_7_AND_8	15:0	RW	0	Programmable ancillary data detection type for video data streams 7 and 8. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A040	ANC_DD_ANC_TYPE2_DS_7_8_REG	ANC_DD_ANC_TYPE2_DS_7_AND_8	15:0	RW	0	Programmable ancillary data detection type for video data streams 7 and 8. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A041	ANC_DD_ANC_TYPE3_DS_7_8_REG	ANC_DD_ANC_TYPE3_DS_7_AND_8	15:0	RW	0	Programmable ancillary data detection type for video data streams 7 and 8. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A042	ANC_DD_ANC_TYPE4_DS_7_8_REG	ANC_DD_ANC_TYPE4_DS_7_AND_8	15:0	RW	0	Programmable ancillary data detection type for video data streams 7 and 8. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A043	ANC_DD_ANC_TYPE5_DS_7_8_REG	ANC_DD_ANC_TYPE5_DS_7_AND_8	15:0	RW	0	Programmable ancillary data detection type for video data streams 7 and 8. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A044	ANC_DD_ANC_TYPE6_DS_7_8_REG	ANC_DD_ANC_TYPE6_DS_7_AND_8	15:0	RW	0	Programmable ancillary data detection type for video data streams 7 and 8. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A045	ANC_DD_ANC_TYPE7_DS_7_8_REG	ANC_DD_ANC_TYPE7_DS_7_AND_8	15:0	RW	0	Programmable ancillary data detection type for video data streams 7 and 8. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A046	ANC_DD_ANC_TYPE8_DS_7_8_REG	ANC_DD_ANC_TYPE8_DS_7_AND_8	15:0	RW	0	Programmable ancillary data detection type for video data streams 7 and 8. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.

Semtech Confidential Information
Kent Lin
DIVA Laboratories. Ltd.
09/03/2026

A047	ANC_DD_ANC_TYPE9_DS_7_8_REG	ANC_DD_ANC_TYPE9_DS_7_AND_8	15:0	RW	0	Programmable ancillary data detection type for video data streams 7 and 8. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A048	ANC_DD_ANC_TYPE10_DS_7_8_REG	ANC_DD_ANC_TYPE10_DS_7_AND_8	15:0	RW	0	Programmable ancillary data detection type for video data streams 7 and 8. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A049	ANC_DD_CTRL_DS_7_8_REG	RSVD	15:2	RO	0	Reserved.
		ANC_DD_EXCLUDE_V_FROM_VANC_DS_7_AND_8	1:1	RO	0	When HIGH, indicates that the VANC indicators will be computed when the H signal is LOW only. When LOW, indicates that the VANC indicators will be computed when H signal is LOW and the V signal is HIGH.
		ANC_DD_ANC_CSUM_INS_DS_7_AND_8	0:0	RO	0	When HIGH, enables checksum error correction on packets present on data streams 7 and 8.
A04A	ANC_DD_STATS_0_DS_7_8_REG	RSVD	15:2	RO	0	Reserved.
		ANC_DD_DS8_FRAME_ANC	1:1	RO	0	When HIGH, indicates that ancillary data packet(s) selected for detection has/have been detected on DS8_I in the HANC or the VANC part of the video signal. This signal is set at the beginning of every video frame, but is based on the detection of the previous frame.
		ANC_DD_DS7_FRAME_ANC	0:0	RO	0	When HIGH, indicates that ancillary data packet(s) selected for detection has/have been detected on DS7_I in the HANC or the VANC part of the video signal. This signal is set at the beginning of every video frame, but is based on the detection of the previous frame.
A04B	ANC_DD_STATS_1_DS_7_8_REG	RSVD	15:6	RO	0	Reserved.
		ANC_DD_DS8_CS_ERR	5:5	ROCW	0	When HIGH, indicates that the calculated checksum for ANC data packet selected for detection on DS8_I channel does not match the incoming packet checksum value.

Semtech Confidential Information
Kent Lin
DIVA Laboratories. Ltd.
09/08/2026

		ANC_DD_DS7_CS_ERR	4:4	ROCW	0	When HIGH, indicates that the calculated checksum for ANC data packet selected for detection on DS7_I channel does not match the incoming packet checksum value.
		ANC_DD_DS8_LIVE_VANC_ANC	3:3	ROCW	0	Signal that will be set HIGH when an ancillary data packet selected for detection is present during the VANC of the DS8_O output video signal.
		ANC_DD_DS8_LIVE_HANC_ANC	2:2	ROCW	0	Signal that will be set HIGH when an ancillary data packet selected for detection is present during the HANC of the DS8_O output video signal.
		ANC_DD_DS7_LIVE_VANC_ANC	1:1	ROCW	0	Signal that will be set HIGH when an ancillary data packet selected for detection is present during the VANC of the DS7_O output video signal.
		ANC_DD_DS7_LIVE_HANC_ANC	0:0	ROCW	0	Signal that will be set HIGH when an ancillary data packet selected for detection is present during the HANC of the DS7_O output video signal.
A04C	ANC_DD_HANC_ANC_CNT_DS_7_REG	ANC_DD_DS7_HANC_ANC_COUNT	15:0	RO	0	DS7 ancillary data packet word count. This signal gets updated at the beginning of every video frame (but is based on the detection of the previous frame) and represent the number of ancillary data words that were part of ancillary data packet(s) selected for detection and that were found in the HANC part of DS7_I.
A04D	ANC_DD_VANC_ANC_CNT_DS_7_REG	ANC_DD_DS7_VANC_ANC_COUNT	15:0	RO	0	DS7 ancillary data packet word count. This signal gets updated at the beginning of every video frame (but is based on the detection of the previous frame) and represent the number of ancillary data words that were part of ancillary data packet(s) selected for detection and that were found in the VANC part of DS7_I.
A04E	ANC_DD_HANC_ANC_PKT_CNT_DS_7_REG	ANC_DD_DS7_HANC_ANC_PKT_COUNT	15:0	RO	0	DS7 ancillary data packet count. This signal gets updated at the beginning of every video frame (but is based on the detection of the previous frame) and represent the number of ancillary data packets selected for detection and that were found in the HANC part of DS7_I.

Semtech Confidential Information
Kent Lin
DIVA Laboratories, Ltd.
09/08/2026

A04F	ANC_DD_VANC_ANC_PKT_CNT_DS_7_REG	ANC_DD_DS7_VANC_ANC_PKT_COUNT	15:0	RO	0	DS7 ancillary data packet count. This signal gets updated at the beginning of every video frame (but is based on the detection of the previous frame) and represent the number of ancillary data packets selected for detection and that were found in the VANC part of DS7_I.
A050	ANC_DD_HANC_ANC_CNT_DS_8_REG	ANC_DD_DS8_HANC_ANC_COUNT	15:0	RO	0	DS8 ancillary data packet word count. This signal gets updated at the beginning of every video frame (but is based on the detection of the previous frame) and represent the number of ancillary data words that were part of ancillary data packet(s) selected for detection and that were found in the HANC part of DS8_I.
A051	ANC_DD_VANC_ANC_CNT_DS_8_REG	ANC_DD_DS8_VANC_ANC_COUNT	15:0	RO	0	DS8 ancillary data packet word count. This signal gets updated at the beginning of every video frame (but is based on the detection of the previous frame) and represent the number of ancillary data words that were part of ancillary data packet(s) selected for detection and that were found in the VANC part of DS8_I.
A052	ANC_DD_HANC_ANC_PKT_CNT_DS_8_REG	ANC_DD_DS8_HANC_ANC_PKT_COUNT	15:0	RO	0	DS8 ancillary data packet count. This signal gets updated at the beginning of every video frame (but is based on the detection of the previous frame) and represent the number of ancillary data packets selected for detection and that were found in the HANC part of DS8_I.
A053	ANC_DD_VANC_ANC_PKT_CNT_DS_8_REG	ANC_DD_DS8_VANC_ANC_PKT_COUNT	15:0	RO	0	DS8 ancillary data packet count. This signal gets updated at the beginning of every video frame (but is based on the detection of the previous frame) and represent the number of ancillary data packets selected for detection and that were found in the VANC part of DS8_I.
A054		RSVD	15:3	RO	0	Reserved.

Semtech Confidential Information
Kent Lin
DIVA Laboratories. Ltd.
09/08/2026

	ANC_DEL_CTRL_DS_1_AND_2_REG	ANC_DELETE_ALL_DS_1_AND_2	2:2	RW		Signal that is active only when ANC_DATA_DELETE_DS_1_AND_2 is HIGH. When it is the case, if this signal is HIGH, the block will modify the DID of all the ANC packets for the SMPTE “marked for deletion DID” or will overwrite all the HANC and VANC spaces by blanking values specified on DS1_BLANK_0, DS1_BLANK_1, DS2_BLANK_0 and DS2_BLANK_1. When LOW, the block will modify the DID of all ANC packets except the audio data, audio control, PID and Time-code packets, for the SMPTE “marked for deletion DID” or will overwrite all ANC packets except the audio data, audio control, PID and Time-code packets with blanking values specified on DS1_BLANK_0, DS1_BLANK_1, DS2_BLANK_0 and DS2_BLANK_1.
		ANC_MARKED_DELETE_DS_1_AND_2	1:1	RW		Signal that is active only when ANC_DATA_DELETE_DS_1_AND_2 is HIGH. When it is the case, if this signal is HIGH, the block will modify the DID of certain types of ANC packets for the SMPTE “marked for deletion DID”. When LOW, the block will overwrite certain types of packets with blanking values.
		ANC_DATA_DELETE_DS_1_AND_2	0:0	RW		DS1 and DS2 Data Deletion enable. When HIGH, the block will perform ANC packet deleting on certain types of ANC data packets according to the other configuration setting. When LOW, the block will be put in bypass and will simply retransmit the incoming video signals.
A055	ANC_DEL_ANC_TYPE1_DS_1_AND_2_REG	ANC_DEL_ANC_TYPE1_DS_1_AND_2	15:0	RW	0	Programmable ancillary data type for deletion. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A056	ANC_DEL_ANC_TYPE2_DS_1_AND_2_REG	ANC_DEL_ANC_TYPE2_DS_1_AND_2	15:0	RW	0	Programmable ancillary data type for deletion. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A057	ANC_DEL_ANC_TYPE3_DS_1_AND_2_REG	ANC_DEL_ANC_TYPE3_DS_1_AND_2	15:0	RW	0	Programmable ancillary data type for deletion. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.

Semtech Confidential Information
Kent Lin
DIVA Laboratories. Ltd.
09/08/2026

A058	ANC_DEL_ANC_TYPE4_DS_1_AND_2_REG	ANC_DEL_ANC_TYPE4_DS_1_AND_2	15:0	RW	0	Programmable ancillary data type for deletion. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A059	ANC_DEL_ANC_TYPE5_DS_1_AND_2_REG	ANC_DEL_ANC_TYPE5_DS_1_AND_2	15:0	RW	0	Programmable ancillary data type for deletion. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A05A	ANC_DEL_ANC_TYPE6_DS_1_AND_2_REG	ANC_DEL_ANC_TYPE6_DS_1_AND_2	15:0	RW	0	Programmable ancillary data type for deletion. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A05B	ANC_DEL_ANC_TYPE7_DS_1_AND_2_REG	ANC_DEL_ANC_TYPE7_DS_1_AND_2	15:0	RW	0	Programmable ancillary data type for deletion. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A05C	ANC_DEL_ANC_TYPE8_DS_1_AND_2_REG	ANC_DEL_ANC_TYPE8_DS_1_AND_2	15:0	RW	0	Programmable ancillary data type for deletion. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A05D	ANC_DEL_BLANK_OVERWRITE_EN_DS_1_AND_2_REG	RSVD	15:1	RO	0	Reserved.
		BLANK_OVERWRITE_EN_DS_1_AND_2	0:0	RW	0	When HIGH, the ANC_DATA_DELETION block will use the CSR values for blanking. When LOW, blanking values will be set automatically based on the colour space.
A05E	ANC_DEL_DS1_BLANK_0_REG	RSVD	15:10	RO	0	Reserved.
		DS1_BLANK_0	9:0	RW	0	Blanking value to be used on alternating words in DS1_I.
A05F	ANC_DEL_DS1_BLANK_1_REG	RSVD	15:10	RO	0	Reserved.
		DS1_BLANK_1	9:0	RW	0	Blanking value to be used on alternating words in DS1_I.
A060	ANC_DEL_DS2_BLANK_0_REG	RSVD	15:10	RO	0	Reserved.
		DS2_BLANK_0	9:0	RW	0	Blanking value to be used on alternating words in DS2_I.
A061		RSVD	15:10	RO	0	Reserved.

Semtech Confidential Information
DIVA Laboratories Ltd.
Kent Lin
09/03/2026

	ANC_DEL_DS2_BLANK_1_REG	DS2_BLANK_1	9:0	RW	0	Blanking value to be used on alternating words in DS2_I.
A062	ANC_DEL_CTRL_DS_3_AND_4_REG	RSVD	15:3	RO	0	Reserved.
		ANC_DELETE_ALL_DS_3_AND_4	2:2	RW	0	Signal that is active only when ANC_DATA_DELETE_DS_3_AND_4 is HIGH. When it is the case, if this signal is HIGH, the block will modify the DID of all the ANC packets for the SMPTE “marked for deletion DID” or will overwrite all the HANC and VANC spaces by blanking values specified on DS3_BLANK_0, DS3_BLANK_1, DS4_BLANK_0 and DS4_BLANK_1. When LOW, the block will modify the DID of all ANC packets except the audio data, audio control, PID and TimeCode packets, for the SMPTE “marked for deletion DID” or will overwrite all ANC packets except the audio data, audio control, PID and TimeCode packets with blanking values specified on DS3_BLANK_0, DS3_BLANK_1, DS4_BLANK_0 and DS4_BLANK_1.
		ANC_MARKED_DELETE_DS_3_AND_4	1:1	RW	0	Signal that is active only when ANC_DATA_DELETE_DS_3_AND_4 is HIGH. When it is the case, if this signal is HIGH, the block will modify the DID of certain types of ANC packets for the SMPTE “marked for deletion DID”. When LOW, the block will overwrite certain types of packets with blanking values.
		ANC_DATA_DELETE_DS_3_AND_4	0:0	RW	0	DS3 and DS4 Data Deletion enable. When HIGH, the block will perform ANC packet deleting on certain types of ANC data packets according to the other configuration setting. When LOW, the block will be put in bypass and will simply retransmit the incoming video signals.
A063	ANC_DEL_ANC_TYPE1_DS_3_AND_4_REG	ANC_DEL_ANC_TYPE1_DS_3_AND_4	15:0	RW	0	Programmable ancillary data type for deletion. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A064	ANC_DEL_ANC_TYPE2_DS_3_AND_4_REG	ANC_DEL_ANC_TYPE2_DS_3_AND_4	15:0	RW	0	Programmable ancillary data type for deletion. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.

Semtech Confidential Information
Kent Lin
DIVA Laboratories. Ltd.
09/08/2026

A065	ANC_DEL_ANC_TYPE3_DS_3_AND_4_REG	ANC_DEL_ANC_TYPE3_DS_3_AND_4	15:0	RW	0	Programmable ancillary data type for deletion. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A066	ANC_DEL_ANC_TYPE4_DS_3_AND_4_REG	ANC_DEL_ANC_TYPE4_DS_3_AND_4	15:0	RW	0	Programmable ancillary data type for deletion. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A067	ANC_DEL_ANC_TYPE5_DS_3_AND_4_REG	ANC_DEL_ANC_TYPE5_DS_3_AND_4	15:0	RW	0	Programmable ancillary data type for deletion. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A068	ANC_DEL_ANC_TYPE6_DS_3_AND_4_REG	ANC_DEL_ANC_TYPE6_DS_3_AND_4	15:0	RW	0	Programmable ancillary data type for deletion. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A069	ANC_DEL_ANC_TYPE7_DS_3_AND_4_REG	ANC_DEL_ANC_TYPE7_DS_3_AND_4	15:0	RW	0	Programmable ancillary data type for deletion. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A06A	ANC_DEL_ANC_TYPE8_DS_3_AND_4_REG	ANC_DEL_ANC_TYPE8_DS_3_AND_4	15:0	RW	0	Programmable ancillary data type for deletion. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A06B	ANC_DEL_BLANK_OVERWRITE_EN_DS_3_AND_4_REG	RSVD	15:1	RO	0	Reserved.
		BLANK_OVERWRITE_EN_DS_3_AND_4	0:0	RW	0	When HIGH, the ANC_DATA_DELETION block will use the CSR values for blanking. When LOW, blanking values will be set automatically based on the colour space.
A06C	ANC_DEL_DS3_BLANK_0_REG	RSVD	15:10	RO	0	Reserved.
		DS3_BLANK_0	9:0	RW	0	Blanking value to be used on alternating words in DS3_I.
A06D	ANC_DEL_DS3_BLANK_1_REG	RSVD	15:10	RO	0	Reserved.
		DS3_BLANK_1	9:0	RW	0	Blanking value to be used on alternating words in DS3_I.
A06E		RSVD	15:10	RO	0	Reserved.

Semtech Confidential Information
Kent Lin
DVA Laboratories Ltd.
09/08/2026

	ANC_DEL_DS4_BLANK_0_REG	DS4_BLANK_0	9:0	RW	0	Blanking value to be used on alternating words in DS4_I.
A06F	ANC_DEL_DS4_BLANK_1_REG	RSVD	15:10	RO	0	Reserved.
		DS4_BLANK_1	9:0	RW	0	Blanking value to be used on alternating words in DS4_I.
A070	ANC_DEL_CTRL_DS_5_AND_6_REG	RSVD	15:3	RO	0	Reserved.
		ANC_DELETE_ALL_DS_5_AND_6	2:2	RW	0	Signal that is active only when ANC_DATA_DELETE_DS_5_AND_6 is HIGH. When it is the case, if this signal is HIGH, the block will modify the DID of all the ANC packets for the SMPTE “marked for deletion DID” or will overwrite all the HANC and VANC spaces by blanking values specified on DS5_BLANK_0, DS5_BLANK_1, DS6_BLANK_0 and DS6_BLANK_1. When LOW, the block will modify the DID of all ANC packets except the audio data, audio control, PID and TimeCode packets, for the SMPTE “marked for deletion DID” or will overwrite all ANC packets except the audio data, audio control, PID and TimeCode packets with blanking values specified on DS5_BLANK_0, DS5_BLANK_1, DS6_BLANK_0 and DS6_BLANK_1.
		ANC_MARKED_DELETE_DS_5_AND_6	1:1	RW	0	Signal that is active only when ANC_DATA_DELETE_DS_5_AND_6 is HIGH. When it is the case, if this signal is HIGH, the block will modify the DID of certain types of ANC packets for the SMPTE “marked for deletion DID”. When LOW, the block will overwrite certain types of packets with blanking values.
		ANC_DATA_DELETE_DS_5_AND_6	0:0	RW	0	DS5 and DS6 Data Deletion enable. When HIGH, the block will perform ANC packet deleting on certain types of ANC data packets according to the other configuration setting. When LOW, the block will be put in bypass and will simply retransmit the incoming video signals.
A071	ANC_DEL_ANC_TYPE1_DS_5_AND_6_REG	ANC_DEL_ANC_TYPE1_DS_5_AND_6	15:0	RW	0	Programmable ancillary data type for deletion. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.

Semtech Confidential Information
Kent Lin
DIVA Laboratories. Ltd.
09/08/2026

A072	ANC_DEL_ANC_TYPE2_DS_5_AND_6_REG	ANC_DEL_ANC_TYPE2_DS_5_AND_6	15:0	RW	0	Programmable ancillary data type for deletion. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A073	ANC_DEL_ANC_TYPE3_DS_5_AND_6_REG	ANC_DEL_ANC_TYPE3_DS_5_AND_6	15:0	RW	0	Programmable ancillary data type for deletion. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A074	ANC_DEL_ANC_TYPE4_DS_5_AND_6_REG	ANC_DEL_ANC_TYPE4_DS_5_AND_6	15:0	RW	0	Programmable ancillary data type for deletion. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A075	ANC_DEL_ANC_TYPE5_DS_5_AND_6_REG	ANC_DEL_ANC_TYPE5_DS_5_AND_6	15:0	RW	0	Programmable ancillary data type for deletion. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A076	ANC_DEL_ANC_TYPE6_DS_5_AND_6_REG	ANC_DEL_ANC_TYPE6_DS_5_AND_6	15:0	RW	0	Programmable ancillary data type for deletion. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A077	ANC_DEL_ANC_TYPE7_DS_5_AND_6_REG	ANC_DEL_ANC_TYPE7_DS_5_AND_6	15:0	RW	0	Programmable ancillary data type for deletion. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A078	ANC_DEL_ANC_TYPE8_DS_5_AND_6_REG	ANC_DEL_ANC_TYPE8_DS_5_AND_6	15:0	RW	0	Programmable ancillary data type for deletion. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A079	ANC_DEL_BLANK_OVERWRITE_EN_DS_5_AND_6_REG	RSVD	15:1	RO	0	Reserved.
		BLANK_OVERWRITE_EN_DS_5_AND_6	0:0	RW	0	When HIGH, the ANC_DATA_DELETION block will use the CSR values for blanking. When LOW, blanking values will be set automatically based on the colour space.
A07A	ANC_DEL_DS5_BLANK_0_REG	RSVD	15:10	RO	0	Reserved.
		DS5_BLANK_0	9:0	RW	0	Blanking value to be used on alternating words in DS5_I.
A07B		RSVD	15:10	RO	0	Reserved.

Semtech Confidential Information
Kent Lin
DIVA Laboratories, Ltd.
09/08/2026

	ANC_DEL_DS5_BLANK_1_REG	DS5_BLANK_1	9:0	RW	0	Blanking value to be used on alternating words in DS5_I.
A07C	ANC_DEL_DS6_BLANK_0_REG	RSVD	15:10	RO	0	Reserved.
		DS6_BLANK_0	9:0	RW	0	Blanking value to be used on alternating words in DS6_I.
A07D	ANC_DEL_DS6_BLANK_1_REG	RSVD	15:10	RO	0	Reserved.
		DS6_BLANK_1	9:0	RW	0	Blanking value to be used on alternating words in DS6_I.
A07E	ANC_DEL_CTRL_DS_7_AND_8_REG	RSVD	15:3	RO	0	Reserved.
		ANC_DELETE_ALL_DS_7_AND_8	2:2	RW	0	Signal that is active only when ANC_DATA_DELETE_DS_7_AND_8 is HIGH. When it is the case, if this signal is HIGH, the block will modify the DID of all the ANC packets for the SMPTE “marked for deletion DID” or will overwrite all the HANC and VANC spaces by blanking values specified on dS7_BLANK_0, DS7_BLANK_1, DS8_BLANK_0 and DS8_BLANK_1. When LOW, the block will modify the DID of all ANC packets except the audio data, audio control, PID and TimeCode packets, for the SMPTE “marked for deletion DID” or will overwrite all ANC packets except the audio data, audio control, PID and TimeCode packets with blanking values specified on DS7_BLANK_0, DS7_BLANK_1, DS8_BLANK_0 and DS8_BLANK_1.
		ANC_MARKED_DELETE_DS_7_AND_8	1:1	RW	0	Signal that is active only when ANC_DATA_DELETE_DS_7_AND_8 is HIGH. When it is the case, if this signal is HIGH, the block will modify the DID of certain types of ANC packets for the SMPTE “marked for deletion DID”. When LOW, the block will overwrite certain types of packets with blanking values.
		ANC_DATA_DELETE_DS_7_AND_8	0:0	RW	0	DS7 and DS8 Data Deletion enable. When HIGH, the block will perform ANC packet deleting on certain types of ANC data packets according to the other configuration setting. When LOW, the block will be put in bypass and will simply retransmit the incoming video signals.

Semtech Confidential Information
Kent Lin
DIVA Laboratories. Ltd.
09/08/2026

A07F	ANC_DEL_ANC_TYPE1_DS_7_AND_8_REG	ANC_DEL_ANC_TYPE1_DS_7_AND_8	15:0	RW	0	Programmable ancillary data type for deletion. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A080	ANC_DEL_ANC_TYPE2_DS_7_AND_8_REG	ANC_DEL_ANC_TYPE2_DS_7_AND_8	15:0	RW	0	Programmable ancillary data type for deletion. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A081	ANC_DEL_ANC_TYPE3_DS_7_AND_8_REG	ANC_DEL_ANC_TYPE3_DS_7_AND_8	15:0	RW	0	Programmable ancillary data type for deletion. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A082	ANC_DEL_ANC_TYPE4_DS_7_AND_8_REG	ANC_DEL_ANC_TYPE4_DS_7_AND_8	15:0	RW	0	Programmable ancillary data type for deletion. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A083	ANC_DEL_ANC_TYPE5_DS_7_AND_8_REG	ANC_DEL_ANC_TYPE5_DS_7_AND_8	15:0	RW	0	Programmable ancillary data type for deletion. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A084	ANC_DEL_ANC_TYPE6_DS_7_AND_8_REG	ANC_DEL_ANC_TYPE6_DS_7_AND_8	15:0	RW	0	Programmable ancillary data type for deletion. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A085	ANC_DEL_ANC_TYPE7_DS_7_AND_8_REG	ANC_DEL_ANC_TYPE7_DS_7_AND_8	15:0	RW	0	Programmable ancillary data type for deletion. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A086	ANC_DEL_ANC_TYPE8_DS_7_AND_8_REG	ANC_DEL_ANC_TYPE8_DS_7_AND_8	15:0	RW	0	Programmable ancillary data type for deletion. (DID/SDID pair). Bits 15 down to 8 contain the DID and bits 7 down to 0 contain the SDID.
A087	ANC_DEL_BLANK_OVERWRITE_EN_DS_7_AND_8_REG	RSVD	15:1	RO	0	Reserved.
		BLANK_OVERWRITE_EN_DS_7_AND_8	0:0	RW	0	When HIGH, the ANC_DATA_DELETION block will use the CSR values for blanking. When LOW, blanking values will be set automatically based on the colour space.
A088		RSVD	15:10	RO	0	Reserved.

Semtech Confidential Information
Kent Lin
DIVA Laboratories Ltd.
09/08/2026

	ANC_DEL_DS7_BLANK_0_REG	DS7_BLANK_0	9:0	RW	0	Blanking value to be used on alternating words in DS7_I.
A089	ANC_DEL_DS7_BLANK_1_REG	RSVD	15:10	RO	0	Reserved.
		DS7_BLANK_1	9:0	RW	0	Blanking value to be used on alternating words in DS7_I.
A08A	ANC_DEL_DS8_BLANK_0_REG	RSVD	15:10	RO	0	Reserved.
		DS8_BLANK_0	9:0	RW	0	Blanking value to be used on alternating words in DS8_I.
A08B	ANC_DEL_DS8_BLANK_1_REG	RSVD	15:10	RO	0	Reserved.
		DS8_BLANK_1	9:0	RW	0	Blanking value to be used on alternating words in DS8_I.
A08C	ANC_DATA_EXT_DATA_STREAM_SEL_REG	RSVD	15:8	RO	0	Reserved.
		ANC_DATA_EXT_FVH_SEL	7:6	RW	0	FVH selection that will be used by the ANC Data Extraction block. 00 = FVH associated with data streams 1 and 2, 01 = FVH associated with data streams 3 and 4, 10 = FVH associated with data streams 5 and 6, 11 = FVH associated with data streams 7 and 8.
		ANC_DATA_EXT_DATA_STREAM_SEL_B	5:3	RW	1	Second data stream selection for ANC Data Extraction. 000 = DS1, 001 = DS2, 010 = DS3, 011 = DS4, 100 = DS5, 101 = DS6, 110 = DS7, 111 = DS8.
		ANC_DATA_EXT_DATA_STREAM_SEL_A	2:0	RW	0	First data stream selection for ANC Data Extraction. 000 = DS1, 001 = DS2, 010 = DS3, 011 = DS4, 100 = DS5, 101 = DS6, 110 = DS7, 111 = DS8.
A08D	ANC_DATA_EXT_ENABLE_REG	RSVD	15:1	RO	0	Reserved.
		ANC_EXT_ENABLE	0:0	RW	0	Block enable signal. When HIGH, the block will extract ancillary data from the video input data streams. When LOW, the block is disabled.
A08E		RSVD	15:5	RO	0	Reserved.

Semtech Confidential Information
Kent Lin
DIVA Laboratories, Ltd.
09/08/2026

	ANC_DATA_EXT_CFG_REG	ANC_EXT_MEM_BANK_SWITCH_MODE	4:4	RW	0	When HIGH, the block will operate in manual bank switch mode and the selection will be made with the MANUAL_MODE_WRITE_BANK_SELECTION signal. When LOW, the block will operate in auto bank switch mode, which will be done at the end of every video frame.
		ANC_EXT_DS2_HANC_VANC_MEM_USAGE	3:2	RW	0	Data stream B data extraction select. 00 = ANC data will be extracted from both HANC and VANC areas of the selected video input data stream. 01 = data will be extracted only from the HANC area of the selected video input data streams. 10 = data will be extracted only from the VANC area of the selected video input data streams.
		ANC_EXT_DS1_HANC_VANC_MEM_USAGE	1:0	RW	0	Data stream A data extraction select. 00 = ANC data will be extracted from both HANC and VANC areas of the selected video input data stream. 01 = data will be extracted only from the HANC area of the selected video input data streams. 10 = data will be extracted only from the VANC area of the selected video input data streams.
A08F	ANC_DATA_EXT_WRITE_BANK_SELECT_REG	RSVD	15:1	RO	0	Reserved.
		ANC_EXT_MANUAL_MODE_WRITE_BANK_SELECT	0:0	RW	0	When HIGH, the bank 2 memories will be selected to store/write ANC data and bank 1 memories will be selected to read ANC data. When LOW, the bank 1 memories will be selected to store/write ANC data and bank 2 memories will be selected to read ANC data.
A090	ANC_DATA_EXT_DSA_LINE1_CFG_REG	RSVD	15:11	RO	0	Reserved.
		DSA_ANC_EXT_LINE_NUMBER_1	10:0	RW	0	Line number 1 selection for ANC data extraction on data stream A. When this parameter is not set to 0, the block will extract ANC data on the line which matches ANC_EXT_LINE_NUMBER_1. When both ANC_EXT_LINE_NUMBER_1 and ANC_EXT_LINE_NUMBER_2 are set to 0, the block will extract ANC data regardless of the line it is located in.
A091		RSVD	15:11	RO	0	Reserved.

Semtech Confidential Information
DIVA Laboratories. Ltd.
Kent Lin
09/03/2026

	ANC_DATA_EXT_DSA_LINE2_CFG_REG	DSA_ANC_EXT_LINE_NUMBER_2	10:0	RW	0	Line number 2 selection for ANC data extraction on data stream A. When this parameter is not set to 0, the block will extract ANC data on the line which matches ANC_EXT_LINE_NUMBER_2. When both ANC_EXT_LINE_NUMBER_1 and ANC_EXT_LINE_NUMBER_2 are set to 0, the block will extract ANC data regardless of the line it is located in.
A092	ANC_DATA_EXT_DSB_LINE1_CFG_REG	RSVD	15:11	RO	0	Reserved.
		DSB_ANC_EXT_LINE_NUMBER_1	10:0	RW	0	Line number 1 selection for ANC data extraction on data stream B. When this parameter is not set to 0, the block will extract ANC data on the line which matches ANC_EXT_LINE_NUMBER_1. When both ANC_EXT_LINE_NUMBER_1 and ANC_EXT_LINE_NUMBER_2 are set to 0, the block will extract ANC data regardless of the line it is located in.
A093	ANC_DATA_EXT_DSB_LINE2_CFG_REG	RSVD	15:11	RO	0	Reserved.
		DSB_ANC_EXT_LINE_NUMBER_2	10:0	RW	0	Line number 2 selection for ANC data extraction on data stream B. When this parameter is not set to 0, the block will extract ANC data on the line which matches ANC_EXT_LINE_NUMBER_2. When both ANC_EXT_LINE_NUMBER_1 and ANC_EXT_LINE_NUMBER_2 are set to 0, the block will extract ANC data regardless of the line it is located in.
A094	ANC_EXT_DSA_HANC_BANK1_WR_ADDR_REG	RSVD	15:10	RO	0	Reserved.
		DSA_HANC_BANK1_WR_ADDR	9:0	RO	0	Memory write address pointer for the DSA HANC bank 1 memory.
A095	ANC_EXT_DSA_VANC_BANK1_WR_ADDR_REG	RSVD	15:10	RO	0	Reserved.
		DSA_VANC_BANK1_WR_ADDR	9:0	RO	0	Memory write address pointer for the DSA VANC bank 1 memory.
A096	ANC_EXT_DSA_HANC_BANK2_WR_ADDR_REG	RSVD	15:10	RO	0	Reserved.
		DSA_HANC_BANK2_WR_ADDR	9:0	RO	0	Memory write address pointer for the DSA HANC bank 2 memory.
A097		RSVD	15:10	RO	0	Reserved.

Semtech Confidential Information
Kent Lin
DIVA Laboratories, Ltd.
09/08/2026

	ANC_EXT_DSA_VANC_BANK2_WR_ADDR_REG	DSA_VANC_BANK2_WR_ADDR	9:0	RO	0	Memory write address pointer for the DSA VANC bank 2 memory.
A098	ANC_EXT_DSB_HANC_BANK1_WR_ADDR_REG	RSVD	15:10	RO	0	Reserved.
		DSB_HANC_BANK1_WR_ADDR	9:0	RO	0	Memory write address pointer for the DSB HANC bank 1 memory.
A099	ANC_EXT_DSB_VANC_BANK1_WR_ADDR_REG	RSVD	15:10	RO	0	Reserved.
		DSB_VANC_BANK1_WR_ADDR	9:0	RO	0	Memory write address pointer for the DSB VANC bank 1 memory.
A09A	ANC_EXT_DSB_HANC_BANK2_WR_ADDR_REG	RSVD	15:10	RO	0	Reserved.
		DSB_HANC_BANK2_WR_ADDR	9:0	RO	0	Memory write address pointer for the DSB HANC bank 2 memory.
A09B	ANC_EXT_DSB_VANC_BANK2_WR_ADDR_REG	RSVD	15:10	RO	0	Reserved.
		DSB_VANC_BANK2_WR_ADDR	9:0	RO	0	Memory write address pointer for the DSB VANC bank 2 memory.
A09C	ANC_EXT_HANC_VANC_FILLED_UP_REG	RSVD	15:8	RO	0	Reserved.
		DSB_VANC_BANK2_FILLED_UP	7:7	RO	0	When HIGH, this signal indicates that all the addresses of the DSB VANC bank 2 memory have been written to prior to a bank switch.
		DSB_HANC_BANK2_FILLED_UP	6:6	RO	0	When HIGH, this signal indicates that all the addresses of the DSB HANC bank 2 memory have been written to prior to a bank switch.
		DSB_VANC_BANK1_FILLED_UP	5:5	RO	0	When HIGH, this signal indicates that all the addresses of the DSB VANC bank 1 memory have been written to prior to a bank switch.
		DSB_HANC_BANK1_FILLED_UP	4:4	RO	0	When HIGH, this signal indicates that all the addresses of the DSB HANC bank 1 memory have been written to prior to a bank switch
		DSA_VANC_BANK2_FILLED_UP	3:3	RO	0	When HIGH, this signal indicates that all the addresses of the DSA VANC bank 2 memory have been written to prior to a bank switch.

Semtech Confidential Information
Kent Lin
DVA Laboratories Ltd.
09/08/2026

		DSA_HANC_BANK2_FILLED_UP	2:2	RO	0	When HIGH, this signal indicates that all the addresses of the DSA HANC bank 2 memory have been written to prior to a bank switch.
		DSA_VANC_BANK1_FILLED_UP	1:1	RO	0	When HIGH, this signal indicates that all the addresses of the DSA VANC bank 1 memory have been written to prior to a bank switch.
		DSA_HANC_BANK1_FILLED_UP	0:0	RO	0	When HIGH, this signal indicates that all the addresses of the DSA HANC bank 1 memory have been written to prior to a bank switch.
A09D	ANC_EXT_MEMORY_WRITE_ACTIVE_BANK_REG	RSVD	15:1	RO	0	Reserved.
		MEMORY_WRITE_ACTIVE_BANK	0:0	RO	0	Signal indicating which memory bank is currently used for extracting (writing) ANC data. When LOW, indicates that all the bank 1 memories are used in write mode. When HIGH, indicates that all the bank 2 memories are used in write mode.
A09E	ANC_EXT_HANC_VANC_3QUARTER_FULL_REG	RSVD	15:8	RO	0	Reserved.
		DSB_VANC_BANK2_3QUARTER_FULL	7:7	RO	0	Signal used only in manual bank switching mode. When HIGH, indicates that the memory is at least ¾ full. Will be cleared on a MANUAL_MODE_WRITE_BANK_SELECTION change.
		DSB_HANC_BANK2_3QUARTER_FULL	6:6	RO	0	Signal used only in manual bank switching mode. When HIGH, indicates that the memory is at least ¾ full. Will be cleared on a MANUAL_MODE_WRITE_BANK_SELECTION change.
		DSB_VANC_BANK1_3QUARTER_FULL	5:5	RO	0	Signal used only in manual bank switching mode. When HIGH, indicates that the memory is at least ¾ full. Will be cleared on a MANUAL_MODE_WRITE_BANK_SELECTION change.
		DSB_HANC_BANK1_3QUARTER_FULL	4:4	RO	0	Signal used only in manual bank switching mode. When HIGH, indicates that the memory is at least ¾ full. Will be cleared on a MANUAL_MODE_WRITE_BANK_SELECTION change.

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Kent Lin
DIVA Laboratories, Ltd.
09/08/2026

		DSA_VANC_BANK2_3QUARTER_FULL	3:3	RO	0	Signal used only in manual bank switching mode. When HIGH, indicates that the memory is at least ¾ full. Will be cleared on a MANUAL_MODE_WRITE_BANK_SELECTION change.
		DSA_HANC_BANK2_3QUARTER_FULL	2:2	RO	0	Signal used only in manual bank switching mode. When HIGH, indicates that the memory is at least ¾ full. Will be cleared on a MANUAL_MODE_WRITE_BANK_SELECTION change.
		DSA_VANC_BANK1_3QUARTER_FULL	1:1	RO	0	Signal used only in manual bank switching mode. When HIGH, indicates that the memory is at least ¾ full. Will be cleared on a MANUAL_MODE_WRITE_BANK_SELECTION change.
		DSA_HANC_BANK1_3QUARTER_FULL	0:0	RO	0	Signal used only in manual bank switching mode. When HIGH, indicates that the memory is at least ¾ full. Will be cleared on a MANUAL_MODE_WRITE_BANK_SELECTION change.
A09F	ANC_EXT_READING_CTRL_REG	RSVD	15:1	RO	0	Reserved.
		ANC_EXT_GSPI_SERIAL_IF_B	0:0	RW	0	Signal that needs to be programmed to decide where the ancillary data that has been extracted will be output. When HIGH, the reading of the extracted ancillary data will be done through the GSPI interface. When LOW, the reading and outputting of the extracted ancillary data will be done through the ancillary data serial interface.
A0A0	ANC_DATA_SERIAL_IF_ENABLE_REG	RSVD	15:1	RO	0	Reserved.
		ANC_DATA_SERIAL_IF_ENABLE	0:0	RW	0	Block enable signal. When HIGH, the block reads ancillary data stored in memory and serializes it. When LOW, the block is disabled.
A0A1		RSVD	15:3	RO	0	Reserved.

Semtech Confidential Information
Kent Lin
DIVA Laboratories. Ltd.
09/08/2026

	ANC_DATA_SERIAL_IF_CLK_DIV_REG	ANC_DATA_SERIAL_CLK_DIV	2:0	RW	0	ANC data serial clock division factor: 000 = ANC_SI_CLK will be CLK/2 001 = ANC_SI_CLK will be CLK/4 010 = ANC_SI_CLK will be CLK/8 011 = ANC_SI_CLK will be CLK/16 100 = ANC_SI_CLK will be CLK/32 101 = ANC_SI_CLK will be CLK/64 110 = ANC_SI_CLK will be CLK/128 111 = ANC_SI_CLK will be CLK/256 **Note:** CLK varies with data rate with a max frequency of 148.5MHz.
A0A2	ANC_DATA_SERIAL_IF_STATUS_REG	RSVD	15:1	RO	0	Reserved.
		ANC_DATA_SERIAL_CLOCK_NOT_FAST_ENOUGH	0:0	ROCW	0	When HIGH, indicates that the block was in the middle of packet serialization when a rising edge of MEMORY_WRITE_STATUS_UPDATE occurred. When LOW, no such event occurred.
A0A3	BLANK_CUST352M_WD1_3_0	RSVD	15:12	RO	0	Reserved.
		CUSTOM_352M_WD3_0	11:8	RW	0	Bits 3 to 0 of 352M byte 3 value to look for in custom blanking mode.
		CUSTOM_352M_WD1_0	7:0	RW	0	352M byte 1 value to look for in custom blanking mode.
A0A4	BLANK_CUST352M_WD4_0	RSVD	15:5	RO	0	Reserved.
		CUSTOM_352M_WD4_ML_0	4:2	RW	0	Bits 7 to 5 of 352M byte 4 value to look for in custom blanking mode.
		CUSTOM_352M_WD4_BD_0	1:0	RW	0	Bits 1 to 0 of 352M byte 4 value to look for in custom blanking mode.
A0A5	CUSTOM_Y_BLANK_0_0	RSVD	15:10	RO	0	Reserved.
		CUSTOM_Y_BLANK_0_0	9:0	RW	0	Y_BLANK_0 value to use when incoming 352M values match those programmed above.
A0A6	CUSTOM_Y_BLANK_1_0	RSVD	15:10	RO	0	Reserved.
		CUSTOM_Y_BLANK_1_0	9:0	RW	0	Y_BLANK_1 value to use when incoming 352M values match those programmed above.

Semtech Confidential Information
Kent Lin
DIVA Laboratories, Ltd.
09/08/2026

A0A7	CUSTOM_C_BLANK_0_0	RSVD	15:10	RO	0	Reserved.
		CUSTOM_C_BLANK_0_0	9:0	RW	0	C_BLANK_0 value to use when incoming 352M values match those programmed above.
A0A8	CUSTOM_C_BLANK_1_0	RSVD	15:10	RO	0	Reserved.
		CUSTOM_C_BLANK_1_0	9:0	RW	0	C_BLANK_1 value to use when incoming 352M values match those programmed above.
A0A9	BLANK_CUST352M_WD1_3_1	RSVD	15:12	RO	0	Reserved.
		CUSTOM_352M_WD3_1	11:8	RW	0	Bits 3 to 0 of 352M byte 3 value to look for in custom blanking mode.
		CUSTOM_352M_WD1_1	7:0	RW	0	352M byte 1 value to look for in custom blanking mode.
A0AA	BLANK_CUST352M_WD4_1	RSVD	15:5	RO	0	Reserved.
		CUSTOM_352M_WD4_ML_1	4:2	RW	0	Bits 7 to 5 of 352M byte 4 value to look for in custom blanking mode.
		CUSTOM_352M_WD4_BD_1	1:0	RW	0	Bits 1 to 0 of 352M byte 4 value to look for in custom blanking mode.
A0AB	CUSTOM_Y_BLANK_0_1	RSVD	15:10	RO	0	Reserved.
		CUSTOM_Y_BLANK_0_1	9:0	RW	0	Y_BLANK_0 value to use when incoming 352M values match those programmed above.
A0AC	CUSTOM_Y_BLANK_1_1	RSVD	15:10	RO	0	Reserved.
		CUSTOM_Y_BLANK_1_1	9:0	RW	0	Y_BLANK_1 value to use when incoming 352M values match those programmed above.
A0AD	CUSTOM_C_BLANK_0_1	RSVD	15:10	RO	0	Reserved.
		CUSTOM_C_BLANK_0_1	9:0	RW	0	C_BLANK_0 value to use when incoming 352M values match those programmed above.

Semtech Confidential Information
Kent Lin
DIVA Laboratories, Ltd.
09/08/2026

A0AE	CUSTOM_C_BLANK_1_1	RSVD	15:10	RO	0	Reserved.
		CUSTOM_C_BLANK_1_1	9:0	RW	0	C_BLANK_1 value to use when incoming 352M values match those programmed above.
A0AF	BLANK_CUST352M_WD1_3_2	RSVD	15:12	RO	0	Reserved.
		CUSTOM_352M_WD3_2	11:8	RW	0	Bits 3 to 0 of 352M byte 3 value to look for in custom blanking mode.
		CUSTOM_352M_WD1_2	7:0	RW	0	352M byte 1 value to look for in custom blanking mode.
A0B0	BLANK_CUST352M_WD4_2	RSVD	15:5	RO	0	Reserved.
		CUSTOM_352M_WD4_ML_2	4:2	RW	0	Bits 7 to 5 of 352M byte 4 value to look for in custom blanking mode.
		CUSTOM_352M_WD4_BD_2	1:0	RW	0	Bits 1 to 0 of 352M byte 4 value to look for in custom blanking mode.
A0B1	CUSTOM_Y_BLANK_0_2	RSVD	15:10	RO	0	Reserved.
		CUSTOM_Y_BLANK_0_2	9:0	RW	0	Y_BLANK_0 value to use when incoming 352M values match those programmed above.
A0B2	CUSTOM_Y_BLANK_1_2	RSVD	15:10	RO	0	Reserved.
		CUSTOM_Y_BLANK_1_2	9:0	RW	0	Y_BLANK_1 value to use when incoming 352M values match those programmed above.
A0B3	CUSTOM_C_BLANK_0_2	RSVD	15:10	RO	0	Reserved.
		CUSTOM_C_BLANK_0_2	9:0	RW	0	C_BLANK_0 value to use when incoming 352M values match those programmed above.
A0B4	CUSTOM_C_BLANK_1_2	RSVD	15:10	RO	0	Reserved.
		CUSTOM_C_BLANK_1_2	9:0	RW	0	C_BLANK_1 value to use when incoming 352M values match those programmed above.

Semtech Confidential Information
Ken Lin
DIVA Laboratories, Ltd.
09/08/2026

A0B5	BLANK_CUST352M_WD1_3_3	RSVD	15:12	RO	0	Reserved.
		CUSTOM_352M_WD3_3	11:8	RW	0	Bits 3 to 0 of 352M byte 3 value to look for in custom blanking mode.
		CUSTOM_352M_WD1_3	7:0	RW	0	352M byte 1 value to look for in custom blanking mode.
A0B6	BLANK_CUST352M_WD4_3	RSVD	15:5	RO	0	Reserved.
		CUSTOM_352M_WD4_ML_3	4:2	RW	0	Bits 7 to 5 of 352M byte 4 value to look for in custom blanking mode.
		CUSTOM_352M_WD4_BD_3	1:0	RW	0	Bits 1 to 0 of 352M byte 4 value to look for in custom blanking mode.
A0B7	CUSTOM_Y_BLANK_0_3	RSVD	15:10	RO	0	Reserved.
		CUSTOM_Y_BLANK_0_3	9:0	RW	0	Y_BLANK_0 value to use when incoming 352M values match those programmed above.
A0B8	CUSTOM_Y_BLANK_1_3	RSVD	15:10	RO	0	Reserved.
		CUSTOM_Y_BLANK_1_3	9:0	RW	0	Y_BLANK_1 value to use when incoming 352M values match those programmed above.
A0B9	CUSTOM_C_BLANK_0_3	RSVD	15:10	RO	0	Reserved.
		CUSTOM_C_BLANK_0_3	9:0	RW	0	C_BLANK_0 value to use when incoming 352M values match those programmed above.
A0BA	CUSTOM_C_BLANK_1_3	RSVD	15:10	RO	0	Reserved.
		CUSTOM_C_BLANK_1_3	9:0	RW	0	C_BLANK_1 value to use when incoming 352M values match those programmed above.
A0BB	BLANK_CUST352M_WD1_3_4	RSVD	15:12	RO	0	Reserved.
		CUSTOM_352M_WD3_4	11:8	RW	0	Bits 3 to 0 of 352M byte 3 value to look for in custom blanking mode.

Semtech Confidential Information
Ken Lin
DIVA Laboratories Ltd.
09/08/2026

		CUSTOM_352M_WD1_4	7:0	RW	0	352M byte 1 value to look for in custom blanking mode.
A0BC	BLANK_CUST352M_WD4_4	RSVD	15:5	RO	0	Reserved.
		CUSTOM_352M_WD4_ML_4	4:2	RW	0	Bits 7 to 5 of 352M byte 4 value to look for in custom blanking mode.
		CUSTOM_352M_WD4_BD_4	1:0	RW	0	Bits 1 to 0 of 352M byte 4 value to look for in custom blanking mode.
A0BD	CUSTOM_Y_BLANK_0_4	RSVD	15:10	RO	0	Reserved.
		CUSTOM_Y_BLANK_0_4	9:0	RW	0	Y_BLANK_0 value to use when incoming 352M values match those programmed above.
A0BE	CUSTOM_Y_BLANK_1_4	RSVD	15:10	RO	0	Reserved.
		CUSTOM_Y_BLANK_1_4	9:0	RW	0	Y_BLANK_1 value to use when incoming 352M values match those programmed above.
A0BF	CUSTOM_C_BLANK_0_4	RSVD	15:10	RO	0	Reserved.
		CUSTOM_C_BLANK_0_4	9:0	RW	0	C_BLANK_0 value to use when incoming 352M values match those programmed above.
A0C0	CUSTOM_C_BLANK_1_4	RSVD	15:10	RO	0	Reserved.
		CUSTOM_C_BLANK_1_4	9:0	RW	0	C_BLANK_1 value to use when incoming 352M values match those programmed above.
A0C1	BLANK_CUST352M_WD1_3_5	RSVD	15:12	RO	0	Reserved.
		CUSTOM_352M_WD3_5	11:8	RW	0	Bits 3 to 0 of 352M byte 3 value to look for in custom blanking mode.
		CUSTOM_352M_WD1_5	7:0	RW	0	352M byte 1 value to look for in custom blanking mode.
A0C2		RSVD	15:5	RO	0	Reserved.

Semtech Confidential Information
Kent Lin
DIVA Laboratories, Ltd.
09/08/2026

	BLANK_ CUST352M_ WD4_5	CUSTOM_352M_ WD4_ML_5	4:2	RW	0	Bits 7 to 5 of 352M byte 4 value to look for in custom blanking mode.
		CUSTOM_352M_ WD4_BD_5	1:0	RW	0	Bits 1 to 0 of 352M byte 4 value to look for in custom blanking mode.
A0C3	CUSTOM_Y_ BLANK_0_5	RSVD	15:10	RO	0	Reserved.
		CUSTOM_Y_ BLANK_0_5	9:0	RW	0	Y_BLANK_0 value to use when incoming 352M values match those programmed above.
A0C4	CUSTOM_Y_ BLANK_1_5	RSVD	15:10	RO	0	Reserved.
		CUSTOM_Y_ BLANK_1_5	9:0	RW	0	Y_BLANK_1 value to use when incoming 352M values match those programmed above.
A0C5	CUSTOM_C_ BLANK_0_5	RSVD	15:10	RO	0	Reserved.
		CUSTOM_C_ BLANK_0_5	9:0	RW	0	C_BLANK_0 value to use when incoming 352M values match those programmed above.
A0C6	CUSTOM_C_ BLANK_1_5	RSVD	15:10	RO	0	Reserved.
		CUSTOM_C_ BLANK_1_5	9:0	RW	0	C_BLANK_1 value to use when incoming 352M values match those programmed above.
A0C7	BLANK_ CUST352M_ WD1_3_6	RSVD	15:12	RO	0	Reserved.
		CUSTOM_352M_ WD3_6	11:8	RW	0	Bits 3 to 0 of 352M byte 3 value to look for in custom blanking mode.
		CUSTOM_352M_ WD1_6	7:0	RW	0	352M byte 1 value to look for in custom blanking mode.
A0C8	BLANK_ CUST352M_ WD4_6	RSVD	15:5	RO	0	Reserved.
		CUSTOM_352M_ WD4_ML_6	4:2	RW	0	Bits 7 to 5 of 352M byte 4 value to look for in custom blanking mode.
		CUSTOM_352M_ WD4_BD_6	1:0	RW	0	Bits 1 to 0 of 352M byte 4 value to look for in custom blanking mode.

Semtech Confidential Information
Kent Lin
DIVA Laboratories, Ltd.
09/08/2026

A0C9	CUSTOM_Y_BLANK_0_6	RSVD	15:10	RO	0	Reserved.
		CUSTOM_Y_BLANK_0_6	9:0	RW	0	Y_BLANK_0 value to use when incoming 352M values match those programmed above.
A0CA	CUSTOM_Y_BLANK_1_6	RSVD	15:10	RO	0	Reserved.
		CUSTOM_Y_BLANK_1_6	9:0	RW	0	Y_BLANK_1 value to use when incoming 352M values match those programmed above.
A0CB	CUSTOM_C_BLANK_0_6	RSVD	15:10	RO	0	Reserved.
		CUSTOM_C_BLANK_0_6	9:0	RW	0	C_BLANK_0 value to use when incoming 352M values match those programmed above.
A0CC	CUSTOM_C_BLANK_1_6	RSVD	15:10	RO	0	Reserved.
		CUSTOM_C_BLANK_1_6	9:0	RW	0	C_BLANK_1 value to use when incoming 352M values match those programmed above.
A0CD	BLANK_CUST352M_WD1_3_7	RSVD	15:12	RO	0	Reserved.
		CUSTOM_352M_WD3_7	11:8	RW	0	Bits 3 to 0 of 352M byte 3 value to look for in custom blanking mode.
		CUSTOM_352M_WD1_7	7:0	RW	0	352M byte 1 value to look for in custom blanking mode.
A0CE	BLANK_CUST352M_WD4_7	RSVD	15:5	RO	0	Reserved.
		CUSTOM_352M_WD4_ML_7	4:2	RW	0	Bits 7 to 5 of 352M byte 4 value to look for in custom blanking mode.
		CUSTOM_352M_WD4_BD_7	1:0	RW	0	Bits 1 to 0 of 352M byte 4 value to look for in custom blanking mode.
A0CF	CUSTOM_Y_BLANK_0_7	RSVD	15:10	RO	0	Reserved.
		CUSTOM_Y_BLANK_0_7	9:0	RW	0	Y_BLANK_0 value to use when incoming 352M values match those programmed above.

Semtech Confidential Information
Kent Lin
DIVA Laboratories, Ltd.
09/08/2026

A0D0	CUSTOM_Y_BLANK_1_7	RSVD	15:10	RO	0	Reserved.
		CUSTOM_Y_BLANK_1_7	9:0	RW	0	Y_BLANK_1 value to use when incoming 352M values match those programmed above.
A0D1	CUSTOM_C_BLANK_0_7	RSVD	15:10	RO	0	Reserved.
		CUSTOM_C_BLANK_0_7	9:0	RW	0	C_BLANK_0 value to use when incoming 352M values match those programmed above.
A0D2	CUSTOM_C_BLANK_1_7	RSVD	15:10	RO	0	Reserved.
		CUSTOM_C_BLANK_1_7	9:0	RW	0	C_BLANK_1 value to use when incoming 352M values match those programmed above.
A0D3	BLANK_CUST352M_WD1_3_8	RSVD	15:12	RO	0	Reserved.
		CUSTOM_352M_WD3_8	11:8	RW	0	Bits 3 to 0 of 352M byte 3 value to look for in custom blanking mode.
		CUSTOM_352M_WD1_8	7:0	RW	0	352M byte 1 value to look for in custom blanking mode.
A0D4	BLANK_CUST352M_WD4_8	RSVD	15:5	RO	0	Reserved.
		CUSTOM_352M_WD4_ML_8	4:2	RW	0	Bits 7 to 5 of 352M byte 4 value to look for in custom blanking mode
		CUSTOM_352M_WD4_BD_8	1:0	RW	0	Bits 1 to 0 of 352M byte 4 value to look for in custom blanking mode.
A0D5	CUSTOM_Y_BLANK_0_8	RSVD	15:10	RO	0	Reserved.
		CUSTOM_Y_BLANK_0_8	9:0	RW	0	Y_BLANK_0 value to use when incoming 352M values match those programmed above.
A0D6	CUSTOM_Y_BLANK_1_8	RSVD	15:10	RO	0	Reserved.
		CUSTOM_Y_BLANK_1_8	9:0	RW	0	Y_BLANK_1 value to use when incoming 352M values match those programmed above.

Semtech Confidential Information
Kent Lin
DIVA Laboratories, Ltd.
09/08/2026

A0D7	CUSTOM_C_BLANK_0_8	RSVD	15:10	RO	0	Reserved.
		CUSTOM_C_BLANK_0_8	9:0	RW	0	C_BLANK_0 value to use when incoming 352M values match those programmed above.
A0D8	CUSTOM_C_BLANK_1_8	RSVD	15:10	RO	0	Reserved.
		CUSTOM_C_BLANK_1_8	9:0	RW	0	C_BLANK_1 value to use when incoming 352M values match those programmed above.
A0D9	BLANK_CUST352M_WD1_3_9	RSVD	15:12	RO	0	Reserved.
		CUSTOM_352M_WD3_9	11:8	RW	0	Bits 3 to 0 of 352M byte 3 value to look for in custom blanking mode.
		CUSTOM_352M_WD1_9	7:0	RW	0	352M byte 1 value to look for in custom blanking mode.
A0DA	BLANK_CUST352M_WD4_9	RSVD	15:5	RO	0	Reserved.
		CUSTOM_352M_WD4_ML_9	4:2	RW	0	Bits 7 to 5 of 352M byte 4 value to look for in custom blanking mode.
		CUSTOM_352M_WD4_BD_9	1:0	RW	0	Bits 1 to 0 of 352M byte 4 value to look for in custom blanking mode.
A0DB	CUSTOM_Y_BLANK_0_9	RSVD	15:10	RO	0	Reserved.
		CUSTOM_Y_BLANK_0_9	9:0	RW	0	Y_BLANK_0 value to use when incoming 352M values match those programmed above.
A0DC	CUSTOM_Y_BLANK_1_9	RSVD	15:10	RO	0	Reserved.
		CUSTOM_Y_BLANK_1_9	9:0	RW	0	Y_BLANK_1 value to use when incoming 352M values match those programmed above.
A0DD	CUSTOM_C_BLANK_0_9	RSVD	15:10	RO	0	Reserved.
		CUSTOM_C_BLANK_0_9	9:0	RW	0	C_BLANK_0 value to use when incoming 352M values match those programmed above.

Semtech Confidential Information
Kent Lin
DIVA Laboratories, Ltd.
09/08/2026

A0DE	CUSTOM_C_BLANK_1_9	RSVD	15:10	RO	0	Reserved.
		CUSTOM_C_BLANK_1_9	9:0	RW	0	C_BLANK_1 value to use when incoming 352M values match those programmed above.
A0DF	BLANK_CUST352M_WD1_3_10	RSVD	15:12	RO	0	Reserved.
		CUSTOM_352M_WD3_10	11:8	RW	0	Bits 3 to 0 of 352M byte 3 value to look for in custom blanking mode.
		CUSTOM_352M_WD1_10	7:0	RW	0	352M byte 1 value to look for in custom blanking mode.
A0E0	BLANK_CUST352M_WD4_10	RSVD	15:5	RO	0	Reserved.
		CUSTOM_352M_WD4_ML_10	4:2	RW	0	Bits 7 to 5 of 352M byte 4 value to look for in custom blanking mode.
		CUSTOM_352M_WD4_BD_10	1:0	RW	0	Bits 1 to 0 of 352M byte 4 value to look for in custom blanking mode.
A0E1	CUSTOM_Y_BLANK_0_10	RSVD	15:10	RO	0	Reserved.
		CUSTOM_Y_BLANK_0_10	9:0	RW	0	Y_BLANK_0 value to use when incoming 352M values match those programmed above.
A0E2	CUSTOM_Y_BLANK_1_10	RSVD	15:10	RO	0	Reserved.
		CUSTOM_Y_BLANK_1_10	9:0	RW	0	Y_BLANK_1 value to use when incoming 352M values match those programmed above.
A0E3	CUSTOM_C_BLANK_0_10	RSVD	15:10	RO	0	Reserved.
		CUSTOM_C_BLANK_0_10	9:0	RW	0	C_BLANK_0 value to use when incoming 352M values match those programmed above.
A0E4	CUSTOM_C_BLANK_1_10	RSVD	15:10	RO	0	Reserved.
		CUSTOM_C_BLANK_1_10	9:0	RW	0	C_BLANK_1 value to use when incoming 352M values match those programmed above.

Semtech Confidential Information
Ken Lin
DIVA Laboratories, Ltd.
09/08/2026

A0E5	BLANK_ CUST352M_ WD1_3_11	RSVD	15:12	RO	0	Reserved.
		CUSTOM_352M_ WD3_11	11:8	RW	0	Bits 3 to 0 of 352M byte 3 value to look for in custom blanking mode.
		CUSTOM_352M_ WD1_11	7:0	RW	0	352M byte 1 value to look for in custom blanking mode.
A0E6	BLANK_ CUST352M_ WD4_11	RSVD	15:5	RO	0	Reserved.
		CUSTOM_352M_ WD4_ML_11	4:2	RW	0	Bits 7 to 5 of 352M byte 4 value to look for in custom blanking mode.
		CUSTOM_352M_ WD4_BD_11	1:0	RW	0	Bits 1 to 0 of 352M byte 4 value to look for in custom blanking mode.
A0E7	CUSTOM_Y_ BLANK_0_11	RSVD	15:10	RO	0	Reserved.
		CUSTOM_Y_ BLANK_0_11	9:0	RW	0	Y_BLANK_0 value to use when incoming 352M values match those programmed above.
A0E8	CUSTOM_Y_ BLANK_1_11	RSVD	15:10	RO	0	Reserved.
		CUSTOM_Y_ BLANK_1_11	9:0	RW	0	Y_BLANK_1 value to use when incoming 352M values match those programmed above.
A0E9	CUSTOM_C_ BLANK_0_11	RSVD	15:10	RO	0	Reserved.
		CUSTOM_C_ BLANK_0_11	9:0	RW	0	C_BLANK_0 value to use when incoming 352M values match those programmed above.
A0EA	CUSTOM_C_ BLANK_1_11	RSVD	15:10	RO	0	Reserved.
		CUSTOM_C_ BLANK_1_11	9:0	RW	0	C_BLANK_1 value to use when incoming 352M values match those programmed above.
A0EB	BLANK_ CUST352M_ WD1_3_12	RSVD	15:12	RO	0	Reserved.
		CUSTOM_352M_ WD3_12	11:8	RW	0	Bits 3 to 0 of 352M byte 3 value to look for in custom blanking mode.

Semtech Confidential Information
Kent Lin
DIVA Laboratories Ltd.
09/08/2026

		CUSTOM_352M_WD1_12	7:0	RW	0	352M byte 1 value to look for in custom blanking mode.
A0EC	BLANK_CUST352M_WD4_12	RSVD	15:5	RO	0	Reserved.
		CUSTOM_352M_WD4_ML_12	4:2	RW	0	Bits 7 to 5 of 352M byte 4 value to look for in custom blanking mode.
		CUSTOM_352M_WD4_BD_12	1:0	RW	0	Bits 1 to 0 of 352M byte 4 value to look for in custom blanking mode.
A0ED	CUSTOM_Y_BLANK_0_12	RSVD	15:10	RO	0	Reserved.
		CUSTOM_Y_BLANK_0_12	9:0	RW	0	Y_BLANK_0 value to use when incoming 352M values match those programmed above.
A0EE	CUSTOM_Y_BLANK_1_12	RSVD	15:10	RO	0	Reserved.
		CUSTOM_Y_BLANK_1_12	9:0	RW	0	Y_BLANK_1 value to use when incoming 352M values match those programmed above.
A0EF	CUSTOM_C_BLANK_0_12	RSVD	15:10	RO	0	Reserved.
		CUSTOM_C_BLANK_0_12	9:0	RW	0	C_BLANK_0 value to use when incoming 352M values match those programmed above.
A0F0	CUSTOM_C_BLANK_1_12	RSVD	15:10	RO	0	Reserved.
		CUSTOM_C_BLANK_1_12	9:0	RW	0	C_BLANK_1 value to use when incoming 352M values match those programmed above.
A0F1	BLANK_CUST352M_WD1_3_13	RSVD	15:12	RO	0	Reserved.
		CUSTOM_352M_WD3_13	11:8	RW	0	Bits 3 to 0 of 352M byte 3 value to look for in custom blanking mode.
		CUSTOM_352M_WD1_13	7:0	RW	0	352M byte 1 value to look for in custom blanking mode.
A0F2		RSVD	15:5	RO	0	Reserved.

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	BLANK_ CUST352M_ WD4_13	CUSTOM_352M_ WD4_ML_13	4:2	RW	0	Bits 7 to 5 of 352M byte 4 value to look for in custom blanking mode.
		CUSTOM_352M_ WD4_BD_13	1:0	RW	0	Bits 1 to 0 of 352M byte 4 value to look for in custom blanking mode.
A0F3	CUSTOM_Y_ BLANK_0_13	RSVD	15:10	RO	0	Reserved.
		CUSTOM_Y_ BLANK_0_13	9:0	RW	0	Y_BLANK_0 value to use when incoming 352M values match those programmed above.
A0F4	CUSTOM_Y_ BLANK_1_13	RSVD	15:10	RO	0	Reserved.
		CUSTOM_Y_ BLANK_1_13	9:0	RW	0	Y_BLANK_1 value to use when incoming 352M values match those programmed above.
A0F5	CUSTOM_C_ BLANK_0_13	RSVD	15:10	RO	0	Reserved.
		CUSTOM_C_ BLANK_0_13	9:0	RW	0	C_BLANK_0 value to use when incoming 352M values match those programmed above.
A0F6	CUSTOM_C_ BLANK_1_13	RSVD	15:10	RO	0	Reserved.
		CUSTOM_C_ BLANK_1_13	9:0	RW	0	C_BLANK_1 value to use when incoming 352M values match those programmed above.
A0F7	BLANK_ CUST352M_ WD1_3_14	RSVD	15:12	RO	0	Reserved.
		CUSTOM_352M_ WD3_14	11:8	RW	0	Bits 3 to 0 of 352M byte 3 value to look for in custom blanking mode.
		CUSTOM_352M_ WD1_14	7:0	RW	0	352M byte 1 value to look for in custom blanking mode.
A0F8	BLANK_ CUST352M_ WD4_14	RSVD	15:5	RO	0	Reserved.
		CUSTOM_352M_ WD4_ML_14	4:2	RW	0	Bits 7 to 5 of 352M byte 4 value to look for in custom blanking mode.
		CUSTOM_352M_ WD4_BD_14	1:0	RW	0	Bits 1 to 0 of 352M byte 4 value to look for in custom blanking mode.

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A0F9	CUSTOM_Y_BLANK_0_14	RSVD	15:10	RO	0	Reserved.
		CUSTOM_Y_BLANK_0_14	9:0	RW	0	Y_BLANK_0 value to use when incoming 352M values match those programmed above.
A0FA	CUSTOM_Y_BLANK_1_14	RSVD	15:10	RO	0	Reserved.
		CUSTOM_Y_BLANK_1_14	9:0	RW	0	Y_BLANK_1 value to use when incoming 352M values match those programmed above.
A0FB	CUSTOM_C_BLANK_0_14	RSVD	15:10	RO	0	Reserved.
		CUSTOM_C_BLANK_0_14	9:0	RW	0	C_BLANK_0 value to use when incoming 352M values match those programmed above.
A0FC	CUSTOM_C_BLANK_1_14	RSVD	15:10	RO	0	Reserved.
		CUSTOM_C_BLANK_1_14	9:0	RW	0	C_BLANK_1 value to use when incoming 352M values match those programmed above.
A0FD	BLANK_CUST352M_WD1_3_15	RSVD	15:12	RO	0	Reserved.
		CUSTOM_352M_WD3_15	11:8	RW	0	Bits 3 to 0 of 352M byte 3 value to look for in custom blanking mode.
		CUSTOM_352M_WD1_15	7:0	RW	0	352M byte 1 value to look for in custom blanking mode.
A0FE	BLANK_CUST352M_WD4_15	RSVD	15:5	RO	0	Reserved.
		CUSTOM_352M_WD4_ML_15	4:2	RW	0	Bits 7 to 5 of 352M byte 4 value to look for in custom blanking mode.
		CUSTOM_352M_WD4_BD_15	1:0	RW	0	Bits 1 to 0 of 352M byte 4 value to look for in custom blanking mode.
A0FF	CUSTOM_Y_BLANK_0_15	RSVD	15:10	RO	0	Reserved.
		CUSTOM_Y_BLANK_0_15	9:0	RW	0	Y_BLANK_0 value to use when incoming 352M values match those programmed above.

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A100	CUSTOM_Y_BLANK_1_15	RSVD	15:10	RO	0	Reserved.
		CUSTOM_Y_BLANK_1_15	9:0	RW	0	Y_BLANK_1 value to use when incoming 352M values match those programmed above.
A101	CUSTOM_C_BLANK_0_15	RSVD	15:10	RO	0	Reserved.
		CUSTOM_C_BLANK_0_15	9:0	RW	0	C_BLANK_0 value to use when incoming 352M values match those programmed above.
A102	CUSTOM_C_BLANK_1_15	RSVD	15:10	RO	0	Reserved.
		CUSTOM_C_BLANK_1_15	9:0	RW	0	C_BLANK_1 value to use when incoming 352M values match those programmed above.

4.2.12. ANC Extraction Memory Control and Status Registers

Table 4-17 ANC Extraction Memory Control and Status Register

Address$_h$	Register Name	Parameter Name	Bit Slice	R/W	Reset Value$_h$	Description
B000	ANS_EXT_RAM_REG	ANS_EXT_RAM	15:0	RW	0	TBD.

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5. Applications Information

5.1. Typical Application Circuits

5.1.1. Power Pins

Refer to the pinout and RDK reference design.

5.1.2. SDI-to-SDI Configuration

Refer to the RDK reference design.

5.1.3. SDI-to-HDMI Configuration

Refer to the RDK reference design.

5.1.4. HDMI-to-SDI Configuration

Refer to the RDK reference design.

5.2. Programming via SPI or JTAG Interface

It is recommended that JTAG connector footprint be present. Connector don't need to be installed by default. In the case where it was impossible to put the connector, test point should be installed to make JTAG interface accessible.

Preferred method for GS12270 firmware update is from external MCU to GS12270 internal SPI flash directly, using the *FLASH_** pins. Communicate with Semtech if it was identified that firmware update through JTAG interface is required.

Refer to Microchip's PolarFire® FPGA Datasheet DS00003831 for information about JTAG timing.

Refer to "PolarFire_FPGA_and_PolarFire_SoC_FPGA_Programming_User_Guide_VB.pdf" for more information about how to configure device using JTAG interface and how to use FlashPro5 to configure device over JTAG interface.

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5.3. Power Supply

5.3.1. Power Supply Decoupling

Refer to the RDK reference design.

5.3.2. Power Supply Sequencing

Refer to Microchip's PolarFire® FPGA Datasheet DS00003831.

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6. Package and Ordering Information

6.1. Package Dimensions

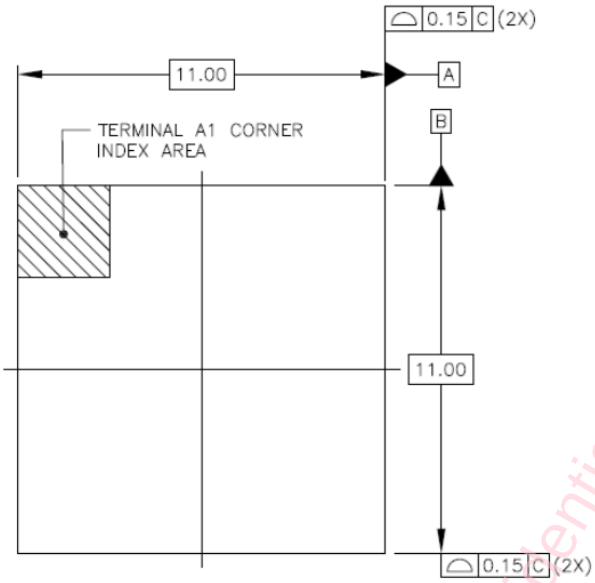

Figure 6-1: Package Dimensions - Top

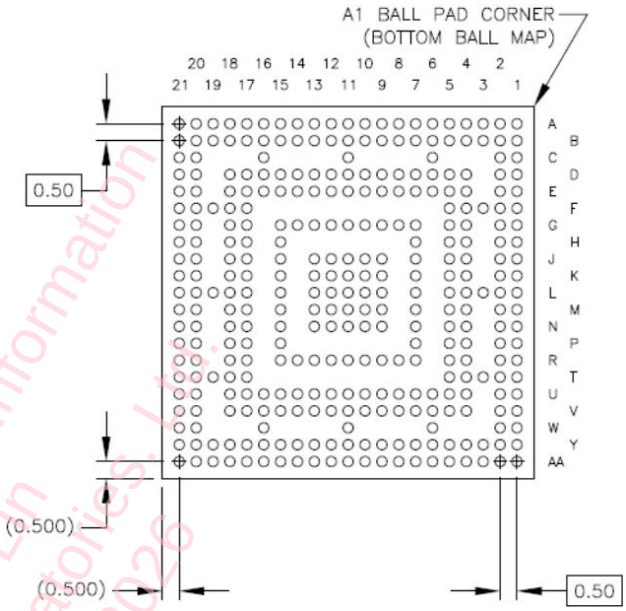

Figure 6-2: Package Dimensions - Bottom

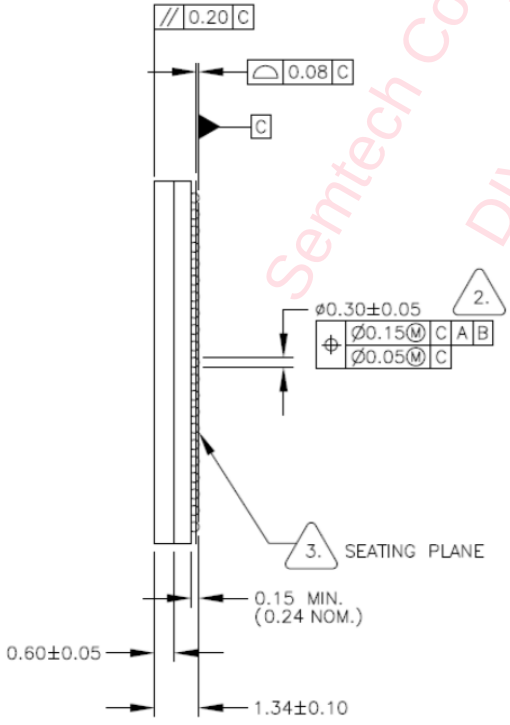

Figure 6-3 : Package Dimensions – Side View

Notes:
1. See polarfire_fpga_packaging_and_pin_descriptions_ug0722_v12.pdf.

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6.2. Marking and Ordering Information

Table 6-1: Marking and Ordering Information

SDI/HDMI Bridge Solution	Ordering Part Number	Packaging Quantity	Package Marking	Package
GS12270	GS12270-CBE3	Tray: 60	GS12270-CBE3-01	325-TFBGA (11mm x 11mm)

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